UNIVERSITY OF OSLO
Department of Informatics

Evaluation of Rectifiers & Voltage References for a Wireless Medical Implant

Master thesis

Svein Berg

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Abstract

In the continuing hunt for better and more powerful monitoring and control, we see an increased interest for small and light electronic devices adapted for these tasks. This is seen both in tracking of goods, machinery, production and other parts of the industry as well as inside the human body. And every day, new areas of use are showing up. Following the IT-age is the enormous amount of information available. Common and revolutionizing for the devices now developed are their ability to deliver the exact information needed from an exact location.

This master thesis discusses the different areas regarding development of a passive (without battery or any device of internal power source) medical implant from an electronic point of view. The introduction shortly presents the medical aspects of the diabetes disease and the reasons for this thesis. An overview of the wireless power transfer used in an inductive link application is given for understanding the physical aspects, environment and demands present for passive implants. This leads to identification of two parts that are essential in any kind of such a passive device, unrelated to the specific task of the implant: A rectifier to recover a DC-voltage from the AC-input signal, and a regulator for providing a stable V_{DD} to the whole implant and its circuitry. These two circuits are fully presented in the last chapters and some different circuit solutions are presented. These solutions are developed for optimal adaption to the inductive link and other important parameters regarding this area. The circuit solutions are presented and produced in the STM CMOS 90nm ASIC[1] process, and the simulated and measured results are investigated and compared.

[1] Application Specific Integrated Circuit

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Contents

Chapter 1

1 Introduction

Many people today are taken ill of diabetes mellitus (shorted *diabetes*). In the latest passed years, this illness has become one of the most common lifestyle related diseases in the world, and is still growing. Diabetes is today an illness which the patient cannot be treated and recover fully from. It can only be controlled by measurements and injections of the hormone *insulin*, several times during a day. These measurements involve a blood sample which the patient must retrieve each time a measurement is performed, about 3-6 times per day. The pain during this procedure often keeps the patients from not performing all the recommended measurements every day, leading to an unstable hormone and glucose balance. People struck by diabetes *type one* as we shall see, is often in their younger years, and the measurements and pain associated with controlling the disease follows them throughout their life's.

This project and thesis are meant to develop an alternative way to monitor and control this disease in a more comfortable way for the patient compared to what is done today. In this specific project, this means an implant containing a glucose sensor (LOAD), an external unit presenting the results (SOURCE), and power and communication between these two, see Figure 1.1. This can hopefully become a part of a fully automated glucose monitoring system for all diabetic patients.

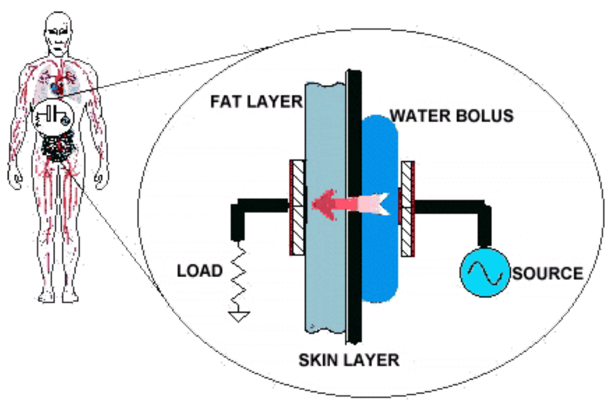

Figure 1.1: The implant (LOAD) and the external unit (SOURCE) placed in the patient's abdomen

A lot of research is daily put into developing systems for monitoring and treating the diabetes disease. Many different approaches have been tried, and are still tried with more or less satisfying results as we shall see in chapter 2. This work is an investigation and development of a system for one of the methods described in V. S. Bertelsen master thesis and work done for Lifecare A/S and Sintef Oslo (1). He investigated and discussed the differences in communication between a *passive* (internal energy source not included) and an *active* (internal energy source included) form of implant for glucose monitoring. From this, the passive way of realizing the implant was chosen as the most suitable for such a monitoring system. In the following, we will present the frames and focus for this thesis based on the passive implant method.

1.1 The main parts and focus of this thesis

The thesis will concentrate on the *wireless power transfer* between the internal and external part (electromagnetic fields), and the internal (implant) electronics. The implant is constructed without an internal energy source, therefore called passive, and the energy is transferred to the implant via an inductive link. The link is also used for communication, either single or dual directed but will not be particularly focused on as this is thoroughly presented in (1). The discussion focuses on reliable design solutions for on-chip, or ASIC[2], realisations for the inductive link and the internal electronics. The later is both discussed and a circuit solution is presented.

It will be quit sensible to divide the glucose monitoring system into three sub-parts: (1) the external unit, (2) the transfer system with the inductive link, and finally (3) the internal unit or implant. Identifying and understanding the vital parameters for the inductive link is important for how the external and the internal unit should be made for best performance. Investigating the inductive link is therefore one of the first focuses.

Because of the passive way of powering the implant, an important property of the internal device is its power consumption. Because of the inductive link's limited maximum energy transfer, the amount of power consumed in the internal device is important. And not to forget, the external unit which powers the link and the internal circuitry should be portable and therefore battery driven. This means, low energy consumption is crucial for obtaining a satisfying lifetime of the battery/system. Thus, the focus will be devoted against making the electronics as efficient as possible, and therefore provide headroom for the needed energy transfer. This is important while designing medical kinds of

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[2] Application Specific Integrated Circuit

devices when reliability and flexibility is of high importance. Furthermore, the thesis will concentrate on the analogue building blocks which are necessary for many of these passive implants. These circuits are identified and investigated in the light of minimum power consume and maximum power efficiency. The aim will be to make proposals for circuits which can be implemented as these building blocks.

The energy- and measurement signals will have to travel some distance through the patient's tissue. Therefore, the electromagnetic properties of human tissue must be considered to obtain an optimal design of the communication system. The EM[3] fields from the power signals will interact with the tissue, and this interaction might in worst case affect the tissue itself. A medical implant is also surrounded by human tissue. Hence, its surface material must be bio-compatible. This implies that the material does not cause harmful reactions in contact with biological tissue. Some materials will cause an immune reaction, other toxic. Making sure this interaction won't be harmful in any way is an area of investigation before the system can become commercial, but will not be considered further here.

The nature of the operating medium, the human body, is complex and causes challenges and care taking for other effects than for short range systems in more traditional and industrial environments. Although the discussion is based on the design of an energy and communication system for a glucose monitoring system, it will be of highly relevance for other applications for short range communication systems and medical implants together with other similar operating environments (RFID and so forth). In the following section we will see which approaches and limitations were taken the work presented in the following chapters was started.

1.2 System solution guidelines

To best adjust the treatment of diabetes, a 24-7 monitoring of the blood glucose level is preferable. As we shall see in chapter 2, one of the most serious limitations of traditional glucose monitoring system today, is the pain associated with obtaining the needed blood every day. Besides of being painful, it also takes time and equipment and therefore makes it difficult to convince diabetics to do all of the necessary number of tests. A new system, besides of being painless for the patient, it also have to be comfortable to wear and not limit his or her overall life quality. The level of user involvement necessary for the system to operate properly is also important, and ideally, it should be zero. This

[3] EM – Electro Magnetic

ideal system would be completely automated, only interfering with the user's daily business if something out of the ordinary is detected. For making this easy as possible for the user, an extensive data acquisition and processing system should be implemented, telling the user precise what have been detected. Furthermore, a communication link and software to a PC or another suitable device could help extract and keep large amount of data from the measuring system. For even more automation, a communication link from the monitoring system to an *insulin pump* would make the system complete. As described in chapter 2, insulin pumps are already developed and in use. This leaves us with a fairly easy task to make a fully automated diabetes treating system when the monitoring system first is at place.

The patient would have to undergo an invasive procedure[4] to get the implant placed inside the body. With such a procedure, it always follows a risk of infection where as the skin forms an outer barrier against foreign objects. The physical shape, size and material must be designed to ease handling and make the invasive procedure as simple as possible. The shape of the implant is especially important to ensure a perfect placement since the alignment to the outer unit is important. Furthermore, the implanted device should be as general and independent of differences in physical appearance of the users as possible, making it easy to mass produce. Individual adjustments always make production far more expensive.

As already mentioned, the monitoring system contains an outer part and an implanted inner part. A simple solution could be to place the implanted device in the lower arm near the wrist of a hand. The outer part could then be a wristwatch, allowing communication with the inner part placed right beneath this watch. This short distance between the two devices would ensure an easy establish of the energy and communication link. The wrist is also quite similar among humans and is not heavily exposed for fat if the patients are overweight. This result in easy energy transfer with a little loss through the tissue, and individual adjustments or costly flexibility would probably not be necessary.

Preliminary investigations undertaken by Lifecare indicated however that the area close to the wrist was unsuitable for glucose level measurements. The measured level in body fluid seemed to change too rapidly and was heavily dependent of muscular activity. This indicates doing the measurement in any limb, arms or legs, would increase the probability of error way above the accepted level. A solution where the patient would have to sit down and rest for some minutes before the reading could take place, are not acceptable and not in intention with this projects aim.

[4] invasive procedure – the skin has to be cut in order to carry out the procedure

The tests done by Lifecare, indicated that the body fluid in the abdomen is more suitable for such measurements, as the conditions were more stable here. This leaves us with a bigger technical challenge. Like many other, type 2 diabetes is considered a lifestyle disease. Therefore, it would not be unreasonable to expect that many diabetics are overweight. A large abdomen implies a larger operating distance. The relatively large attenuation of EM fields in body tissue at radio frequencies, implies harder conditions for the inductive energy transfer. Although there are many possibilities for mounting the system around the abdomen, like putting the outer part in a belt buckle and so forth, caution have to be taken before placing the implant. If the operating distance is too long, a solution like the passive discussed in this thesis will no longer be feasible. Placing the implant at the side of the abdomen is a possibility. A solution like this leads to two obvious possibilities for placing the outer unit. The first is in a belt, like the one athletes use for monitoring the heart rate during exercise and competition. The disadvantages are probably too many and it will be difficult to convince a user for wearing such a belt 24 hours a day. The second solution is to involve the user more in the execution of a measurement. If the user could move a watch containing the external part of the system over the implanted device, he or she could hold it there to the measurement was complete. This solution demands a quick measurement and will solve the distance issue for the energy transfer. It would be a sensational improvement of the glucose measurement system compared to what`s in use today, although it would not fully meet the requirements for the ultimate glucose monitoring system; a complete automated system that monitors the blood sugar 24 hours a day and warns of abnormal levels or changes in the blood glucose level.

After presenting the diabetes disease in *chapter 2*, *chapter 3* will discuss power and communication transfer between the two units (external and implant). *Chapter 4* and *5* will present the internal electronics on the implant and also present circuit solutions.

Chapter 2

2 Diabetes and Monitoring Systems Today

2.1 Short Description of Diabetes and its Treating

Diabetes mellitus[5] is the most common form of metabolism disease today. Diabetes is a condition where regulation of the blood sugar is not functioning properly. Untreated, the condition leads to too high blood sugar levels. Diabetes is a chronic illness caused by lack of production of the hormone *insulin*, or body cells sensitivity towards insulin is reduced. Insulin is a hormone that stimulates the cells` absorption of nutrition. Together with a couple of other hormones, the body uses insulin to regulate this amount of nutrition. When a person digests food, the secretion of these hormones increase. This means, when a person eats, sugar is released into the blood flow from digestion. Because of the lack of the insulin hormone, this sugar will not be picked up and out from the bloodstream into the cells, leading to the person becomes to "sweet". The degree of which this effects, divides the diesis into two types.

Type 1 was formerly known as insulin dependent. Suffers from this condition does not produce insulin as a result of damage to the cells in the pancreas that normally would produce the hormone. The damage is often caused by an autoimmune reaction[6]. These patients are dependent upon regular injections of insulin. Some patients carry a pump that provides this continuous supply of insulin. Without, the body starts to break down fat for fuel (making weight reduction one of the symptoms) (2). A metabolic by-product of fat metabolism is referred to as a *ketone*. The presence of elevated blood ketones in this setting is known as diabetic ketoacidosis. In extreme and untreated cases, this can lead to coma and death.

[5] The information about the diabetes disease and current treatment was mainly retrieved from the web sites of the Norwegian Diabetes Association (45), the American Diabetes Association (7) and the World Health Organization (44)

[6] Autoimmune reaction – a malfunction in the body`s immune system that causes it to attack body cells.

Type 2 was formerly called non-insulin dependent (or insulin *in*dependent). Despite the former name, about 70% need some kind of blood sugar reduction method. For type 2, insulin injection like in *type 1*, or blood glucose controlling tablets are used. For the remaining 30%, a change in diet, more exercise and weight reduction is enough for keeping the illness under control. Type 2 diabetes is caused by a complicated interplay of genes, environment, insulin and abnormalities, increased glucose production in the liver, increased fat breakdown, and possibly defective hormonal secretions in the intestine (3). The condition can develop over a long period of time. This is why many of type 2 patient are people past 40 years of age. The cells become resistant to insulin (4). This leads to lower absorption of glucose in these cells, and the pancreas increases production of insulin as a result. Because of this raise in insulin production, the liver starts to release more glucose from its glucose storage. Eventually, the pancreas becomes less able to produce insulin and the cells become even more resistant. As a result the blood glucose levels slowly start to rise. This process can go on for several years before symptoms of disease appear. Today, it is still no full understanding of how this condition arises, but scientists in Bergen, Norway, have conducted research for the cause of the disease (5). They found a connected with the digestion and are describing this condition as type 3 diabetes. This might be the first little step towards a better understanding of the arising of diabetes dieses.

As already mentioned, diabetes is treated with a strict diet with a low intake of carbohydrates. In some cases, patients are given anti diabetics which increases the effect of insulin and stimulates the insulin production. To keep the right balance between the blood sugar level and the insulin level, it is recommended that patients with diabetes monitor their own glucose level. This is done with a device called a glucose meter. A measurement means a pinprick in a fingertip to get a sample of blood. All fingertips have a large amount of pain receivers. Most patients do not think of it as a problem to carry out this procedure once or twice a day. But to be in full control of the blood sugar level, some diabetics should check their level four to five times a day. Some patients consider these repeated pinpricks quite difficult (6).

From the description above, diabetes type 1 is the worst case of the diabetes disease, and it often strikes young people, like children, youth and young grownups. If type 1 is detected, the person will be a diabetic patient the rest of his or her life. Long term complications of diabetes are more likely to occur if the patient is not given well adjusted treatment. Increased risk of heart disease, eye disorder, kidney failure and nerve damage are some of the complications a diabetic may have to face. Several studies have found a connection between the average blood sugar level and the risk of long term complication. According to the American Diabetes Association, the best known study is the Diabetes

Control and Complications Study conducted in the United States (7). The results were published in 1993 in the New England Journal of Medicine. This proved among other things that among type 1 patients, improved blood glucose control prevents or delays diabetic retinopathy[7]. Therapy that kept blood sugar levels as close to normal as possible reduced the damage to the eyes by 76 percent. Other studies have shown the best control of the glucose level is achieved by more frequent self-monitoring. Monitoring the blood sugar level continuously or at a sufficient rate, would give useful information for the required balancing between the intake of nutrition and the dosing of insulin.

In Norway today (June 2007), there are about 200.000 people suffering from diabetes, and around 25.000 of them from diabetes *type 1*. Around 600 Norwegians gets the diagnose diabetes *type 1* every year, and about 250 of them are children under 15 years old. According to the World Health Organization (WHO) latest figures (June 2007), the number of people suffering from diabetes is approximately 180 million people worldwide (8). This number is likely to more than double by 2030. In 2005, an estimated 1.1 million people died purely of diabetes. The number of deaths per year where diabetes was a contributory condition was in 2005 estimated to 2.9 million. *Type 2* is the most common of the types, constituting around 90 percent of the cases. Besides of the human suffering, the diabetes causes economical costs to individuals, families and the whole society worldwide. The disease often strikes people in their most productive years with depression, anxiety, pain and other discomfort (8). Some economical estimates have been made and the WHO gives examples of such estimates: China in the coming 10 years (2006-2015) will lose 558 billion USD in foregone national income due to heart disease, stroke and diabetes alone. Other calculations have been made and often show the cost of loss in production as a result of diabetes related sufferings equals or exceeds the direct health costs. Summarized in quick facts (8):

- 180 million people suffers from diabetes and it is likely to more than double by 2030
- Diabetes causes about 5% of all deaths globally each year
- 80% of people with diabetes live in low and middle income countries
- Most people with diabetes in these countries are middle aged (45-64)
- Diabetes deaths are likely to increase by more than 50% in the next 10 years
- Diabetes deaths are projected to increase by over 80% in upper middle income countries between 2006 and 2015

[7] Retinopathy – disorder of the retina (the part of the eye where the light sensitive cells are found)

Diabetes *type 2*, the most common, is regarded as *a lifestyle* related disease. The best way to prevent problems related to it would be a change in lifestyle, from a passive life with fast food to a life with regular exercise and a more healthy diet. The next best solution would be to give the affected a good treatment so they can go on living a productive and none-affected life, contributing to society. If there is found a method for monitoring blood sugar levels at higher rates and still comfortable for the user than today's solutions, it would be decisive for its success that the solution is cost effective. This would make it profitable for society to invest in such a system as the mentioned diabetes related loss of production would decrease.

2.2 Glucose Monitoring Systems Available Today

Most currently available glucose monitoring systems designed for self testing are based on measuring techniques that require blood samples. However, a lot of projects are now directed towards automated and painless systems. The Cygnus[8] GlucoWatch G2 Biographer and The MiniMed Paradigm REAL-Time System described at the end of this section are two systems that attempts to provide painless and automatic testing.

But first, the typical reading systems of today: This consists of a device called a sampler and a meter, in some cases also a test strip. The sampler is used to obtain a blood sample by a needle penetrating the skin when activated. Usually a fingertip, containing a lot of blood but also a lot of nerves, is the site used for tests. Some alternative meters offer the possibility of obtaining blood from other places of the body, like the upper and lower arm. However, users have reported problems and there are controversies among the expertise on how reliable these measurements are. Reports are given where differences between tests performed on the arms and tests performed on fingertips are detected (9). Research indicates an half an hour delay of the test results on the arm versus test in the fingertip. There are also more likely to get needle marks left on the arm as these sites are more sensitive. However, new testing sites can be a relief to sore fingers and used properly this might be a fairly good alternative.

When blood has been obtained, it is applied to the test spot, either on a test strip or directly into a meter. The actual measurement can now be carried out. The test spot has a coating of chemicals reacting with the blood and makes it possible to extract the glucose level. The extraction of this level is carried out in one of two ways, optical or electrochemical. They are discussed closer in section 2.4 together with this projects choice of measurement principle and sensor.

[8] Cygnus was in 2005 bought by Animas Corporation

Glucose testing can be quite an elaborate procedure with today's system. Therefore, to reduce the user's workload, many systems have been developed trying to make measuring easier and less painful. This has led to devices where blood collection and glucose testing is done in one. Examples of these systems are the MediSense Sof-Tact from Abbot Laboratories and the One Touch Fast*Take* by Inverness Medical (10). These meters are easy to use, all in one procedure and can often be used other places than in the fingertip. Because it often uses a vacuum pump, pumping blood to right under the skin surface before lancing it, very small lances can be used leaving only a small mark on the skin. This makes these devices more suited for alternative site testing where there are less blood and fewer nerves. The device can also be pre-loaded with strips for some hours, making discrete measurement in public places possible. The amount of blood needed for a test is also getting smaller and smaller with newer devices. But some disadvantages follows. The process takes some time, although faster devices have entered the market. The accuracy is temperature dependent, making readings in cold and hot environment uncertain. It also has to be handled with care, often in own cases and housing, making sure the device is not exposed to anything that can un-calibre the measurement. Maintenance is also an issue. Cleaning after each test is required in some of the devices, making sure no remains affects the next result. Exposure to light, moisture and contamination often limits the lifetime of these devices.

The possibility to store results from tests taken over a longer period of time is a welcomed functionality. This makes important statistical parameters, like averages, trends, maximums and minimums over a longer period of time easily accessible, which again helps keep a better long term control. Many of the newer meters can store in the hundreds of tests. Some users still complains and would like even more storage capacity. If you perform 5 tests a day, you will have about 150 results in a month. This fills rather quickly up the limited space and the user would have to transfer the data over to a computer with a suited PC link. This is something to note when making an automated monitoring glucose system where a lot more than 5 tests per day are possible.

Two of the most promising and fairly automated systems available today are the *GlucoWatch G2 Biographer* from *Cygnus* and the *The MiniMed Paradigm REAL-Time System* from *Medtronic*, both companies located in California, USA. These are what we can call third generation monitoring system. The Glucowatch Biographer is one of the first systems attempting to fulfil the goal of a painless and automated system. The device is a non-invasive and automatic measurement for children from 7 to 17 and adults from 18 years of age (11). It is warn like a watch and made up by 2 pieces. A sensor pad called the AutoSensor is first attached to the skin. Then a watch is placed upon it and is thereby connected to the AutoSensor. The system makes a reading every 10^{th} minute and stores the result (up to 8,500 readings) in the memory of the watch. One AutoSensor can perform maximum 76 measurements, thus up to 13 hours wear in one sensor. Besides of showing the result, it also have an built-in alarm warning the patient for too high or too low measured values.

To work satisfactory, the system has to go through a two hour warm-up period. After this period, you have to calibrate the device with a regular meter (12). Despite this calibration, every reading has an overall 11% variation from the actual value, and every fourth reading will differ with more than 30% from the actual value. A glucose sample obtained with the GlucoWatch will also lag about 15 minutes behind a blood sample taken at the same time.

The GlucoWatch measures not on blood, but on interstitial fluid[9]. The sample is obtained by applying a small current across the skin. The glucose is then extracted from the sample and is drawn into hydrogel disks in the AutoSensor. Here it reacts with the enzyme glucose oxidase. This forms into hydrogen peroxide, and the sensor picks up the electric signal generated from this converting. This small electric signal is then translated into a blood glucose value and sent to the watch and displayed for the patient.

It is stressed from the FDA[10] that the GlucoWatch G2 Biographer is not a replacement of a regular glucose meter. Because of the many conditions under which it does not operate optimal and many sources of error, the probability of mall-function is too great. Because of this uncertainty associated with the measurements, it is not recommended to make large adjustments in the treatment or fully relay on the results from the GlucoWatch. Also, many users get skin irritations from wearing the sensor, and the system is easy to un-calibre under use, by not storing new AutoSensors in the right temperature, by too much movement on the device and so forth. Despite all the error sources, GlucoWatch was the first of a new generation meters allowing continuous testing over a period of time.

The *MiniMed Paradigm REAL-Time System* from *Medtronic* is another measuring system created for continuous monitoring for people down to seven years of age. Unlike the GlucoWatch, this system also includes an insulin pump (13). The monitoring unit together with the pump makes it the first complete and

[9] Fluid between the cells
[10] The American Food and Drug Administration

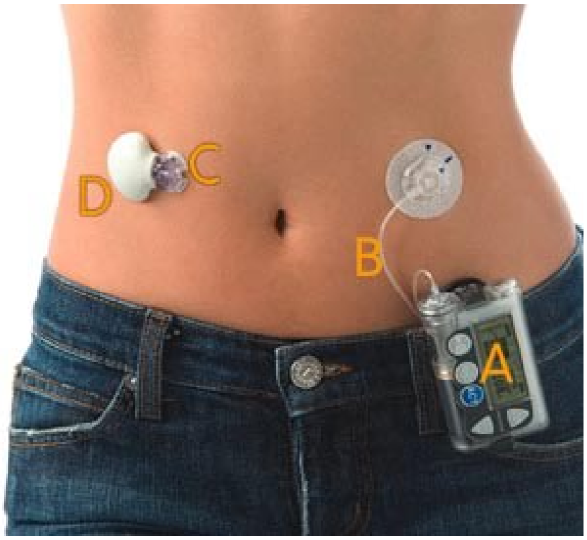


Figure 2.1 The three parts in the MiniMed Paradigm RealTime System© from Medtronic (13)

fully automated treating-system for a period of time for diabetes disease. The system is built up by two separate parts, monitoring device (C and D) and insulin pump (A and B), communicating with one another by an RF-link, see Figure 2.1. The monitoring system is also made up by two parts; a sensor pad (C) and a communication transmitter (D). The sensor pad is attached to the skin, and has a hypodermic needle mounted on. The needle is inserted through the skin for making measurements possible. The transmitter is then connected to the sensor pad, sending the results to the insulin pump which also presents the readings to the patient. The sensor pad can be inserted for three days at a time. After this you need a new sensor and a new location to insert it. The transmitter is rechargeable and can be used several times if treated carefully.

Like the GlucoWatch, the MiniMed needs an initialization period of two hours after insertion. It also needs calibration at least twice a day, once every 12 hours, but it is recommended that the system is calibrated three to four times a day. This calibration is provided by the patient's regular meter and the result needs to be entered into the insulin pump. The sensor is an electrode measuring glucose levels in the interstitial fluid and can be inserted by the patient himself. A hypodermic needle is used to insert the electrode and is then pulled out, leaving only the flexible electrode underneath the skin. The sensor pad has to be mounted at least two inches away from the insulin pump, avoiding errors in the measurement while insulin is inserted.

Experimental results and other functionality reports are, unlike the GlucoWatch, hard to find for the MiniMed Paradigm REAL-Time System. But, like the

GlucoWatch the FDA again stresses that the MiniMed system is not a replacement for the regular meter. It is only a supply for the regular measuring method and treatment cannot rely by measurements done by the monitoring system alone. Together with restrictions given for use, like places for insertion, the temperature dependent storage of sensors, need for calibrations and all the other cautions, it is likely to believe the accuracy of the measuring results of MiniMed is not far from the ones from the GlucoWatch. However, the MiniMed Paradigm REAL-Time System is one of the first and the most advanced automated monitoring- and treating system available today.

2.3 New Solutions under Development

There are a lot of projects around the world in every continent concerning diabetes. Especially in the latest 5 years, a lot of attention has been given to this very common people disease. Large amounts of money are invested in research, both electronically and medically. Therefore, solving one of the diabetes many questions means a lot of attention and lot of earnings. This leads to competition between the researches and the researching companies, making information about coming solutions hard to find. Every firm is holding their cards close to their chest. But based on what we can see today, we can make some assumptions of what we can expect in the coming years.

Many different approaches are attempted. They span all the way from fully implanted to non-invasive. Some measures blood, some on interstitial fluid, some utilizes magnetic fields through an impedance spectroscopy. Also, we see that fully automated systems, measurement and treating in the same system, is the future. This combined with painless and continuous measurement and injection, is the ultimate goal for the electronically diabetes treating system. A brief view of some of the interesting ongoing projects is given below. The information is obtained mainly from *diabetesnet* homepage (14) and the homepages of the companies.

The *Optiscan Biomedical Corporation* is developing a glucose measuring method using middle infrared radiation. This semi-invasive method applies IR-radiation with 9-10 different wavelengths and measures the phase-shift of the returning waves. This is done after rapidly cooling down an area of skin for test. One disadvantage is absorption of the IR-waves in water, which is the major component of blood and interstitial fluid. Another is because there is no temperature difference between the glucose and the water beneath the skin, they cannot be differentiated from one another. However, accuracy appears to be good in very limited testing. It is however is reduced by individual variations, such as skin temperature, black body radiation, cooling speed and other factors.

It is still not known whether or not the system needs regularly calibration with another meter.

The Therasense FreeStyle Navigator is a semi-invasive continuous meter under FDA review (2007). The monitoring system is divided in three parts: Part one is the sensor designed to be worn for several days at a time. The sensor is placed just under the skin like a patch on the abdomen or the upper arm. The sensor measures interstitial fluid 5-6mm beneath the skin surface as frequently as once per minute. The second part is a transmitter located at the sensor site. The third part is a receiver, about the size of a pager, and can be carried anywhere on the patient’s body. The receiver displays the glucose value, trends and also has a high and low alarm. It also stores the results for further investigations. Some issues are reliability, size, waterproofness and time of each sensor wear.

The Synthetic Blood International is developing a device called Implantable Glucose Biosensor. As the name indicates, this is an implanted device with an inner- and outer part. The inner part is of course the sensor, monitoring continuously the patient’s blood glucose level. It is equipped with a titanium battery and a micro-processor. The size of the device is twice a cardiac-pacemaker, and made in the same bio-material as this. Results are digitally displayed by the outer unit, with a size like a beeper. The total implant lifetime is about a year.

2.4 Sensor Technology

Many ways of measuring glucose or other chemicals have been tested and/or used in the past years of diabetes research. Two of the main principles are the optical sensor and the current sensor. Some of them utilises blood or a body fluid directly, while others use reflection in the skin or detecting changes in radio waves. The oldest and the most common type of sensor and often used as reference because of the superior accuracy, are the two types of test strip measurements. In both cases, a drop of blood is collected on a test strip and fed into the sensor. This sensor is either optical or electrochemical. In both cases, the drop of blood are mixed with other chemicals and then tested on. In the optical case, the mixed chemicals form a blue colour. By measuring the intensity of this blue colour, the glucose level is extracted (15). Although this method gives accurate results and measurement, the newer electrochemical is about to become superior. This method has a lot lesser demands of cleaning and maintenance compared with the optical. This ensures even more polite results. Again, by adding a drop of blood to a test strip and mixing it with other chemicals, the level of glucose can be extracted by *measuring the current* trough the sample. About 1μl blood is needed and the measurement only takes second.

Because of the human- and chemical factors involved, one of the largest sensor challenges is to make a sensor capable of providing reliable measurements over a long period of time without maintenance like cleaning and so forth. Also, when making a sensor for long time implantation, the use of a reactant to perform the measurement is excluded. This is a crucial success factor in continuous monitoring systems where the sensor cannot be repeatedly extracted for maintenance and reactant refilling. Many promising sensors and monitoring systems have failed because of the human body tend to reject foreign objects or clots have formed in the sensor mechanism. The sensor used for this project is based on osmotic pressure. The sensor is a closed chamber with a reference liquid inside and a semipermeable membrane as one of the chamber walls. This membrane separates the internal reference liquid from the interstitial fluid, but it also act as a tunnel for molecules smaller than a given size. This means, small water molecules can flow through the membrane, larger dissolved particles cannot. The large particles, based on the density in the reference liquid versus in the interstitial fluid, will therefore cause a chemical potential to arise across the membrane. This potential will enforce a net diffusion of water through the membrane in a try to equalize the two concentrations. Eventually, a equilibrium between the internal and the interstitial fluid concentration is reached and the water diffusion will come to a stop. The pressure change inside the reference chamber is dependent on the amount of water flown in or out through the membrane. The amount of water is again dependent on the concentration difference inside and outside the membrane.

This means, if we could make a membrane selective for glucose molecules alone, we would have a perfect sensor. This is however not the case. The membranes selectivity is based on a diffusion resistance depending on the molecule size. This means, if we could draw a resistance curve versus molecule size, it would show an increasing resistance for increasing particle size. However, the membrane cannot guarantee molecules in any given size to pass or not pass through the sensor membrane. This lack of a sharp cut-off in particle size is a source of error. Also, second order effects will be present if other substances than glucose could change the water diffusion. The membrane stiffness is also an error-source as the volume inside the reference chamber would change if the membrane were flexible. Response time is also an important factor. How rapid changes in the glucose concentration can the sensor and membrane follow? And, the body tends to reject all foreign objects introduced to it. Which effect would this have on the response time and the long time stability of the sensor and system? These points and questions are crucial when a sensor is developed and later tested.

Chapter 3

3 System Review and Energy transfer Theory

One of the goals in this project is to make the implant so small it can be fitted into any part of the body. Because the size is important, batteries or other power sources cannot be mounted onto the implant. We therefore have to feed the implant with power from outside. The easiest way of doing this is of course by having wires through the skin, from a battery mounted outside the body to the implant on the inside. From an electronic point of view, this would be the most effective and safest way of providing enough energy at all times. This is not possible however. The human body and skin will not allow this kind of solution, as it will immediately lead to inflammation, poisoning and other unwanted reactions. Energy must therefore be transferred wirelessly from the external unit to the internal. This chapter will present this kind of energy transfer, and look at some aspects and formulas connected to such a system. It will start with going through a total system description and review of its parts and functionality. The following sections look at the basic physics in such inductive energy transfer, before a possible system solution is presented. At the end, some additional aspects are discussed, forming a complete picture of the energy transfer.

3.1 System Review

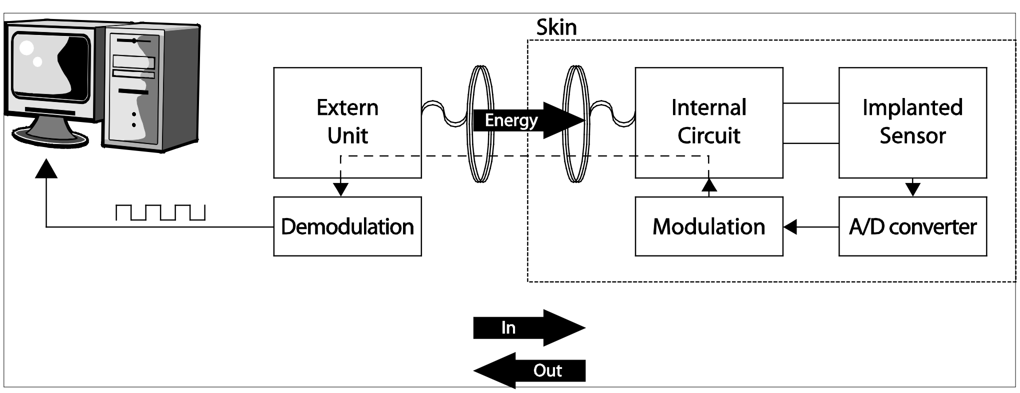


Figure 3.1 The different system parts

Figure 3.1 shows a graphic overview of the complete system. Starting on the outside of the body, or the skin, we find the *external unit*. This is the unit the patient will experience, and its tasks will be:

- powering itself and the internal unit
- receive the measurements from the internal unit
- process and present the readings and results to the patient
- storing an amount of results and be compatible with PC/Mac to transfer results for long term storing and control

Inside this *external unit* it will have to be a coil, and the *internal unit* must also contain a coil. In Figure 3.1, these coils are drawn individually from the external and internal units for better illustration of the system. These two coils are the main part in the wireless energy and communication transfer. By placing two coils on top of each other in a fairly distance from one another, we will create what is called an inductive link. This rather large field of physics and electronics will be discussed and calculated further in the following sections.

Inside the body, together with of the mentioned coil, we find the implant. Again in Figure 3.1, the sensor itself, the A/D converter and the modulator are drawn separately from the internal unit for better illustration. However, all this circuits are fabricated on the same PCB[11]/ASIC. We will use Figure 3.1 and specify the internal unit-, sensor-, A/D converter- and the modulator tasks separately:

The Internal Circuit tasks will be:

- convert the incoming AC power-signal to DC current
- charge a supply capacitor for use as battery during measurements
- regulate the power signal to a stable 1V supply

The Implanted Sensor tasks will be:

- measure the glucose level in the patient interstitial fluid
- change its resistance based on the measured glucose level

The A/D converter tasks will be:

- convert the current signal from the sensor into a digital signal

[11] PCB – Printed Circuit Board

The Modulation tasks will be:

- modulate the digital signal from the A/D converter
- transfer the modulated signal to the external unit for patient presentation

This quick overview shows all that's needed for making a fully automated glucose monitoring system. Beside of this electronic part, some medical areas need to be investigated. Some of them are what materials the implant can be made of that the body won't reject, places to implant the sensor where the readings are accurate, how long the implant will survive in the body before it has to be replaced and so forth. This thesis will not discuss these questions further, but rather concentrate on the inductive link and the electronics of the Internal Circuit.

3.2 Inductance

The sensor and implant need energy to function and to do the measurements. Of reasons mentioned earlier, this energy needs to come from outside and be picked up and stored by the implant. A well known method of transferring energy over short distances is by electromagnetic induction, known as an inductive link. In the following, we will look at the basic physics of this electromagnetism and induction.

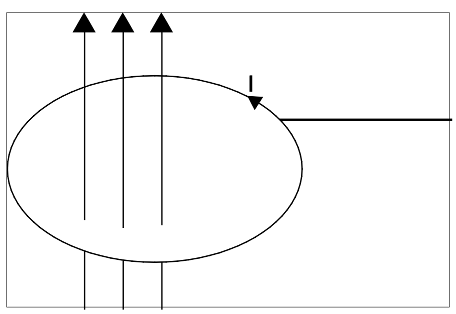


Figure 3.2 Electrical leader inside magnetic field

In a homogenous magnetic field, we denote the field strength **B**. By placing a circular electric leader inside the field we get what is shown in Figure 3.2. The magnetic flux, denoted $\mathbf{\Phi_B}$**,** is defined as the field strength through a given area (the circular area given by the electric leader):

$$\Phi_B = \int \vec{B} \cdot dA \qquad (3.1)$$

If the magnetic field is changed over time, i.e. changes direction, the flux is changed and it will induce a *charge*. This is known as the Faradays induction principle and defined as:

$$\varepsilon = -\frac{d\Phi}{dt} \tag{3.2}$$

where ε denotes the induced electromagnetic charge.

Biot-Savarts law defines how the magnetic field contribution in a single point is affected by an infinitesimal current, *Idl*:

$$d\vec{B} = \frac{\mu_0 I d\vec{l} \times \vec{r}}{4\pi |\vec{r}|^3} \tag{3.3}$$

where r is the distance between the point and the current source, and μ is the permeability. Figure 3.3 shows this magnetic inductance in a point P.

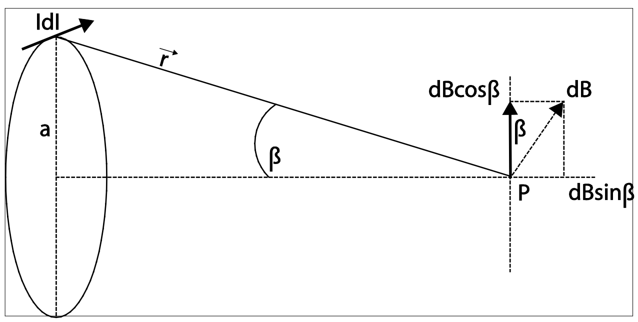


Figure 3.3 Magnetic field contribution in a single point P

By integration of the whole current-loop, the total magnetic field is derived:

$$\vec{B} = \oint \frac{\mu_0 I d\vec{l} \times \vec{r}}{4\pi |\vec{r}|^3} \tag{3.4}$$

In equation 3.4 it is seen that the magnetic field is direct proportional to the current. This also means the magnetic flux is proportional to the current and can be expressed as:

$$\Phi_B = L \bullet I \tag{3.5}$$

where L is a constant expressing the relationship between the current and the magnetic flux density, also known as *inductance* and measured in the SI unit Henry (H):

$$1H = 1\left[\frac{V \bullet s}{A}\right] \tag{3.6}$$

An inductor can be looked at as simply a lot of current-loops connected together. If we put N current-loops together and using formulas (3.4) and (3.5), we can derive the expression of an inductor:

$$L = \frac{N\Phi_B}{I} = \frac{N\int \vec{B} \bullet d\vec{A}}{I} = \frac{N\mu_0}{4\pi}\int \frac{d\vec{l} \times \vec{r}}{|\vec{r}|^3} \tag{3.7}$$

From (3.7) it is seen that L is decided from the number of turns N, the radius r, and the geometrical shape of the turns/inductor. Formula (3.7) can be seen in a numerous types of forms based on the shape and type of inductor.

3.3 Mutual Inductance

A common definition of mutual inductance is: two separated current-loops where an alternating current *in the first* will make a change in magnetic flux, and there on induce a charge *in the second*. This will be the case if we place two electrical conductors in the same magnetic field **B**, as in Figure 3.4.

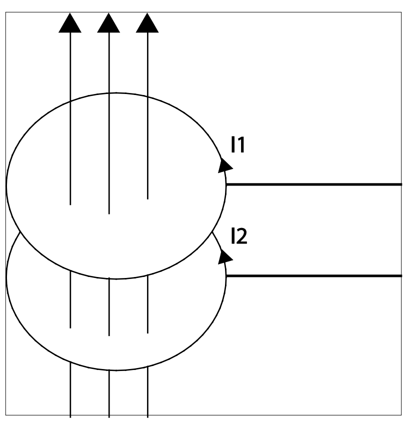


Figure 3.4 Mutual Inductance; two current loops placed closely together will interfere with one another and affect the charge and current flowing through the two leaders

By having this figure in mind, we will derive an expression for the mutual inductance. Each inductor will have two flux contributions; let us start with the second one. The first contribution is its own current, I_2, which we can denote $\Phi_{22} = L_2I_2$. The second contribution is from the variation of the current in inductor one, inductive coupled to our second inductor, and can be denoted Φ_{21}. In the same way as Φ_{22} is proportional to the current I_2, Φ_{21} will be proportional to I_1. A constant, denoted M_{xx}, will therefore fulfil and connect the relationship between the two inductors and their currents. We can therefore write:

$$\Phi_{21} = M_{21}I_1 \tag{3.8}$$

By using the same principles as for (3.7) we can derive what is known as Neumanns formula, an expression of mutual inductance:

$$M = M_{12} = M_{21} = \frac{\mu_0}{4\pi}\oint_1 \oint_2 \frac{d\vec{l_1} \bullet d\vec{l_2}}{|\vec{r}|} \tag{3.9}$$

The mutual inductance M is, like the self inductance L, a geometrical dependent constant affected by the two loops shape and placing to one another. By deciding this, for example two similar inductors placed above each other, the mutual inductance M can be expressed as a function of only distance r between the two coils.

The last but important factor we will mention is the coupling coefficient, denoted k. Since the magnetic flux from loop one working on loop two, Φ_{21}, never can be greater than Φ_{22}, the factor k is used and we say $\Phi_{21} = k_{21}\ \Phi_{22}$. Since $\Phi_{22} = L_2I_2$, and $\Phi_{21} = M_{21}\ I_2$, M_{12} can be expressed as:

$$M_{21} = \frac{\Phi_{21}}{I_2} = \frac{k_{21}\Phi_{22}}{I_2} = k_{21}L_2 \tag{3.10}$$

Keeping in mind (3.9), we look at the flux contribution on loop one, giving $M_{12} = k_{12}L_1$ and there on $M^2 = M_{12}M_{21} = k_{21}k_{12}L_1L_2$, means:

$$M = \sqrt{M_{12}M_{21}} = \sqrt{k_{12}k_{21}L_1L_2} = k\sqrt{L_1L_2} \tag{3.11}$$

and

$$k = \frac{M}{\sqrt{L_1L_2}} \overset{L=L_1=L_2}{=} \frac{M}{L} \tag{3.12}$$

where $k = k_{12}k_{21}$ can adopt values between 0 and 1. This is a very useful parameter/constant and is given much attention during coil and system design. A large k, close to one, will ensure good "contact" and energy transfer between the two coils.

3.4 The System

One of the important goals in developing this type of system is the energy loss, or energy dissipation. Especially because the external unit is battery powered, high efficiency in the power transfer is therefore important. One of the key elements in this is the resonance circuit in both the internal and the external unit (16) (17) (18) (19). In the literature it is augmented for using 2. order RLC filters in series in the external unit, and in parallel in the internal. Both filters should be tuned into the same resonanc frequency which equals the frequency of the AC signal produced by the external unit. Table 3.1 shows the two different circuits and their impedance which is the key for making use of resonanc circuit.

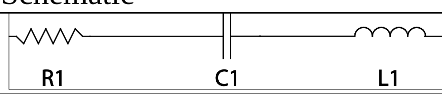
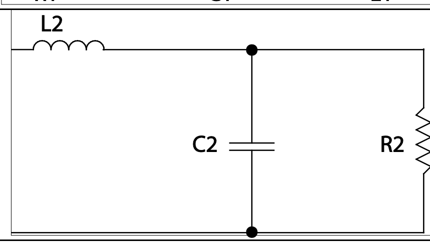
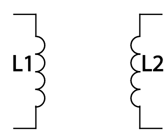
	Circuit	Schematic	Impedance
Z1	*RLC - series*		$R_1 + \frac{1}{j\omega C_1} + j\omega L_1$
Z2	*RLC - paralell*		$j\omega L_2 + \frac{R_2}{j\omega R_2 C_2 + 1}$
Z12	*Inductive link*		$j\omega kL$

Table 3.1 RLC configuration for 2. order filters

At resonance, only the real part of the impedance will be energy dissipating. The imaginary part of the impedance will cancel out and therefore lowering the total amount of energy dissipated in the transfer system. Thus, by using these resonating filters we can draw the first schematic overview of the total system, Figure 3.5[12]

[12] The internal circuitry is somewhat simplified for better showing the RLC filters in the inductive. In addition to the rectifier/chargepump and voltage regulator unit, the internal system

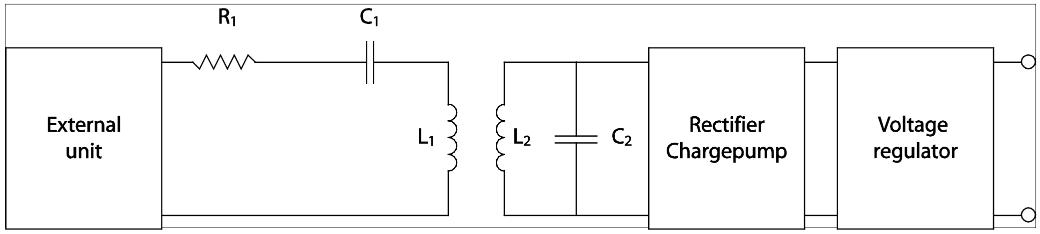


Figure 3.5 System overview

In the following investigation, we are interested in what voltage we can induce on L_2 from $L_{1,}$ and there on what voltage we can expect to deliver to the chargepump circuit. In help for this investigation, we will use the simplified circuit in Figure 3.6. In this figure the chargepump and the following circuits are substituted with the resistance R_2. Making it easier and less notation during the calculations of the desired voltage across it. Also, L_1 and L_2 are divided into two inductors on each side, this for separating the mutual inductance from the self inductance and for help to keep them apart during calculation. The calculations are in thread with the standard procedure used for such systems. Similar methods it used in the earlier mentioned (16) (17) (18) (19).

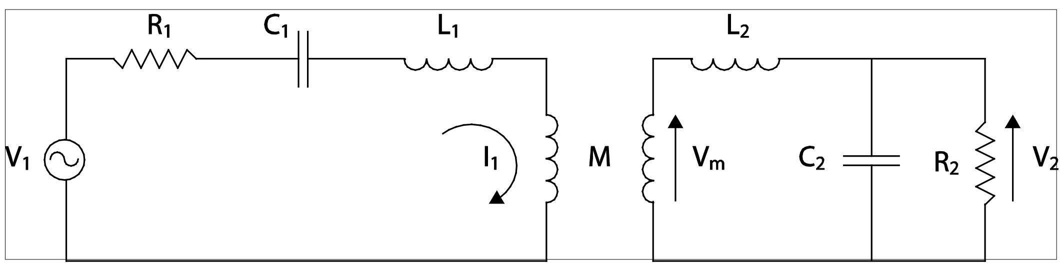


Figure 3.6 Inductive link elements with load resistance modulating the internal circuitry

By combining equation (3.2) and (3.5), the *electromotorical* voltage is derived:

$$\varepsilon = -\frac{d\Phi_B}{dt} = -L\frac{dI}{dt} \tag{3.13}$$

By applying the theory from the mutual inductance and equation (3.8)

$$\Phi_{21} = M_{21} I_1 \tag{3.8}$$

---

consists of a storage capacitor, voltage protection diode and the circuit boxes shown in Figure 3.1

we can derive an expression of the induced voltage by means of change in the magnetic flux between two current loops in a fairly distance from each other.

$$\varepsilon_1 = -L_1 \frac{dI_1}{dt} + M_{21} \frac{dI_2}{dt} \tag{3.13}$$

The index in equation (3.13) indicates a current in the second loop affecting loop 1. However, by changing the indexes, the opposite can be found; a current in loop 1 affecting loop 2 and thereby inducing a voltage, ε_2. As for our intention of providing a voltage across L_2 in Figure 3.5 as high as possible, L_1 must be exited with an alternating current at a curtain frequency. A brief discussion of the actual choice of frequency will follow in section 3.5. As we want oscillation on both sides (external and internal) for ensuring maximum power transfer efficiency, the frequency and the capacitor and inductor values must be chosen to achieve that. For the external series resonating circuit, this means:

$$f_r = \frac{1}{2\pi\sqrt{L_1 C_1}} \tag{3.14}$$

The real impedance of L_1 and C_1 in series is equal to zero at oscillation frequency; R_1 is therefore the only ohmic resistance and will be a current limiting resistance in this system.

In the internal oscillating circuit, L_2 is placed in parallel with capacitor C_2. Although this may look as a short, their impedance at the resonance frequency is ideally infinite. Therefore, high voltages can be achieved over these elements, and the leakage will be approximately zero. This voltage can then be taken out across R_2, or in Figure 3.5, the chargepump circuit. In the following, we want to calculate this voltage, V_2, based on the induced voltage; V_m. V_2 is therefore just a voltage divided between L_2, C_2 and R_2:

$$V_2 = \frac{\dfrac{R_2 \dfrac{1}{j\omega C_2}}{R_2 + \dfrac{1}{j\omega C_2}}}{j\omega L_2 + \dfrac{R_2 \dfrac{1}{j\omega C_2}}{R_2 + \dfrac{1}{j\omega C_2}}} V_m = \frac{R_2}{j\omega L_2 (1 + j\omega C_2 R_2) + R_2} V_m \tag{3.15}$$

As equation 3.15 is a very useful formula for the internal circuit itself, we want to extend it into an expression where we include the current in the external unit. This means, substituting V_m to I_1. As V_m is the induced voltage across L_2 caused by the mentioned current I_1 in the external unit, we get the relationship:

$$V_m = j\omega M I_1 \tag{3.16}$$

This leads to

$$V_2 = \frac{R_2}{j\omega L_2(1 + j\omega C_2 R_2) + R_2} j\omega M I_1 \tag{3.17}$$

by combination of (3.15) and (3.16). As our ultimate goal is to find an expression for V_2 given V_1, we need to apply Ohm's law together with (3.17). This implies to find the total impedance on the external circuit. First, the impedance in the internal circuit is:

$$Z_2 = j\omega L_2 + \frac{R_2}{1 + j\omega C_2 R_2} \tag{3.18}$$

The relationship of the impedance through the inductive coupled coils are stated in (20) and gives the Z_{12}, the impedance in the internal circuit through the inductive link and working on the external unit:

$$Z_{12} = \frac{\omega^2 M^2}{Z_2} \tag{3.19}$$

The total impedance of the external unit is therefore:

$$Z_1 = R_1 + j\omega L_1 + \frac{1}{j\omega C_1} + Z_{12} \tag{3.20}$$

This implies, by exciting the external circuit with the voltage V_1, the following expression yields for the current I_1:

$$I_1 = \frac{V_1}{R_1 + j\omega L_1 + \frac{1}{j\omega C_1} + Z_{12}} \tag{3.21}$$

As for the final step, combining (3.21) and (3.17) gives:

$$V_2 = \frac{\dfrac{R_2 j\omega M V_1}{R_1 + j\omega L_1 + \dfrac{1}{j\omega C_1} + \dfrac{\omega^2 M^2}{Z_2}}}{j\omega L_2(1 + j\omega C_2 R_2) + R_2}$$

$$\downarrow \tag{3.22}$$

$$V_2 = \frac{R_2 j\omega M V_1}{j\omega L_2 R_1(1 + j\omega C_2 R_2) + R_1 R_2 + j^2\omega^2 L_1 L_2(1 + j\omega C_2 R_2) + j\omega L_1 R_2 + \dfrac{j\omega L_2(1 + j\omega C_2 R_2)}{j\omega C_1} + \dfrac{R_2}{j\omega C_1} + \dfrac{j\omega^3 M^2 L_2(1 + j\omega C_2 R_2)}{Z_2} + \dfrac{\omega^2 M^2 R_2}{Z_2}}$$

As stated earlier in the section, by keeping the transfer frequency fixed and choosing L_1C_1/L_2C_2 to oscillate at this frequency, expression (3.22) can be simplified[13] (not shown here) to:

$$\left|\frac{V_2}{V_1}\right| = \frac{kR_2\sqrt{\dfrac{L_1}{L_2}}}{\sqrt{(R_1 + k^2 R_2 \dfrac{L_1}{L_2})^2 + (\omega_r k^2 L_1)^2}} \tag{3.23}$$

From (3.23) we see the coupling coefficient *k*, is present both in the numerator and denominator. This complicates the calculations, and if (3.23) is derived with respect to *k*, it becomes clear that $|V_2|/V_1|$ shows a maxima at a certain value of *k*, called k_{crit}. As *k* is a function of distance, it is easy to imagine a looser coupling when the spacing of the two coils is increased. However, $|V_2|/|V_1|$ is also lowered when the distance is shorter than the distance of k_{crit}. This is not so simple to realize. A closer connection between the two coils leads to a higher Z_{12}. This will lower I_1, and then again lower the induced voltage across L_2.

As k_{crit} is an important value, *Q-factor* (quality factor) is also mentioned in such systems. Q-factor is also used in describing other systems and also smaller components like coils and so forth. In connection with the above, we define the Q-factor as (21):

[13] When $\omega^2 = 1/L_2C_2$, the Z_{12} becomes real (the imaginary part is zero), and therefore the presents of the internal unit trough the coupling *M* will not alter the resonance frequency of the external circuitry. Keeping Z_{12} purely real for all values of *k* is important for the resonance and the total functionality of the transfer system.

$$Q = 2\pi \frac{\text{Energy stored in the circuit}}{\text{Energy dissipated in the circuit during one periode}}$$

The Q-factor of the coils used in the system above is therefore $Q_{L1} = \frac{\omega L_1}{R_{L1}}$ where R_{L1} is the self resistance in the coil L_1. Efficiency and Q-factor have been in focus when designing inductive power links the past few years. From the definition of the Q-factor above, we will look briefly at some of the calculation methods of the efficiency in an inductive link. Figure 3.7 defines the different efficiencies in an inductive link, denoted η.

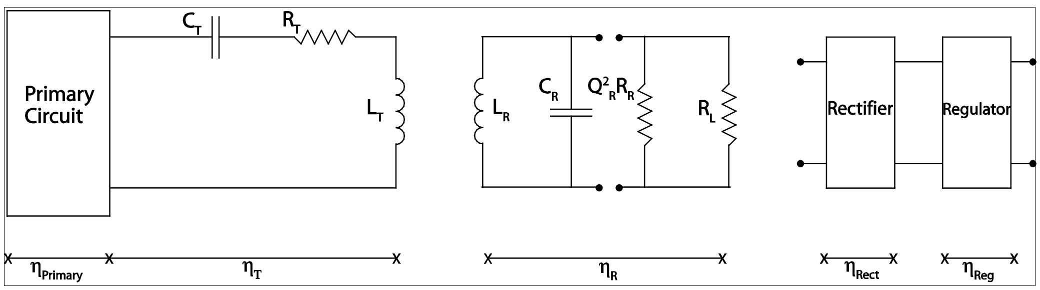


Figure 3.7 A sketch of the whole system showing the different parts and their efficiency. The load connected here is the resistance RL, however, the load in the finished system will be the rectifier, regulator and so forth

From Figure 3.7 the Q-factor of the series RLC transmitting circuit is given by

$$Q_T = \frac{\omega L_T}{R_T} \tag{3.24}$$

when no magnetic field is involved, ω is the frequency of oscillation and R_T is the total resistance. When *no* load is present[14] in the receiving circuit, the Q-factor becomes

$$Q_R = \frac{\omega L_R}{R_R} \tag{3.25}$$

[14] Both the R_L and $Q_R^2 R_R$ are not connected/taken away from the system in Figure 3.7

where R_R is a combination of the receive coil series resistance and C_R equivalent series resistance. If now R_L is added and we assume $Q_R^2 >> 1$ so that $Q_R^2 + 1 \approx Q_R^2$, we can define the receive efficiency, η_R, for the receiver circuit as (22):

$$\eta_R = \frac{1}{1 + \frac{R_L}{Q_R^{\,2} R_R}} = 1 - \frac{Q'_R}{Q_R} \tag{3.26}$$

where Q'_R is the quality factor of the receiving circuit *with* load:

$$Q'_R = \frac{(Q_R^{\,2} R_R) \parallel R_L}{\omega L_R} \tag{3.27}$$

This indicates when load R_L is added, power is lost due to heating in the receiving resonance circuit. Thus, for high efficiency it should be ensured that $Q_R^2 R_R >> R_L$. For high receive efficiency, Q'_R will be much less than Q_R.

Finally, we will try to find the transmitting efficiency, η_T. As already augmented for, at oscillation, the impedance seen from the transmitting circuit into the receiving is purely resistive (real). This inductive coupled load can therefore be seen as a resistance in series with the transmit coil, now called $R_{Lreflect}$ (not drawn in Figure 3.7). If we deliver power P to $R_{Lreflect}$, then $\eta_R P$ will be delivered to the load. The efficiency at which we deliver this power to the load is limited by the voltage divider of R_T (drawn in Figure 3.7) and $R_{Lreflect}$ (not drawn in Figure 3.7). From this the transmit efficiency can be derived (23)

$$\eta_T = \frac{k^2 Q_T Q'_R}{1 + k^2 Q_T Q'_R} = k^2 Q'_T Q'_R \tag{3.28}$$

where $Q'_T = \dfrac{\omega L_T}{R_T + R_{Lreflect}}$ is the quality factor of the loaded transmit circuit.

From Figure 3.7 we now have found η_{link}, as this is defined as

$$\eta_{link} = \eta_T \eta_R \tag{3.29}$$

Investigations show that the receive efficiency, η_R, can be close to one if the unloaded receive coil has a high Q_R. Thus, the power efficiency is primarily dependent on the transmit efficiency, η_T. To maximize η_T, Q'_T and Q'_R must be made as high as is practical. However, designing for high Q-factors has is risks as the bandwidth of the resonance circuit is given by ω/Q. So a high Q implies a narrow operating region, not well suited for component variation, stray capacitances or even the presence of conductive materials near the coil. To avoid this, Q_T and Q'_R should be limited by potential of component variation, and then again, focus should be on designing for the optimal coupling coefficient, *k*, for achieve high transmit efficiency, η_T. Figure 3.7 also contains other efficiency measurands, like $\eta_{Primary}$, these will not be treated further in this thesis.

3.5 Choice of Frequency

In choice of operating frequency there are many considerations. First of all, the demand of free radio frequencies is great, and authorities have therefore regulated these into bands. This is done by several instances, internationally by the International Telecommunication Union (ITU), regionally for Europe the European Conference of Postal and Telecommunications Administration (CEPT) and so on. But most important is the national regulation of the country where the frequency is intended to be used (24). Besides of the frequency itself, other parameters are also regulated. Examples are duty cycles, channel separation and out of band dampening. This has to be taken into account when choosing operation frequency. Some bands are especially allocated to different tasks and areas of use. These are to be found in the ITU Radio Regulations, Article S5, Frequency allocations. For the medical use, some parts of the spectrum well suited for this, are set aside for what is called *Industrial, Scientific and Medical* use other than communication (ISM-band). Although medical equipment because of its significance can get dispensation and use other frequencies, choosing a frequency in the ISM-band if possible saves a lot of effort trying to get the product approved and sold on the market. These ISM-bands are also more or less internationally accepted, making special adaptation for other markets unnecessary.

Lower Frequency (MHz)	**Upper Frequency (MHz)**	**Center Frequency (MHz)**
6.765	6.795	6.780
13.553	13.567	13.560
26.957	27.283	27.120
40.660	40.700	40.680

Table 3.2 The four lower ISM-bands defined by the ITU-R

Frequency Band	Maximum Radiated Effect	Allowed for
119 – 135kHz	72dBµA/m at a distance of 10m reduced by 3dB every octave from 30kHz	Inductive applications
135 – 140kHz	42dBµa/m at a distance of 10m	Inductive applications
140 – 148,5kHz	37,7dBµA/m at a distance of 10m	Inductive applications
6,765 – 6,795MHz	42dBµA/m at a distance of 10m	Inductive applications
13,553 – 13.567MHz	42dBµA/m at a distance of 10m	Inductive applications
26,957 – 27,283	42dBµA/m at a distance of 10m	Inductive applications
402 – 405MHz	25 µW effectively radiated power Channel separation up to 300kHz	Medical implant communication

Table 3.3 Frequency bands allowed for inductive applications and medical implants from the Norwegian Post- og teletilsynet, FOR-2007-04-20-439.

From an energy point of view, we are interested in transferring as much energy as possible through the inductive link before and during the measurement, ensuring stable operation and correct results. This implies a high transmission frequency if the amplitude is fixed. However, absorption in biological tissue and energy loss is larger with increasing frequency. In addition, the efficiency is affected by different frequencies. Thus, an optimal frequency would occur if it were to be measured on a complete implanted working system, with one type of coil, separation distance and alignment. Because patients are different, implant-depth can vary and other parameters can differ, this optimal frequency can only be found by a qualified guess during system construction. Also, the biological damage in the tissue when radiated several times a day must be well inside the accepted levels (25). In addition, IEEE have done a project and stated safety levels with respect to human exposure in the frequency bands between 3 kHz and 300 GHz which should be followed (26). Similar projects reports on different transfer frequencies, and many around 13MHz (27) (28). In thread with these reports and the possible frequency bands in Table 3.2 and Table 3.3, 13.56MHz is chosen as transfer frequency when designing the following circuitry (rectifier/chargepump and regulator).

3.6 Considerations around coil design

To ensure the energy transfer, we need two good coils in the system. One placed on the implant, and one on the external unit. Let us first look at the implanted. One of the design goals of the implant is size, making it as small as possible. The coil may be the largest single unit on the implant. It should be made planar, and ideally integrated on the implant. It is possible to make a coil on the silicon wafer, together with other electronics. With this solution the implant will be very compact and without too many components mounted on it. The coil can be placed around on the chip where it is space for it, filling the “holes” in the electronic. This solution however, is difficult to both make and calculate. We saw in equation (3.7) the geometrical shape of the inductor played a role in its inductance, and it may be difficult to ensure the needed power and signal transfer in this way.

A planar coil as discrete component mounted on top of the implant may in the first prototypes be the best choice. In this way the two coils (implant and external unit), can be made similar in geometrical shape and even size. When it comes to shapes, square and circular are commonly used. Even though circular coils give better performance because of the lower self resistance[15], square coils are often used because of its simplicity during fabrication. In addition, the shape and mounting on the implant can be done in a way helping to keep the implant in place and not allow it to rotate as this is crucial for the alignment against the external coil. The fabrication material of the coil has, like the rest of the implant, of course to be bio-compatible, like gold or platina. Further protection between the coil and the tissue at the implanted site should be considered for patient comfort and lower health risk. Examples are noble metals, types of soft sealing like bio-compatible rubber and other types of housing for the implant. As for the coil in the external unit, this is not so critical.

The main goal when designing and choosing coils are making the power and signal transfer strong enough under all circumstances. From equation (3.9) we remember the placement of the two coils affected the mutual inductance. The coils should therefore be made in the light of the two unit’s placement to one another. This means in practice choosing coils from their size, shape and value in a trade off between coupling and misalignment sensitivity (29).

[15] A geometrical fact which is true if the coil material (copper leaders in example) has equal resistance per length as each windings in the square coil would be longer (in distance) compared to the circular winding.

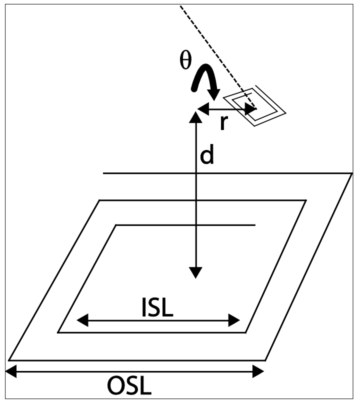


Figure 3.8 Sketch of a planar coil showing the different geometrical parameters. Also, a second coil representing the transmitter/receiver is shown in top of the figure, describing the different misalignment parameters which is important for "good connection" between the two

If we describe the coil like Figure 3.8, *ISL*; inner side length, *OSL*; outer side length, *GR*; inner side length divided by outer side length (*ISL/OSL*), some rules of thumb comes in handy. For maximized coupling coefficient, the *OSL* of the external coil should be twice the separation distance for a *GR* of 0.8 and three times the separation distance for a *GR* of 0.2, yielding for separation distances of 0~30mm (29). In addition, an external coil with a smaller *GR* has a higher coupling coefficient at small separation distances (<20mm) but showing more sensitivity to axial separation. More important for our use is the sensitivity of lateral misalignment as the external unit can slide away from the implant during the patient's daily business. External coils with smaller *OSL* show the most sensitivity to lateral misalignment. Therefore, a larger external transmitter coil is desirable to ensure good coupling both in our project and other where lateral misalignment can happen. This often means a balance needs to be struck between higher working *k* and displacement tolerance.

Since a perfectly parallel placement of the two coils is optimal, it is important that the implant is not able to rotate. It will be catastrophic if the patient has to undergo another invasive operation because the implant has rotated. The external unit should be given as much area of placement as possible. Movement is unavoidable during use and its affect on the performance should be as little as possible. An alarm for the user when the external unit looses contact with the implant could maybe be included in the finished system, but interference with the patient daily life should be avoided as far as possible. We will not in this chapter or this thesis go further in on coil analysis, but the interested reader will find good material in (30) (31) (32).

Chapter 4

4 Rectifier and Charge Pump

From the most fundamental physics, there are two ways to transport electrical energy in wires. One, and the most common in low-voltage system, is direct current, shorted DC. The other is the alternating current, shorted AC, and is in far more use in high-voltage systems. We can convert between these two ways of energy in different ways based on which voltages and currents that are used. In this chapter we will look at ways of converting between AC and DC, called rectification. We will first look shortly at some basic physics before investigating some different topologies and fundamental ideas. Three different circuits and simulation results will conclude the chapter.

4.1 pn-junction and diode

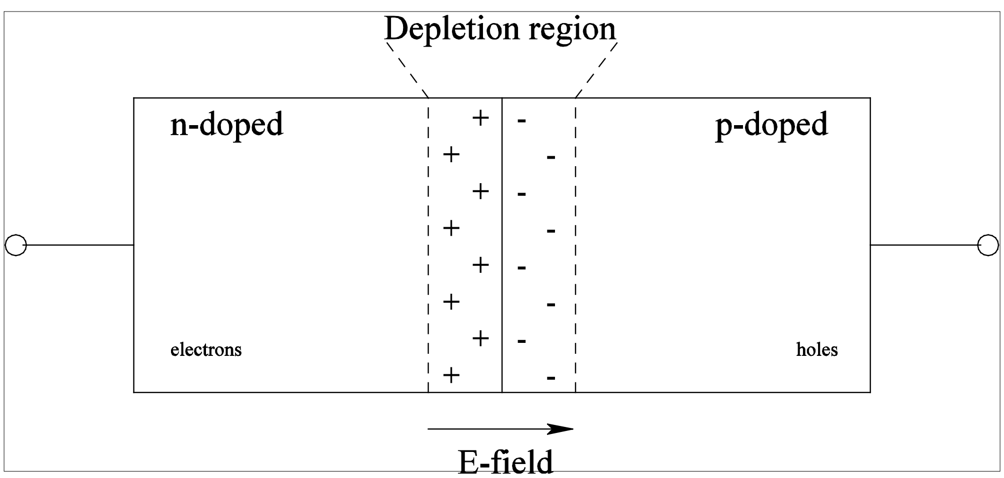


Figure 4.1 Ordinary pn-junction

In the literature regarding rectification, which is a quite old knowledge, *diodes* are used for performing the conversion from AC to DC. These diodes can be looked at as nothing more than a *pn-junction*. This combines two semiconductors of p-type and n-type placing them together, as in Figure 4.1. As p-type and n-type semiconductor are both relatively conductive, this junction should be able to transport electrical current. However, by placing them together, a nonconductive layer, the depletion zone, is formed by electrons and holes recombination. This means, in steady state where no external voltage is applied on either n- or p-type regions, the junction acts as a resistance, blocking for any current transfer. This blocking resistance can be manipulated by applying voltage across the junction, either as forward or reverse bias. As forward bias, the p-type region is connected to the positive terminal of a battery, and the n-type region to the negative. This causes the holes in the p-type and electrons in the n-type push toward each other, reducing the depletion zone between them. This lowers the barrier in potential, and can be looked upon as a decrease in resistance. With increasing bias voltage, the nonconductive depletion zone becomes so thin that the charge carriers can flow through it and across the barrier. Thought of as resistance, this means such a low value that the current is ideally not affected. We will however see when designing diodes, the resistance is still present, causing a voltage drop across the junction.

As reversed biased, the potentials from the battery are switched, connecting the p-type region to the negative battery terminal and the n-type region to the positive. This pulls the holes in p-region and electrons in the n-region away from the depletion zone, widening the nonconductive area. Again, thought of as a resistance; leading to higher resistance between the two areas. This will of course block all current from passing through the junction and the diode is non-conductive. By increasing the reversed bias potential, the depletion zone and the resistance will increase until the potential reaches the diode’s breakdown voltage. This effect is caused by a large increase of the electrical field across the two areas, and the junction becomes conductive. These effects, often spoken about as *Zener* or *avalanche* breakdown processes, are frequently in use, often for safety in various means as the breakdown is non-destructive. However, this breakdown will be against our cause, and will not be discussed further.

4.2 Diode in CMOS

In the none-ideally world, making diodes is somewhat more complicated than described in the past section. In CMOS 90nm technology, diodes can be made with starting point in a transistor. There are four essentially different ways, or connections, of doing this which all performs like a diode. These four

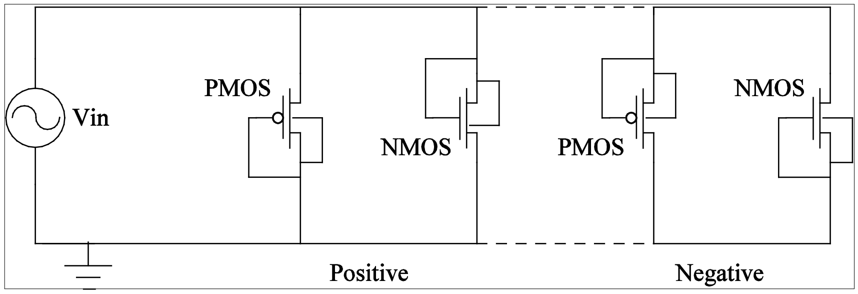


Figure 4.2 Four different transistor-based diodes

topologies, two NMOS- and two PMOS-transistors, are drawn in Figure 4.2. Although their differences in connection, they all make the standard pn-junction.

As mentioned above, the junction will always contain a resistance, even when strongly forward biased. This dynamic resistance leads to a threshold of conduction, meaning that the voltage across it needs to exceed a certain level before the junction becomes conductive. For making the rectification as efficient as possible, this voltage should ideally be zero, or as low as possible as we want the highest possible voltage on the rectified side of the junction, i e. not allowing the junction to “steal” too much of the available voltage level. Using diodes with low threshold voltage and a steep conduction curve (like a Schottky diode) is therefore preferable. Also, by connecting the gate of the transistor to a potential and not letting it float, the performance of the diode can be changed. By connecting it to one of the sides of the pn-junction, some ordinary transistor characteristics can be used. This means, for an NMOS positive rectification diode, connecting the gate to the input of the diode increases the rectification performance as a channel is created below the gate, analogue to ordinary use of transistors. This lowers the conduction barrier and the resistance through the diode. The negative side of this is the leakage current which are slightly increased.

Simulations of these diodes were done by using Cadence (Hspice) as analysing tool. The Amscad STM 90nm process provides four different transistor types depending on which voltage to be used. These are 1V, 1.8V, 2.5V and the 3.3V transistors. The difference of these transistors is the thickness of the oxide layers and wells. The different types have some different parameter values, and the most important for diode-design is the threshold-voltage. Table 4.1 shows these thresholds for the four different types[16].

[16] The 1V type does also include two other transistors beside the standard which is referred in table 1. These are a special low-threshold type and a high-threshold type. The low-threshold would be preferable to use as the voltage loss across would be minimum, however, for the reasons given later, using the 1V transistor type will not be possible in this application.

Device	**V_t - 1V 1µm/0.1µm**	**V_t - 1.8V 10µm/0.2µm**	**V_t - 2.5V 10µm/0.28µm**	**V_t - 3.3V 10µm/0.38µm**
NMOS	0.24V	0.48V	0.48V	0.57V
PMOS	0.29V	0.48V	0.45V	0.53V

Table 4.1 Threshold voltage of different STM 90nm transistor types, all minimum length and 10µm width.

Based on the application and the need for a high voltage internally on the implant, one should choose the transistors used for diodes with care. First, the transistor diodes must withstand the voltage applied to them from the external unit. Second, it must be oversized in a balanced way; giving headroom for boosting the applied voltage if needed, but at the same time having low threshold voltage (which is realised with low voltage transistors). The internal V_{DD} voltage and the size of the storage capacitor must be calculated and chosen for providing enough energy for the whole measurement, conversion and transfer of the measured result. A calculation of the storage capacitor size is to be found in Appendix A[17].

As we want, for now, to place a voltage as high as 3.3V across the storing-capacitor, using the 3.3V transistors is natural. However, it will not be used in this thesis. Cadence H-spice has not built in simulation models for these 3.3V types. And in addition, as one wafer is only compatible with one of these different devices in addition to the standard 1V transistors, the 2.5V device is chosen for more flexibility with other circuits to be produced on the same wafer.

[17] This calculation is performed by assumptions of the energy consume of the implant circuitry, and is not the final value. This capacitor value should be chosen after a more complete simulation/prototyping of the whole circuit and its energy consume.

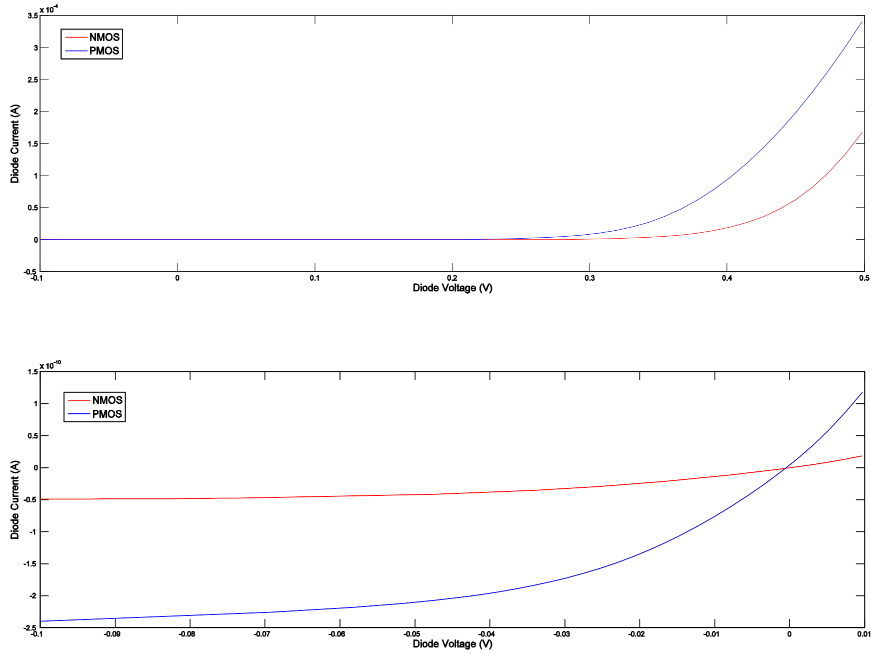


Figure 4.3 Diode current in positive rectification

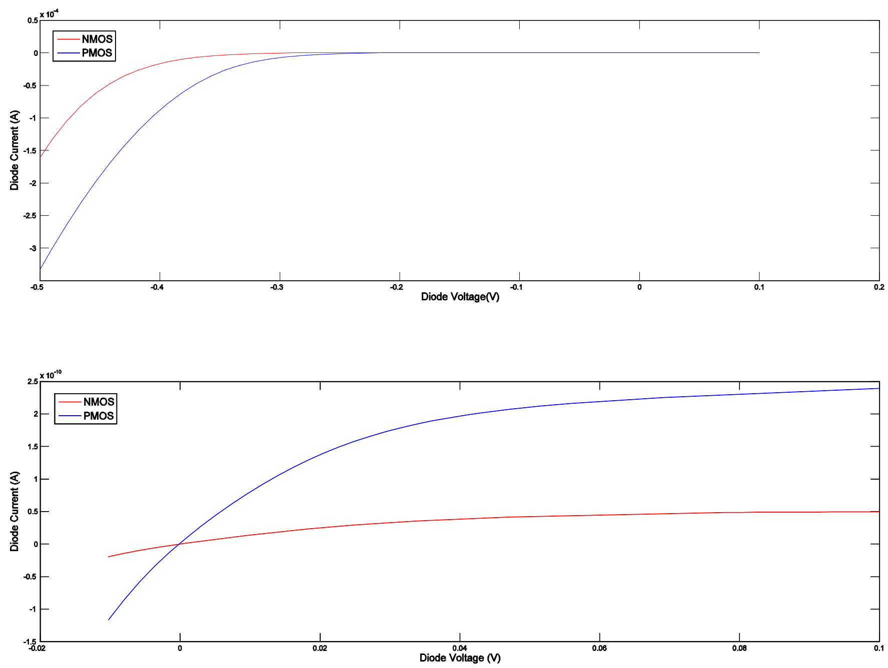


Figure 4.4 Diode current in negative rectification

From Table 4.1, the 2.5V transistor types have threshold voltages of 0.48V and 0.45V for NMOS and PMOS respectively. This gives the PMOS an advantage as it will not steal too much of the available voltage compared to the NMOS. Figure 4.3 and Figure 4.4 shows NMOS and PMOS rectifying in both positive and negative ways respectively. The current through the diode is plotted on the y-axis versus the voltage across the diode on the x-axis. It is clear that PMOS starts to conduct current a lot earlier than NMOS, and in the chosen voltage range, it is superior. The leakage of the diodes when reversed biased are also shown. We see the PMOS has a larger leakage current than NMOS. However, these currents are in the pA region, and the lower leakage current of NMOS will not defend the disadvantage of higher conduction/threshold voltage. The mobility difference between NMOS and PMOS gives NMOS an advantage however, as the mobility of electrons are better than for holes. This indicates, if maximum voltage is desired, PMOS should be used. If maximum current trough the diode in a certain voltage range is preferable, NMOS should be chosen. Thus, the load of the diode becomes important. Figure 4.5 shows simulation of NMOS and PMOS diodes with 100Ω and 1kΩ loads respectively. Both the input amplitude, frequency and the transistor sizes are the same. The input waveform is also displayed for a quarter of a period. The lower figure shows the property of NMOS which easier leads more current and thus, drives smaller loads. When the load becomes large, as in the upper figure, a smaller current will pass through the system and the PMOS will dominate. This is primarily due to the lower V_t. It is also noticeable the point of conduction, as in both cases the PMOS leads current earlier than the NMOS. This, together with the voltage difference between the three curves, is as we could expect from Table 4.1.

In the finished system however, the load of the rectifier is more complicated than just a single resistor. It will, based on the different topologies later discussed, be a combination of capacitors and resistances from the following circuitry. Small capacitors, in the loading circuitry, behaves like an open circuit for dc, the impedance is >1kΩ. The circuit following the rectifier, the regulator discussed in Chapter 5, should have an large input impedance. Also this supports the choice of PMOS as diode. There is however one noticeable point to consider. The large storage capacitor which the rectifier will try to charge to a given voltage, will behave as a short when the system is turned *on* (the impedance is approximately zero when the storage capacitor is “empty” and consumes all available current during the early stages of the power up). However, later investigation and simulations will still show an advantage by using PMOS instead of the NMOS as diodes. We will therefore primarily use PMOS transistors as diodes.

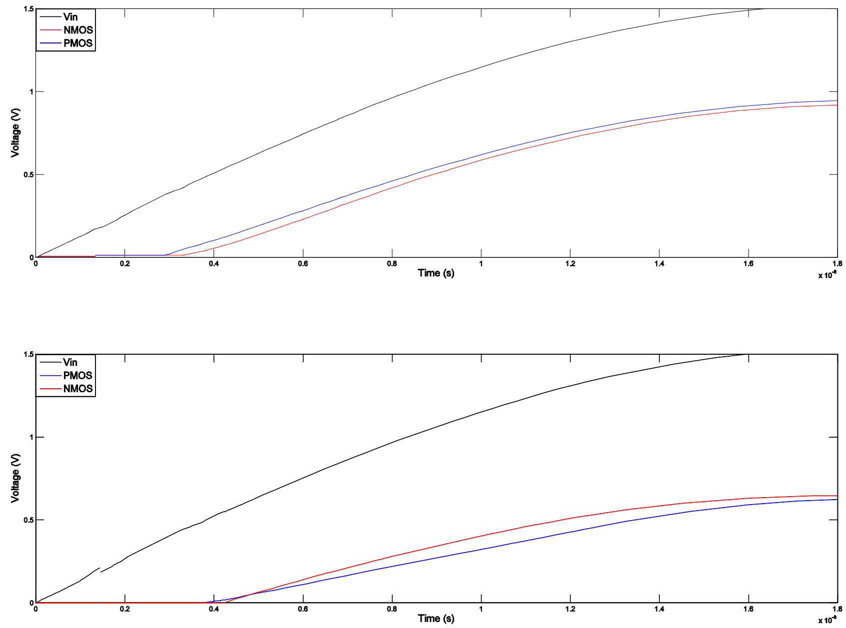


Figure 4.5 Output voltage from two diodes across a resistor. Upper: 1kΩ. Lower: 100Ω. The input of the diode is also displayed

4.3 Rectifying topologies and possibilities

In the following we will use *diode* when we denote the pn-junction formed with the chosen PMOS-transistor. We will also use the diode figure in addition to diode-coupled transistor figure (like in Figure 4.2) when drawing circuits and schematics in the rest of this chapter. Three different circuits are presented, first considered in general matter, and later the results of the performance of the circuit are presented.

4.3.1 Rectifying Circuit 1 – The Circuit

Consider the rectifier topology shown in Figure 4.6. This is a semi full-wave rectifier consisting of two diodes and two capacitors. It is formed by connecting two half-wave rectifiers (just a single diode) to one of the AC-inputs. This results in a full rectification of this single input. The second input is in this case the reference or ground lead. Both diodes are diode-connected CMOS transistors as mentioned earlier. For the cause of testing, the DC-positive rectification diode is a PMOS, the DC-negative rectification diode is a NMOS.

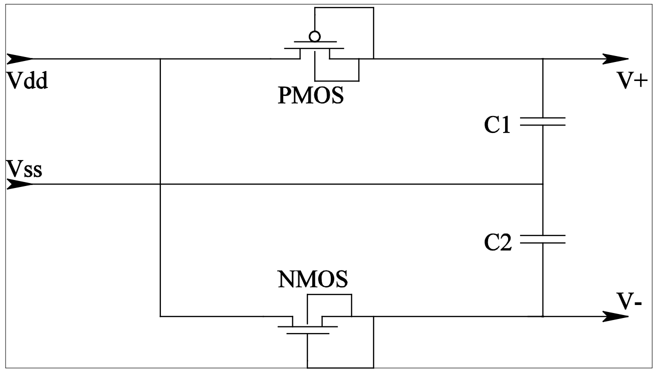


Figure 4.6 Semi full-wave rectifier topology

A brief analysis gives the functionality of the circuit: In the positive half-period of the input, the DC-negative rectification diode (NMOS) is turned *off* and no current ideally flows through this lead. The DC-positive rectification diode (PMOS) is turned *on*, and current flows through the diode and in to the capacitor. This current ideally starts to flow when the voltage across the diode passes the threshold voltage of the diode-coupled transistor. When the input voltage falls back below the threshold-voltage, the PMOS diode shuts off, and no current flows either ways. This sequence is repeated in every positive half-period of the input until the voltage across the capacitor reaches its maximum value. At this stage, only a small current is flowing replacing the leakage current which is present in the negative half-period of the input signal. The maximum voltage across the capacitor when it is fully charged is given by

$$V_{C1} = V^{+}{}_{peak} - V_d \tag{4.1}$$

where V_d is the voltage drop across the diode. In the DC-negative lead, the functionality is the same as for the positive, only in the opposite way: When the input is at its negative half-period, the DC-negative NMOS diode is turned *on*, and the DC-positive rectification diode (PMOS) turned *off*. As the input voltage is lower than the voltage across capacitor C_2, current starts to flow from the capacitor and out through the diode. Again, this is repeated in every negative half-period of the input until the voltage across C_2 reaches its peak value, given by

$$V_{C2} = V^{-}{}_{peak} + V_d \tag{4.2}$$

As these two voltages, V_{C1} and V_{C2} together add up to the total output voltage, we can derive the formula for V_{out}:

$$V_{out} = V_{C1} - V_{C2} = V^{+}{}_{peak} - V_d - (V^{-}{}_{peak} + V_d)$$
$$\downarrow \tag{4.3}$$
$$V_{out} = V_{peak-peak} - 2V_d$$

The second part of formula 4.3 is true if V_d of both diodes are the same. For achieving high V_{out}, it is important to keep the voltage drop across the diodes at low levels. In order to do so, low-threshold transistors are available in some processes, and these transistors should then be preferred. This is the case for the 90nm STM 1V supply transistors. However, for the 2.5V supply option, low-threshold transistors are not available. Instead, we need to look at the formula for the V_d of a transistor in order to reduce this voltage.

For easier notation, let us consider an NMOS diode-coupled transistor in a positive rectifying lead. Since the gate and drain are short connected, the transistor works in saturation region. From the transistor current formula in the saturation region we can derive

$$V_d = V_{ds} = \sqrt{\frac{2I_{ds}}{\mu_n C_{ox} \frac{W}{L}}} + V_{th} \tag{4.4}$$

as a formula of the voltage drop (33) (34). As we want the lowest possible V_d, it is clear that choosing transistors with the lowest V_{th} is preferable as already mentioned. In addition, the *W/L* relationship also affects the voltage drop. Thus, by making the transistor wide and short will give us better performance and a total lower V_d. This can easily be realized intuitively by thinking of the transistor channel as a resistance. By making the channel wide and short, the resistance is reduced and so is the voltage drop. Table 4.2 shows the different parameter values of the circuit in Figure 4.6.

Device/Parameter	PMOS	NMOS	C1	C2
Width	100μm	100 μm	-	-
Length	0.4 μm	0.4 μm	-	-
Value	-	-	11.43pF	11.43pF

Table 4.2 Device-parameter values for circuit in Figure 4.6

The capacitors require a large fraction of the chip-area for values of tenths of pF. Finding the most efficient capacitance per area is therefore important for keeping the circuit size to an acceptable level. The capacitor values are also important for the performance of the circuit, as these limits the maximum current through the circuit according to $I_{max} = V_{p-p} \times C \times freq$ for an AC input signal. From the equation, we see a large capacitance is needed for maximising the current throughput and for driving larger loads. The 90nm-STM kit provides a range of different capacitor types, varying in layer and field of use. Four of the most useful for this application are listed in Table 4.3. Because of the superior capacitance per area, the Poly-Well capacitor will be used in this and the following circuits. The high capacitance/area value makes large capacitors on-chip possible, and is suited for our use despite the unlinearity. This is because the exact capacitor value is not critical, as we only want as large capacitance as possible. A change in capacitance during pumping period will not change the final output voltage; only the pumping time will be affected as the value changes with changing voltage across it. Figure 4.7 shows the change in capacitance for a 20 x 200µm capacitor over a voltage range of -2V – 2V. The value is low when the voltage across it is approximately zero. With rising voltage, the capacitor value increases almost exponentially and reaches acceptable values fast enough for our application. In the layout the Poly-Well capacitors are made from ordinary PMOS transistors, using the gate as one plate, and connecting the drain, bulk and source together as the other. This makes a *Poly-PWell* capacitor in the size according to the width and length of the original transistor. One could argue against this method of making a capacitance by pointing on the well known gate-leakage current present in the CMOS transistor. This current is absolutely not wanted as it becomes wasted energy and decreases the efficiency of the circuits. Therefore, if available, high-threshold transistors should be used for making such a capacitor as their gate-leakage current are smaller than for standard- and low-threshold transistors. However, later circuits and simulations shows a highly dependence between output voltage and capacitor values, making the leakage current well worth sacrificing in exchange of higher capacitor values on-chip.

Type	**C typ ($fF/\mu m^2$)**	**Remarks**
Fringe Capacitor	1,20	Total allowed capacitance: 100fF<C_{tot}<10pF
Metal Plate Stacked	0,10	
MIM Capacitor	2,00	
Poly-Well	6,30	Unlinear

Table 4.3 Different capacitors and values available in 90nm-STM (from the STM process documentation)

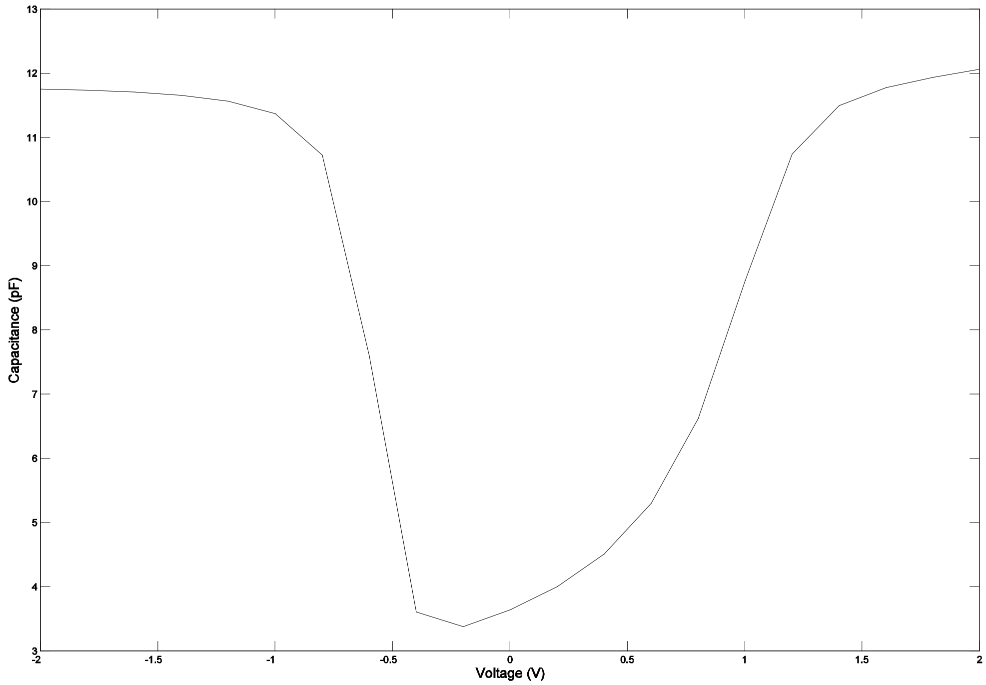


Figure 4.7 Capacitance of a Poly-PWell capacitor 20 x 200µm

4.3.2 Rectifying Circuit 1 – Simulation Results

As a first approximation, we excite the circuit with a 13.56MHz sinusoidal input with 1V amplitude and put $V_d \approx V_{th}$. From formula 4.3 and Table 4.1, we can calculate the expected output voltage:

$$V_{out} = 2V - 0.48V - 0.45V = \underline{1.07V} \tag{4.5}$$

This brief calculation does not take into account the effect of any load impedance. And in addition, the 1V input amplitude also needs to enter the diodes without any damping. In the following paragraph we will argue for how to test the circuit for the most realistic results.

The circuit in Figure 4.6 is simulated in Cadence (HSpice) and Figure 4.8 shows the test bench. The input is a sinusoidal voltage source with 1V amplitude and frequency of 13.56MHz as used in the calculation above. A 50Ω resistor, R_S, is added in series from the source. This is for making the source non-ideal and giving more realistic results. This value of resistance may however not be a perfect choice. From chapter 3, R_S is a complex impedance which value is given from the inductive link and the resonance circuit. Although we can affect its value by choosing other component values, it cannot be explicit chosen and therefore it will be decided from other parts of the system development than adapting it to the rectifier and chargepump alone.

In addition to the circuit under test, two ideal capacitors are used to simulate the effect the connection-pad will have on the measurements on the produced chip. Further, following in parallel, an ideal resistor is placed between the outputs. This load resistor R_L modulates the following circuitry, and should be chosen to best adapt the expected input impedance of this. Last, a 200nF storage capacitor C_S is connected. The rectified charge from the system is placed across this capacitor and the measurements are done on this element.

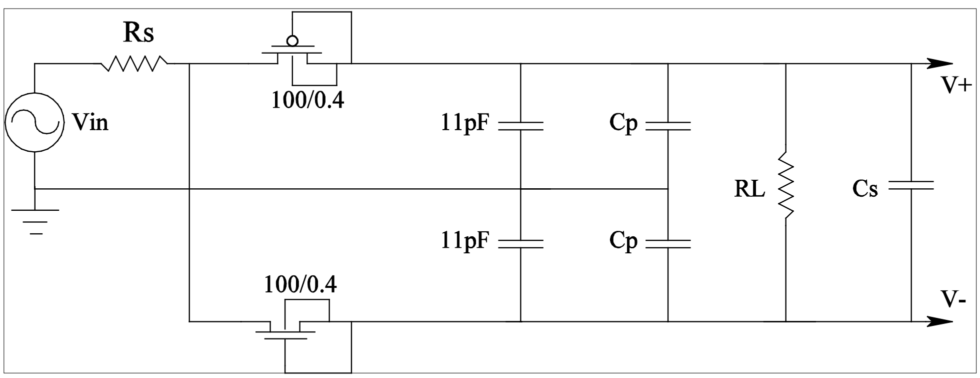


Figure 4.8 Circuit topology of rectifier test bench

Parameter	V_{in}	Freq	R_S	C_P	R_L	C_S
Basic setup	$2V_{p-p}$	13.56MHz	50Ω	10pF	100KΩ	200nF

Table 4.4 Element values from the Circuit 1 test bench

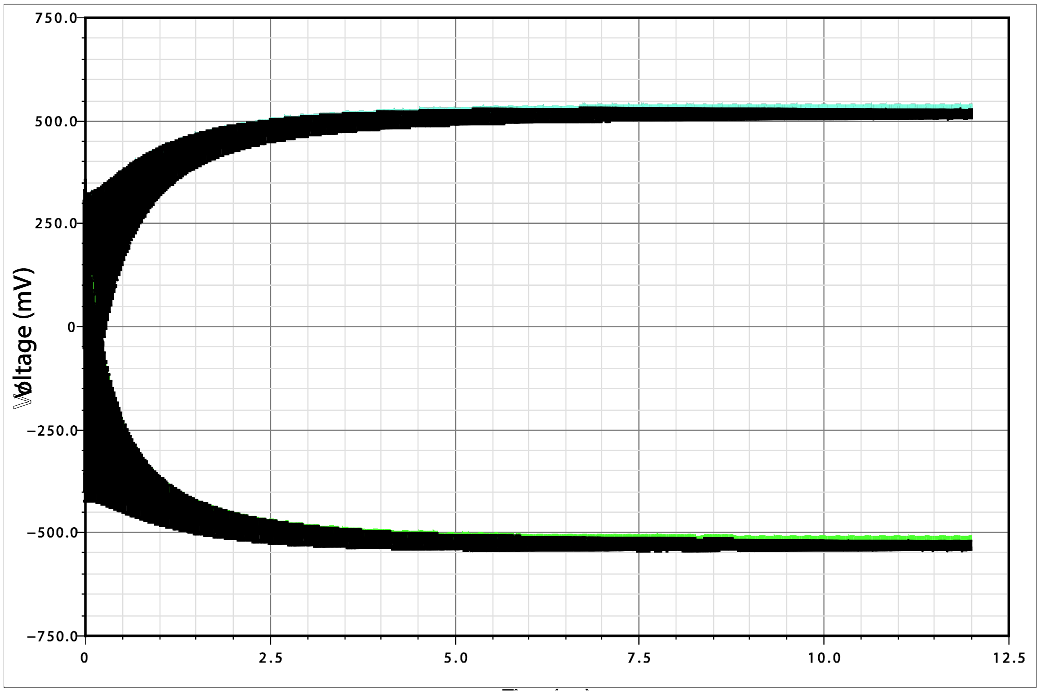


Figure 4.9 Simulated output voltage, basic setup

Measurement @12ms	Positive max	Positive min	Negative max	Negative min	Output Voltage	ΔVin
Schematic simulation	543.95mV	509.40mV	-471.15mV	-505.69mV	1.0151V	1,98825V

Table 4.5 Performance of Circuit 1, basic setup

Figure 4.9 shows a 12ms transient analysis of the circuit. The chosen parameter values are given in Table 4.4. In addition to the already commented values, C_P is set to 10pF. This is a roughly estimate for the value of capacitance the pad on the chip will generate. This value is kept trough all the following measurements. The load, R_L, is set to 100kΩ. This fairly high value of resistance shows the circuits fully voltage potential and at the same time allows some leakage current. In the final system, this resistance will probably be lower and also not simply resistive. However, simulation and measurement with this value gives an indication on what performance we can expect from the diodes and the circuit.

All start-up conditions are zero, and clearly from the graph, the output voltage starts at zero. Early in the simulation, during power up, the voltage varies in a high amount. This variation is wearing off as the voltage rises, and is at its minimum when the capacitor reaches maximum output voltage. This variation, as from now on called ripple, is found in both positive and negative lead. Table 4.5 shows the measured key-values from the simulation. After 12ms, the output voltage (positive max – negative max) has become 1.0151V. At this output voltage, the ripple in the positive lead are of 6.4% and in the negative 6.8% of the (individual) maximum output value respectively. The effect of the ripple caused by the input through the diodes are not wanted and will occur as a variation on the power supply (V_{DD}) for the following circuitry. The ripple also increases in amplitude as the load increases (R_L decreases in value). However, the ripple in both positive and negative lead tends to be in phase, meaning if the two outputs are referred to one another and not to an external ground, the output voltage will seem steadier. In the finished system, this is how the V_{DD} and V_{SS} shall be generated and used. Thus, if the two leads of the rectifier do not shift phase individually (away from each other), the ripple may not be a problem.

The output voltage of 1.051V is about half the input peak-to-peak voltage. We see the brief calculation done earlier suits well with the simulated results. The ΔVin value of 1.98825V from Table 4.5 is the effective input voltage swing across the diodes, meaning the voltage obtained behind the input resistance, R_S. For obtaining the voltage across the two diodes, ΔVin is divided by two and positive max and negative min respectively is subtracted:

$$V_{diode+} = \frac{\Delta Vin}{2} - positive\,\max = \frac{1.98825V}{2} - 543.95mV = 450.02mV \qquad (4.6)$$

$$V_{diode\div} = \frac{\Delta Vin}{2} - negative\,\min = \frac{1.98825V}{2} - 505.69mV = 488.44mV \qquad (4.7)$$

By recalling the threshold voltages from Table 4.1, we see the obvious relationship and the measurements are as expected. We also want to know the efficiency of the circuit. The voltage amplitude across R_S is

$$V_{R_S\,ampl} = \frac{V_{in} - \Delta V_{in}}{2} = \frac{2 - 1.98825}{2} = 5.875mV \qquad (4.8)$$

The *rms-voltage* across R_S assuming a perfect sinusoidal input are given by

$$V_{R_S\,rms} = \frac{V_{R_S\,ampl}}{\sqrt{2}} = \frac{5.875mV}{\sqrt{2}} = 4.154mV \tag{4.9}$$

The current through the resistor is given by Ohm's law

$$I_{R_S\,rms} = \frac{V_{R_S\,rms}}{R_S} = \frac{4.154mV}{50\Omega} = 83.080\mu A \tag{4.10}$$

The power consumed by R_S is

$$P_{R_S} = V_{R_S\,rms} \times I_{R_S\,rms} = 4.154mV \times 83.080\mu A = 0.345\mu W \tag{4.11}$$

The total power provided by the source is

$$P_{in} = V_{in\,rms} \times I_{R_S\,rms} = \frac{2V}{2\sqrt{2}} \times 83.080\mu A = 58.746\mu W \tag{4.12}$$

The power consumed by R_L based on 1.0151V_{DC} is

$$P_{R_L} = \frac{V_{R_L}^2}{R_L} = \frac{1.0151V^2}{100K\Omega} = 10.304\mu W \tag{4.13}$$

This means, the power lost in the diodes is

$$P_{diodes} = P_{in} - P_{R_S} - P_{R_L} = 58.746\mu W - 0.345\mu W - 10.304\mu W = 48.097\mu W \tag{4.14}$$

The rectifying efficiency without taking the R_S loss into account is then

$$\eta_{efficiency} = \frac{P_{R_L}}{P_{R_L} + P_{diodes}} = \frac{10.304\mu W}{10.304\mu W + 48.097\mu W} = 17.64\% \tag{4.15}$$

Thus, the efficiency of the rectification, based on sinusoidal signals with zero phase shifts is 17.64%. This calculation shows how and where energy disappears in the circuit. However, because of the large load resistance, R_L, the system goes into cut off, in the meaning of the system cannot deliver more voltage (charge) across the R_L, but it is possible to deliver more current. An upper limitation of available current is set by the AC charge formula for capacitances. This means, if the load resistance R_L is reduced, the output voltage will not change significantly as long the current needed is inside this limitation. For circuit one, this upper limitation is

$$I_{\max} = V_{p-p} \times C \times freq = 2 \times (11pF + 10pF) \times 13.56MHz = 570\mu A$$

which at 1.07V output gives an optimal power throughput of

$$P = U \times I = 1.07V \times 570\mu A = 610\mu W \ (at\, 1.88k\Omega)$$

If the small decrease in output voltage is weighted against the increase in current, the total efficiency of the system will increase. Simulation and calculation in Cadence and MatLab shows in Figure 4.10 the relationship between efficiency and different resistance values[18]. A ridge is forming at $R_L \approx$ 12kΩ. The efficiency increases with increasing R_S. This seems at first glance strange, as one could expect the opposite. The reason for this is however because we do not include the R_S loss in the calculation. Therefore, the circuit is at its most efficient at low currents (if R_S was included, the efficiency would drop because of the voltage drop (and current limitation) across this resistor with increasing value). At R_S = 950Ω however, the efficiency is at 27%. From the form of the graph, we see this tendency probably will continue beyond the measured values in the figure. With increasing R_S, the current through the circuit decreases as mentioned, and the available power on the rectified side decreases in the same amount. We want however as much available power as possible delivered to the following circuitry, and therefore we want to know the power we can expect from the circuit with different input and output loads. Figure 4.11 shows this relationship. The z-axis is now available power across the output resistance, while the x- and y-axis are the same as before.

As we could expect, the available power from the circuit with the same input conditions held constant, is clearly increasing with lower R_S values. The peak of the curve is placed at R_S = 50Ω and R_L = 2.5kΩ and the available power is ≈ 80µW. This means, for maximising the power throughput, a low R_S and an R_L approximately of 2.5kΩ is optimal. The simulated efficiency at this R_S and R_L values is ≈ 19% which gives a theoretical power of:

$$P = P_{theoretical} \times efficiency = 610\mu W \times 19\% = 116\mu W$$

We see the optimal simulated power throughput is below our calculated value. This is not so strange. The calculation does not incorporate the voltage loss across R_S, which implies a lower effective peak-peak voltage for the pump to

[18] The MatLab scripts used for the three calculations are to be found in Appendix B together with the raw-data file.

utilize (when calculating I_{max}, we did the simplification of using the source input voltage as $V_{p\text{-}p}$, and not the real input voltage for the circuit found behind the R_S resistance). In addition, the capacitances used changes value according to the voltage applied to them. The value used for calculation (11pF) may therefore not be precise the value found/used during simulation. Actually, from the type of testbench used, the voltage across capacitor C1 and C2 newer excides the maximum individual lead voltage referred to ground. This implies the value of these capacitors is reduces according to Figure 4.7 and further limits the maximum current throughput. We note the simulated optimal R_L is somewhat higher than calculated. This suits well with the lower current throughput because of the reduced capacitance.

Finally, we can multiply these two curves and obtain an illustration of which conditions gives the largest available power most efficiently. Figure 4.12 shows this relationship. We clearly see the peak coming from the power-figure and also the ridge behind it coming from the efficiency-figure. Together, this gives an optimal operation area where R_S is small and $R_L \approx 4\text{k}\Omega$.

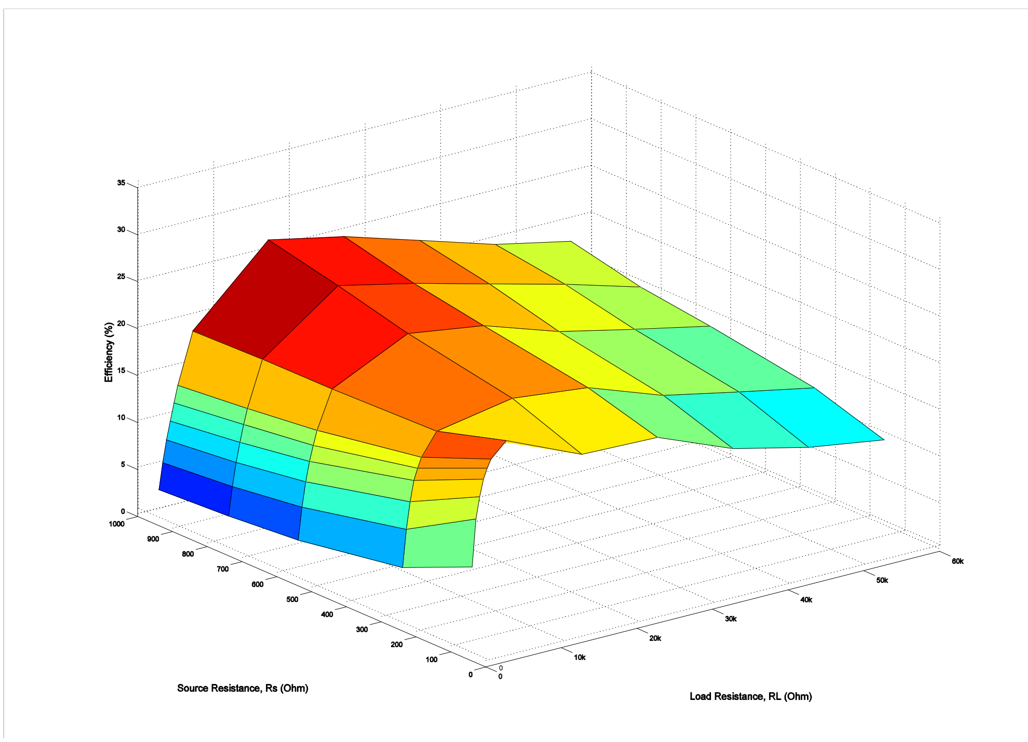


Figure 4.10 Efficiency of rectification, Circuit 1

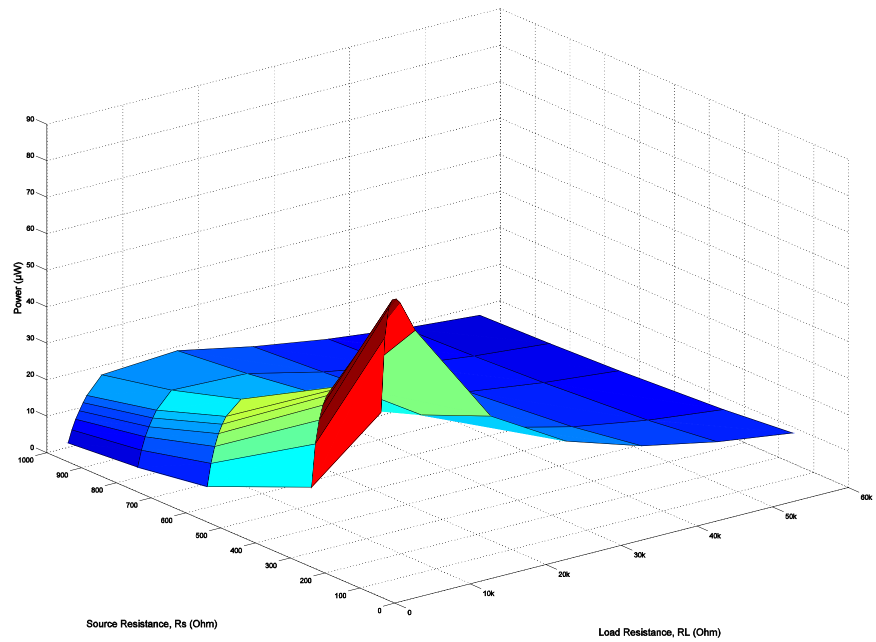


Figure 4.11 Available power on the output, Circuit 1

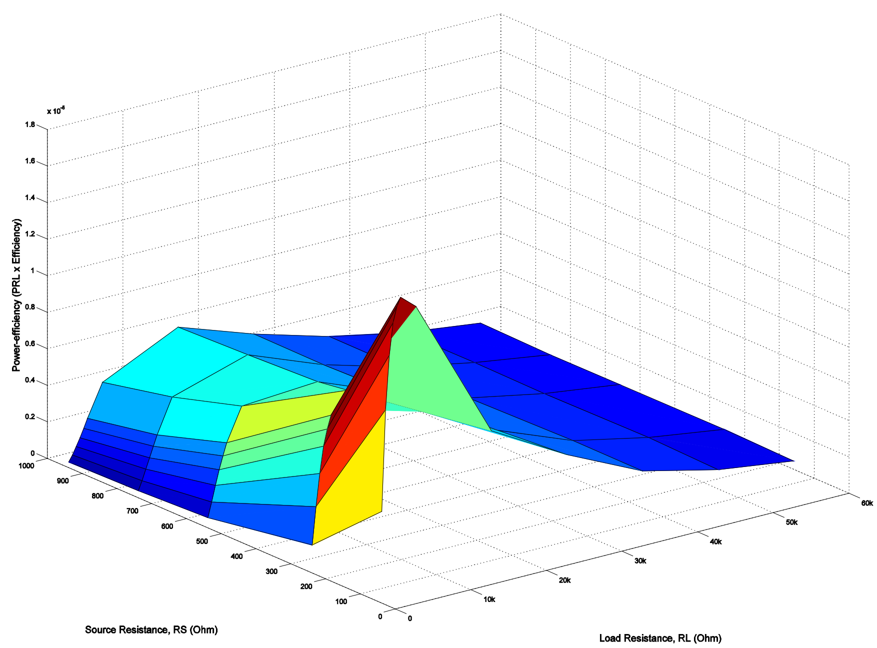


Figure 4.12 Efficiency multiplied with Available power. Shows which circumstances that provides the most available power most efficient, circuit 1C

4.3.3 Rectifying Circuit 1 – Production

This circuit was produced together with this thesis` supervisor, Philipp Häfliger, who actually made the layout. This layout is shown in Figure 4.13. The total size of the circuit became 100µm in length and 65µm in width. The capacitors dominate the picture with its large poly-areas. The two transistors are bent into ten fingers each, and displays on the left side of the red capacitors.

Although the circuit was sent to production, there were not found enough time to make the measurements[19]. Instead, time and effort was concentrated on developing and simulate alternative circuits. Therefore, the only results available are the simulated, and obviously, no comparing between simulated and measured results is conducted.

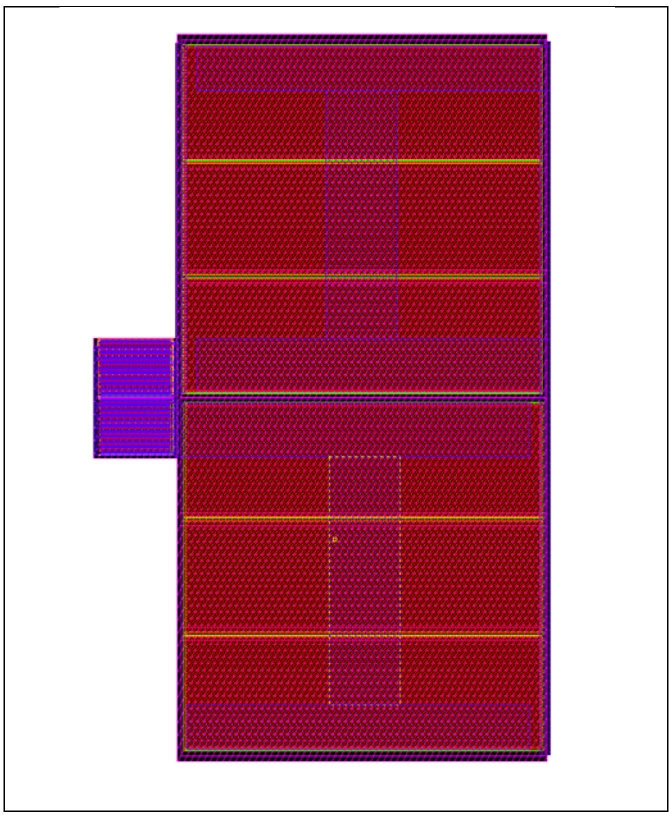


Figure 4.13 Layout of Circuit 1. The total size is 65µm x 100µm

[19] A PCB for testing the different chargepumps was developed together with a fellow student, Trygve K Halvorsen, and the layout of it is to be found in Appendix D.

4.3.4 Rectifying Circuit 2 – The Circuit

The second rectifier is a semi full-wave rectifier and chargepump, developed from (33) (35). Figure 4.14 shows the schematic drawing of the circuit. It consists of two rectifying diodes, eight pumping diodes and ten capacitors, making the circuit rather large in size. From the positive input lead, two PMOS diode-coupled transistor is to be found. These are the rectification diodes for V_+ and V_- respectively. PMOS diodes/transistors are chosen because of its lower threshold voltage compared to the NMOS. This is especially important in such a circuit when there are multiple diodes connected in series. We will later see the threshold voltage of each diode is subtracted from the possible output voltage when calculated. The transistors are internally connected as illustrated earlier in the chapter. This way of connection provides the lowest resistance and threshold when the diode is forward biased. The leakage is however limiting the performance, but still, the PMOS transistor with the sown connection gives overall the highest output voltage. The capacitors C_{in} works as the pumping mechanism in addition to being DC-blocks. Not allowing any current that are being pumped flowing back to the input and the source. Capacitors C_s are storage capacitors for each step in the chargepump.

For understanding the functionality of the pumping mechanism, Figure 4.15 shows a single step, consisting of two diodes and the additional capacitors. Capacitor C_n and C_{n-1} can be looked upon as DC-voltage sources under steady state. Coupling capacitor C_{in} combines the input voltage V_{in} and V_{n-1}. This means, on the negative half-period, or steady state, we can obtain

$$V_C = V_{n-1} - V_{tn-1} \tag{4.16}$$

and

$$V_C = V_n + V_{tn} \tag{4.17}$$

where V_{tn} is the voltage drop across the diodes. If the transistor type and W/L relationship of the two diodes are the same, they have the same voltage drop ($V_{tn} = V_{tn-1}$) and by combining (4.16) and (4.17) we obtain

$$V_C = \frac{V_n + V_{n-1}}{2} \tag{4.18}$$

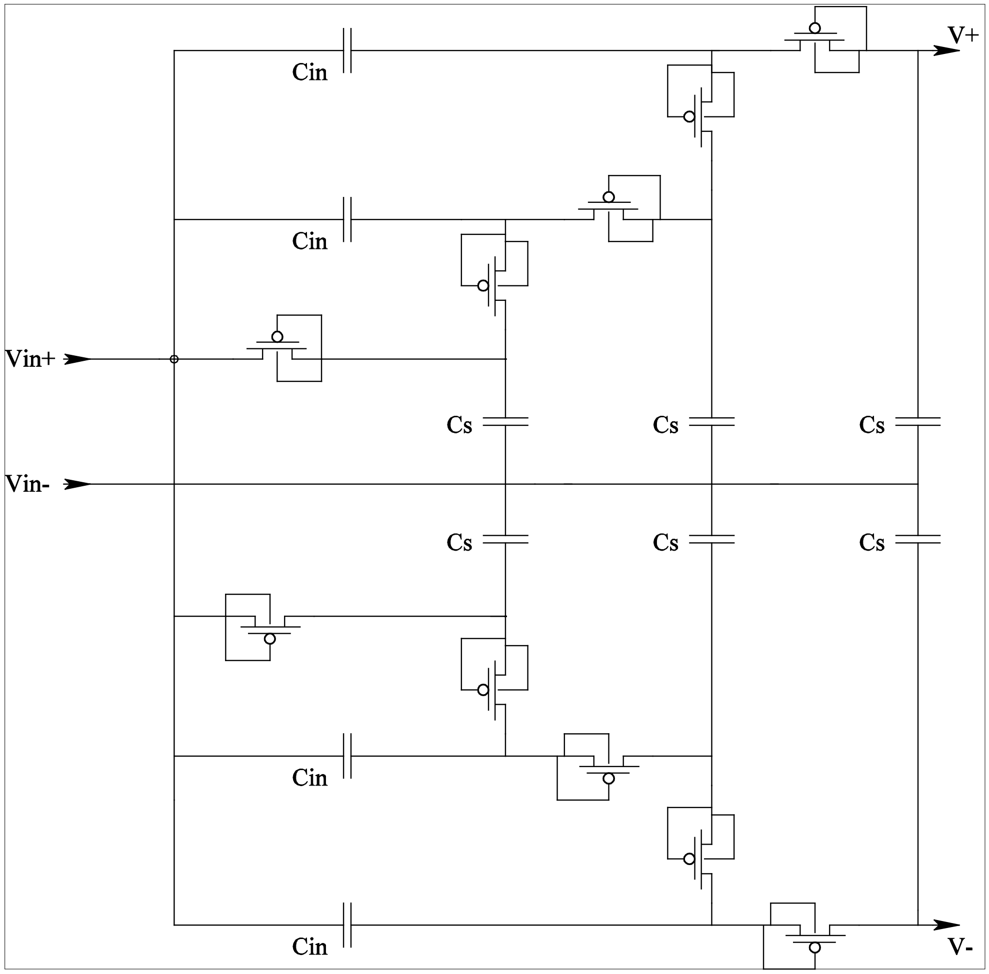


Figure 4.14 Circuit 2 schematic

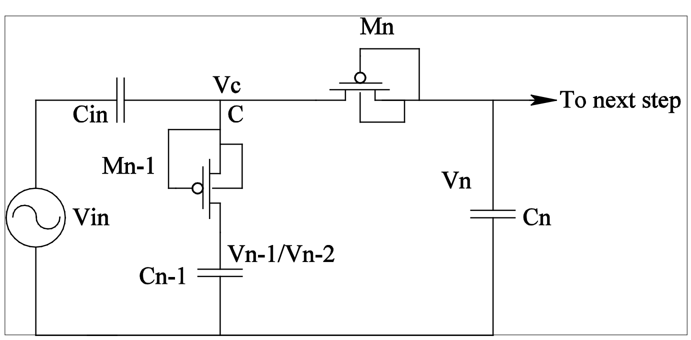


Figure 4.15 Schematic Circuit 2, single step

Then, when the next positive half-period arrives, the voltage in the V_C junction becomes

$$V_{C_{pos}} = V_{C_{neg}} + V_{in} \tag{4.19}$$

This means, the input signal for M_n is the voltage in junction V_C at the earlier negative half-period, added with the input amplitude in the following positive period. Now assuming ΔV is a unit increment

$$\Delta V = V_{in-amplitude} - V_{tn} \tag{4.20}$$

and combining it with (4.18), we obtain

$$V_n = \frac{V_n + V_{n-1}}{2} + \Delta V \tag{4.21}$$

$$\downarrow$$

$$V_n = V_{n-1} + 2\Delta V \tag{4.22}$$

From this we can generalize and say that the pumping step in Figure 4.15 can be any step in the chain. And because the unit increment also applies to the first rectification diode, the output voltage can be written as

$$V_n = n\Delta V = n(V_{in} - V_{tn}) \tag{4.23}$$

where n is the number of the transistor in the pumping chain and V_{in} is the voltage amplitude of the input signal. Formula 4.23 applies to the positive lead if all the diodes are of same type and size. For the negative lead we assume the same unit increment as the diodes are the same, and with the same sizes as in the positive lead. This means the total output voltage from the chargepump becomes

$$V_{out} = 2n\Delta V = 2n(V_{in} - V_{tn}) \tag{4.24}$$

The general essence of chargepumps' working mechanism and also in this pump, is formula 4.19. Every step in the pump utilizes the voltage from the previous step as an offset, and adding the input amplitudes (the peak-to-peak voltage) on the offset signal. By doing this, higher voltages are obtained by adding more steps in the pump. In the ideal case, this can be carried on forever, pumping the output voltage to infinite. In reality, many factors are present to not give such a performance. Stray capacitances and resistances are added in each step and diodes are not ideal so leakage is an issue. But most important is the efficiency of the circuit. The efficiency in each of the higher steps is decreased (because of longer current paths, increasing stray capacitances and so forth), making them less and less valuable. For this reason, a weighting between using higher input voltage and fewer steps versus lower input voltage and more steps with respect to overall power transfer efficiency has to be done. Also, as each step demands two capacitances added in both leads, size becomes an issue as the capacitances are rather large. For these reasons, we use two pumping steps (in both positive and negative lead) in this circuit.

The same points of consideration regarding sizes and parameters yields here as for circuit 1. We will therefore not repeat the arguments for sizes and transistor types, but Table 4.6 shows the different parameter values chosen for circuit 2.

Device	**PMOS**	$\mathbf{C_{in}}$	$\mathbf{C_S}$
Size	100μm/0.38μm	12.344pF	12.344pF

Table 4.6 The chosen parameter sizes for Circuit 2

The chosen parameters are based on a weighting between theory and H-spice simulations of the circuit. Figure 4.16 and Figure 4.17 shows two parametric analyses used in this matter. In the first figure, the transistor widths vary while all other parameters are kept constant and R_L = 50kΩ. We see the 50μm transistors (red) perform well in this simulation and are the most symmetrical around zero (ground) of the three. Also, its positive output is the highest compared to the other. The 100μm transistor (blue) is not so symmetrical and has a lower positive output voltage compared with 50μm. The negative output voltage is however better. The total output of the two ($V_{DD} - V_{SS}$) gives the 50μm transistor an advantage as it is a few millivolts better. The 150μm transistors show the highest negative output of the three, but the worst positive. Its total output voltage is also lower than the other two. In addition, the 150μm transistors obviously occupy the most chip-area.

But why choose the 100μm transistors? From the theory, large transistors should perform better than smaller because of its ability to deliver more current and charge (less resistance). This means if the environment changes, if the input amplitude and/or the load are increased/decreased, the picture will change. In the final product, it is difficult to estimate good values of both input and output conditions. A conservative choice is therefore the 100μm transistor despite the larger size and larger stray capacitances.

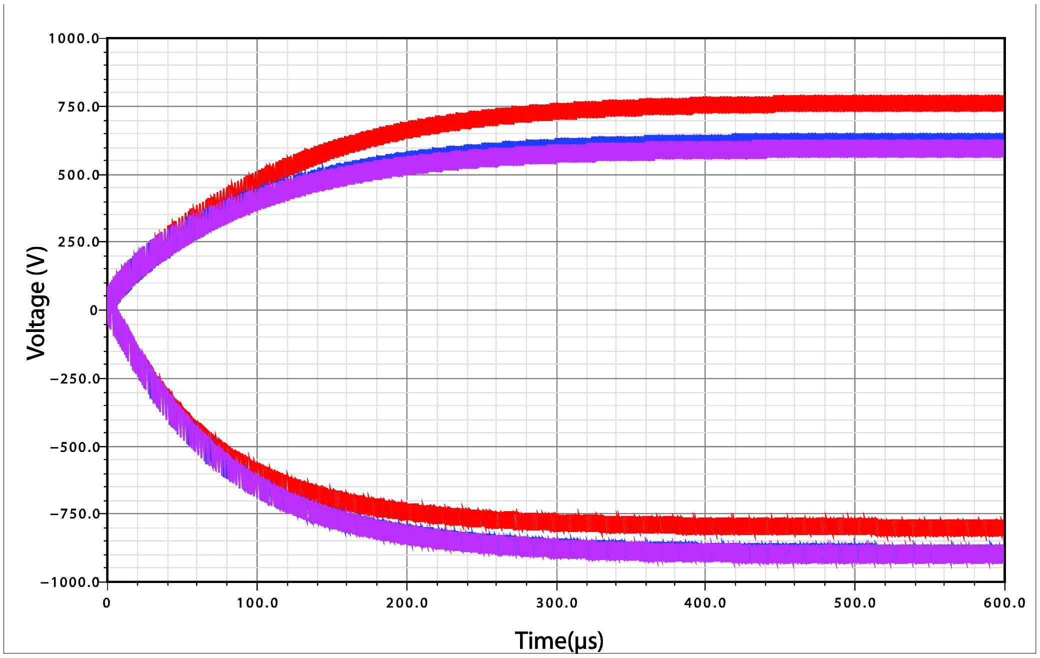


Figure 4.16 Parametric analysis of the transistor widths in Circuit two: Red = 50μm, Blue = 100μm, Pink = 150μm (Basic setup, R_L=50kΩ)

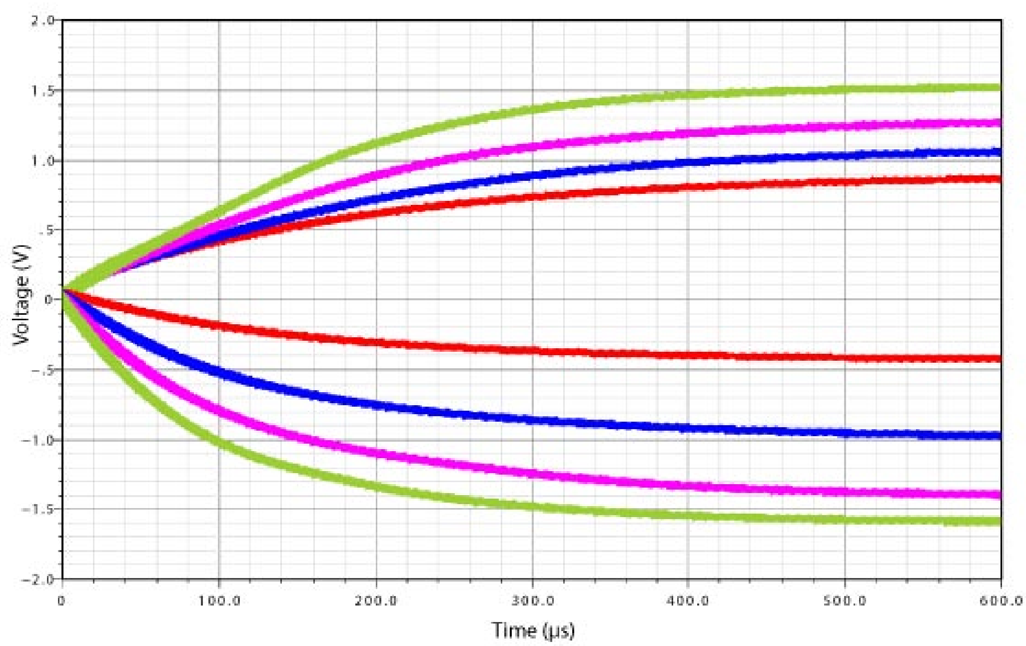


Figure 4.17 Parametric analysis of capacitance sizes: Red = 5pF , Blue = 8,8pF, Pink = 12.6pF, Green = 16,4pF (Basic setup)

Figure 4.17 shows the output voltage of different capacitor values. Both C_{in} and C_S are varied simultaneously, they always have the same value according to the parametric simulation. All other parameter values are kept the same through the simulation. The red inner curves are of 5pF value. This gives the lowest output voltage of the different sizes simulated. Also, we note the difference in the positive and negative output voltages. The positive side seems more efficient than the negative for this capacitor value. As the value increases, the output voltage increases dramatically. This is due to the current limitation as discussed for circuit one, as the load resistance used for simulation is small enough to pull all available current out of the circuit. The value of the pink curve is 12.6pF, nearest to the used 12.3pF in the produced circuit. We clearly see the advantage of the large capacitors on the output voltage. For this capacitance value, the different *individual* output voltages have changed compared with the 5pF measurement, and now the negative side seems more efficient. This trend can also be seen in the last, 16.4pF measurement. These not balanced and individually changing relative output voltages are caused by the change of performance of the Poly-PWell capacitor used. From the graph in Figure 4.7 we saw how the capacitance changed with changing voltage. Because this change is not equal on both sides (not balanced around zero) it affects the output voltage of the two leads differently. By comparing the output voltage from Figure 4.17 and the capacitance graph in Figure 4.7, the relationship and the reason for the difference in output voltages becomes clear[20]. As the charging time of the circuit is not severely affected, large capacitors are to prefer due to the current limitation. However, as there are ten capacitors in the circuit, the chip-area becomes quickly and issue and has to be considered (for this reason, as augmented for in circuit 1, the Poly-PWell capacitor is used). All values are chosen according to Table 4.6 from a weighting between performance and area consumption.

4.3.5 Rectifying Circuit 2 – Simulation Results

For a first approximation the circuit is excited with a 13.56MHz and 1V amplitude sinusoidal signal, the same as for circuit one. From formula 4.24 and Table 4.1 we can make an estimate of what to expect of output voltage

$$V_{out} = 2n(V_{in} - V_{tn}) = 2 \times 5 \times (1V - 0.45V) = \underline{5.5V} \tag{4.25}$$

[20] For a fully adequate argument for this reason, Figure 4.7 should be plotted for every capacitance value in Figure 4.17 to show the exact change in value with respect to voltage for each capacitor. However, as the shape of the curve is almost similar for the different capacitances and we in this only wants to find the reason for the different output voltages of the two leads, only the 12.3pF (Figure 4.7) is shown and used for demonstrating the issue.

This brief calculation does not take into account the effects of a large load resistance. Also it does not incorporate the effect of a possible source resistance but assumes 1V effective input amplitude across the circuit. Also, the differences of performance with different capacitor sizes are not accounted for and we will see from the simulations that this will affect the output voltage.

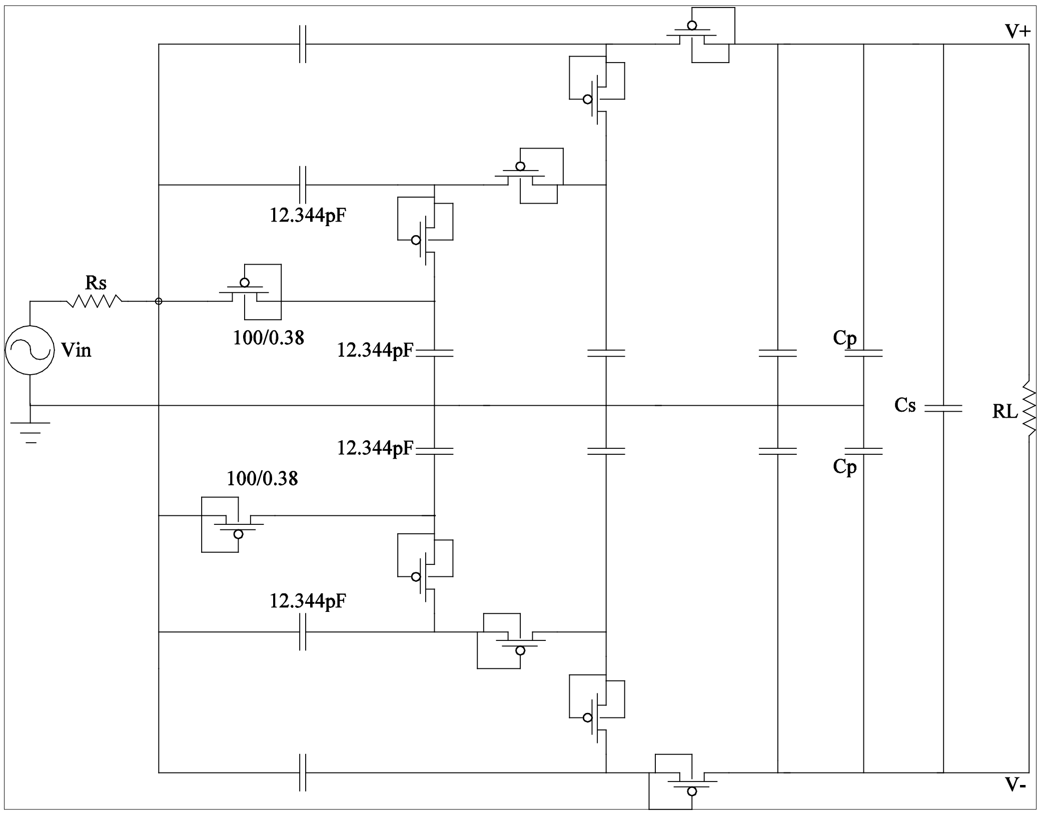


Figure 4.18 Circuit 2 testbench

Parameter	V_{in}	Freq	R_S	C_P	R_L	C_S
Basic setup	$2V_{p\text{-}p}$	13.56MHz	50Ω	10pF	100KΩ	2nF

Table 4.7 Parameter values of basic setup

Figure 4.18 shows the test bench used for simulations in Cadence. Table 4.7 shows the parameter values for the test bench elements. For comparing the results of the simulations from circuit to circuit, the basic setup is similar for each. However, in this circuit, the storage capacitor, C_S, is changed from 200nF to 2nF. This reduces the convergence time of the output voltage. With 200nF the simulation would take too long and use too much storage space. These relatively “longer” simulations with this 2nF capacitor give a better image to compare with the other circuits instead of a “shorter” simulation with the 200nF capacitor. This means, the source of error with the 2nF capacitor is the difference in final output voltage to what it would be with a 200nF capacitor. With a 200nF C_S, the simulation time would not be long enough to see what the final result of the simulation would be. This is a larger and more severe error than using the 2nF, and for this reason, the storage capacitor is changed.

Figure 4.19 shows a 1 ms transient analysis of the circuit with the basic setup shown in Table 4.7. The two outputs have splitted up nicely and we see the circuit pumps the two leads to a positive and a negative output voltage respectively. From the curve forms, the output voltage has stabilized and further increase in output voltage cannot be expected. With the small 2nF storage capacitor, the transient shows the circuit need no more than 1ms to reach its maximum value. With the 200nF storage capacitor, this time would be significantly longer and the curve slopes not as steep as shown here. However, the output voltage would be approximately the same for the two capacitors if the pumping/simulation time was significantly long, i.e. a second or more. As for circuit one, the two outputs has a ripple. The outputs are as seen not individually stable, but because the ripples of the two leads are in phase, we got the same situation as for circuit 1.

In the test bench, the negative input is grounded and all input swing is applied to the positive. This is however not necessary, as all voltages are only relative to something and do not have to be compared to an external ground potential. From the circuitry point of view, it is of no concern whether or not the two outputs of the chargepump are stable compared to ground, only the relative difference of the two are of interest. This implies together with formula 4.19 in the previous subchapter, where V_{in} is the peak-peak voltage, that none of the inputs do necessary need to be grounded. The peak-to-peak voltage is the same when referred to the negative input, also when this is not externally grounded. In circuit 3 this will be demonstrated further when the test bench not is connected to ground but directly to the output of an inductor.

Table 4.8 shows the performance of the circuit, and at 1 ms we see the output voltage reaches 2.694V, and the different lead voltages and respectively ripples are also presented. The output voltage is about half of what was calculated, and the difference is therefore quit large. This is not so strange however, as we in the simulation loads the circuit, and the diodes used are not ideal and include leakage. A simulation of the circuit with 1MΩ load was performed to visualize the difference from the different loads. The plot is found in Appendix E and shows an output voltage of 5.485V which suits very well with our calculated value. The reason for this difference is the mentioned current limitation of the capacitors. The theoretical maximum current throughput is

$$I_{\max} = V_{p-p} \times C \times freq = 2 \times 12.344 pF \times 13.56 MHz = 335 \mu A$$

which at 5.5V output gives an optimal power throughput of

$$P = U \times I = 5.5V \times 335 \mu A = 1.842 \mu W \; (at\, 16.42 k\Omega)$$

We already now see without any further investigations that this assumption does not hold according to the simulations. Already at R_L = 100kΩ which is used in Figure 4.19, the output voltage does not fully reach 2.7V. According to our calculations, maximum output voltage of 5.5V should be delivered for loads >16.42kΩ. The reason for this is the changing capacitance values. This affects the output current more heavily than for circuit one because the voltage across the first storage capacitor never exceeds $V_{amp} – Vth = 1V – 0.45V = 0.55V$. At this voltage, the capacitance value from Figure 4.7 is not more than 5.2pF (this is actually also the case for circuit one, but that circuit had the C_P capacitance in addition to keep the capacitance fairly high). I_{max} now becomes

$$I_{\max} = V_{p-p} \times C \times freq = 2 \times 5.2 pF \times 13.56 MHz = 141 \mu A$$

which at 5.5V output gives an optimal power throughput of

$$P = U \times I = 5.5V \times 141 \mu A = 776 \mu W \; (at\, 39 k\Omega)$$

Still, the current is further limited in the circuit. This is probably caused by the long path the current must take for reaching the output. Although the capacitance values are higher in the later steps, all current must pass on to all of them before reaching the output, and we see this multiple component path limits the current severely compared to circuit one.

The mentioned ripples are 3.6% and 3.8% of the maximum value of the positive and negative lead respectively, somewhat better than for circuit one.

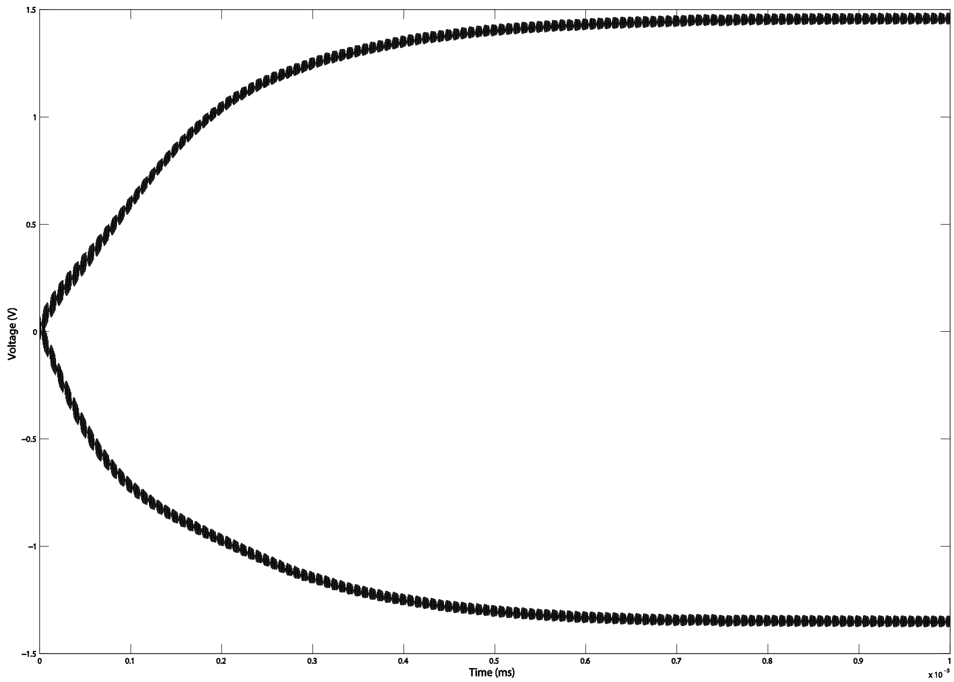


Figure 4.19 A 1ms transient analysis of Circuit 2 (basic setup)

Measurement @1ms	**Positive max**	**Positive min**	**Negative max**	**Negative min**	**Output Voltage**	**ΔVin**
Schematic simulation	1.485V	1.432V	1.376V	1.324V	2.809V	1,948V

Table 4.8 Performance of Circuit 2, basic setup

As for circuit one, we want to know the efficiency of the circuit and the rectification. Based on the schematic in Figure 4.18, we retrieve the simulation data through Cadence. In the same way as was described for circuit one, the efficiency is calculated and Figure 4.20 shows the result[21]. Now however, the same values for R_S is used but not for R_L. This is because the circuit did not show any maxima inside the original R_L limits. These are therefore increased and give the graph a larger “area” compared to circuit one. The reason for this

[21] The MatLab script used for calculation is the same as for circuit one. The result of the calculation and the raw-data file are to be found in Appendix B.

increase is because the current limitation of this circuit limits the load sizes it can power to feasible voltages. We also see this connection between loading of circuit one and circuit two in the power calculations done above and for each circuit. Maximum theoretical power throughput for circuit one was found at R_L = 1.88kΩ as it was for circuit two calculated to be at 39kΩ.

It is obviously clear, that the efficiency is also for this circuit very dependent on the load resistance. However, there are no pure uniformity and the efficiency peak is found at R_S = 50Ω and R_L = 233kΩ with a value of 52%. If we look at the area of the graph besides the peak, the efficiency is quite stable. However, for lower load values than the peak, the efficiency is rapidly decreasing. The R_S dependency is even more stable, and we see the large planar area of the graph for all higher values. However, the peak is found at the lowest R_S, not surprisingly, although the R_S loss itself is subtracted. Compared to circuit one, the efficiency is superior although it is obtained at higher loading values.

Again we want to know when to obtain the maximum power throughput of the circuit. Figure 4.21 shows this relationship. In contrast to the case of *circuit one*, the two graphs (efficiency and power) now follow each other more closely and the peak in both graphs is at about the same point. The plane shows maxima at R_L = 183kΩ and R_S = 50Ω. For this circuit, the maximum power is ≈ 84µW under these conditions, slightly better than for circuit one. The simulated efficiency at this R_S and R_L values is ≈ 38% which gives a theoretical power of

$$P = P_{theoretical} \times efficiency = 776\mu W \times 38\% = 295\mu W$$

We see the optimal simulated power throughput si below our calculated value, same as for circuit one. The theoretical calculation does not incorporate the voltage loss across R_S, which implies a lower effective peak-peak voltage for the pump to utilize. In addition, the capacitances used changes value according to the voltage applied to them as mentioned earlier. The value used for calculation (11pF) may therefore not be precise the value found/used during simulation. We note the *simulated* optimal R_L is higher than calculated. This suits well with the lower current and power throughput.

The point of where to operate the circuit with respect to the input and loading resistance becomes clear in both the two graphs, and the third, Figure 4.22 where the two are multiplied will of course only underline this assumption. A low R_S and a R_L = 233kΩ gives the largest available power and efficiency and is the optimal conditions for the circuit. This follows what is the general rule and behaviour of almost all electronics. Best performance is obtained when the output resistance of the foregoing circuit is low and the input resistance of the following circuit is high.

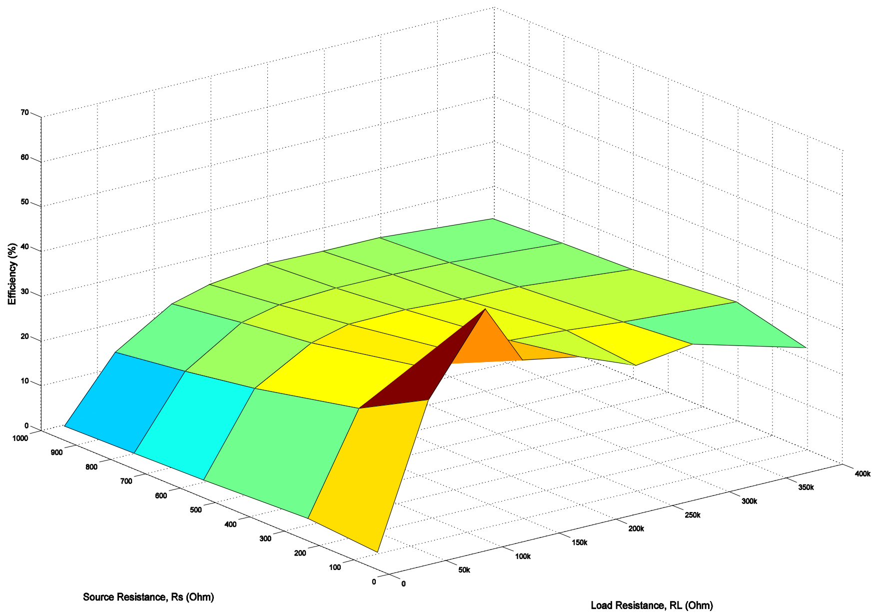


Figure 4.20 Efficiency of rectification, Circuit 2

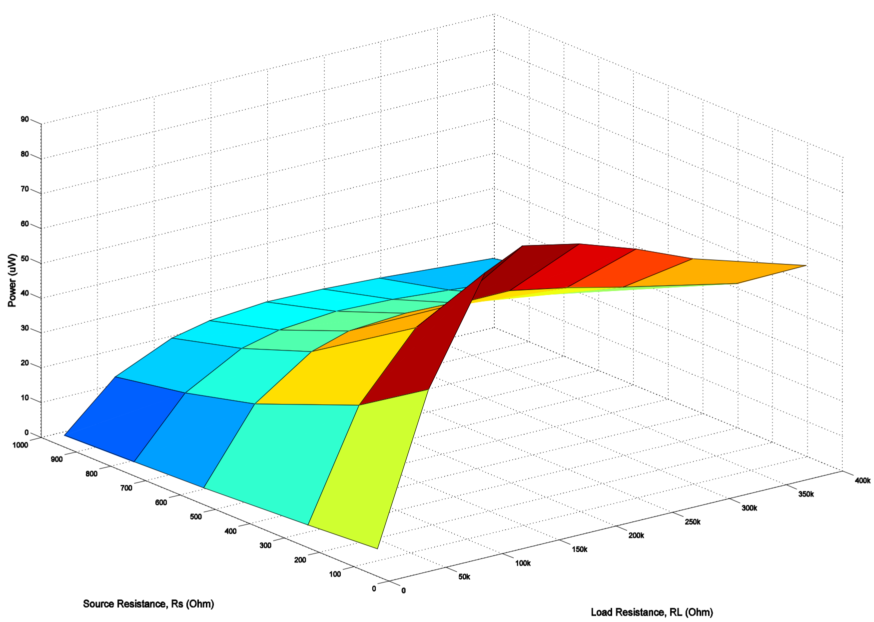


Figure 4.21 Available power on the output, Circuit 2

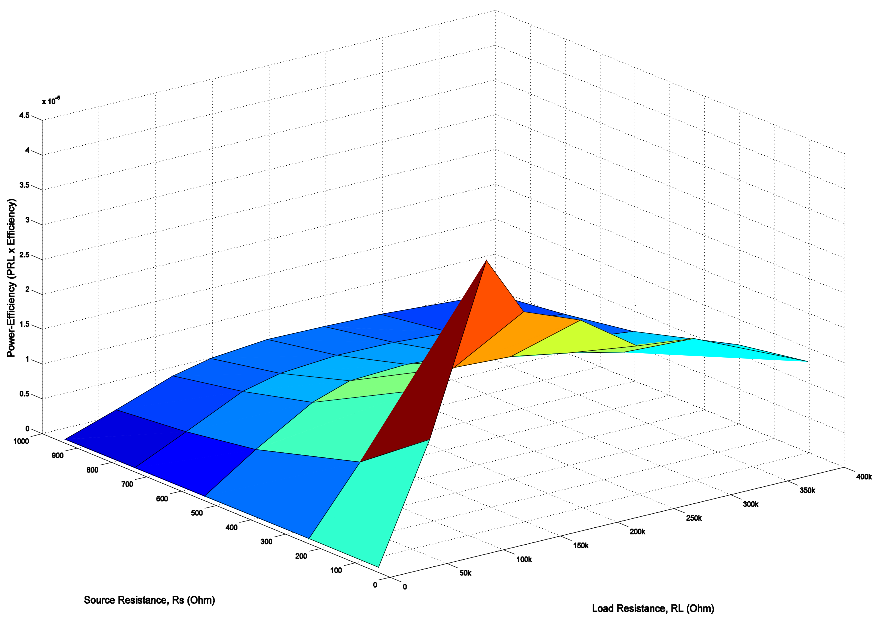


Figure 4.22 Efficiency multiplied with Available power. Shows which circumstances that provides the most available power most efficient, Circuit 2

4.3.6 Rectifying Circuit 2 – Production

The circuit layout is shown in Figure 4.23. The total size of the circuit is 330µm in length and 140µm in width. The capacitor dominates the picture with its large poly-areas. The transistors are placed in between the capacitors and not bent into any fingers, making a long contact area possible. Wide internal metal wires are used reducing the internal resistance for optimized current flow. The ground lead is placed in the middle of the circuit and all devices connecting to ground are placed around it. It is also carefully placed in a star-shape out from this centre lead, not forming any kind of loops where radiation can be picked up and become noise. This is especially important to keep in mind when we know which application such a circuit is used. The two outputs are carefully placed at distance from both ground and the input, making sure they are not affected by any of them, nor themselves.

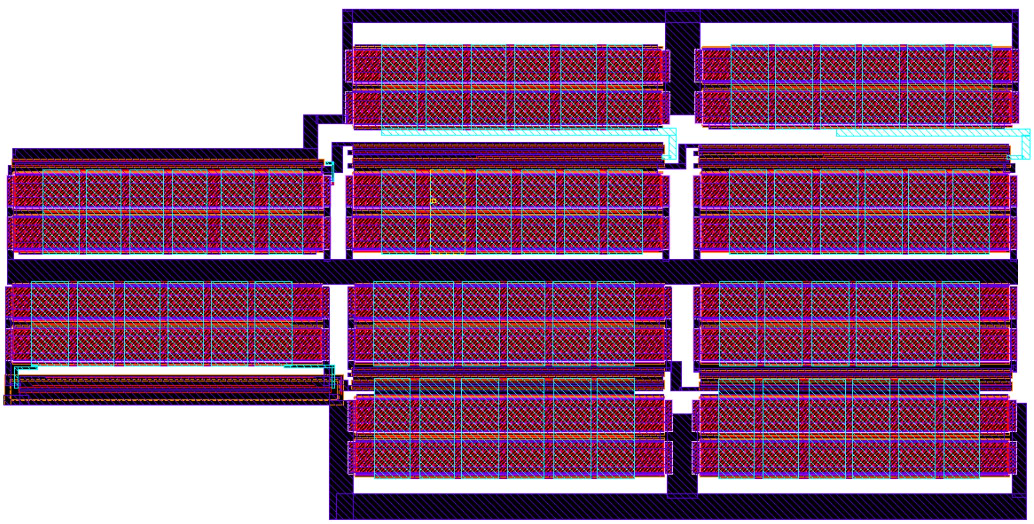


Figure 4.23 Layout of Circuit 2. Total size is 330µm x 140µm

4.3.7 Rectifying Circuit 3 – The Circuit

Circuit three is a full-wave rectifier followed by a single stage pumping unit shown in Figure 4.24. In difference from the earlier two circuits, this circuit utilizes both inputs in the rectification. This means, the negative V_{in-} are now not used as a reference node only, but as an input in the same way as the positive V_{in+} is used. This configuration is possible because the inductor used in inductive link obviously has two output connections which both alternates with respect to the sinusoidal input of the system. In the two foregoing circuits, we have only utilized one of them by forcing the other to ground in the test bench. This, in turn, means all the signal amplitude is taken out over one input alone. If the second input is not forced to ground but is instead floating, input swing can also occur in this input. By a symmetrical rectifier and chargepump, swing in both inputs is utilized without having to force a potential. In addition, inductor without centre tap can be used, as this topology does not use a stable reference for its pumping unit.

The first part of the circuit is a purely rectification part. This traditional and well known topology invented by Leo Graetz are broadly presented and can be found in almost any electronic teaching textbook in addition to (36). It is commonly referred to as a full wave rectifier and also a bridge rectifier. In difference from the first chargepump (circuit two), the *rectifier diodes* are here connected directly to the output of the circuit. In circuit two, we recall the current had to go through all the pumping steps before reaching the output. Here, both the rectifier and the chargepump are individually connected directly to the output. For the

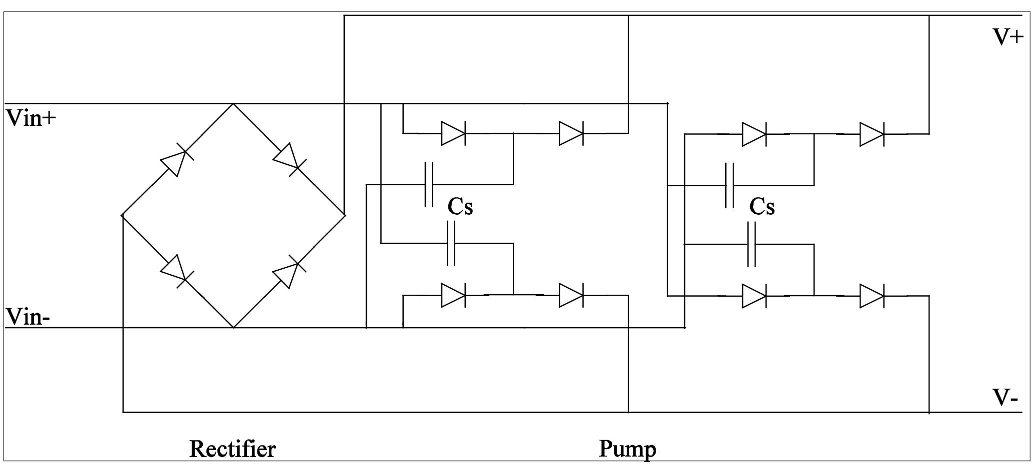


Figure 4.24 Schematic of Circuit 3

rectifier part, this means when the output voltage is low (or zero), the rectifying diodes will give an output voltage similar to the input voltage minus the threshold of the diodes. When the output voltage rises and exceeds the level of voltage the rectifier itself can deliver, this part is turned *off*, meaning that the diodes will always operate in cut-off and no current are flowing through this part. At this point on, only the pumping stage is active and leads current to the output. If the load is small (high resistance) so the output stays at a continuously high voltage, the rectifier will not have any purpose accept in the power-up phase when all the voltages were zero. This has some interesting qualities.

At power-up and when the output voltage is low, the current from the input does not have to go the long way through many pumping diodes before reaching the output. This gives a shorter start-up time. Second, if the load changes and the output fall below the point of conduction of the rectifier, this will again start to conduct, and the current will have an easier way to the output. And finally, as this part do not include any capacitances, we do not have the current limit issue as found in the other two circuits (in the chragepump part of this circuit, capacitances limits the maximum output current, but the rectifier alone do not. Therefore, the output voltage level is decisive for the current limitation). Summarized, this means if the load is small and easy to drive, we can obtain a high output voltage using the pumping stage. If the load is large and we struggle to deliver enough current, we use only the rectifying part, capable of delivering large currents at mediate voltage.

The functionality of the pumping unit is almost equal to the one in circuit two. In order to get an idea of this mechanism, let us consider the first four diodes and two capacitances connected right after the rectifier. In phase one, V_{in+} goes high and V_{in-} low. If we now look at the positive output lead, the first upper diode becomes conductive and current passes through to the capacitance C_S. The initial voltage across this capacitor is low because V_{in-} is low in this phase. At phase two, V_{in+} goes low and V_{in-} high, lifting the voltage stored on the capacitor the amount V_{in-} rises. At this moment, the first diode is turned *off* and the second, leading to the output, is turned *on* as the voltage on the capacitor rises to a level higher than the output. This cycle is then repeated for every input swing, and the same mechanisms occur at the negative pumping lead, here pumping the output lower for each time.

One point to consider however complicates this way of thinking. In difference from the pump in circuit two, we now have not got any stable point to reference any voltage to. This means all the voltages that are being considered are referred to (one of) the two phases. For example, let us consider the pumping unit if one of the input, say V_{in-}, are stable and with no input swing and the two outputs are connected to a capacitance as it will be in the real circuit. Again we look at the positive part of the first four diodes and two capacitors. Input V_{in+} goes high and V_{in-} stays the same (at a lower voltage than V_{in+}). The first upper diode becomes conductive and charge is placed on the storage capacitor C_S. In the next phase, V_{in+} goes low and V_{in-} stays the same (now at a higher voltage than V_{in+}). This means, the pumping effect of the charge capacitor is now no longer present as the V_{in-} input does not change. However, the output V_+ and V_- are lowered the amount of which the V_{in+} decreases from the positive to the negative phase. This means, referred to the stable V_{in-} input, the output voltages V_+ and V_- decreases, but referred to each other, as they both decreases with the same amount, they are stable. But V_+ now referred to the point we consider, the storage capacitor, have decreased below the voltage placed on C_S. The second diode therefore becomes conductive and pumping is still ongoing although we can say one of the inputs is "grounded". This behave results in the output signal from the pump which is internally stable, but seen referred to a ground potential, they are present in the way shown in Figure 4.25. Summarized, this means the circuit functions independent of input swing, whether the amplitude is to be found in one of the inputs alone or divided in some amount between the two. All input swing is therefore utilized. The same arguments can be applied to circuit two, and therefore as mentioned in the subchapter concerning this circuit, none of the inputs do necessary has to be grounded.

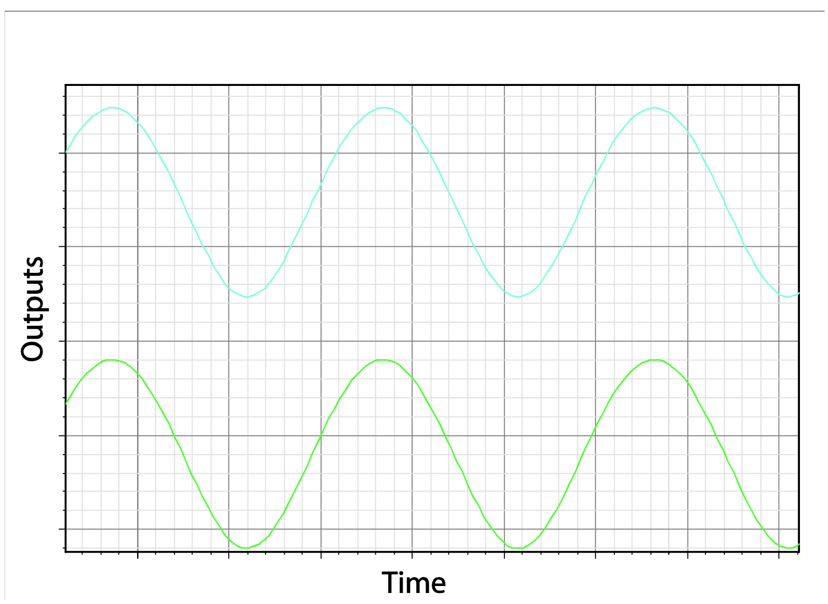


Figure 4.25 Outputs of circuit with grounded input. Output difference is stable

What is then the difference between circuit two and circuit three? Besides the difference in the schematic drawing, it is not very much. We can divide the difference into two cases: (1) If none of the inputs are grounded; the input swing in the negative input in circuit two will not be rectified but only used for the pumping mechanism. In circuit three, the swing in the negative will in addition to the one in the positive input be rectified. (2) If one of the inputs is grounded; the rectifying part of circuit three becomes the same as in circuit two. However, circuit three needs to shift the output voltage levels referred to a stable reference (as in Figure 4.25) in order to keep the pumping mechanism going. For circuit two, this is not necessary as it utilizes the positive input to drive the pumping and the changing output voltages referred to a stable reference becomes in the magnitude of the ripples mentioned in its subchapter.

The theoretical output voltage from this circuit is quite straightforward as we only have one pumping stage. Let us first consider the rectifier alone. This can be compared to circuit one and the same equations yields here for this circuit. This means the output voltage can be written as

$$V_{out} = Vin_{peak-peak} - 2V_d \tag{4.26}$$

because there are always two diodes leading current, one in the positive and one in the negative way.

For the pumping unit, we look at the positive rectification for the positive input for one period when the outputs are connected to a capacitance. After a negative swing, the positive swing in our period places a charge in the magnitude of

$$V_{C_S} = Vin_{amplitude} - V_d \tag{4.27}$$

across the C_S capacitance where V_d is the threshold voltage of the diode. The following negative swing in the second period lowers the output voltage with one amplitude. The voltage across C_S is now one amplitude higher than the output, so current flows through the last diode towards the output storage capacitance, giving an output voltage of

$$V_{out+} = V_{C_S} + Vin_{amplitude} - V_d = 2Vin_{amplitude} - 2V_d \tag{4.28}$$

The same occurs for the negative output, and the same equations with changed indexes will yield for this case. Also, realizing that $2V_{amplitude} = 1V_{peak\text{-}peak}$ gives us the output voltage of the circuit

$$V_{out} = V_{out+} + V_{out-} = 2Vin_{peak-peak} - 4V_d \tag{4.29}$$

The different parameter values are chosen for the same reasons as for the other two circuits. However, a bit more experimental this time compared to circuit two which is quite similar to this. We remember the diode widths of 100µm and capacitor sizes of 12.34pF from circuit *two*. Now, the ratio is turned slightly around by trying larger diodes and smaller capacitances. The parameter values are chosen according to both theory and H-Spice simulations. But because the real-life performance can differ from what is expected, a more liberal choice of sizes are done compared with the ones in circuit two, but still, as mentioned in good thread with the simulations results below.

Figure 4.26 shows a parametric analysis of the circuit with different diode sizes. The positive output is plotted against time, a similar but flipped output can be obtained in the negative output. The output voltage rises with larger diode sizes as expected. Also, it is clear that the advantage of larger diodes is exponentially decaying, as the different simulation graphs becomes closer and closer. This means, the advantage of increasing the diode sizes decreases when the sizes becomes large. As the difference between the pink 217µm diode and the 300µm transistor is only 18mV, a 250µm transistor is chosen. This is 150µm larger than the diodes in circuit two.

Figure 4.27 shows a similar simulation but with the capacitances varied. Again it is the positive output which is plotted. We see the output raises with larger capacitances. Recalling from circuit two, the same case were present there. As for the diode size graph, the advantage with larger capacitances decays exponentially and it seems capacitors above 10pF will have limited use. However, for differentiate this circuit from circuit two, a capacitor value of 5pF is chosen. The blue trace of the graph corresponds to 4pF capacitances, making a 5pF capacitance close in performance to the best 10pF capacitance. This 5pF chosen capacitor in this circuit is 7.4pF smaller than the capacitance chosen in circuit two. Based on these arguments and simulations, parameter sizes are chosen according to Table 4.9.

Device	**NMOS**	**PMOS**	**C_S**
Size	250µm/0.40µm	250µm/0.40µm	4.97pF

Table 4.9 Parameter values for Circuit 3

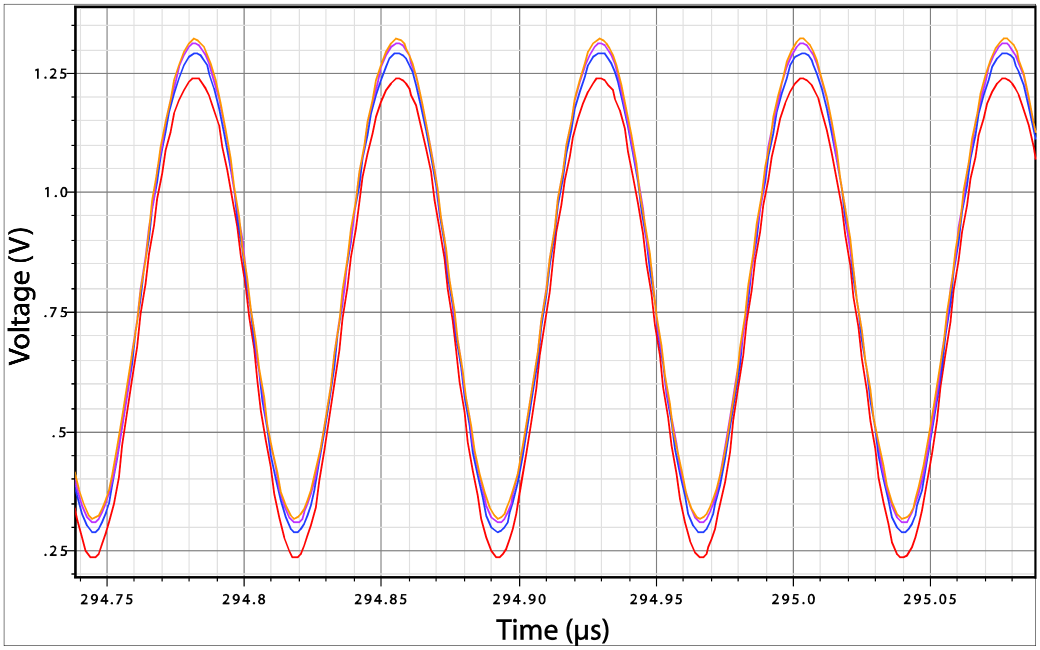


Figure 4.26 Parametric analysis of circuit 3 with four different diode widths: Red: 50µm Blue: 133µm Pink: 217µm Orange: 300µm

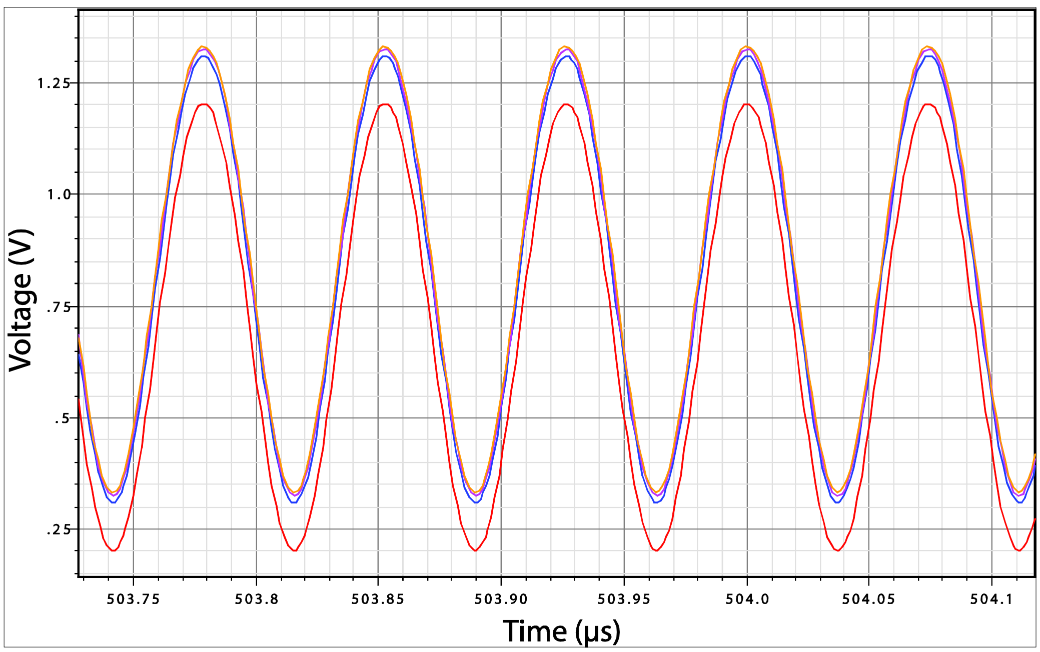


Figure 4.27 Parametric analysis of circuit 3 with four different capacitor sizes: Red: 1pF Blue: 4pF Pink: 7pF Orange: 10pF

4.3.8 Rectifying Circuit 3 – Simulation Results

The modified testbench for circuit three is shown in Figure 4.28. Compared to the testbench for circuit *two*, some changes have been made: (1) The input is now not only a single source, but now also containing an ideal transformer with equally number of turns on both side, meaning the input voltage is amplified with 1 (the output from the transformer is the same as the input). This element gives the circuit the same condition it will experience if used in such a real-life system. (2) It isolates the circuit inputs from ground, leaving both inputs floating and input signal can occur at both leads. This is in contrast from circuit two where one of the inputs is forced to ground. Now, because the input signal can occur at both inputs, input resistance is placed on both V_{in+} and V_{in-}. The output circuitry with loading resistance, storage capacitor and pad-capacitances are the same as for the other circuits. The different parameters for the circuit are shown in Table 4.10.

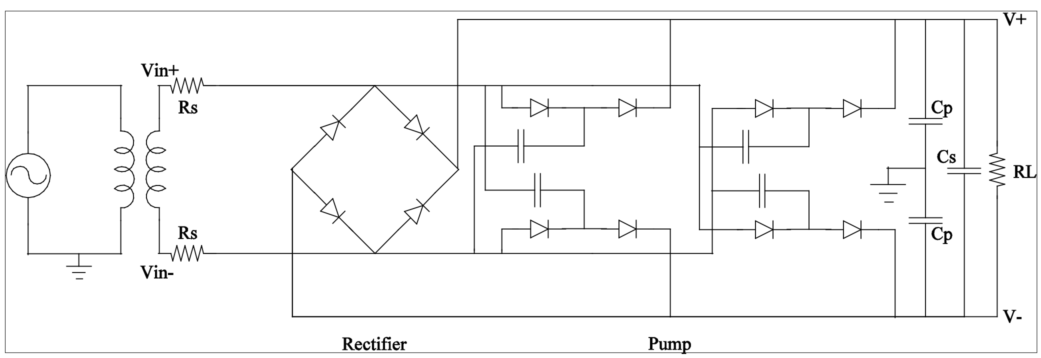


Figure 4.28 Testbench for Circuit 3

Parameter	**V_{Gen}**	**Freq**	**R_S**	**C_P**	**R_L**	**C_S**
Basic setup	$2V_{p-p}$	13.56MHz	50Ω	10pF	100KΩ	2nF

Table 4.10 Testebench parameters for Circuit 3

As for the other circuits, a 1ms transient analysis is performed and shown in Figure 4.29. The figure is two plots, *upper without* the pad-capacitance (C_P) and the *lower with*. The severe difference is clearly seen. The pad-capacitance is as earlier mentioned something which we will experience when the produced circuit is measured on, as its inputs and outputs are connected to a measuring pad. These pads have stray capacitances towards ground and are in the range of some pF. These capacitors will function as a discharge capacitor and therefore stabilize the two outputs when the circuit are measured on (lower part of Figure 4.29). However, when the circuit is used together with other circuitry and not directly connected to in form of a measuring pad, these capacitances are not present and the output will be as the upper half of Figure 4.29. Despite the differences, the output voltage is the same for the two setups, in the ratio of 1.183-1.185mV, shown in Table 4.11 (the upper numbers in parentheses are for the upper plot in Figure 4.29). Equation 4.29 gave us a brief calculation of the output voltage, and for the conditions used in our simulations, we could expect an output voltage of

$$V_{out} = 2V_{p-p} - 4V_d = 2\times 2V - 4\times 0.45V = \underline{2{,}2V}$$

We see the calculated value is above the simulated, in the same way as for circuit two. This is partly due to the simplifications in the calculated case and mainly by the effect of the source resistance R_S which the equation not accounts for. We remember from circuit two an output voltage of ≈ 2.8V was obtained and the calculated value was 5.5V. This means for both circuits (two and three), the simulated voltage is about the half of the calculated output voltage with the basic setup testbench. Also, we see the output of circuit 2 is more than double the output of circuit 3. This is because circuit 2 had two pumping stages in series behind the first rectifier. Here, the rectifier part and the pumping mechanism are connected in parallel, and also, only one pumping step is used. This gives output voltages which are almost not comparable. More interesting is the difference in efficiency of the two circuits, which we will later calculate and discuss. Increasing the input voltage is absolute desirable if the efficiency of the internal circuitry is higher when this is done (compared to a pumping circuit demanding a lower input to deliver the 3.3V output but at a lower efficiency).

Beside the difference of the two circuits (two and three) regarding ripple, ΔVin also shows a difference between the two setups. The excitation voltage is $2V_{P\text{-}P}$, and because of the equal number of turns in the transformer, the same voltage is to be found on the right side as on the left side. But because the two input leads now can move freely, is floating, this $2V_{P\text{-}P}$ are distributed on two different ways depending on the setup. In the upper case of Figure 4.29, almost all of the 2V swing is obtained in one of the input leads, and only a weak swing in the other.

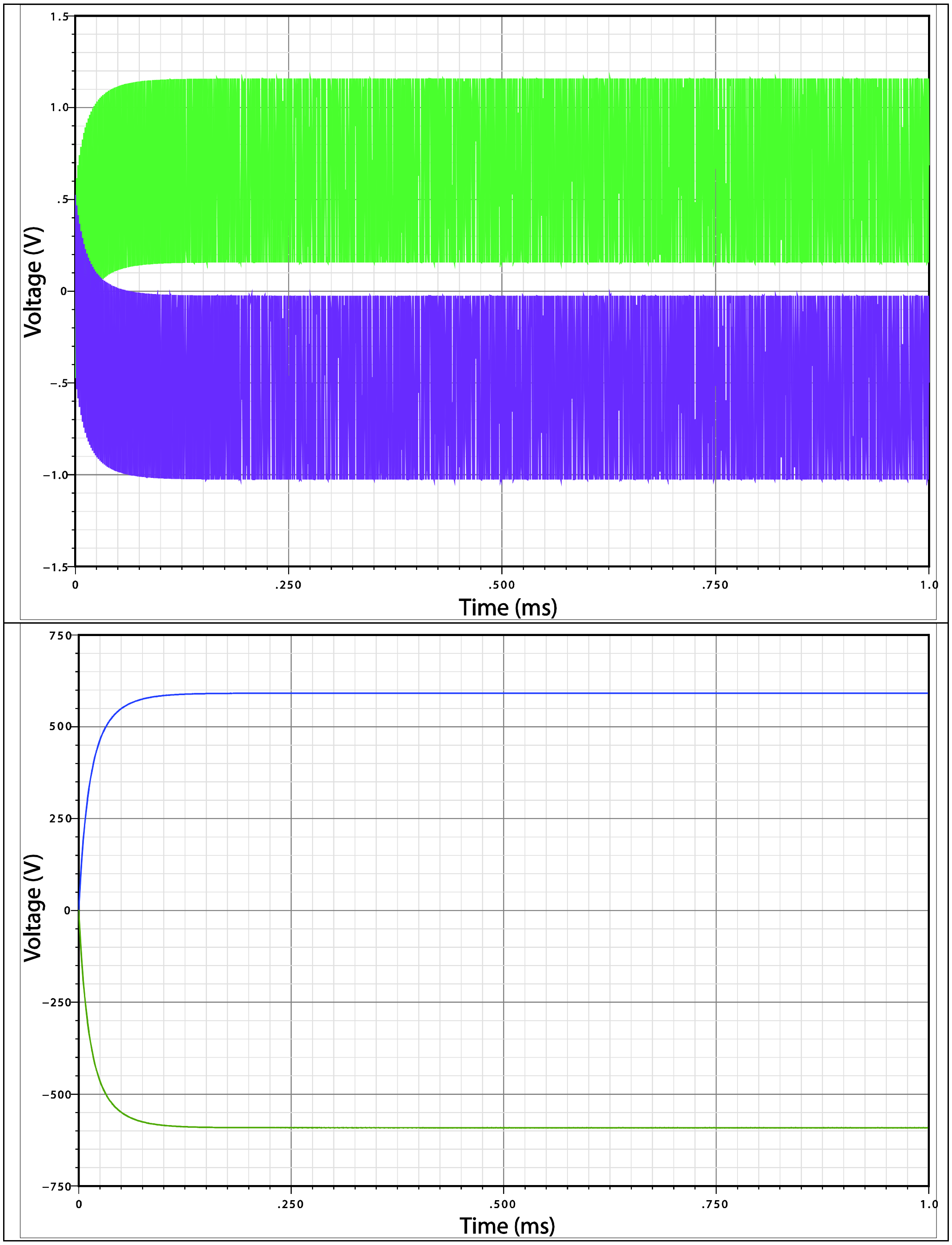


Figure 4.29 A 1ms transient analysis of Circuit 3, upper: without CP, lower: with CP

Measurement @1ms	Positive max	Positive min	Negative max	Negative min	Output Voltage	∆Vin
Schematic simulation	(1.158V) 591.3mV	(158.4mV) 591.4mV	(-25.35mV) -591.3mV	(-1.025V) -591.4mV	(1.185) 1.183	(1.981V) 982.8V

Table 4.11 Performance of Circuit 3 with basic setup

The peak-to-peak voltage obtained behind the source resistance R_S is therefore in the same matter as it is for circuit two and measured to be 1.981V. With C_P connected however, the input voltage is evenly distributed between the two leads, leaving a lower peak-to-peak voltage internally because now the two inputs are switching with the same amplitude but 180^o phase shifted. As earlier discussed, this does not affect the performance of the circuit severely because of the symmetry. This leaves us with a very adaptive circuit and with the same output voltage as for the first case. In the following simulations, C_P will be held connected as the testbench shows.

As for the other circuits, we want to know the efficiency. This is measured in the same way as for the two earlier circuits. Now, when the source resistance is varied, both resistors is changed, meaning the two input resistors always is at the same value and varied simultaneously. The result of the simulations is shown in Figure 4.30[22]. As for the other circuits, the efficiency is very dependent on the load resistance. Not surprisingly, smaller loads (larger resistance value) give better conversion efficiency. It increases uniformly and starts to flatten when R_L increases above 30kΩ. One interesting point to consider is the dependency to the source resistance R_S. First, for large loading resistance values, the efficiency increases with increasing source resistances. Second, for smaller load resistance, the efficiency increases with decreasing source resistance, which is the same as found for circuit two. Third, for large source and load resistances, the efficiency is just slightly changed around the maximum point at $R_S \approx 550\Omega$, showing s slightly looser dependency than for the other two circuits.

Overall performance is however severely lowered compared to the other two, and was not expected. We see the circuit shows a 9.5% efficiency performance at best, about 40% behind circuit two.

As for the other circuits, we want to know the maximum available power and this is shown in Figure 4.31. As for circuit one, the efficiency and power figures

[22] The MatLab script used for calculation is the same as for circuit one. The result of the calculation and the raw-data file are to be found in Appendix B.

shows no sign of significant correlation. However, the power-figure for all three circuits is quite similar with no further comparison. Maximum available power is obtained when the source resistance is low and the load resistance in the range of 6-7kΩ. In this area, the total available power is ≈ 50μW which is lower than both the other circuits. It seems however although the efficiency is low, the power transfer is not as much affected. This fact is probably connected to the unlimited current throughput for the rectifier part of this circuit.

Finally, if we multiply these to figures, and Figure 4.32 is obtained. It shows the optimal point of operation with a low R_S and a R_L in the range of 5-10kΩ. This is what we could expect from the forms of the first two graphs of course: A clearly defined maximum from the power figure but the peek widened by the efficiency figure. This means this circuit behaves somewhat like the first circuit, and an optimal output resistance is defined.

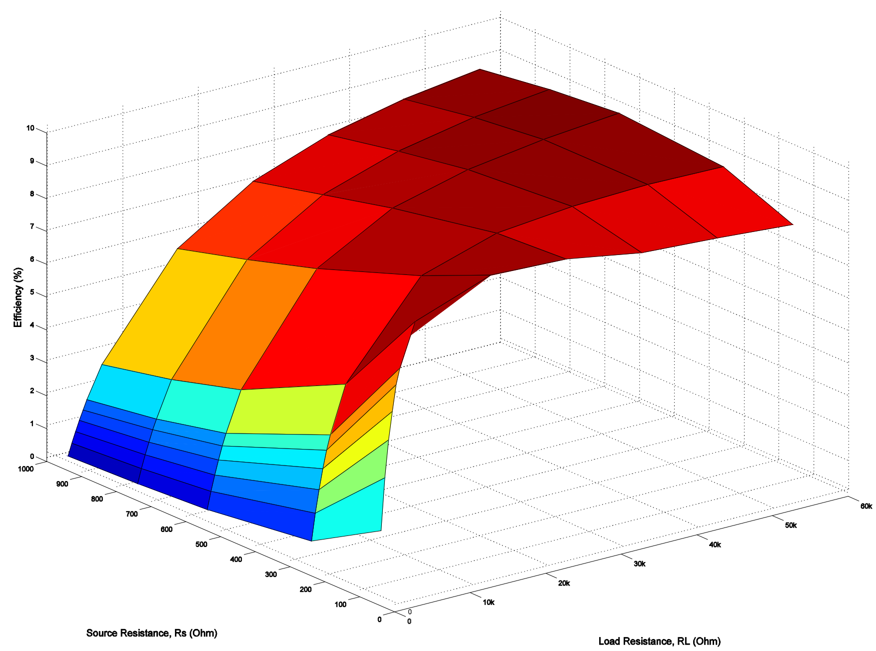


Figure 4.30 Efficiency of rectification, Circuit 3

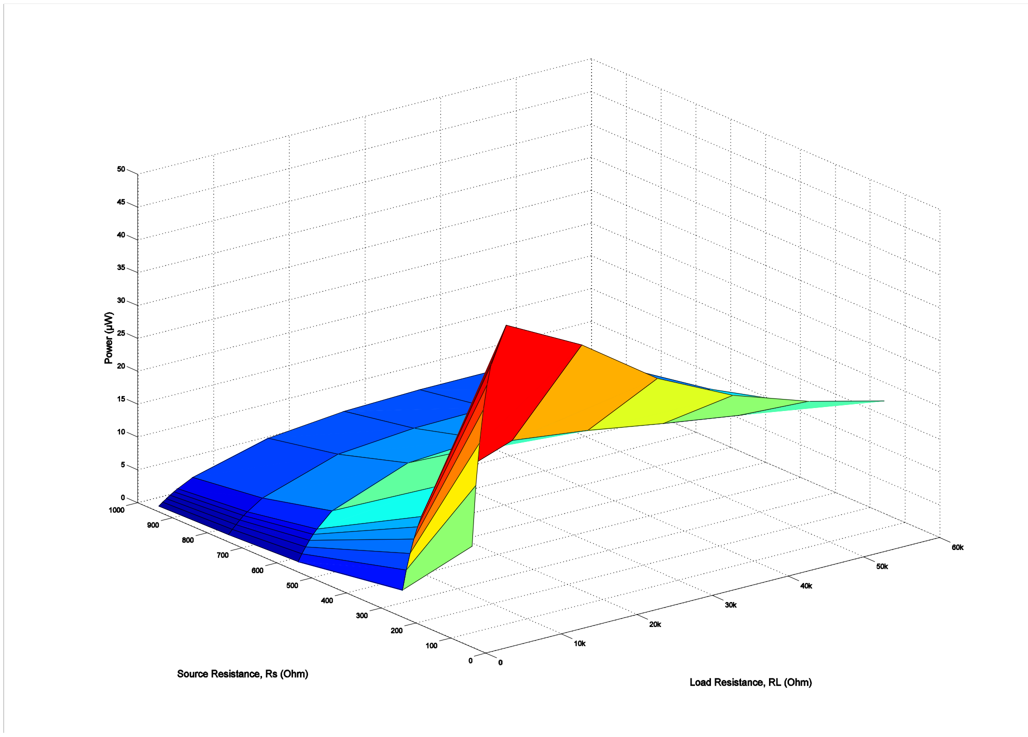


Figure 4.31 Available power on the output, Circuit 3

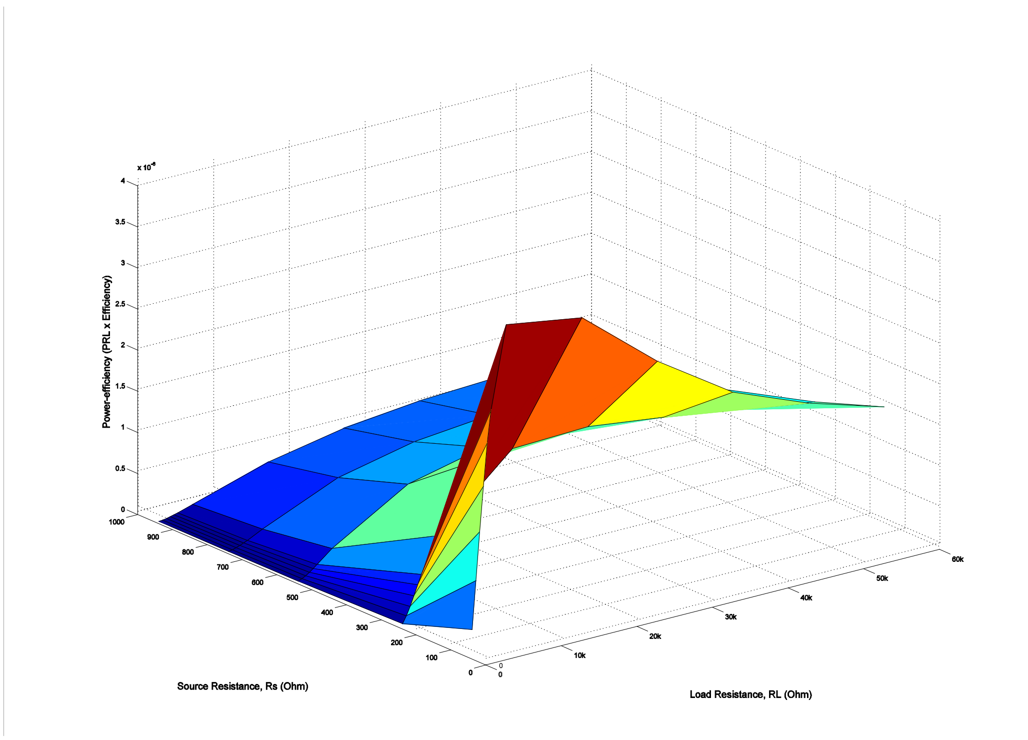


Figure 4.32 Efficiency multiplied with available power. Shows which circumstances that provides the most available power most efficient, Circuit 3

4.3.9 Rectifying Circuit 3 – Production

This circuit was produced together with this thesis` supervisor, Philipp Häfliger who made the layout as for circuit one. Figure 4.33 shows the layout of the circuit. The dimension of the circuit became 158μm in length and 115μm in width. We see the red capacitors again dominate the picture while the blue transistors are bent into fingers to match the lengths of the capacitors and placed vertically at the ends.

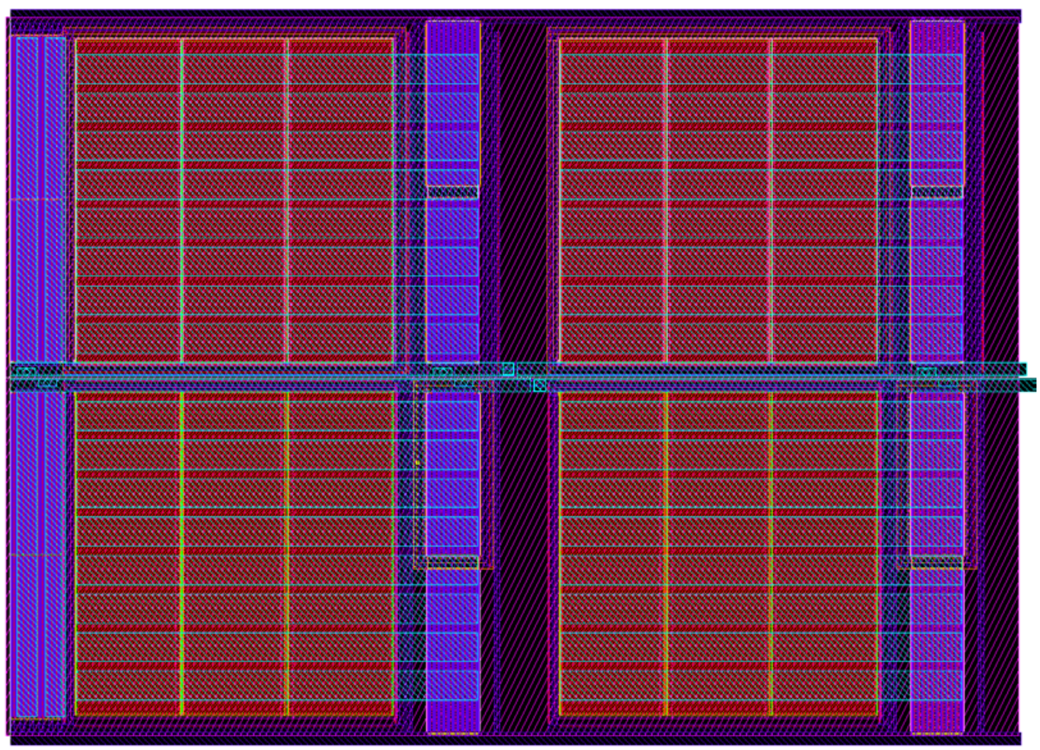


Figure 4.33 Layout of Circuit 3. Total size is 158μm x 115μm

Chapter 5

5 Voltage Reference

Amplifiers are often said to being the most common electronic circuit in the world today. It is highly useful, can handle almost any sort of conditions, and fulfil many demands, more or less like the potato. But even more used than the amplifier, and often highly necessary for making even amplifiers work, is another common and basic circuit. Regardless of whether the system is integrated CMOS, discrete components or BJTs, *bias circuits* in some form are one of the main and most important building-block. These circuits are like the butler in a restaurant, it ensures proper conditions and operation in any circumstances. It serves the potato.

5.1 Voltage references

Bias-circuits come in many forms and used for lot of tasks, but in this thesis we will only concentrate on the *voltage* circuits, or *voltage references*. The voltage reference field is still investigated and research is still put in to it, although the circuit is quite old and many of them have become more or less traditional. New technology, processing methods and lowering of the supply voltage demands some changes in the old and well known reference circuit design. However, this chapter will not focus on new and revolution ways of designing and making voltage references. But rather, with focus on the total measuring system as one complete unit, try to find a useful and adapted voltage reference for our needs and demands. From the previous chapters, we know these demands as: Supply voltage “independent”, a stable output voltage (of course), high power efficiency and polite against movement, electric and magnetic radiation and so on.

There are typically two main ways to design a voltage reference: (1) using the physical condition of pn-junction forming what is called a *bandgap reference* and (2) a design based on purely elements from the technology chosen, i.e. transistors, resistors and so forth. We shall take a closer look on both of the two different types.

A *bandgap* reference is actually described in the name, in the words *band* and *gap*. *Band* refers to the physical difference between the valence band and the conduction band, which the electrons are connected to. *Gap* describes the voltage difference between these two bands, and together makes the essential idea for the voltage reference. More specific, the *gap* is the difference between the top of the valence band and bottom of the conduction band. This difference is changing regarding to which materiel that are considered. As electrons can only be tied to one of these bands, the electrons jump from one to the other and give a stable voltage which can be used to make a stable output from such a circuit.

This bandgap needs to be formed somewhere in the circuit, and are easily obtained in BJT technologies (in bipolar circuits). In CMOS however, bipolar transistors are not available, and a bandgap needs to be formed somewhere else. This is often done by an arrangement of pn-junctions or making a “p-n-p” transistor with an n-well. The p_+ source-drain diffusions serve as the emitter, the n-well as the base, and the substrate as the collector. This p-n-p arrangement however demands the collector of the transistor to be at substrate potential. This arrangement is therefore often used as a ground diode, where the emitter is the anode and the cathode is the base and collector tied together.

A bandgap circuit is often made by connecting two such p-n-p’s together in two parallel leads with a transistor mirror on top, as done in the Brokaw cell (37). This arrangement allows an output voltage based on the parameter (sizes) chosen and compensating for temperature drift, which will be further discussed later.

A “*purely technology based*” circuit can be designed and produced in many ways. Common for these types of references are the use of resistances as the main regulating part. Compared to the bandgap, there not a typical way of designing such a circuit, however, a generalization can be made by dividing it into some subparts: (1) A regulation core typically by two parallel leads containing a mirror and two or more resistances, (2) an amplifier which controls the current through the two resistor leads and therefore adjusts the output voltage, and (3) a start-up circuit and biasing circuit for the amplifier. These types of circuits are typical not as stable as the bandgap circuits, and tends to be quite large when strict operation constraints are placed on them. However, they are made by only known CMOS elements and can be made fairly power efficient. As the hunt for low-power circuits still goes on, the purely technology dependent regulators finds it place of use, especially if some part of the performance can be tolerated not to be perfect.

One point to consider for both the described technologies is their change of performance with changing temperatures. This is often one of the most difficult constraint to meet when designing a voltage reference, both because of large temperature range a system often is operated in, and the effect from the self-heating when many circuits are placed closely together on large PCB's. Such temperature drift are often accounted for by placing different elements with different temperature coefficient in such a manner that when added or subtracted, the total temperature drift becomes zero. Such elements are described as either CTAT (complementary to absolute temperature) or PTAT (proportional to absolute temperature). If two elements, one from each type and having the same temperature curve form, i.e. a linear slope, are placed together and subtracted, the total temperature dependence becomes zero. This ensures a reference circuit independent of temperature, making the output stable even with changing temperatures.

For *bandgap circuits*, this is done by using the p-n-p transistors in the two parallel leads. For one such transistor, the V_{BE} is a quite linear CTAT. However, this CTAT V_{BE} is of course also found in the other transistor, but now operated with another collector current. This current difference gives two linear but different CTAT curves for the two transistors. The needed PTAT curve must be generated to compensate for the CTAT element in the output voltage lead. This is done by, and also a reason for why two parallel leads are used in bandgap circuit, taking the difference between the two different $\mathrm{V_{BE}}$'s (37).

For references other than bandgaps, typically with circuits where the operation are based on resistors, the temperature is compensated in much the same way as for bandgaps. Two different kinds of resistor types (materials) are used in the two leads with different temperature characteristics. As the one lead becomes a PTAT, the other is a CTAT, and when the leads are subtracted, the output voltage becomes temperature independent. However, this mean of temperature compensation is not as good as the one for bandgaps. Because there are no materials which is similar enough to make two perfect symmetrical leads and at the same time get the PTAT/CTAT temperature slopes cancelling the temperature dependence, the result is often not good enough. It often leads to temperature dependence, mismatch between leads and higher power consumption.

One point to consider for our use of the total system and for this reference circuit, is regarding the change in temperature. The whole system is to be placed a distance inside a human's body. In such a location, the temperature can be considered quite stable. And if it is not, the performance of the circuit is no longer interesting for obvious reasons. In addition, the circuit is only switched on when a measurement is to be performed, making self-heating not a severe problem considering the time the system uses for taking a single measurement. Therefore, issues regarding power consumption and power supply stability overshadow the demand of temperature stability. These topics are therefore weighted in the design of our reference circuit.

The chosen regulator circuit for this system is not a bandgap circuit. Despite its supremacy regarding stability, temperature and fairly uncomplicated circuitry besides the bandgap-core, a pure CMOS device is developed for several reasons. First the lowered temperature demand discussed above, secondly the possibility of making a bandgap circuit efficient enough and at the same time keep the thesis inside it frames of size and time. Third, as other people involved in the project where this thesis is a part of also were concentrating on this circuitry and part of the system, there became a point of not making the same kinds of circuits which will give the final product more possible circuits to choose from. And finally, some excitement was found in trying to make such a circuit which satisfies our demands to it.

In the next paragraphs, a circuit is presented in two different forms/types where only one of them are produced and measured on. Finally, a conclusion is drawn in Chapter 6 from its performance, and a short discussion regarding its measured results and our desired results is presented.

5.2 Proposed Regulator One

The regulator chosen for this project is as mentioned a typical CMOS voltage reference. It is developed for maximum power efficiency and V_{DD} working range because of its field of use just discussed. Stability and power supply rejection ratio were other important goals in the development. The proposed voltage regulator is based on the idea of the voltage reference made by K N Leung, P K T Mok and C Y Leung (38). The regulator is designed and produced in the 90nm ATM process from STM (this led to many changes compared to regulator proposed in the paper, and the paper can therefore be looked at more as an idea than a circuit solution). A brief illustration of the circuit is shown in Figure 5.1.

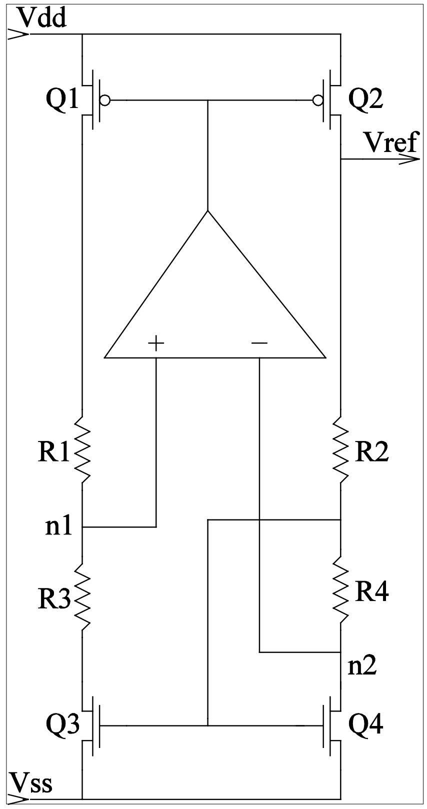


Figure 5.1 Simplified circuit scheme for regulator one

The four resistors (R1~R4), the two regulator transistors (Q1,Q2) and the two active loads (Q3,Q4) are what we can call the regulator core. In addition, an error amplifier is set to perform, or administrate, the regulation. The idea in this scheme is to divide the supply voltage into fragments in the two branches. The amplifier forces the two nodes *n1* and *n2* to fairly the same potential. The amplifier also detects the changes in voltage in the two branches, and makes adjustment on its output to re-establish steady state with the output from the circuit at 1V. Before looking at the whole circuit scheme, some points are worth mentioning. The amplifier, as already mentioned, takes care of the voltage regulation. The temperature regulation however, is not active regulated. But this can be affected by choosing the right material for the resistors. By selecting the material for R1 and R2 with positive temperature coefficient (PTAT), and negative for R3 and R4 (CTAT), the temperature dependence can be adjusted. In this regulator, unsilicided N+ poly resistor with a temperature dependence of 0.0136%/^{o}K are used for R1 and R2, for R3 and R4 unsilicided P+ poly resistor with a dependence of -0.0171%/^{o}K are used. As R3 and R4 have smaller resistance value than R1 and R2 and the dependence is given in percent of its resistance value, this choice of temperature dependent resistance material should in theory be optimal for good compensation. However, we will later see this is not the case and the circuit will show a severe temperature dependency.

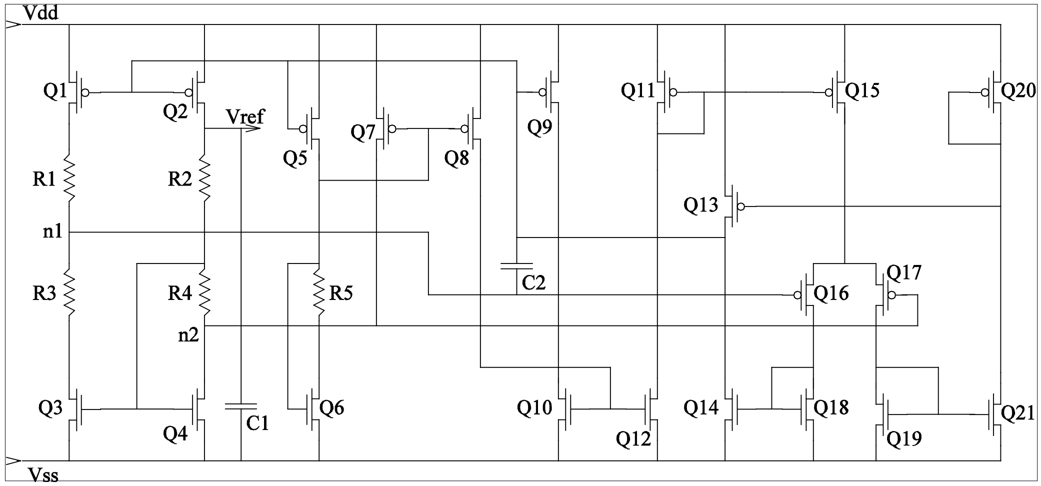


Figure 5.2 Complete schematic scheme for regulator one

Device	Q1	Q2	Q3	Q4	R1	R2	R3	R4
Sizes	15/0.3	15/0.3	45/0.3	5/0.3	144.6k	58.1k	38.4k	33.6k

Device	Q11	Q15	Q16	Q17	Q18	Q19	C1	C2
Sizes	8/0.3	2/0.3	20/0.3	20/0.3	20/0.3	10/0.3	6,38pF	1.04pF

Table 5.1 Transistor- and element sizes for regulator one

Figure 5.2 shows the whole circuit schematic for the proposed voltage regulator. Again we see the regulator core (Q1~Q4 and R1~R4), the start-up circuitry (Q5~Q8 and R5), some bias transistors and the error amplifier (Q9~Q21). In Table 5.1 the most important sizes and values are listed.

For establishing an intuitive way of functionality, looking at a steady 3.3V supply voltage stage before a voltage drop (on V_{DD}) makes it more clear: When V_{DD} are 3.3V, the V_{ref} is steady at about 1V. Then a voltage drop on V_{DD} occurs, leading to lower voltages in the two regulator branches. The V_G for Q3 and Q4 drops and since these are NMOS, the resistance rises. The point *n2* therefore raises leading to a higher V_G at Q17, the input of the amplifier. This leads to lower V_G at Q21 and higher V_G at Q13. Also, the point *n1* falls because of the resistance between *n1* and Q3, leading to a drop in V_{DS} for Q14. Eventually, this lowers the V_G for Q1 and Q2, leading more current and the output voltage climbs back to its original value and eventually steady state are again established. This means, any changes in the voltage in the two branches are picked up by the amplifier, causing this to make adjustments on its output. Figure 5.3 illustrates the output of the circuit in the described case above.

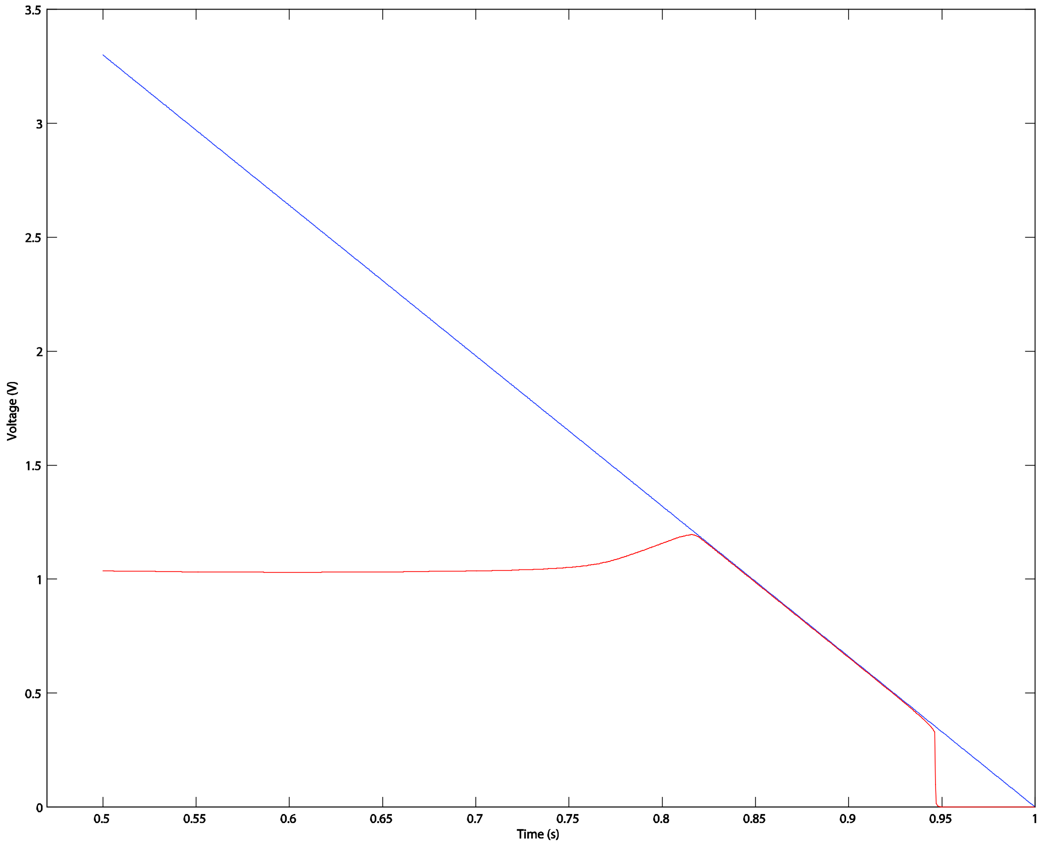


Figure 5.3 After a steady state with V_{DD} = 3.3V (blue trace), a voltage drop occurs and the V_{DD} falls to 0V during a 0.5 seconds time. The output of the regulator is the red trace

We want to derive a formula for the output voltage during steady state. This is not intuitive because of the different feedbacks and we therefore do some simplifications: First we isolate the abstract circuit figure and derive the formula on this scheme. Further we do the calculation without loading the circuit, meaning no current can pass through the output but has to stay in the two branches. V_{DD} = 3,3V and we want 1V to be our reference voltage. This implies transistor Q1 and Q_2 to be in saturation and the current through the two branches is therefore similar. And since the two inputs to the amplifier always is at same potential, this current is similar to

$$I = \frac{V_3}{R_3} = \frac{V_4}{R_4} = VQ_4 \frac{W_{Q4}}{L_{Q4}} g = VQ_3 \frac{W_{Q3}}{L_{Q3}} gm = \frac{V_2}{R_2} \tag{5.1}$$

where g is an adjusted transconductance (which we soon will look at).

The voltage across transistor Q_4 is

$$VQ_4 = V_3 + VQ_3 \tag{5.2}$$

where V_3 is the voltage across resistance R_3 because of the mentioned amplifier inputs. We need to be able to compute the *g* in (5.1), and (39) states this as

$$g = \frac{I_S}{2 \times U_t^2} \times (VQ_4 + V_4 - V_t) \tag{5.3}$$

where U_t is the thermal voltage and V_t is the transistor threshold voltage. Finally, as we want an expression for the output voltage, we can clarify our goal with

$$V_{ref} = VQ_4 + V_4 + V_2 \tag{5.4}$$

According to (5.1)

$$VQ_3 = VQ_4 \frac{W_4 / L_4}{W_3 / L_3} \tag{5.5}$$

and substituting for VQ_3 in (5.2) yields

$$VQ_4 = \frac{V_3}{1 - \frac{W_4 / L_4}{W_3 / L_3}} \tag{5.6}$$

If we take $V_3/R_3=VQ_4*(W_{Q4}/L_{Q4})*gm$ from (5.1) and substitutes *gm* from (5.3) and express V_4 with V_3, we have

$$V_3 = R_3 \times \frac{I_S}{2 \times U_t^2} \times (VQ_4 + \frac{V_3 \times R_4}{R_3} - V_t) \times \frac{W_4}{L_4} \times VQ_4 \tag{5.7}$$

$$\downarrow$$

$$V_3 \times (1 - \frac{I_S}{2 \times U_t^2} \times R_4 \times \frac{W_4}{L_4} \times VQ_4 = R_3 \times \frac{I_S}{2 \times U_t^2} \times \frac{W_4}{L_4} \times VQ_4 \times (VQ_4 - V_t) \tag{5.8}$$

If we now solve (5.8) for V_3, we have

$$V_3 = \frac{R_3 \times \dfrac{I_S}{2 \times U_t^{\,2}} \times \dfrac{W_4}{L_4} \times VQ_4 \times (VQ_4 - V_t)}{1 - \dfrac{I_S}{2 \times U_t^{\,2}} \times R_4 \times \dfrac{W_4}{L_4} \times VQ_4} \tag{5.9}$$

If we now substitute V_3 into (5.6) we get

$$VQ_4 = \frac{R_3 \times \dfrac{I_S}{2 \times U_t^{\,2}} \times \dfrac{W_4}{L_4} \times VQ_4 \times (VQ_4 - V_t)}{(1 - \dfrac{I_S}{2 \times U_t^{\,2}} \times R_4 \times \dfrac{W_4}{L_4} \times VQ_4) \times (1 - \dfrac{W_4 / L_4}{W_3 / L_3})} \tag{5.10}$$

which is a 2. degree equation with respect to VQ_4. Solving this equation gives two solutions:

I: $VQ_4 = 0$

and

II: $$VQ_4 = \frac{R_3 \times V_t}{R_3 + R_4 \times (1 - \dfrac{W_4 / L_4}{W_3 / L_3})} + \frac{1 - \dfrac{W_4 / L_4}{W_3 / L_3}}{\dfrac{I_S}{2 \times U_t^{\,2}} \times \dfrac{W_4}{L_4} \times (R_3 + R_4 \times (1 - \dfrac{W_4 / L_4}{W_3 L_3}))}$$

As Q_3 and Q_4 has the same gate voltage and we now have an expression for the voltage across Q_4, we can again use the amplifier input fact an retrieve a voltage for V_3 based on the size-scaling of Q_3 and Q_4:

$$V_3 = VQ_4 \times (1 - \frac{W_4 / L_4}{W_3 / L_3}) \tag{5.11}$$

From this (5.10) we can easily calculate the current through the branch from

$$I = \frac{V_3}{R_3} \tag{5.12}$$

And finally for retrieving the output voltage in (5.4):

$$V_4 = I \times R_4 \qquad , \qquad V_2 = I \times R_2$$

There are two regulating parts in these equations. First, the current through the branches, given by the saturated Q1 and Q2 transistor depends on the output voltage of the amplifier. This output depends again on the voltage found *in* the two branches. This forms a loop of dependency and is the first regulating mechanism in the circuit. Second, VQ4 regulated by its gate voltage which is collected from above the second resistor in the branch. This transistor can therefore be looked at as a dynamic resistance, and its changing resistance is the second regulating mechanism.

Power consume is an important design criteria in all system parts. Since the system are based on a passive power source with only the storage capacitor to provide current, the efficiency of each part in the system are critical. This has some consequences for the design of the regulator. First of all it leads to larger resistors in the regulator core. A larger current through the two branches would increase the voltage stability on the output against variation and rise/fall on the V_{DD}. It would also been preferable against ripple, giving a larger damping, and make it possible to drive bigger loads. However, the current will rise linearly[23] with the lowered resistance, leading to higher power consumption. Rather large resistors are therefore used in the two regulator branches. Furthermore, reducing the current trough the amplifier will decrease the power consumption. Relatively small transistors are therefore chosen in this part of the circuit. The trade-offs are a rather slow amplifier and smaller gain. A start-up circuitry is added with sizes as small as possible, making sure the circuit starts when power is switched on. With smaller resistors R1-R4 and larger Q1 and Q2 and therefore a lot more

[23] From a first order aproximation

current through the branches, need for this start-up circuit. But despite of the power consumed in the start-up circuit, it is still feasible to have a smaller current through the branches and make need for this start-up circuitry, as the power consumption through this part is very small.

Finally, the stability and frequency compensation are considered. Because the regulator is connected to the sensor, it is important that oscillations and ripple are avoided on its output. Also, because of the environment the circuit is operated in, it is important that it can handle some ripple on the input without becoming unstable. For reducing this type of error, two measure have been used; capacitor C1 and C2. C1 is a well known way to reduce ripple on a regulated output voltage. By charging a capacitor on the output, a kind of “headroom” is achieved while the capacitor absorbs and delivers charge in phase with the ripple. The disadvantage is a higher load on the output and a slower circuit. Therefore, weighing has to be done between these cases. As we do not need a very fast circuit, C1 is chosen to be 6,4pF (Table 5.1). Capacitor C2 is placed between the positive input and the output of the error amplifier. The capacitance can be chosen very small because of the Miller multiplication effect (40). This capacitor provides better frequency stability, ripples rejection and also reduces noise. The disadvantage of a large C2 is longer start-up time. C2 is chosen to be 1pF.

5.3 Simulation

The circuit is simulated with Cadence H-spice, and
Figure 5.4 shows the testbench used for recovering the results. R_L is if nothing else is stated = 1MΩ and C_L = 10pF.

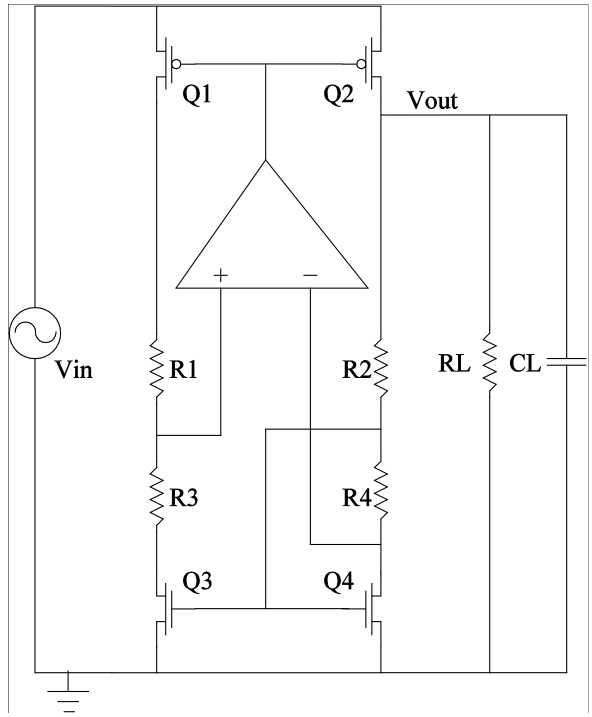


Figure 5.4 Testbench for Regulator One

Let us first look at the behaviour at start-up of the circuit and system. Figure 5.5 shows the output from the circuit (red) when V_{DD} (blue) starts at 0V and by 500ms rises to 3.3V. The performance of the circuit is clear. It gives the correct output voltage when V_{DD} rises above 1.585V. Below this value, the circuit does not function correctly and therefore this value is the lowest operational voltage of the circuit. We can also see, just when the point of 1,585V is passed, the output climbs to 1,058V before falling to a stable 1,035V which it tries to maintain. This means, for better accuracy, the lowest operational voltage from climbing V_{DD} (start-up) is 1.715V. Before looking further on stability and accuracy of the circuit, let us examine the case where V_{DD} falls from 3,3V to 0V.

Figure 5.6 shows this scenario. Now, the regulator output (red) climbs away from the desired voltage value before following the V_{DD} towards 0V. This is in other words not the same behaviour as the start-up where the output jumped from “not working” to “working”. This means, the lowest value of function at falling V_{DD} is decided by demands of stability, how much raise/fall in the output that is tolerated. This toleration can be decided by a percentage of variation with

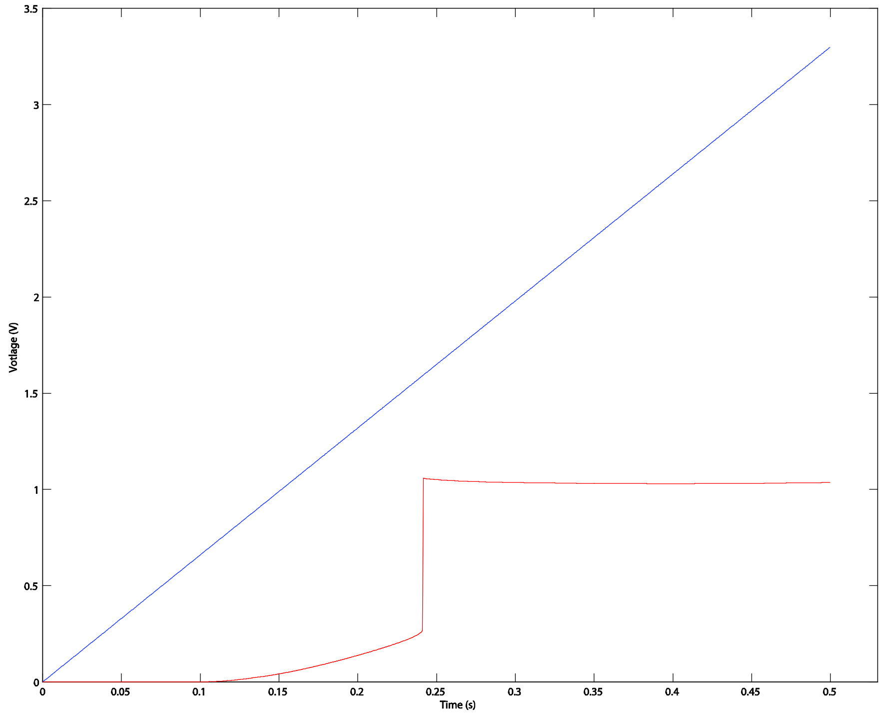


Figure 5.5 Transient analysis of regulator one. V_{DD} (blue trace) starts at 0V and during a half second climbs to 3.3V. The red trace shows the output of the circuit during this period

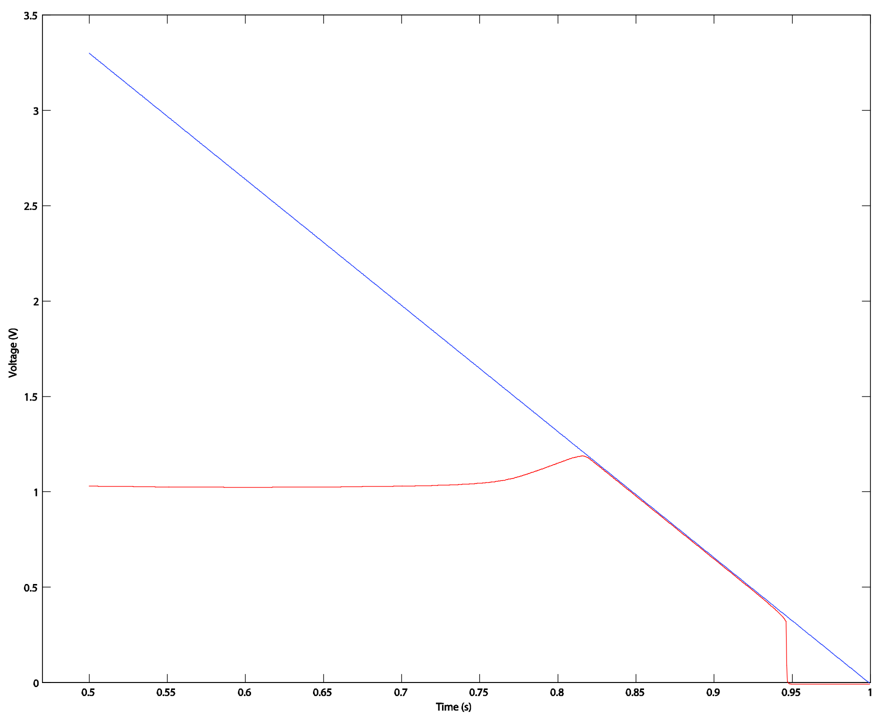


Figure 5.6 The V_{DD} (blur trace) drops from 3.3V to 0V during a half second of time. The red trace is the output from the regulator (same figure as used for illustration in Figure 5.3)

respect to the output voltage. The baseline[24] of the output voltage of the circuit is 1.036V. Given a 1% tolerated change, the V_{DD} working range becomes 1.715V~3.3V (on rising V_{DD}) and the same 3.3~1,715V (on falling V_{DD}). Based on this working range, Figure 5.7 shows the output behaviour when *Vin* changes from 1.7V – 3.3V – 1.7V. There are a couple of points to notice with this graph. First, the curve has on each side of the maximum 3.3V point a parabolic shape. This curve form is, for V_{DD} kept in the mentioned interval, optimal because variation from the baseline value is on both sides. This ensures the largest interval of function within a given tolerated variation. Of course, a straight line would be optimal, but this is in practice not achievable.

If we do a worst-case calculation on the *output stability* (deviation due to variation on V_{DD}), we would find the stability based on V_{DD} between 2.55V (which is the output minima of the output voltage curve) and 3.3V (which is the maxima on the same curve) to be:

V_{DD} range: 3.3V – 2.55V = 0.75V

Output variation: 1.0350V – 1.0301V = 4.90mV

V_{DD}-sensitivity$_{wc}$: 4.90mV / 0.75V = <u>6.53mV/V</u>

This shows the instability of the circuit with respect to the input voltage. This could obviously be calculated to a better figure by choosing other points on the graph. But because of the uncertainty of what the input voltage (V_{DD}) is at the time of sampling, worst-case is what that needs to be accounted for. However, one could argue that it is an identical procedure used every sampling, giving a sampling time close to each other each time, ideally. This means, the input voltage (V_{DD}) is at the same value at every sampling. This narrows the expected variation of the input voltage and therefore also the output expected variation of the voltage range, leaving a smaller output voltage error than calculated above (where we calculated the worst case over the whole functioning voltage range, meaning a sampling could take place at any time and at any input (V_{DD}) voltage). Ideally, the sampling is done at the same time and with the same input voltage each time. But as long as this cannot be guaranteed, this in best case reduces the V_{DD} range and ensures no more than a *probably* better variation figure between each measurement.

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[24] The baseline is here defined as the “correct” output value. This can of course be selected in many ways, however, in this case to value is found by measuring the output voltage at a stable 3,3V Vdd input. The *greatest* Vdd working range can be found if the “optimal” baseline is chosen. By choosing the baseline in such a manner that the lowest output voltage is barely kept inside the tolerated 1% change, the Vdd working range becomes 1,662V~ and ~1,662V.

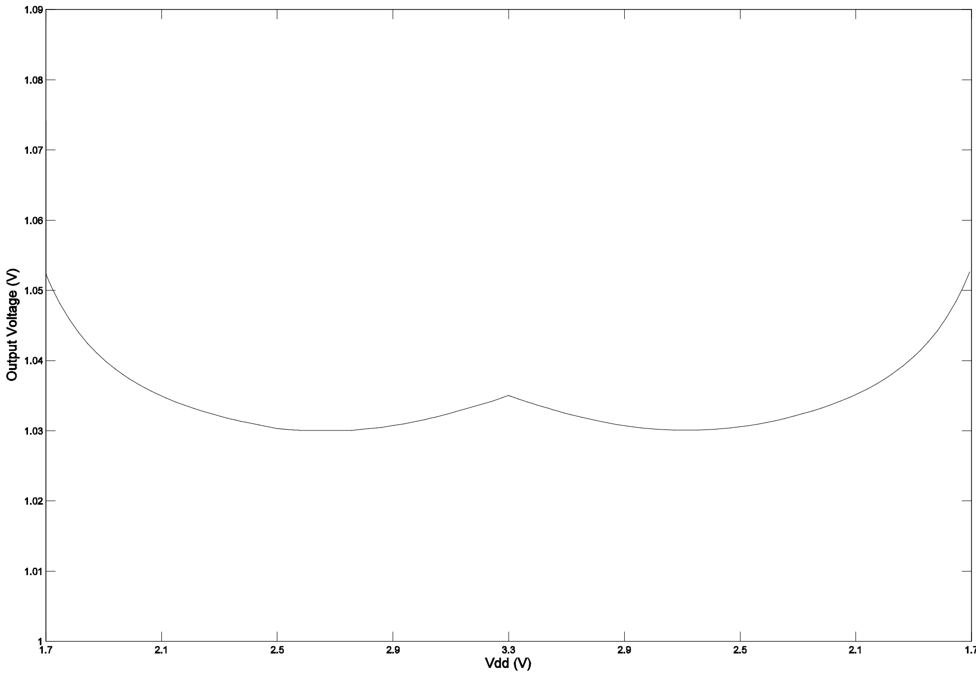

Figure 5.7 The output of the regulator shown with the input voltage (V_{DD}) on the x-axis. The unstability in the output voltage is clearly seen with the fine pitch used on the y-axis

Another important point when considering the output voltage is to ensure a proper operation from each produced circuit. This is done by a Monte Carlo simulation where both the mismatch and process variations are here taken into account. Such a simulation tells us what to expect when we take a random circuit of the produced amount and measures its performance. The worst case from such a simulation is if a certain percent of the produced amount of circuits do not function at all. From this to the perfect circuit, there are many degrees of how much "off" they are from ideal when it comes to output voltage level, output voltage variation, noise, PSRR, efficiency and so on. Table 5.2 shows the result of 2000 Monte Carlo runs.

MC	Runs	Mean Value	Std dev.
Value	2000	1,05743V	19,883mV

Table 5.2 show the performance of Regulator One at 2000 runs with both missmatch and process variation are accounted for. Mean Value shows the mean output voltage value from the 2000 runs. Std.dev shows in voltage ± one σ from the Mean Value

The same testbench are used as before. The input voltage is a steady 3.3V and the load used is the known 1MΩ resistance and 10pF capacitance. The mean output voltage of circuits from a production line is expected to be 1.05743V. More interesting is the standard deviation. This number tells that 68.3% of the produced circuits will have an output voltage inside the range of the mean value ± one standard deviation if the produced amount of circuits follows a normally distribution of performance. This means, 68.3% will have an output voltage between:

$$1.05743V \pm 0.01988V = \{1.03755V - 1.07731V\}$$

This result can be said to be very good, and absolutely acceptable for our project. All the circuits in the 2000 runs worked properly, and a standard deviation of 19,883mV is well inside our demand limits. When discussing these numbers, we got to remember every finished product is calibrated after implantation, and also repeatedly calibrated after some time of use. This small difference in output voltage from circuit to circuit is therefore taken care of in the calibration of the sensor and system.

Although we have augmented for the not so critical dependency with respect to temperature, we still want to investigate the temperature performance of the circuit. The voltage reference can of course be used in other tasks and projects where temperature may be more critical. Also, some excitement is tied to whether or not the temperature compensation through the different choices of materials in the resistors will have any effect in practice. Therefore, we make a temperature simulation trough H-spice and Figure 5.8 shows the output from the circuit with respect to temperature (-20^{o}C and 70^{o}C) with input voltage stable at 3.3V. At first glance, we see the circuit is not stable with respect to temperature. When the temperature rises, the output voltage falls. This means the way of compensating for temperature used here do not work satisfactory if stability regarding temperature were demanded. Because the output voltage falls with rising temperature, the *PTAT* compensation is too small compared to the *CTAT*. One approach to improve its stability is by choosing another resistance material with larger *PTAT* dependency. Or if even more dramatically changes are needed, the *CTAT* material can sometimes be replaced by a *PTAT*. However, the choice of resistance material is not only affected by its temperature behaviour, but other matters do also come into account, like resistance/area, mismatch and so forth. Therefore, if good temperature stability is needed, investigations need to be done to perform the right types of measures.

There is one positive point however. The output voltage falls strict linearly with temperature. There are no forms of higher order behaviour. The temperature can therefore quite easily be compensated for if a circuit with a

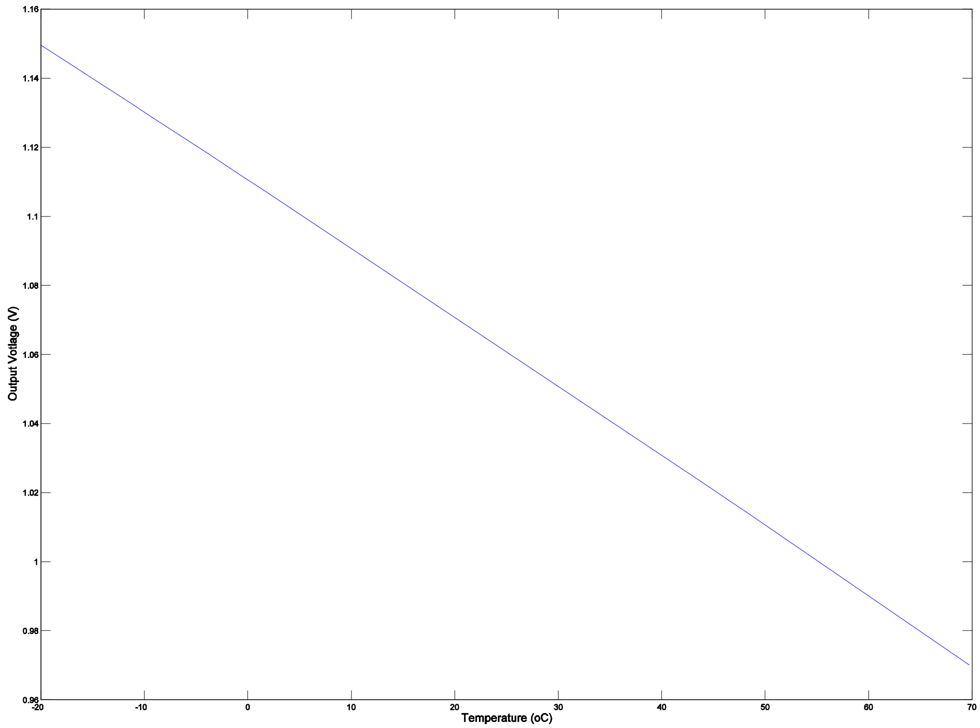

Figure 5.8 The output voltage of regulator one plotted against temperature

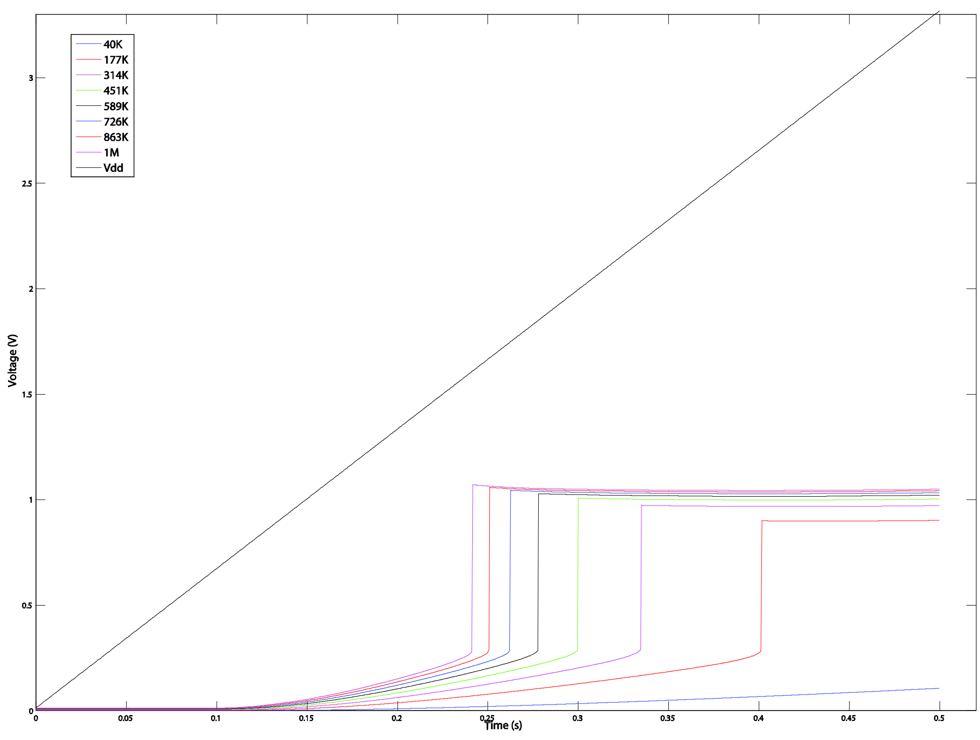

Figure 5.9 Parametric analyses with different resistance values of the load (R_L)

positive voltage-to-temperature circuit are placed behind the regulator. This places some demands on this compensating circuit however as it also needs a linear but positive dependence with the same gradient as the regulator circuit. This can for instance be done in a voltage follower (buffer) placed on the output of the regulator. This would also have a positive effect on the loading issue of the regulator which are discussed in the following paragraph. However, for reasons mentioned earlier of this system’s temperature demands, no further investigations will be performed here.

The load the regulator must power can sometimes be quite complex and hard to estimate exactly before all the following circuitry is developed. This is the case for our system and therefore investigating the loading capabilities during the development have been a handy way of ensuring proper function in the prototype and finished system. Figure 5.9 shows the circuit performance during power-up when V_{DD} (black trace) climbs from 0V to 3.3V. The capacitive load is kept constant at 10pF while the resistive load is changed according to the figure. The output voltage of the regulator is plotted together with the input (V_{DD}) which is the same for all traces.

The behaviour of the circuit is what we could have expected. The output voltage falls to lower values as the loading resistance falls. At 40kΩ the circuit do not work properly at all, and the output voltage never reaches the wanted value inside the 0 – 3.3V V_{DD} range. At a load resistance of 177kΩ, the output voltage reaches 0.905V at a V_{DD} voltage of 2.641. This gives a V_{DD} working range of 3.3V – 2.641V = 0.659V. This range is probably too narrow for our system and the load needs to be smaller (higher resistance value) for ensuring enough time to make the measurement. One positive point to mention is however the edge-effect. We saw in Figure 5.5 and Figure 5.6, which are with the same conditions as the pink 1MΩ trace shown here, the round edge of the output curve limited the V_{DD} range (depending on the variation we allowed). When the load is increased (output resistance decreased) more current flows through the circuit and the edge on the output curve becomes more square and the variation is decreased, giving a square and flat curve as the red trace in Figure 5.9 shows.

As the load resistance increases, the output voltage is raised and the V_{DD} working range is increased as seen in the other traces in the figure. In general, increased load *resistance* gives: higher output voltage and larger V_{DD} working range, but at the same time large edge effects and internal variation on the output value. Depending on the load actually connected to the regulator, a follower circuit must be considered.

As discussed in the previous paragraph, power supply rejection ratio (PSRR) is an important parameter because of the way to power the system. The different capacitances used to give an desired performance are also already mentioned and a AC-analyse gives the plot in Figure 5.10. In this simulation the testbench is altered; no load is connected to the circuit. If the load capacitance were kept in place, the result would be better as this capacitor is connected to ground. Keeping the capacitor in place would therefore be a source of error, camoflashing the performance of the circuit alone.

As seen in the figure, the regulator damps -33dB between 0 and 10kHz. At 1MHz, -6dB damping is obtained before at 13,56MHz the damping reaches −19dB. The top at 1MHz is a trade-off between start-up time, the speed of the circuit and damping. The damping at 13,56MHz is worth noting, as this is the excitation frequency for the power and communication waves. Compared to the results in the paper used as idea to this circuit (38), and other papers concerning similar circuits (41) (42), it performs quite well. At 10MHz, the PSRR in (38) is -10dB and the curve is increasing towards -9dB. Also at 10kHz, we measured a -33dB damping compared to -12dB in (38). For the similar circuits in (41) and (42), a damping of -9dB/-1.5dB and -23dB is obtained at 1MHz respectively. They do not report for higher frequencies, although for both cases the curve form indicates increasing results (towards -0dB) for increasing frequency.

All the different parts of the system should be made as power efficient as possible, but still ensuring reliable and correct performance and behaviour at any time and under all conditions. The amount of current drawn from the source were continuously checked through the whole development process and would in the end lead to a necessary choice of one of two ways of making this circuit.

The circuit presented in this paragraph is one of the ways, therefore referred to as regulator *one*. This topology is reliable in its way of function and with respect to the load connected to it. However, it utilizes a start-up circuitry and a fairly large amount of current is drawn through the two branches for giving such a flexibility of different loading. The second and slightly changed regulator which is presented in sub-chapter 5.5 is more power efficient compared to the first. This is mainly achieved by larger resistances through the two branches and by removing the start-up circuitry. This leads to a very efficient regulator but it also greatly reduces the loading capability. In practice, this means it demands a buffer with a large input impedance to amplify the output current. We will follow this thought in 5.5.

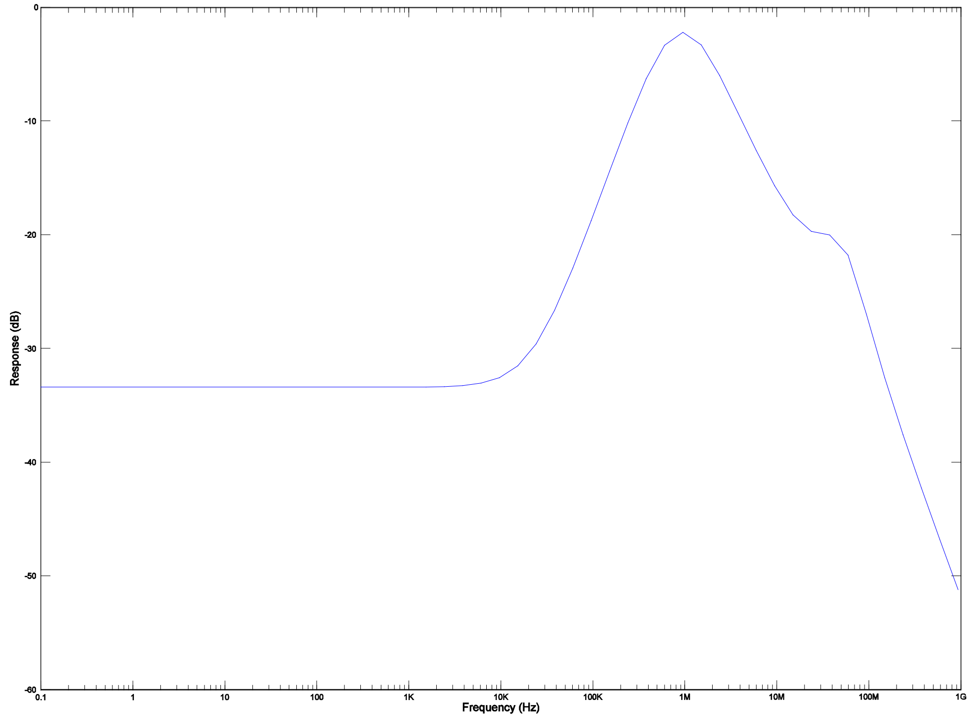

Figure 5.10 An AC-analyses showing the PSRR performance of the circuit. Frequency range is 1Hz – 1GHz and damping of Vripple-in/Vripple-out is shown in dB on the Y-axis

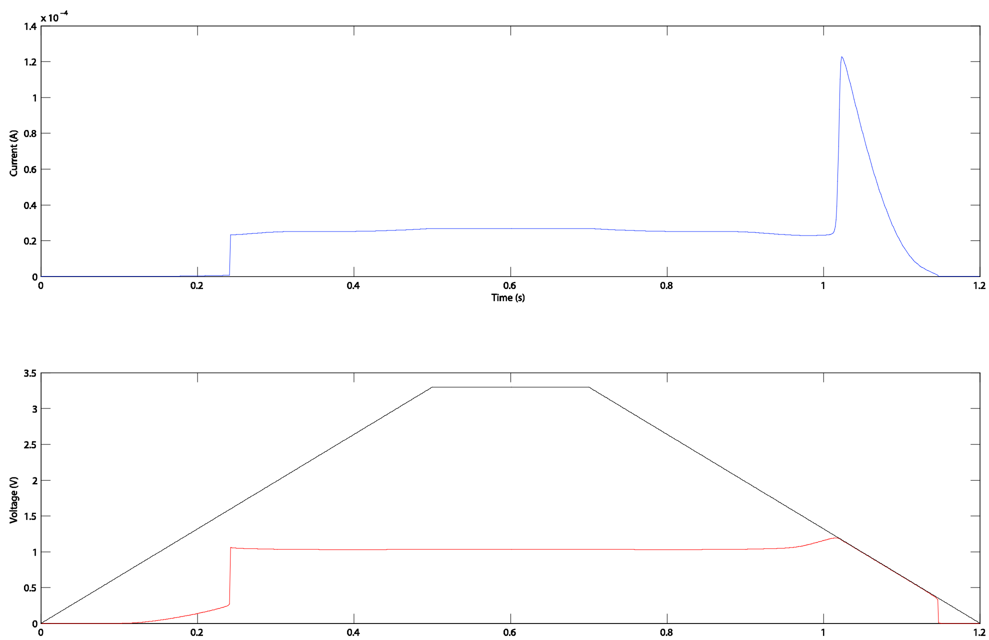

Figure 5.11 The upper half of the figure shows the current drawn from the source and through the circuit at each point of input voltage (V_{DD}) shown in the black trace in the lower half. The output voltage of the circuit is included for convenience (red trace)

Figure 5.11 shows the current drawn from the source during the whole working cycle. We see in the lower half of the figure the input voltage (V_{DD} – black), and the regulated output voltage (red) which now are familiar. In the upper half, the total current through the circuit are shown. The x-axis in the two halves is common, which means the current can be seen in all the different parts of the performance. It is clear, during power-up, the circuit does not draw current in a significant matter before the point where the output voltage climbs to its supposed value. Actually, the two curve forms (output voltage and current consumption) are quite similar. During proper function, V_{DD} between 1.7V and 3.3V, the current changes from a minimum 23.1µA (V_{DD} = 1.715V) to 26.286µA (V_{DD} = 3.3V) with the circuit simulated without loads[25]. This means a maximum power consumption during operation of

$$P = V_{DD} \times I_{DD} = 3.3V \times 26.286\mu A = 86.744\mu W$$

In the figure we also notice the large current peak when the input voltage falls below the point of operation. This phenomenon occurs because the inputs to the amplifier becomes too low. This causes the output from it to fall and the two PMOS transistors in Figure 5.1 opens. At V_{DD} still falling, the amplifier goes into sub-threshold and is no longer working. It`s output falls to zero and the two PMOS transistors opens fully. As the resistance in the two branches falls, the current rises and the peak in the figure become evident. In a system where a capacitor is charged and used as a power source, this behaviour would, in theory, empty its available current and shut the system off. Whether this behaviour is a disadvantage or not depends on the operation of the other circuitry on the implant. But for the circuitry presented in this thesis, this phenomenon would not cause any severe effects other than the instantaneously but neglibly heating of the circuit and implant.

[25] In this simulation the load resistance and capacitance are removed to isolate the current drawn only from the circuit. The load could however been simulated connected to the circuit if the current trough the resistance were subtracted from the total current delivered to the circuit.

5.4 Measurements

In this chapter we will look upon the measured results of the produced circuit and compare it to the ones we have simulated before. We will also go through the measuring devices used for the measurements and some different error sources during the inspection of the figures and curves.

The circuit was produced in STM 90nm process and the layout is shown in Figure 5.12. The total size of the circuit is 180µm x 80µm and we see the two capacitors are the two dominating parts. The resistances occupy a rather small area compared to the total size of the circuit. They are seen in the upper middle of the figure and are all placed together with dummy devices on both sides for reducing mismatch. The input V_{DD} lead is placed on the left hand side while the output of the circuit is on the right. The output is placed a far distance from both V_{DD} and ground, ensuring as little pickup as possible of any kind. Both the ground and the input are placed around the circuit without making any loops. This reduces the magnetic pickup to a minimum and is crucial when a circuit is used in an environment as here. The different transistors are placed around the resistances on both sides in such a way of making long wiring unnecessary.

The circuit was produced on an 800µm x 800µm silicon wafer (after it is cut into single chips from the larger (round) wafer) together with some other circuits for the same project. It was used ordinary packaging in 52 pin housing. A PCB[26] [27] was made for testing all the circuits and the layout is shown in Figure 5.13. It obviously contains the socket for the ASIC in the middle, a simple inductor for first order testing of an inductive link in the upper right corner, different connectors to each pin and some surface mounted variable resistances. For the regulator however, the upper half of the left hand side of the ASIC is used and only a pair of connectors for input and output is connected to each pin.

All the measurements are carried out inside a Faraday cage. This ensures proper shielding against electromagnetic radiation. (43). Further, all cabling to and from the circuit are of coax type. Although we do not involve higher frequencies in our measurement, it shields the signals from external sources and also protects the circuit from its own radiation. In addition, pickup loops are avoided all the way from the circuit to the measuring units.

[26] PCB – Printed Circuit Board
[27] The PCB was fabricated together with the supervisor of this thesis

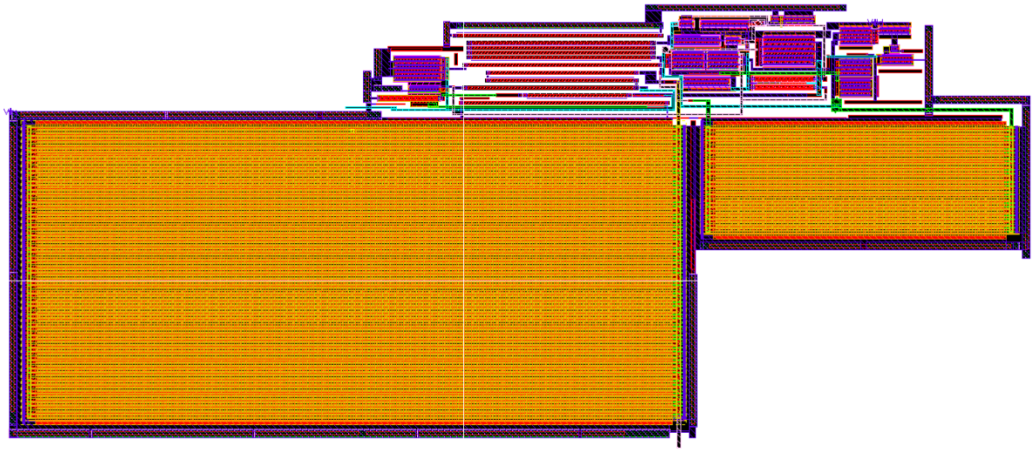

Figure 5.12 Layout of regulator one. The size of the circuit is 180µm x 80µm

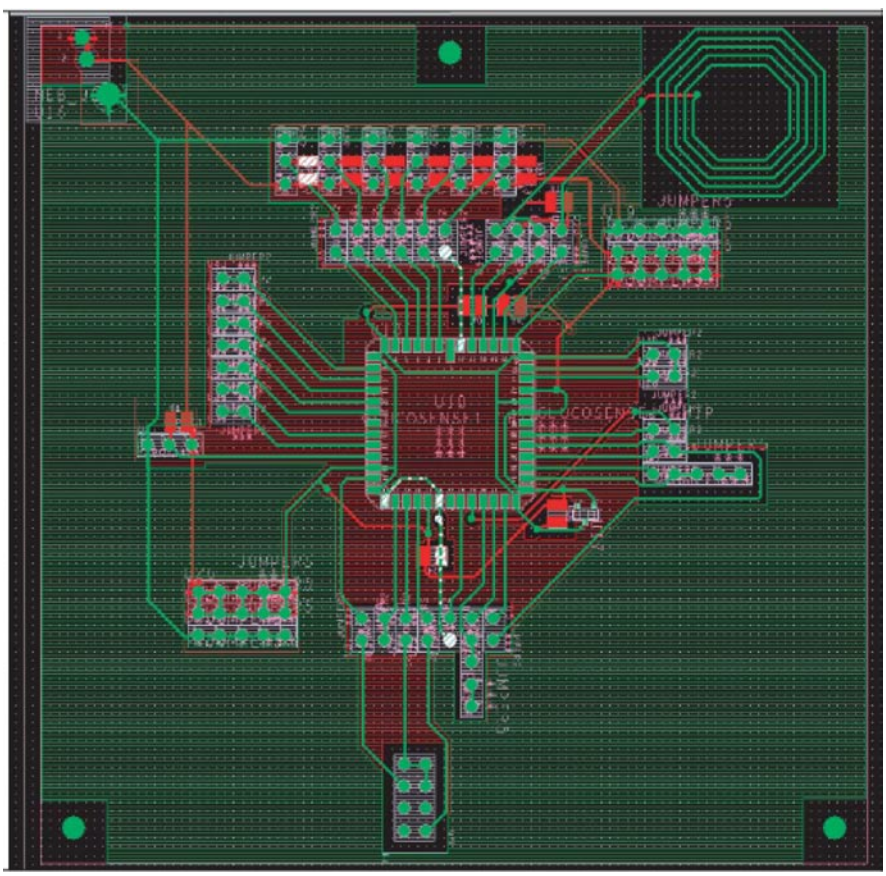

Figure 5.13 The PCB-layout for regulator testing

The output from the circuit is read through an *Agilent HP54622 oscilloscope* and a GPIB bus. The input source is a *Keithley 236 current and voltage source*. This source is both used to give an input voltage (V_{DD}) and also to read back its output current for the power consumption measurements In addition, a second Keithley source is used to power the pad-frame of the ASIC, which includes the voltage protection diodes. MatLab is used to control the GPIB bus and to perform the measurements. The fundamental MatLab script used is enclosed in Appendix C. Only small changes are done to perform all the different readings. The temperature was kept steady at 37°C trough all the measurements. The same temperature is used during simulation which allows us to compare the results in the following investigations.

First we look at the output voltage from the regulator for different input voltages. Figure 5.14 shows this voltage (red) together with the increasing input voltage (V_{DD} - blue). We see the regulator works as expected: The output stays low until the input voltage passes the point of "conduction" which the output then quickly rises to about 1V. As the input voltage keeps rising, the output voltage falls some millivolts before the steady output voltage is obtained. Depending on the allowed output variation, a stable voltage is found when the input rises above ≈1.85V. Up until the maximum 3.3V, the output is satisfactory steady.

Before comparing it to the simulated curve, we remember we found a difference in the output voltage when the input crossed the point of conduction on decreasing way compared to the increasing way. Therefore, Figure 5.15 shows the output voltage (red) with decreasing input voltage (blue). Now however, we see the output voltage curve is similar for V_{DD} on both increasing and decreasing way, and the point of conduction is at the same V_{DD} value for both cases. This difference is probably caused by (1) some capacitances which came into account in the simulation because of the speed chosen (short simulation time). In the measurement, the circuit had long time between each sampling to settle and discharge any capacitances that could cause this effect. Turning up the speed of the measurement to try to recreate such a behaviour is first; difficult because the generator and oscilloscope do not handle so many operations (change the input voltage and read the voltage) in such a short time if any demands of accuracy is kept, second; it is not wanted as the input voltage to the regulator will not change in such speeds because of the large storage capacitance (which is the V_{DD} to the regulator) and the small currents which all the following circuits draws from it. (2) can be the difference in loading of the circuit. In the simulation we loaded the circuit with a 1MΩ resistance and a 10pF capacitance. In the measurement, a 1MΩ resistance was connected between the output and the PCB ground. This ground plane may have added a resistance (small compared to the load resistance however) in series with the

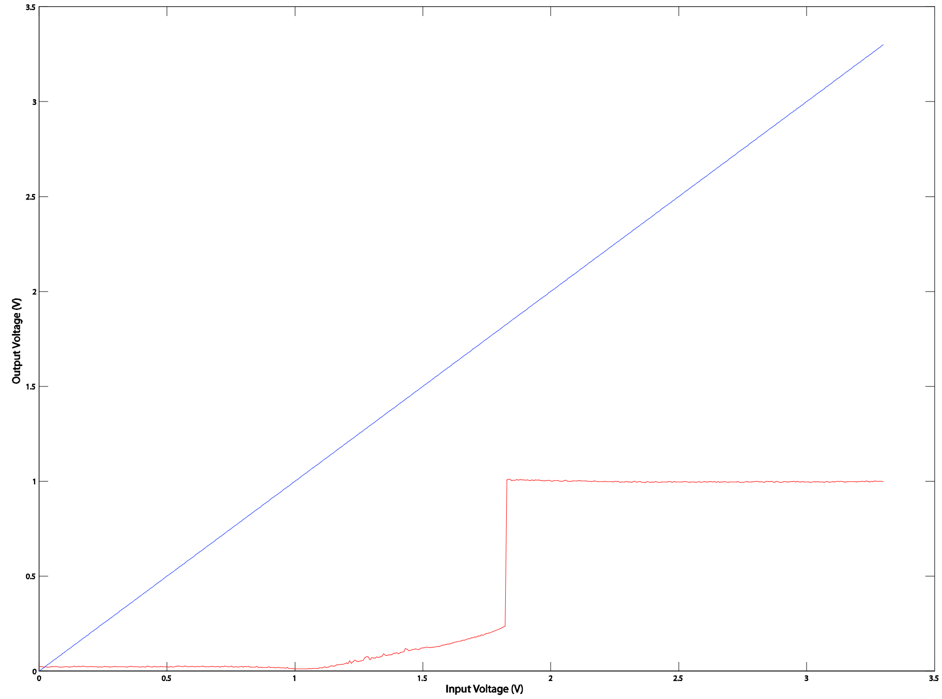

Figure 5.14 shows the output voltage (red trace) measured on the produced regulator one circuit for *increasing* input voltage. Input voltage is shown on the x-axis but for convenience, the blue trace also shows this voltage (V_{DD}) for easier comparison

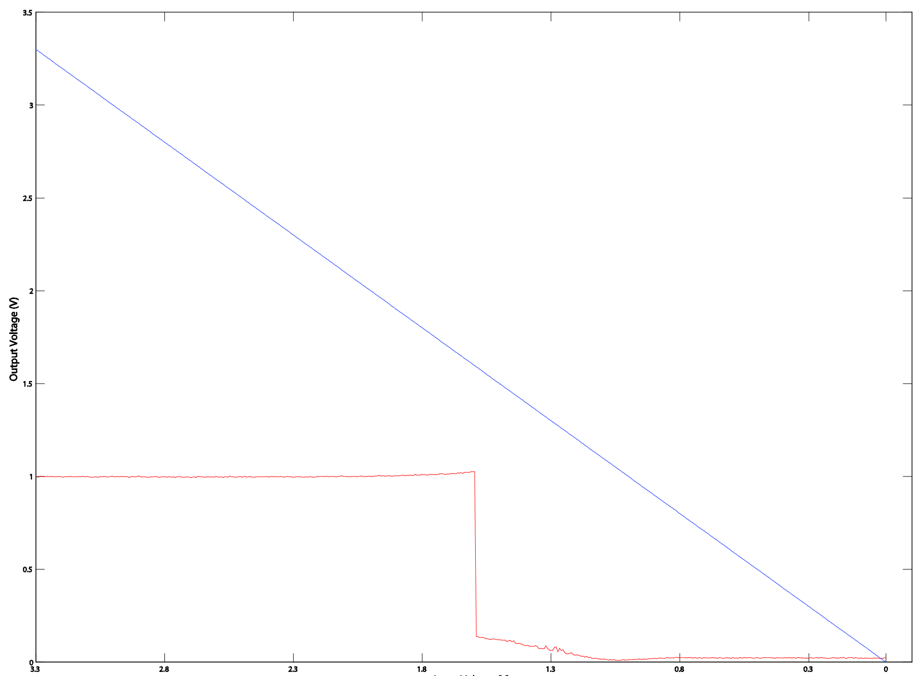

Figure 5.15 shows the output voltage (red trace) measured on the produced regulator one circuit for *decreasing* input voltage. Input voltage is again shown on the x-axis and for convenience, the blue trace also shows this voltage (V_{DD}) for easier comparison

load resistance and therefore increased this value. The 10pF was a roughly estimate of in which amount the pin of the ASIC represents a capacitance. We have no further investigation or information about this choice of value and therefore this may also have an influence to the difference from the measurement to the simulations.

The upper half of Figure 5.16 shows a common input (V_{DD} - blue) and the output from both the measurement (red) and the simulation (black) case of the regulator. The lower half shows the difference between the measured and the simulated values/curves (difference = measured - simulated). In this part of the figure the difference between the measured and the simulated results becomes clear: Only a small difference is seen up until V_{DD} reaches 1,5V. At this point, the simulated circuit reaches its point of "conduction" and the difference quickly rises. The first negative peak in the lower half of the figure is therefore caused by the difference between the two circuits point of conduction. The late point of conduction in the produced circuit is highly unwanted as we want the largest V_{DD} working range as possible. However, the stability of the measured circuit is better compared to the simulated right after passing the point of conduction. Therefore, the effective working range when stability is taken into account is not so different. As commented when investigating the simulation results separately, the simulated circuit's output falls some millivolts after the point of conduction on rising V_{DD}. This difference from the measured results seems to be caused by the high simulation resolution of the Cadence H-spice program (infinite small input voltage steps could cause states where some transistors is turned on and other is still off or in a state in between). In the measured case, the input voltage is stepped in 3.3V/500 = 6.6mV discrete points. Together with stray capacitances, internal resistance in the wires and body effects, this can add to higher transistor threshold voltages and what we can call the "semi-stable conduction output area" seen in the simulation curve is therefore not present in the measured curve.

When the measured circuit starts functioning about 0,2V later than the simulated, the difference between the circuits is again approximately zero. The measured output is however slightly lower than the simulated. This can be caused by many different factors. The most affecting are; (1) the effective resistance values of the two branches in the produced circuit[28] is different from the simulated, (2) environmental/temperature difference during measurement (a slightly higher temperature than 37^{o}C during measurement would cause a lower output voltage) and (3) not a perfect 1MΩ load resistance used during the measurements. A lower output voltage from the measured circuit is also

[28] STM states in the production manual to the 90nm process a typical value of 440Ω/sq for the Unsilicided P+ poly resistance, however, the worst case are 380Ω/sq (minimum) to 500Ω/sq (maximum).

connected to the late point of conduction. In the investigation of the performance of the circuit with other load resistance values, a clear correlation was observed between a late point of conduction and low output voltage.

The two outputs follow each other closely until the second point of conduction where the difference again becomes severe. The simulated and the measured case have two quite different ways of terminating the output voltage. Although it seems the measured case terminates at a much higher input voltage compared to the simulated, this is not the case if strict stability demands are kept. As seen when investigating the simulation results separately, the output voltage started to rise when the input voltage passed a certain voltage and was decreasing. This point (of input voltage) is about the same for the two, leaving an operational V_{DD}-range equal for both cases. For the systems overall performance, this difference shown in the lower half is not interesting as the point of conduction (with our stability demands) is equal for them both and sets the lowest V_{DD} level (a glucose measurement with V_{DD} voltage below this point would in both cases lead to wrong results of the reading).

The stability of the output voltage inside the working range is of course crucial. In the last Simulation-subchapter we looked closely at the output stability in the input voltage range of 1.7V - 3.3V - 1.7V. Now, because of the later point of conduction in the measured case, this range is not so interesting. Figure 5.17 shows in the upper half this range and the plot does not become very useful. In the lower half however, the V_{DD} range is limited to 1.85V - 3.3V - 1.85V and both the simulated (blue) and the measured case (red) is shown. The similarity in the curve form of the two cases is obvious and if placed upon each other, it would be a good match. The noise on the measured curve is also noticeable as no averaging is performed on it. A three or five point averaging would give a smoother curve, and a five point averaging is used in the following calculation of variation[29]:

[29] The rawdata files is to be found in Appendix C

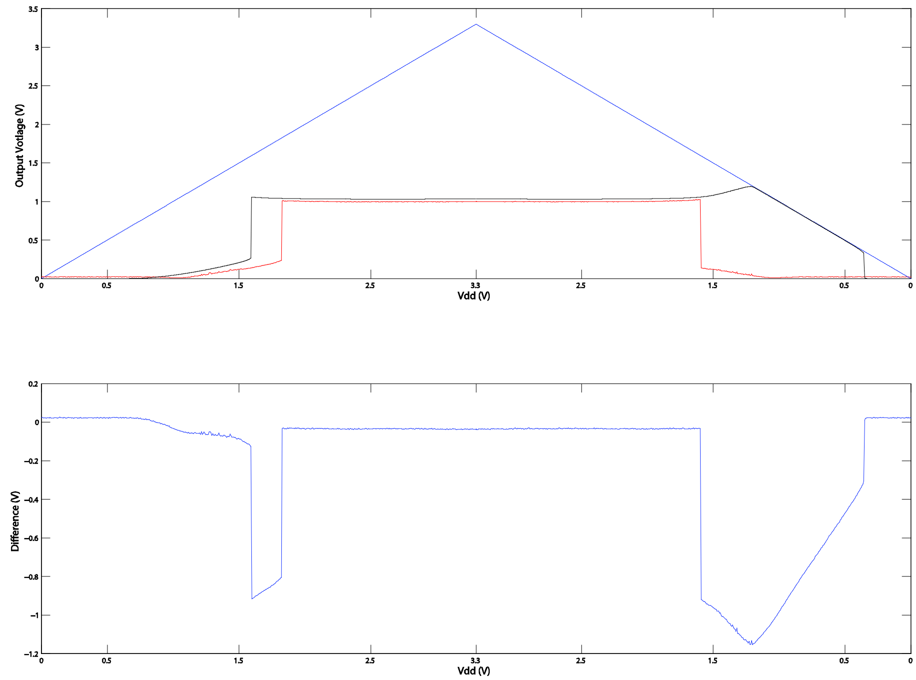

Figure 5.16 The upper half shows the input voltage (V_{DD} - blue trace) which is common for both the measured (red trace) and the simulated (black trace) output voltage of the regulator. The lower half shows the difference between the two cases with common x-axis with the upper plot

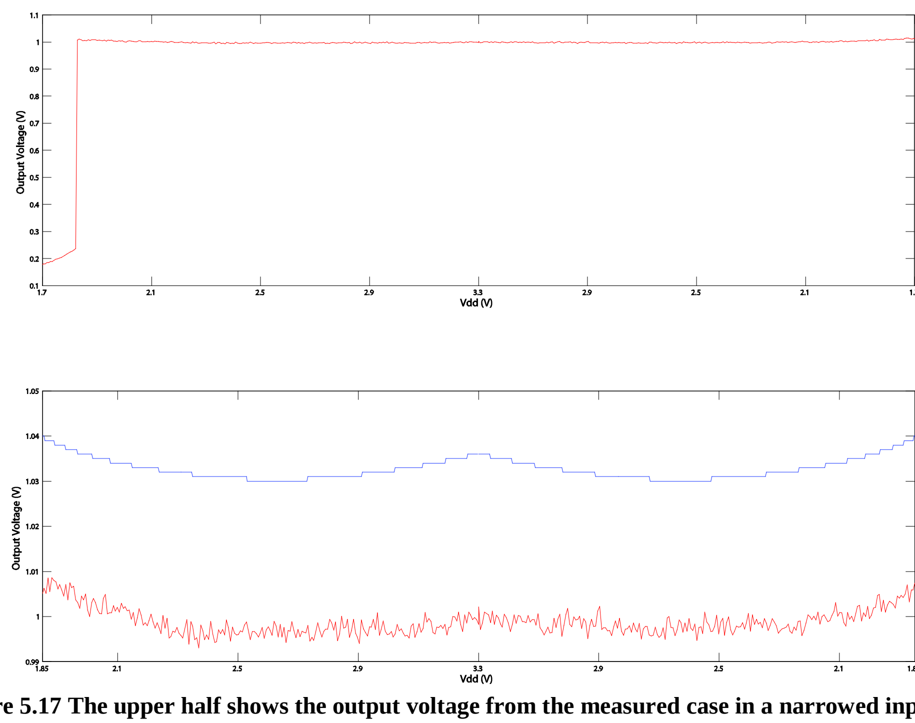

Figure 5.17 The upper half shows the output voltage from the measured case in a narrowed input voltage range. In the lower half, both the measured (red trace) and the simulated (blue trace) output voltage of the circuit is shown in the V_{DD} range of 1.85V - 3.3V - 1.85V

The simulated curve shows a maximum output value in the outer ends of

$$Vout_{Simulated\text{-}max} = 1.040V \ @ \ 1.85V$$

and minimum

$$Vout_{Simulated\text{-}min} = 1.030V \ @ \ 2.60V$$

which gives a stability of

$$V_{DD\text{-}Simulated}\text{-sensitivity} = \frac{1.04V - 1.03V}{2.60V - 1.85V} = \underline{13.3mV/V}$$

For the measured case, the maximum output is also at the outer ends

$$Vout_{Measured\text{-}max} = 1.0066 \ @ \ 1.85V$$

and minimum at

$$Vout_{Measured\text{-}min} = 0.9959 \ @ \ 2.56V$$

which gives a stability of

$$V_{DD\text{-}Measured}\text{-sensitivity} = \frac{1.0066V - 0.9959V}{2.56V - 1.85V} = \underline{15.1mV/V}$$

It is clear, both visually and mathematically, the measured case is somewhat more unstable compared to the simulated case from the minimum voltage towards the points of conduction (worst case). However, from the minimum point towards the centre, V_{DD} = 3.3V, the relationship is:

$$V_{DD\text{-}Simulated}\text{-sensitivity} = \frac{1.036V - 1.03V}{3.3V - 2.6V} = \underline{8.6mV}$$

and

$$V_{DD\text{-}Measured}\text{-sensitivity} = \frac{0.9998V - 0.9959V}{3.3V - 2.56V} = \underline{5.3mV}$$

This shows, the stability is about the same for both the simulated and the measured case. Beside of the off-set and the noise[30] on the measured signal, the simulated curve agrees closely to the measured.

[30] A short noise investigation were performed is to be found in Appendix C

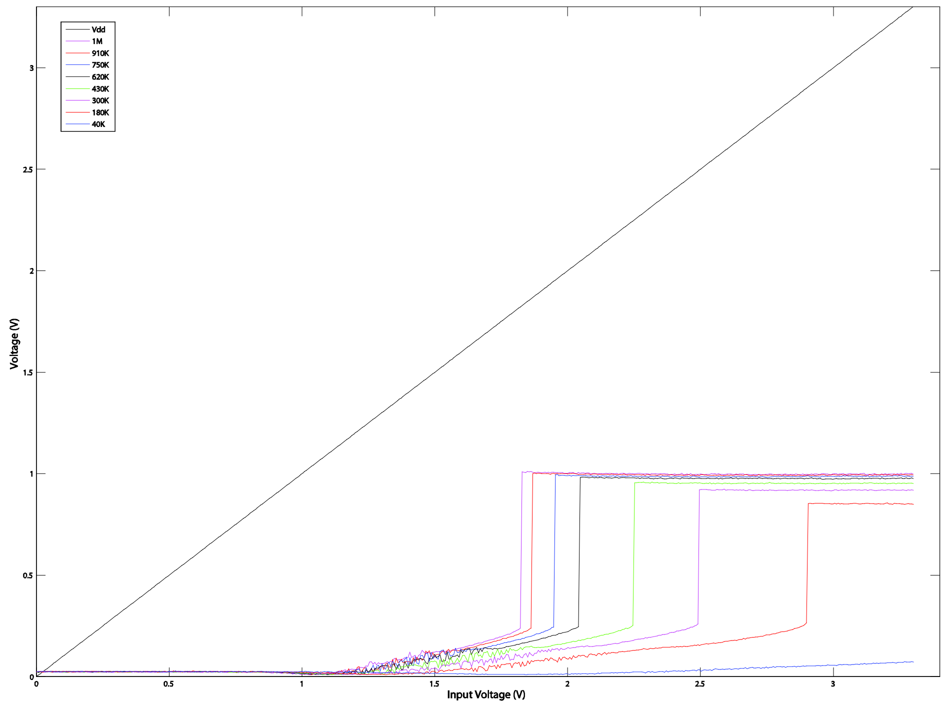

Figure 5.18 Parametric analyses with changing load resistance. The input voltage (V_{DD}) is shown together with the different output voltages from the produced circuit

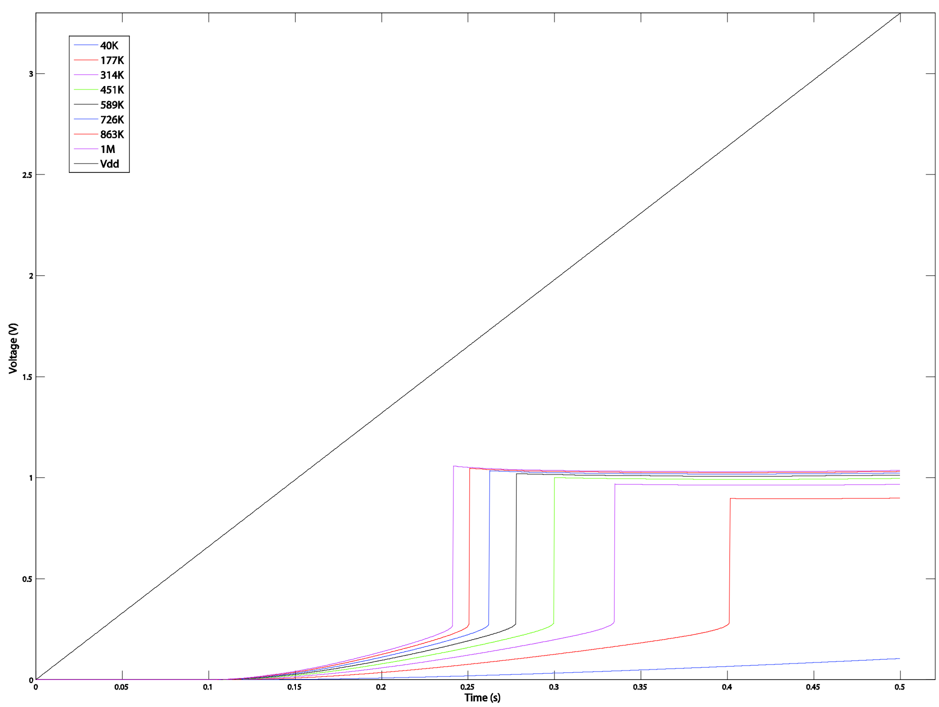

Figure 5.19 The simulated parametric analyses with changing load resistance. The input voltage (V_{DD}) is shown here as for the measured case together with the different output voltages

From the simulations we remember the difference in behavior depending on the load connected to the circuit. Figure 5.18 shows the *measured* results with about the same resistance values used in the simulations. In Figure 5.18 the simulated results are repeated for convenience (note the difference in axis-values). The two graphs show quite many similarities: Except from the noise in the measured case, the behavior before the point of conduction for each resistance value is the same. Also, the individual distance, both in point of conduction and in output voltage, from one another is equal. And in both cases, the 40kΩ resistance *shorts* the output, and inside the $3.3V_{DD}$ range no point of conduction is reached with this value and the output stays low.

A couple of differences, as we could expect from the other measurements, can be noted however. The point of conduction comes later for the measured case. It can be seen that all the different graphs are shifted some hundred millivolts to the right. This means for every resistance value, a higher input voltage is needed before the point of conduction is reached compared to the simulated case. But as we noted earlier when comparing the output curves, the shapes (the voltage fall in the output right after the point of conduction) makes this difference from the measured and the simulated case not as large as it first seems. A second difference is the slightly lower output voltage with all the different resistances for the measured case. This tendency was seen already when we first compared the outputs with 1MΩ load, and this result is in good harmony with what we could expect after investigating the reasons for the lower output. (the reasons are therefore not repeated here).

Although the environment around the regulator in this project ensures a quite stable temperature during operation, other applications can be dependent on the temperature characteristic. Figure 5.20 shows the temperature dependency of the circuit[31]. The y-axis shows the output voltage, the x-axis the temperature. The blue trace is the simulated value from Cadence and the red is the measured result. The input voltage is kept stable at 3.3V and the circuit is given 600 seconds (10 minutes) to adapt to each temperature before a reading. The temperature range used is from 2^oC to 70^oC which encloses our temperature of interest well (on both sides of 37^oC). The measurement is done twice and the readings are middle of the two runs.

[31] The rawdata from the temperature measurements and simulation are to be found in Appendix C

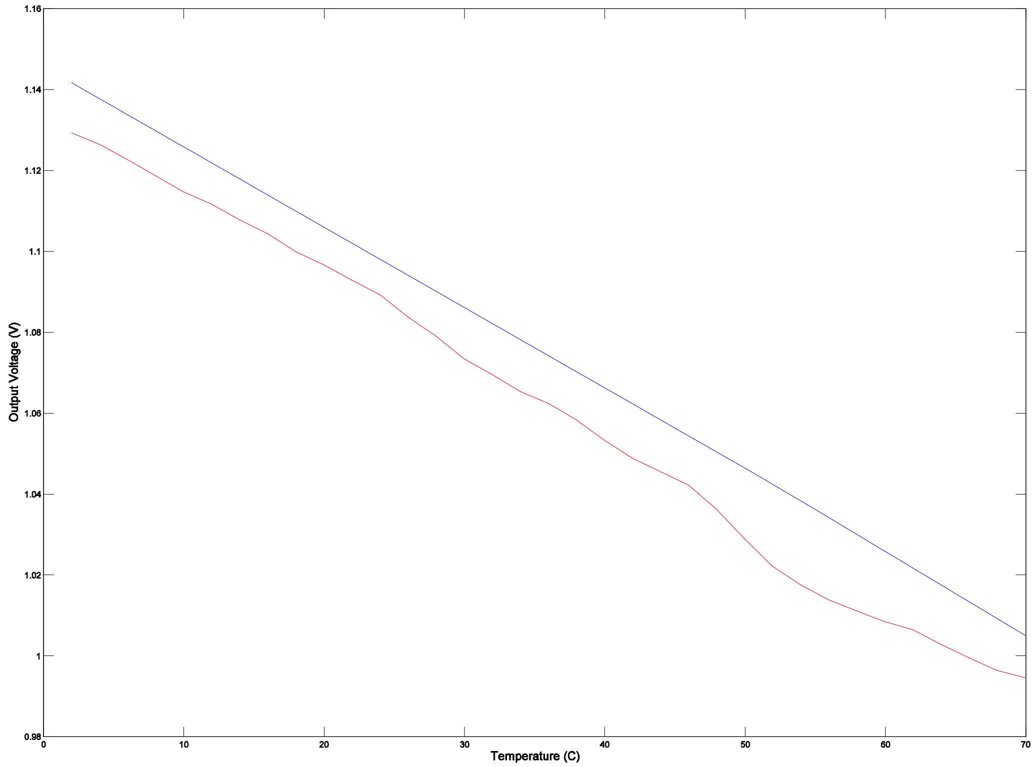

Figure 5.20 The *simulated* temperature curve is shown in the blue trace while the *measured* is shown in the red. We see the two lines are parallel and the measured output is somewhat lower than the simulated.

First, it is clear the simulated and the measured result matches quite well. When the temperature rises, the output voltage of the two traces both drops. And, they drop with the same amount; the difference in output voltage is about the same for all temperatures. This difference in output voltage, which can be seen as an off-set, is the difference we have seen and commented earlier when comparing other simulated and measured results. The causes for this difference (off-set) are therefore the same as before. Second, the measured trace is close to linear, which is the case for the simulated trace. It is only the area about 50-60^{o}C which not shows this behavior. This “dip” in the trace is hard to see what can cause, and is probably a result of too few runs. If the measurement were done multiple times, the measured graph would probably show an even stronger linear behavior and the “dip” would “climb” up and straighten out the trace.

Although a zero temperature dependency should be a goal when designing a regulator, a linear response is more easily compensated than a non-linear. The mentioned environment will not make this necessary for our project, however, we want to know dependency somewhat closer than through a graph. Because of the mentioned "dip" in the measured trace, the temperature area from 2^oC to 44^oC are used for calculation:

Simulated: $$\frac{Vout_{C1} - Vout_{C2}}{{}^oC2 - {}^oC1} = \frac{1.1073 - 1.0250}{43 - 1.6} = 1.988mV/{}^oC$$

Measured: $$\frac{Vout_{C1} - Vout_{C2}}{{}^oC2 - {}^oC1} = \frac{1.1293 - 1.0458}{44 - 2} = 1.988mV/{}^oC$$

The calculation shows a ≈$2mV/^oC$ dependency for both the simulated and the measured case. This shows the good agreement between the two traces in Figure 5.20, and is the number to compensate for if found necessary.

Finally, the current consumption is investigated. As for the simulation, the measurement is done without the 1MΩ load connected to the circuit. The output is therefore "open" and sees an infinite resistance (which is the reason for the changed output voltage curve, with an earlier point of conduction and larger V_{DD} working range). No current can therefore disappear through the output and isolates the current consumption to the circuit alone. The upper half of Figure 5.21 shows the current dissipating trough the circuit, while the lower part shows the input and output voltage to and from the circuit. The x-axis is common for the two halves and the current consumption can therefore be directly related to the operation of the circuit in any position. For convenience, the *simulated* current consumption plot is repeated in Figure 5.22 below (note the difference in axis during comperance).

At first glance it is clear the simulated and the measured curves are quite similar, both in shape and value. The large peak when the input voltage falls below the point of conduction has about the same form and at about the same place, however not the same peak value. For the measured case the peak value is about 58µA as for the simulated case it is about 125µA. This is an improvement, but as discussed earlier, this peak and its maximum value is not crucial for the operation of the circuit. What is worse is the peak seen in the measured curve when the increasing V_{DD} passes the point of conduction. The current consumption rises to almost 29µA in a short period. This rise in current is also the reason for the two corners formed at the output voltage curve. Although the duration of this peak is small, it is not wanted as it appears during power-up of the system and therefore will draw the current from a not fully charged storage capacitor. If the input current to this capacitor is larger than the peak current drawn through the regulator, this is not a problem as the input voltage will continue to climb and the current decrease again. However, it is for sure not wanted and is not appearing on the simulated curve.

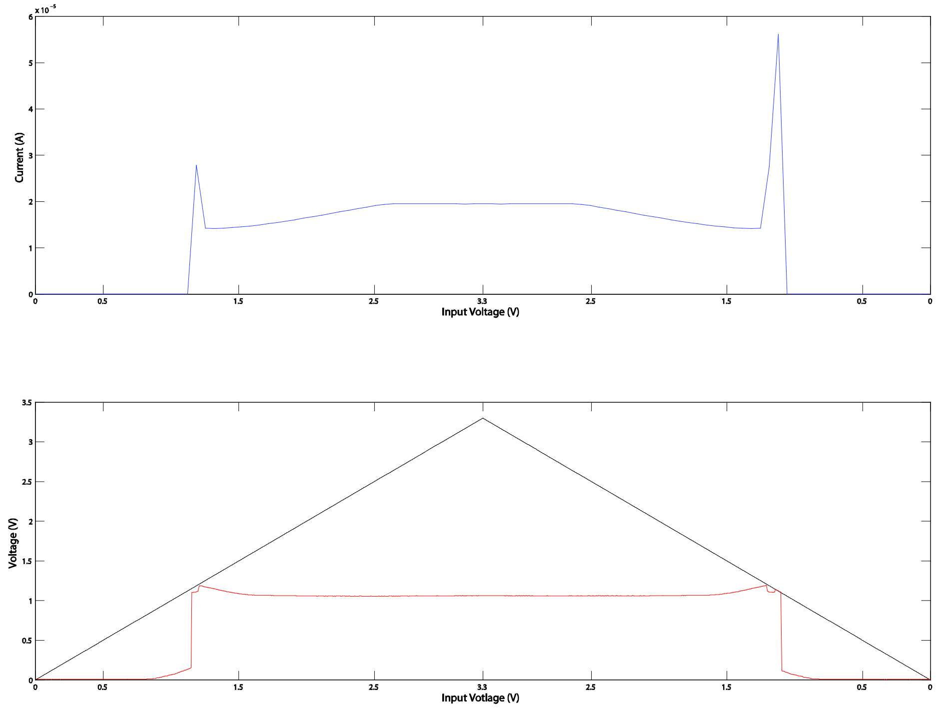

Figure 5.21 The upper half of the figure shows the current consumption of the produced circuit versus input voltage. In the lower half, both the input and the output voltage is included for convenience

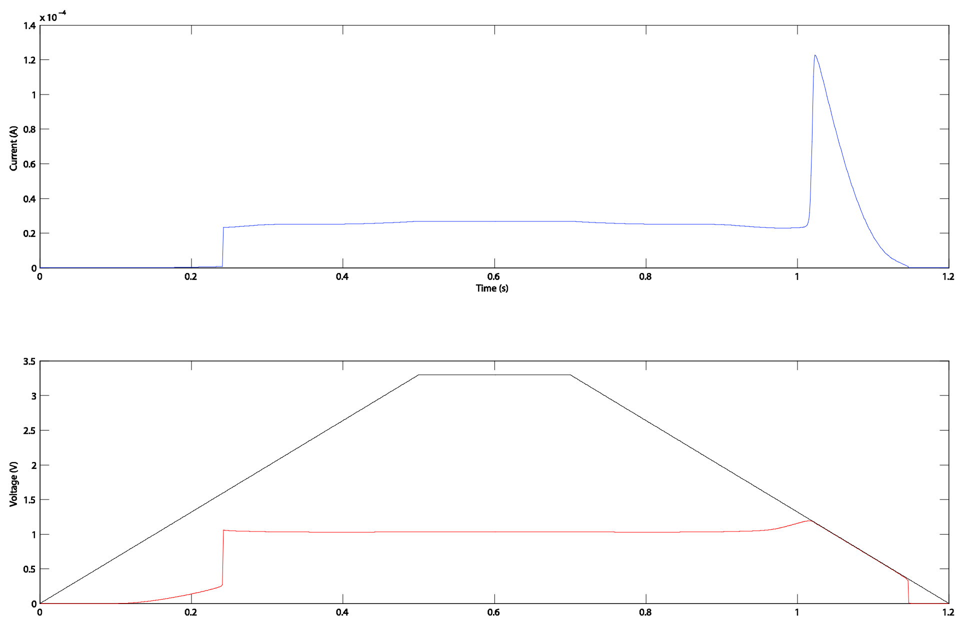

Figure 5.22 shows in the upper half the simulated current consumption. The input and output voltage is also here included for better comparing to the measured case (as the x-axis in the two figures are not identical)

A reason for this peak seems to be some capacitors which must be charged when the output "switches" from low (≈0V) to 1V. Again, some uncertainty is present around the capacitance connected to the output-pin of the ASIC. This might be a contributor to this peak. And further, any stray capacitances which becomes charged when the output voltage shifts can affect this measurement.

We see and remember the *simulated* current consumption was 26,286µA at 3.3V input. The *measured* consumption is 19.551µA at 3.3V, which means a power consumption of

$$P = V_{DD} \times I_{DD} = 3{,}3V \times 19{,}551 \mu A = 64{,}518 \mu W$$

which is $22{,}2\mu W$ lower than the *simulated*. This was no expected after what we saw in the simulation, but the difference is however pleasant. Some of the difference can be tied to the lower output voltage measured from the circuit compared to the simulated. We earlier stated that this difference is probably caused by higher resistances in the two regulator branches. This would naturally lead to lower current consumption. Without other measured results from other ASIC in the produced lot, further explanation will only be speculations. These could be questioning the test set-up and the readings from the Keithley source, to current dissipating through the pad-protecting diodes on the ASIC which could replace some of the needed current and would pass around our measuring device as this pad-frame is powered from another, separate source. However, the positive result compared to the simulation is noted before the future work would include measurements on the other ASICs.

5.5 Proposed Regulator Two

The second regulator proposed here is as mentioned not produced. It is only available in schematic form, and therefore are all the following simulations are done on the schematic. The reason for this becomes obvious after some inspection of the circuit's performance. The same paper (38) as for regulator *one* was used as starting point, and this regulator is therefore only another form of the first. The similarities become obvious when we look at the schematic in Figure 5.23. Compared to circuit one, the start-up circuit is removed and the component values are changed. The values are shown in Table 5.3. Worth mentioning is the increased resistance in the two leads. This is the main reason for this circuits decreased energy consumption compared to circuit one. In addition, other component values are slightly changed for optimizing performance with this architecture.

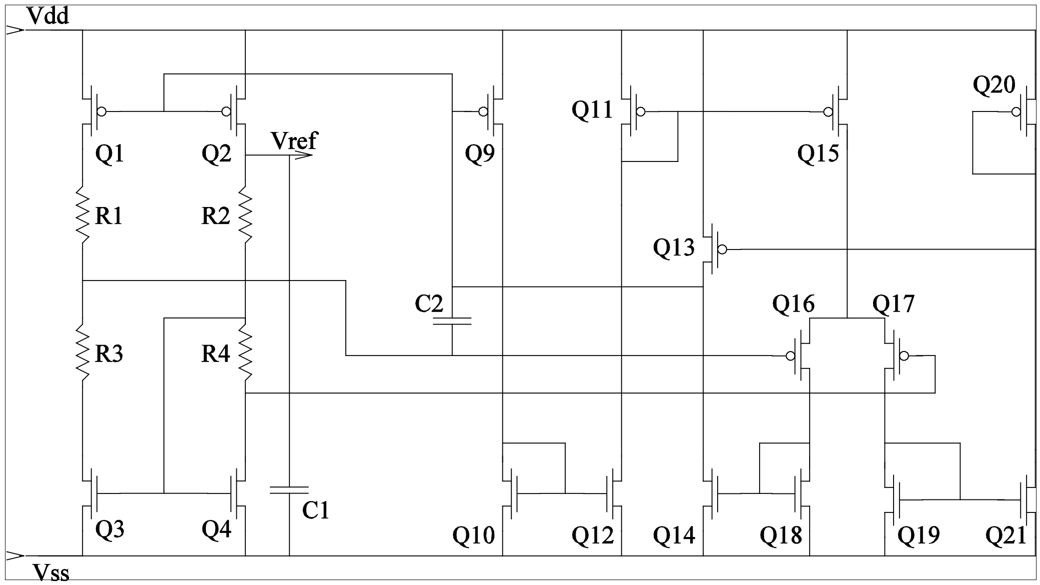

Figure 5.23 Schematic of regulator two

Device	Q1	Q2	Q3	Q4	R1	R2	R3	R4
Sizes	10/0,3	10/0,3	52/0,3	10/0,3	289,4k	145,9k	65k	70k

Device	Q11	Q15	Q16	Q17	Q18	Q19	C1	C2
Sizes	8/0,3	2/0,3	20/0,3	20/0,3	20/0,3	5/0,3	6,38pF	1pF

Table 5.3 Parameter sizes and values for regulator two

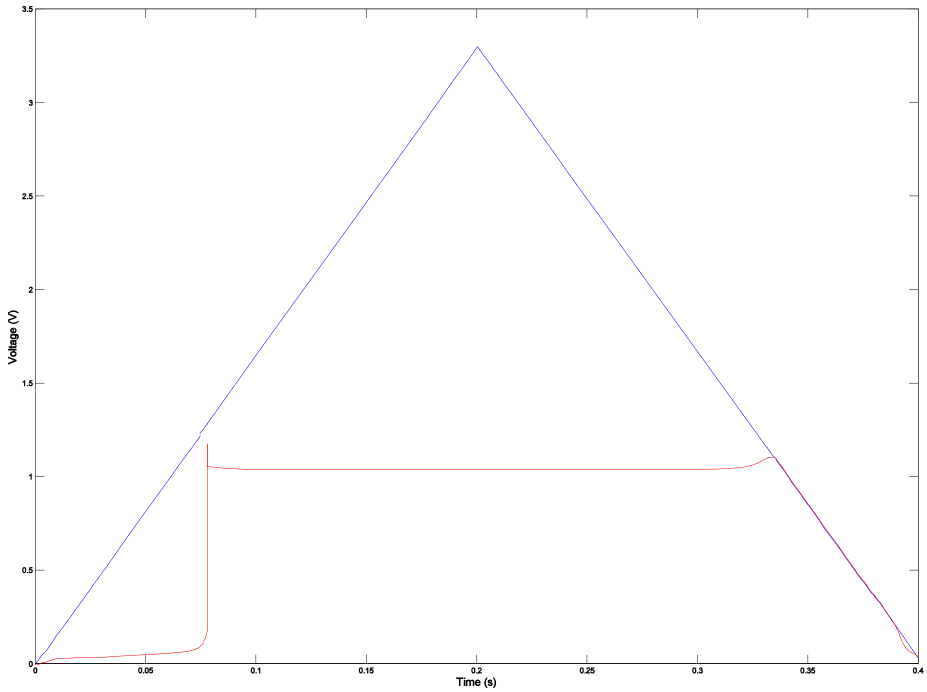

Figure 5.24 The output voltage from regulator two is shown in the red trace, while the blue is the input voltage (VDD) to the circuit

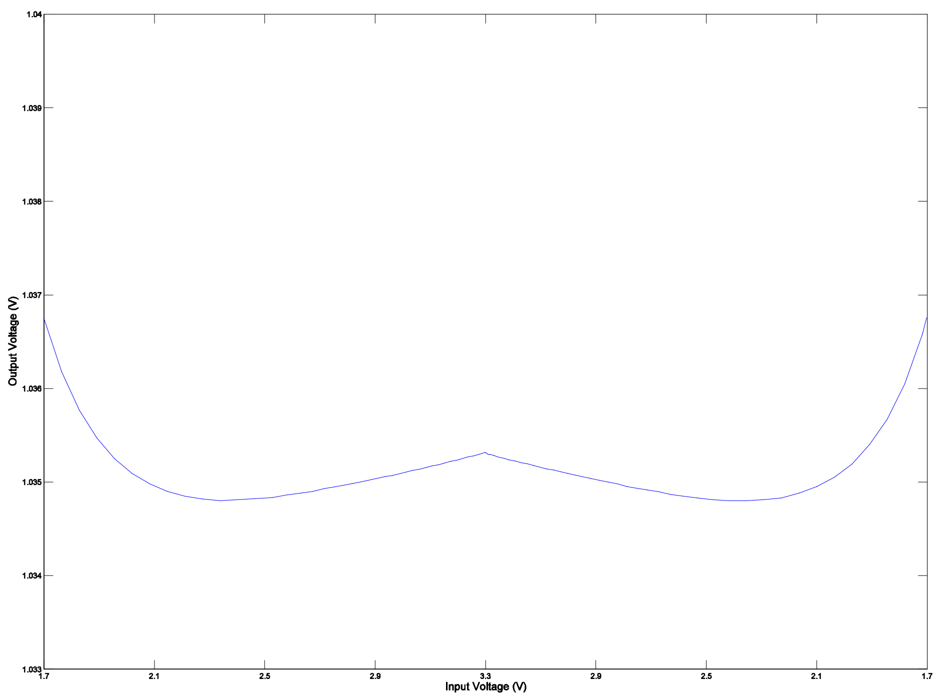

Figure 5.25 shows the output voltage in the narrowed input voltage range. The variation is clearly seen as the y-axis pitch is very fine. In input voltage range is shown on the x-axis

In the following simulations, the same testbench as for regulator *one* is used. The load resistance is however changed and are in Figure 5.24 1GΩ. The output characteristic and curve form is quite similar to the ones for circuit one. The working input voltage range and output variations are about the same. In fact, for circuit two it seems in the figure slightly better than for circuit one. This is however caused by the 1GΩ load and the picture changes dramatically when this is lowered. This is the case in Figure 5.26 which is a parametric analysis of the circuit's output voltage with different load resistances.

It is clear in this figure the mentioned issue is severe. When the load resistance decreases, more current must flow through the two branches for maintaining the output voltage. However, because of the large resistances in the branches and the output will work as a short (although the resistance is very high) the circuit will not reach the desired output voltage. Not before the load resistance is higher than about 600MΩ will the circuit work properly and be able to deliver a 1V output. When the load resistance obtains this value or higher, we see the output is nicely placed around the desired voltage.

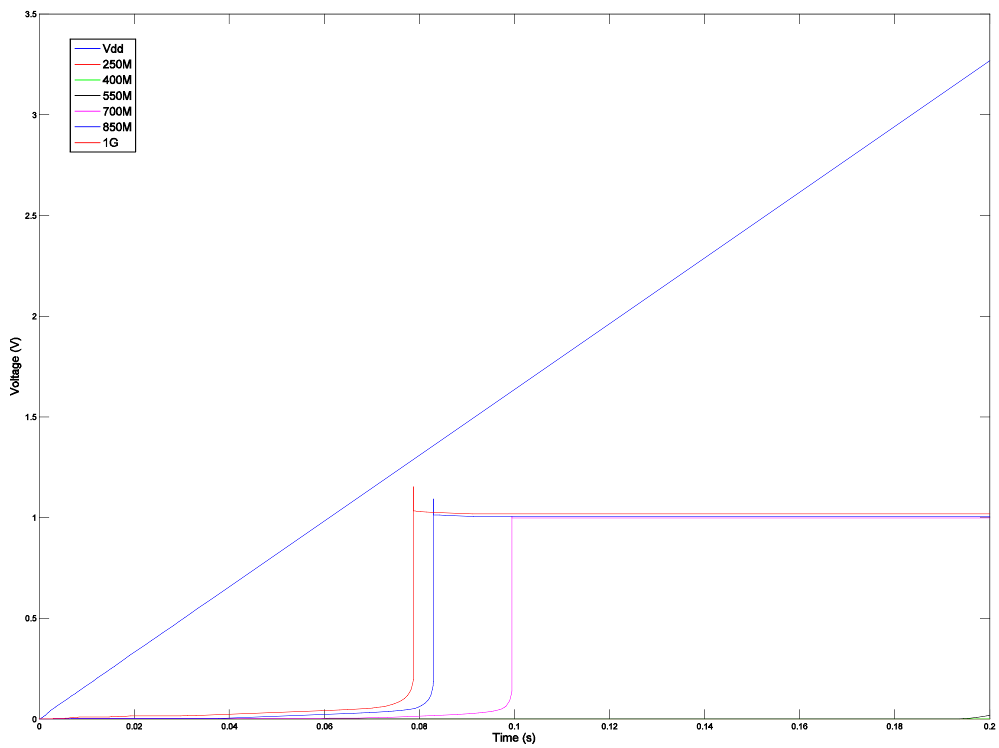

Figure 5.26 shows the output voltage of the regulator with different loads (the loads used is shown in the figure). The input voltage is included in the blue trace for convenience. Note the higher loads used here compared to the same simulation for regulator *one*

At first glance on Figure 5.26, one could say that a start-up circuitry would cure the loading issue. And a matter a fact, it will in a certain amount. A start-up circuitry like the one in circuit one would in first hand lead to the 550MΩ load curve to function properly. However, the 400MΩ would still not reach the desired output voltage, and at the same time, the power consumption increases with this start-up help. This leads to an issue the designer needs to consider: How large is the load the circuit must be able to handle? If the load represents a resistance value in the range of ≥600MΩ, *circuit two* can be used without any modifications. If the load represents a resistance in the range of ≥400kΩ, *circuit one* could be used without any changes. If the load represents a resistance in the range of 0≤150kΩ, more current must be passed through the two branches of circuit one and the power consumption would increase. It must therefore be done a weighting between passing more current through the circuit for therefore be able to power larger loads, or, consider the load resistance so low that a buffer or voltage follower would be needed to power it. Therefore, two directions of implementing such a regulator system points out and must be considered with respect to the load and power consumption: (1) Using the reference alone (like circuit one), passing enough current through the two branches to power the actual load. (2) Using a very low power consuming regulator (like circuit two) and a source follower circuit (buffer)[32] with a very high input impedance to power the load. The most power efficient (and reliable) way should of course be preferred, and which of the ways should therefore be chosen after the load of the circuit is investigated.

Finally, a Monte Carlo and the current consumption of *reference two* with 1GΩ load is simulated and shown in Table 5.4 and Figure 5.27. After 2000 runs, the mean value becomes 1.03481V and the standard deviation 24.2488mV. This is a satisfactory result but compared to circuit one (1.05743V/19.883mV), a little less stable.

MC	Runs	Mean Value	Std dev.
Value	2000	1,03481V	24,2488mV

Table 5.4 shows the result from a 2000 run Monte Carlo simulation of regulator two

[32] Source followers and buffers (also called common-drain amplifier from the way they are internally connected) made in CMOS have typically large input resistances because of the connection to the gate. Ideally this resistance is ∞ and the voltage gain is unity. In practice, the input resistance is some GΩ and the voltage amplification somewhere less than unity.

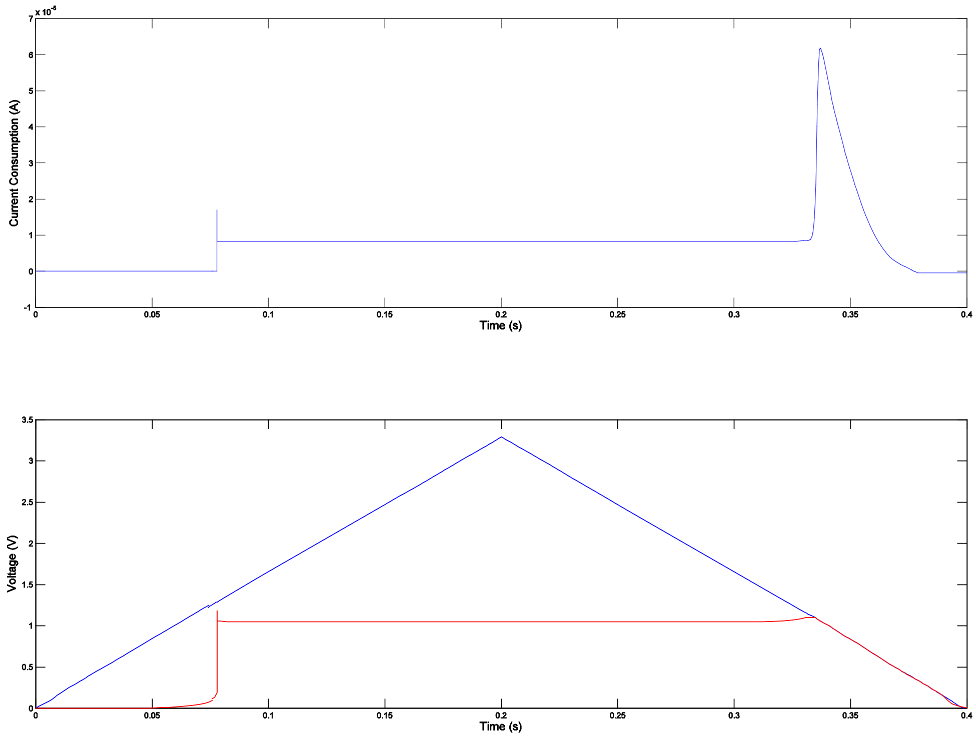

Figure 5.27 The upper half of the figure shows the simulated current consume of regulator two. The lower half shows the input voltage (V_{DD} - blue trace) and the output voltage (red trace). The x-axis is identical for the two halves

For the power efficiency, we see in the lower half of Figure 5.27 the input voltage (V_{DD} – blue) and the regulated output voltage (red) as we also saw for circuit one. In the upper half, the total current through the circuit is shown. The x-axis in the two halves is common, which means the current can be seen in all the different parts of the performance. It is clear, during power-up, the circuit does not draw current in a significant matter before the point where the output voltage climbs to its supposed value. At this point, the current does a "kick-start" and jumps to almost 17µA. However, the duration of this peak is approximately zero and will probably not imply any problem if the circuit is produced. During proper function, V_{DD} between 1.7V and 3.3V, the current changes from a minimum 8.45µA (V_{DD} = 1.7V) to 9.361µA (V_{DD} = 3.3V) with the circuit simulated without load. This means maximum power consumption during operation of

$$P = V_{DD} \times I_{DD} = 3{,}3V \times (9{,}361\mu A - 1nA) = 30{,}888\mu W$$

In the figure we also notice the current peak when the input voltage falls below the point of operation of the circuit. This is the same phenomenon as for circuit one and occurs because the inputs to the amplifier become too low.

Compared to circuit one, we remember the power consumption of 86.744µW (although we *measured* it to a lower value later), circuit two is a lot more power efficient. And as discussed, circuit two can be preferable in some cases. However, as mentioned, only circuit one was produced and of course been concentrated on in this thesis. The other simulations, *temperature* and *PSRR* showed such a similarity to the ones for regulator one and was therefore not included.

Chapter 6

6 Conclusion

6.1 Conclusion Rectifier and Chargepump

We have by calculation and simulation investigated three different rectifying topologies where two included a chargepump. Without any measuring results available, we summarize the simulated key figures and present it in Table 6.1. All these figures are retrieved from cadence with similar input signal and environment (expect R_L for circuit 2 for efficiency/power/powerxefficiency graphs) for the circuits. The numbers are therefore quite comparable.

Circuit *one* separates from the other by only consisting of a rectifier stage. Without any pumping mechanism, it has the lowest output of the three circuits as expected. We remember the $2V_{p\text{-}p}$ sinusoidal input signal for all circuits, leaving circuit one with an output about half the input voltage. The efficiency of this circuit is 27%, a little less than participated for such a configuration. A low R_S and a high R_L was expected to deliver the best efficiency. But for our way of testing, this is not the case since we remove R_S in the equation. However, the power throughput is superior compared to circuit three with 80µW. This indicates, if high power is necessary, this circuit is suited when operated with large capacitors. By turning up the input amplitude sufficiently for obtaining the wanted rectified output voltage, this circuit can deliver more current than any of the other circuits because the need for fewer capacitances, allowing each of them to be larger covering the same area as the other two.

Circuit	**Output voltage**	**Efficiency**	**Power throughput**
One	1.015V @ R_L = 100kΩ	27% @ R_S=950Ω R_L=12kΩ	80µW @ R_S=50Ω R_L=2.5kΩ
Two	2.809V @ R_L = 100kΩ	52% @ R_S=50Ω R_L=233kΩ	84µW @ R_S=50Ω R_L=183k Ω
Three	1.185V @ R_L = 100kΩ	9% @ R_S=550Ω R_L=55kΩ	50µW @ R_S=50Ω R_L=6.5k Ω

Table 6.1 shows the performance parameters for the three rectifier and chargepump circuits

Circuit *two* showed impressing results compared to the other circuits. Because of the topology with a long current path and many limiting capacitances, the lowest conversion efficiency of the three was expected. However, the circuit delivered 2.8V output with a $2V_{p-p}$ input, and the maximum efficiency is the best of the three with 52%. This efficiency is obtained with the conditions expected: A low R_S and a high R_L. The R_L did also have to be increased to find the circuit`s maximum. This fact complicates the comparing between the three circuits, and if the R_L maximum limit of 55kΩ as for the other two was kept, the maximum efficiency would been lower. The power throughput is the highest of the three circuits with 84μW. Also this obtained with a larger R_L. This makes the circuit suited for lower current demands where it can deliver a high output voltage with low input amplitude.

Circuit *three* was the most advanced circuit of the ones investigated here. It utilized the full wave rectification stage with a clever connection with the pumping unit, allowing it to run in different “modes”: A clean rectification, a clean chargepumpe and a stage in between where both stages were active. High expectations were put on this configuration but were not met. It seems strange that this circuit can only deliver about half the input voltage at efficiency as low as 9% when we compare it to the other circuits. This immediately directs some suspicion to the way this circuit was tested. In difference from the other circuits, a transformer was used together with now two R_S resistances, one on both input leads. Although the transformer was ideal, it seems this may have affected the readings. However, the output voltage was measured to 1.185V. This is some millivolts higher compared to the purely rectifying circuit *one*. This indicates, the rectifying part of circuit *three* have done its job during power up and at this output voltage, it is shut *off*. This leaves the pumping stage turned *on*, and maybe this pumping topology is the flaw of this circuit. Although it is quite similar to the mechanism in circuit *two*, they are not identical and this may cause the disappointing results, both in output voltage and in efficiency.

The power throughput is better compared to the efficiency results, but still a little worse than we could expect. Again, the rectification part alone could probably easily provide this power and a lot more, compared to what we saw for circuit *one*. But yet again, the pumping mechanism which is active at the measured output voltage may not be able to deliver more than the obtained 50μW. However, as the power throughput was simulated for many load resistance values, one could expect a higher power on the output with lower values where the rectifier part was conducting alone. This was as we saw not the case with the test conditions used here.

Pronouncing a winner of the tree different circuits is however not easy without knowing the exact input/output conditions and demands. The circuits should therefore be evaluated together with the whole system. Based on such tests, the most suited circuit should be chosen, whether it is the powerful circuit *one* with a large input voltage swing, or the more sophisticated circuit *two* with lower input swing and high output voltage. And not to forget, maybe circuit *three* could be the optimal choice when all three are tested with a complete inductive link and connected to a more complex load than only a real resistance.

6.2 Future work

As all three circuits are already produced, the future work will be measuring their performance. This will give a complete picture of their efficiency and robustness compared to the simulations alone. Also, it may indicate if the more complicated circuits like circuit two and three will have any advantage compared to the pure rectifier in circuit one. Although measuring the performance would reveal fully comparable results from all three circuits, further simulations would be preferable on circuit *three*. Developing an alternative testbench may be relevant together with testing the other two circuits in the testbench used for circuit three.

It will also be highly relevant to make a more complete test-setup and investigate the circuit's performance during similar conditions as it will experience in the finished product. This will in example be connecting the circuits to some *of the shelf* inductors for testing the inductive link input. The output connected to a capacitor of a given size and further to the produced regulator from chapter 5. This would probably give realistic test results and make comparing between the circuits easy to establish. It would also give the most useful information and results before a final circuitry should be chosen.

6.3 Conclusion Regulator

A 1V low power voltage regulator has in this thesis been described, developed, produced and tested in the STM 90nm CMOS process. In addition, a second regulator slightly different from the produced circuit was developed and described through simulations. Both references were made using only CMOS elements and resistors. The final goal of the development was a voltage reference circuit optimal for our use and project. That ment; a 1V stable output, a large V_{DD} voltage range, low power consumption and adaption to the whole system regarding input and output conditions and loading. Which of the goals were achieved?

For regulator one, we can summarize the following:

Output Voltage:	0.9959V – 1.0066V
V_{DD} Range:	1.85V – 3.3V
Power Consumption$_{max}$:	64.518µW
Temperature Stability:	1.988mV/^{o}C
Load Resistance:	≥160KΩ (depending on performance demand)
Source Resistance:	≤50Ω (which was used during tests)

The output voltage level satisfies the demands set on the circuit. Some millivolts variation is found across the V_{DD} range and compromises the stability. This variation is however not severe and is fully acceptable when following are taken into account: A measurement is performed by charging the storage capacitor to 3.3V. When this voltage is reached, the measuring circuitry is turned on and the voltage starts to drop. The sensor signal is registered and transmitted to the outer (external) circuit. When this is complete, the circuitry discharges and is turned off. This way of functioning is repeated each time, which means the point where the sensor signal is read is about at the same storage capacitor voltage each time. Ideally, the effective V_{DD} range when measurements are performed becomes limited and therefore so does the variation on the output voltage. A calibration after insertion to the patient ensures the correct value and therefore only the sensor signal changes the measured results. Although this fact cannot be guaranteed in any way, it helps to limit the possible variation between measurements caused by other effects than the sensor.

The V_{DD} range satisfies our realistic demands. Although the goal was as large range as possible, a lower boundary of 1.85V gives the time and available storage capacitor voltage drop needed for both performing the measurement and transmitting the signal to the outer unit.

Power consumption is probably the worst results of the measured performance parameters. The worst-case power consumption of 64.518µW is somewhat more than first expected. During pre-study, a realistic goal was set below 50µW. This showed however hard to achieve and had to be adjusted somewhat. For this reason, regulator two was developed which were capable of function with a much lower power consumption, but showed highly dependent on the loading of the circuit. The measured power consumption for regulator one was however much lower than the simulation predicted. Although 64.5μW is still much, this was a positive result after the indications found in the simulation.

Temperature stability was a demand which were not taken into consideration if it came in conflict with another demand. Although a theoretical way of compensating for the temperature was tried through different materials in the resistances, it was not successful. Therefore, the circuits show a severe dependency on temperature and should not be used in a changing environment if accurate and stable output voltage is important without other compensation. Because of the strong linear relationship between temperature and output voltage, additional compensation is easily possible. However, in a stable environment as out project, the regulator is still highly relevant despite its temperature dependency.

When it comes to adaption to the surrounding circuitry, it was important to make a robust circuit which could handle some output resistance of the unregulated V_{DD} and also able to directly power the sensor and its circuitry. A lot of effort was put in to this adaption, and is also what makes the circuits well suited for the finished product. This tolerance to both load and source is some of the reason to the high power consumption. It showed difficult to make a circuit which was both robust for the output resistance of the unregulated V_{DD} and output load, and at the same time low power consuming. This became mainly the reason for dividing the circuit into two parts. Regulator one can handle a wide range of loading without severely affecting the performance. Regulator two provides a 1V regulated output with low power consumption at perfect operational conditions. If these conditions can be provided for regulator two with a follower (buffer) connected to it and the total power consumption of this arrangement is still below the consumption of regulator one, this also becomes a possible solution (compared to using regulator one without a follower stage connected on the output, if possible depending on the load the sensor and its circuitry represents).

6.4 Future work

The future work will for regulator *one* be further testing against the surrounding circuitry and fully uncover whether or not the power consumption is inside the acceptable. For regulator *two*, it would be layout and production before testing its performance. Some excitement is connected to whether or not the power consumption is close to the simulated. If a lowering of the consumption would be found in the same amount as for circuit one, this circuit may be highly useful together with for example a buffer stage. And generally, a study of the total power consumption and delivery from the external unit has to be done to decide whether or not use one of the proposed regulators or a completely new circuit.

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Appendix

8 Appendix A

Capacitor size calculation:

The sensor and its circuitry are driven by DC current from a capacitor mounted external (probably) on the implant-chip. This capacitor is charged to 3,3V which are regulated down to 1V and fed into the sensor circuitry. With this setup this external capacitor works as a storage capacitor and its amount of charge it can hold and deliver is crucial for the implants operation. This makes the size of it important and it should be chosen after carefully consideration. A brief calculation is given below.

The sensor and its circuitry consumes about 50µW under operation. In addition, the regulator consumes about 50µW. This gives us

$$W_{tot} = W_{sensor} + W_{regulator}$$

$$W_{tot} = 50\mu W + 50\mu W = 100\mu W$$

At 3.3V, we get

$$I = P/U \quad \rightarrow \quad I = 100\mu W/3.3V \approx 30.3\mu A$$

A measurement takes about 20ms, which gives us

$$I = Q/t$$

$$Q = I*t \quad \rightarrow \quad Q = 30.3\mu A*20ms \approx 606nC$$

If we assume the regulator can deliver a stable 1V with a supply voltage drop of 3.3V to 1.8V, we derive the capacitance

$$C = Q/\Delta V$$

$$C = 606nC/1,5V \approx \underline{404nF}$$

As we can see, a 404nF storage capacitance would provide the needed energy for the whole measurement. However, during the time of the measurement, the storage capacitor will be continuously recharged from the external unit/magnetic field and will contribute to the energy needed. Therefore, based on the assumptions above on the circuitry's energy dissipation, a 200nF capacitor is chosen, which can store energy equal to

$$E_{stored} = 1/2CV^2$$

$$E_{stored} = ½*200nF*3{,}3^2V \approx \underline{1{,}089\mu J}$$

9 Appendix B

B.1.1 MatLab script – Efficiency Rectifier and CP

```
%MatLab Script - Efficiency Rectifier Circuit 1


% Input from file
Vin = 2;
load Grunnlag_fra_Cadence.txt;

for i =1:5
    Rs(i) = Grunnlag_fra_Cadence(i*11,1);
end



for i =1:12
    RL(i) = Grunnlag_fra_Cadence(i,2);
end

Vout = Grunnlag_fra_Cadence(:,3);
dVin = Grunnlag_fra_Cadence(:,4);


%Calculation
for a = 1:length(Rs)
    for i = 1:length(RL)
        VRsrms = (Vin - dVin((a-1)*(length(RL))+i))/(2*sqrt(2));

        IRsrms = VRsrms/Rs(a);

        PRs = VRsrms*IRsrms;
        Pin = (Vin*IRsrms)/(2*sqrt(2));

        PRL = ((Vout((a-1)*(length(RL))+i))^2)/RL(i);

        Pdiodes = Pin - PRs - PRL;

        Peffc(a,i) = PRL/(PRL + Pdiodes);
    end
end


%3D Plot
surf(RL, Rs, Peffc);
Peffc
```

B.1.2 MatLab script – Power

```
%MatLab Script - Power Rectifier Circuit 1


% Input from file
Vin = 2;
load Grunnlag_fra_Cadence.txt;


for i =1:5
    Rs(i) = Grunnlag_fra_Cadence(i*11,1);
end


for i =1:12
    RL(i) = Grunnlag_fra_Cadence(i,2);
end

Vout = Grunnlag_fra_Cadence(:,3);
dVin = Grunnlag_fra_Cadence(:,4);


%Calculation
for a = 1:length(Rs)
    for i = 1:length(RL)
        VRsrms = (Vin - dVin((a-1)*(length(RL))+i))/(2*sqrt(2));

        IRsrms = VRsrms/Rs(a);

        PRs = VRsrms*IRsrms;
        Pin = (Vin*IRsrms)/(2*sqrt(2));

        PRL(a,i) = ((Vout((a-1)*(length(RL))+i))^2)/RL(i);
    end
end

%3D Plot
surf(RL, Rs, PRL);
PRL
```

B.1.3 MatLab script – Power*Efficiency

```
%MatLab Script - Power*Efficiency Rectifier Circuit 1


% Input from file
Vin = 2;
load Grunnlag_fra_Cadence.txt;


for i =1:5
    Rs(i) = Grunnlag_fra_Cadence(i*11,1);
end


for i =1:12
    RL(i) = Grunnlag_fra_Cadence(i,2);
end

Vout = Grunnlag_fra_Cadence(:,3);
dVin = Grunnlag_fra_Cadence(:,4);


%Calculation
for a = 1:length(Rs)
    for i = 1:length(RL)
        VRsrms = (Vin - dVin((a-1)*(length(RL))+i))/(2*sqrt(2));

        IRsrms = VRsrms/Rs(a);

        PRs = VRsrms*IRsrms;
        Pin = (Vin*IRsrms)/(2*sqrt(2));

        PRL = ((Vout((a-1)*(length(RL))+i))^2)/RL(i);

        Pdiodes = Pin - PRs - PRL;

        Peffc = PRL/(PRL + Pdiodes);
        measure(a,i) = PRL*Peffc;
    end
end

%3D Plot
surf(RL, Rs, measure);
measure
```

B.2.1 Return from MatLab script – Efficiency Circuit 1

```
Peffc =

0.1212    0.1336    0.1528    0.1853    0.1877    0.2229
0.2075    0.1986    0.1881    0.1706    0.1478    0.0977

0.1445    0.1607    0.1774    0.2063    0.2154    0.2010
0.1775    0.1667    0.1547    0.1331    0.1048    0.0652

0.1622    0.1792    0.1976    0.2245    0.2364    0.1979
0.1579    0.1431    0.1269    0.1063    0.0803    0.0463

0.1719    0.1954    0.2161    0.2372    0.2554    0.1977
0.1492    0.1332    0.1152    0.0951    0.0703    0.0399

0.1884    0.2056    0.2304    0.2551    0.2720    0.1956
0.1418    0.1244    0.1058    0.0869    0.0638    0.0358
```

B.2.2 Return from MatLab script – Power Circuit 1

```
PRL =

   1.0e-04 *

0.1556    0.1844    0.2258    0.2917    0.4129    0.7009
0.7873    0.7992    0.8000    0.7798    0.7023    0.4993

0.1373    0.1613    0.1954    0.2471    0.3332    0.4666
0.4638    0.4516    0.4292    0.3904    0.3276    0.2122

0.1202    0.1401    0.1681    0.2085    0.2680    0.3058
0.2689    0.2500    0.2268    0.1949    0.1513    0.0898

0.1126    0.1311    0.1565    0.1921    0.2408    0.2478
0.2034    0.1849    0.1638    0.1382    0.1040    0.0605

0.1070    0.1240    0.1473    0.1796    0.2212    0.2074
0.1613    0.1444    0.1248    0.1042    0.0774    0.0442
```

B.2.3 Return from MatLab script – Power*Efficiency Circuit 1

```
measure =

   1.0e-04 *

0.0189    0.0246    0.0345    0.0541    0.0775    0.1562
0.1634    0.1588    0.1505    0.1331    0.1038    0.0488

0.0198    0.0259    0.0347    0.0510    0.0718    0.0938
0.0823    0.0753    0.0664    0.0520    0.0343    0.0138

0.0195    0.0251    0.0332    0.0468    0.0634    0.0605
0.0425    0.0358    0.0288    0.0207    0.0122    0.0042

0.0194    0.0256    0.0338    0.0456    0.0615    0.0490
0.0303    0.0246    0.0189    0.0132    0.0073    0.0024

0.0202    0.0255    0.0339    0.0458    0.0602    0.0406
0.0229    0.0180    0.0132    0.0091    0.0049    0.0016
```

B.2.4 Return from MatLab script – Efficiency Circuit 2

```
Peffc =

    0.2541    0.3237    0.3071    0.3573    0.3805    0.5152    0.3428    0.0295
    0.2927    0.3094    0.3214    0.3298    0.3370    0.3248    0.2596    0.0416
    0.2691    0.2918    0.2954    0.3022    0.3005    0.2785    0.2082    0.0311
    0.2636    0.2814    0.2861    0.2861    0.2798    0.2600    0.1818    0.0266
    0.2542    0.2733    0.2737    0.2759    0.2611    0.2376    0.1606    0.0228
```

B.2.5 Return from MatLab script – Power Circuit 2

```
PRL =

   1.0e-04 *

    0.5832    0.6810    0.7485    0.8028    0.8368    0.7862    0.4898    0.0677

    0.4479    0.5170    0.5553    0.5857    0.5849    0.5452    0.3623    0.0538

    0.3279    0.3673    0.3868    0.3975    0.3864    0.3531    0.2420    0.0375

    0.2738    0.3029    0.3159    0.3203    0.3068    0.2799    0.1917    0.0293

    0.2322    0.2551    0.2631    0.2652    0.2510    0.2271    0.1552    0.0229
```

B.2.6 Return from MatLab script – Power*Efficiency Circuit 2

```
measure =

   1.0e-04 *

    0.1482    0.2204    0.2298    0.2868    0.3183    0.4051    0.1679    0.0020

    0.1311    0.1600    0.1785    0.1932    0.1971    0.1771    0.0940    0.0022

    0.0882    0.1072    0.1142    0.1201    0.1161    0.0983    0.0504    0.0012

    0.0722    0.0852    0.0904    0.0916    0.0859    0.0728    0.0348    0.0008

    0.0590    0.0697    0.0720    0.0732    0.0655    0.0540    0.0249    0.0005
```

B.2.7 Return from MatLab script – Efficiency Circuit 3

```
Peffc =

0.0834    0.0852    0.0866    0.0906    0.0915    0.0832
0.0703    0.0655    0.0577    0.0493    0.0380    0.0223

0.0919    0.0924    0.0915    0.0893    0.0821    0.0551
0.0408    0.0364    0.0311    0.0250    0.0181    0.0099

0.0945    0.0923    0.0890    0.0832    0.0706    0.0396
0.0276    0.0240    0.0200    0.0157    0.0111    0.0058

0.0925    0.0899    0.0855    0.0781    0.0642    0.0335
0.0227    0.0198    0.0163    0.0127    0.0088    0.0046

0.0895    0.0863    0.0813    0.0730    0.0584    0.0290
0.0195    0.0166    0.0138    0.0107    0.0074    0.0038
```

B.2.8 Return from MatLab script – Power Circuit 3

```
PRL =

   1.0e-04 *

0.2113    0.2399    0.2786    0.3336    0.4140    0.4732
0.4180    0.3896    0.3532    0.3039    0.2409    0.1496

0.1587    0.1730    0.1898    0.2083    0.2226    0.1818
0.1417    0.1274    0.1106    0.0900    0.0664    0.0370

0.1147    0.1203    0.1251    0.1271    0.1197    0.0757
0.0542    0.0474    0.0399    0.0315    0.0224    0.0118

0.0953    0.0980    0.0994    0.0975    0.0869    0.0499
0.0344    0.0301    0.0249    0.0195    0.0136    0.0071

0.0803    0.0813    0.0809    0.0771    0.0659    0.0352
0.0239    0.0205    0.0171    0.0133    0.0092    0.0047
```

B.2.9 Return from MatLab script – Power*Efficiency Circuit 3

```
measure =

   1.0e-05 *

0.1763    0.2044    0.2411    0.3021    0.3788    0.3939
0.2938    0.2553    0.2039    0.1498    0.0915    0.0333

0.1459    0.1598    0.1738    0.1860    0.1828    0.1001
0.0578    0.0463    0.0343    0.0225    0.0120    0.0037

0.1084    0.1110    0.1114    0.1058    0.0845    0.0300
0.0149    0.0114    0.0080    0.0049    0.0025    0.0007

0.0882    0.0881    0.0850    0.0761    0.0558    0.0167
0.0078    0.0059    0.0041    0.0025    0.0012    0.0003

0.0719    0.0702    0.0658    0.0563    0.0385    0.0102
0.0047    0.0034    0.0024    0.0014    0.0007    0.0002
```

B.3.1 Rawdata for MatLab script (Circuit 1)

R_S	R_L	V_{out}	dV_{in}
50	55000	0.925	1.974
50	45000	0.911	1.972
50	35000	0.889	1.970
50	25000	0.854	1.968
50	15000	0.787	1.955
50	5000	0.592	1.935
50	3000	0.486	1.921
50	2500	0.447	1.916
50	2000	0.400	1.911
50	1500	0.342	1.904
50	1000	0.265	1.900
50	500	0.158	1.892
250	55000	0.869	1.900
250	45000	0.852	1.894
250	35000	0.827	1.883
250	25000	0.786	1.872
250	15000	0.707	1.831
250	5000	0.483	1.732
250	3000	0.373	1.691
250	2500	0.336	1.677
250	2000	0.293	1.667
250	1500	0.242	1.643
250	1000	0.181	1.612
250	500	0.103	1.591
550	55000	0.813	1.821
550	45000	0.794	1.810
550	35000	0.767	1.791
550	25000	0.722	1.769
550	15000	0.634	1.708
550	5000	0.391	1.566
550	3000	0.284	1.501
550	2500	0.250	1.481
550	2000	0.213	1.462
550	1500	0.171	1.439
550	1000	0.123	1.414
550	500	0.067	1.382
750	55000	0.787	1.779
750	45000	0.768	1.773
750	35000	0.740	1.752
750	25000	0.693	1.717
750	15000	0.601	1.659
750	5000	0.352	1.498
750	3000	0.247	1.427
750	2500	0.215	1.409
750	2000	0.181	1.383
750	1500	0.144	1.358
750	1000	0.102	1.334
750	500	0.055	1.301
950	55000	0.767	1.754
950	45000	0.747	1.736
950	35000	0.718	1.717
950	25000	0.670	1.682
950	15000	0.576	1.618
950	5000	0.322	1.441
950	3000	0.220	1.368
950	2500	0.190	1.343
950	2000	0.158	1.322
950	1500	0.125	1.299
950	1000	0.088	1.278
950	500	0.047	1.251

B.3.2 Rawdata for MatLab script (Circuit 2)

R_S	R_L	V_{out}	dV_{in}
50	383000	4.726	1.953
50	283000	4.390	1.957
50	233000	4.176	1.950
50	183000	3.833	1.954
50	133000	3.336	1.955
50	100000	2.804	1.969
50	50000	1.565	1.971
50	5000	0.184	1.953
250	383000	4.142	1.833
250	283000	3.825	1.816
250	233000	3.597	1.809
250	183000	3.274	1.803
250	133000	2.789	1.808
250	100000	2.335	1.815
250	50000	1.346	1.849
250	5000	0.164	1.861
550	383000	3.544	1.681
550	283000	3.224	1.668
550	233000	3.002	1.651
550	183000	2.697	1.649
550	133000	2.267	1.659
550	100000	1.879	1.665
550	50000	1.100	1.699
550	5000	0.137	1.685
750	383000	3.238	1.614
750	283000	2.928	1.595
750	233000	2.713	1.581
750	183000	2.421	1.573
750	133000	2.020	1.585
750	100000	1.673	1.595
750	50000	0.979	1.606
750	5000	0.121	1.583
950	383000	2.982	1.553
950	283000	2.687	1.539
950	233000	2.476	1.519
950	183000	2.203	1.519
950	133000	1.827	1.519
950	100000	1.507	1.523
950	50000	0.881	1.515
950	5000	0.107	1.488

B.3.3 Rawdata for MatLab script (Circuit 3)

R_S	R_L	V_{out}	dV_{in}
50	55000	1.078	1.948
50	45000	1.039	1.942
50	35000	0.9875	1.9334
50	25000	0.9132	1.9234
50	15000	0.788	1.905
50	5000	0.4864	1.879
50	3000	0.3541	1.873
50	2500	0.3121	1.873
50	2000	0.2658	1.869
50	1500	0.2135	1.868
50	1000	0.1552	1.864
50	500	0.0865	1.855
250	55000	0.9342	1.8092
250	45000	0.8823	1.7908
250	35000	0.8151	1.765
250	25000	0.7217	1.7302
250	15000	0.5778	1.6768
250	5000	0.3015	1.583
250	3000	0.2062	1.5526
250	2500	0.1785	1.5468
250	2000	0.1487	1.5366
250	1500	0.1162	1.5282
250	1000	0.0815	1.5174
250	500	0.0430	1.5056
550	55000	0.7943	1.6824
550	45000	0.7357	1.6532
550	35000	0.6618	1.6176
550	25000	0.5638	1.5722
550	15000	0.4238	1.5036
550	5000	0.1946	1.3988
550	3000	0.1275	1.367
550	2500	0.1089	1.3596
550	2000	0.0893	1.3494
550	1500	0.0687	1.3416
550	1000	0.0473	1.3326
550	500	0.0243	1.3216
750	55000	0.7239	1.6182
750	45000	0.6642	1.588
750	35000	0.5899	1.550
750	25000	0.4937	1.501
750	15000	0.3611	1.4334
750	5000	0.1579	1.3286
750	3000	0.1016	1.3036
750	2500	0.0867	1.2956
750	2000	0.0706	1.288
750	1500	0.0541	1.2798
750	1000	0.0369	1.2712
750	500	0.0188	1.2622
950	55000	0.6645	1.5644
950	45000	0.6048	1.5332
950	35000	0.532	1.4942
950	25000	0.4389	1.4452
950	15000	0.3143	1.3782
950	5000	0.1326	1.2818
950	3000	0.0847	1.257
950	2500	0.0716	1.2506
950	2000	0.0585	1.2426
950	1500	0.0446	1.2354
950	1000	0.0303	1.2288
950	500	0.0154	1.220

10 Appendix C

C.1 MatLab Measuring Script – Regulator

```
% Input data
%----------------------------------------------------------------

% Vdd padframe
Vdd = 3.3;
% Vmin, lowest input voltage to DUT
Vmin = 0;
% Vmax, highest input voltage to DUT
Vmax = 3.3;
% n, number of discrete steps of input voltage
n = 50;

%----------------------------------------------------------------

% Initialize the instruments
addpath(genpath('~mes/src/matlab/gpib/linux'));
K236_SetVLimit(3.4, 12);
K236_SetVLimit(3.4, 30);

% Make a input vector
Vin = [Vmin:(Vmax-Vmin)/n:Vmax];
% Make the inverted input vector
Vin2 = [Vmax:-(Vmax-Vmin)/n:Vmin];

% Set Vdd/Padframe on K236 GPIB 12
K236_SetVolt(3.3, 12);
% Switch the output on
K236_Read(12);
% Set input voltage on K236 GPIB 30
K236_SetVolt(0,30);
% Switch the output on
K326_Read(30);

% Measurements
for i=27:length(Vin),
% Step the Vin vector on K236 GPIB 30
K236_SetVolt(Vin(i),30);
% Pause to make sure the output signal is stable
pause(1)
% Read the measured current on K236 GPIB 30
Iout(i)=K236_Read(30);
```

```
% Pause to make sure the output signal is stable
pause(0.1)
% Read the measured output voltage with ocsiloscope
Vout(i)=HP54622_MeasVrms(2,24)
% Pause before new reading
pause(1)
end

for i=35:length(Vin2),
% Step the Vin vector on K236 GPIB 30
K236_SetVolt(Vin2(i),30);
% Pause to make sure the output signal is stable
pause(1)
% Read the measured current on K236 GPIB 30
Iout(i+length(Vin))=K236_Read(30);
% Pause to make sure the output signal is stable
pause(0.1)
% Read the measured output voltage with ocsiloscope
Vout(i+length(Vin))=HP54622_MeasVrms(2,24)
% Pause before new reading
pause(1)
end

% Turn off the Vref supply voltage
K236_SetVolt(0,30);

% Plot the result in figure(1)
figure(1); plot(Vin,Iout);
% Plot the result in figure(2)

% Save the measuring data
save Measurement_Regulator_Time Time Vout;
save Measurement_Regulator_Vin Vin Vin2 Vout;
```

C.2 Rawdata Regulator, Vout Simulated (Vin = 1.85V – 1.85V)

1.0400	1.0360	1.0330	1.0320	1.0310	1.0300	1.0310
1.0400	1.0360	1.0330	1.0320	1.0310	1.0300	1.0310
1.0400	1.0360	1.0330	1.0320	1.0310	1.0300	1.0310
1.0390	1.0360	1.0330	1.0320	1.0310	1.0300	1.0310
1.0390	1.0350	1.0330	1.0320	1.0310	1.0300	1.0310
1.0390	1.0350	1.0330	1.0320	1.0310	1.0300	1.0310
1.0390	1.0350	1.0330	1.0320	1.0310	1.0300	1.0310
1.0390	1.0350	1.0330	1.0320	1.0310	1.0300	1.0310
1.0390	1.0350	1.0330	1.0320	1.0310	1.0300	1.0310
1.0390	1.0350	1.0330	1.0320	1.0310	1.0300	1.0310
1.0390	1.0350	1.0330	1.0320	1.0310	1.0300	1.0310
1.0390	1.0350	1.0330	1.0310	1.0310	1.0300	1.0310
1.0390	1.0350	1.0330	1.0310	1.0310	1.0300	1.0310
1.0380	1.0350	1.0330	1.0310	1.0310	1.0300	1.0310
1.0380	1.0350	1.0330	1.0310	1.0310	1.0300	1.0310
1.0380	1.0350	1.0330	1.0310	1.0310	1.0300	1.0310
1.0380	1.0350	1.0330	1.0310	1.0310	1.0300	1.0310
1.0380	1.0350	1.0330	1.0310	1.0310	1.0300	1.0310
1.0380	1.0350	1.0330	1.0310	1.0310	1.0300	1.0310
1.0380	1.0350	1.0330	1.0310	1.0300	1.0300	1.0310
1.0380	1.0350	1.0330	1.0310	1.0300	1.0300	1.0310
1.0380	1.0350	1.0330	1.0310	1.0300	1.0300	1.0310
1.0380	1.0340	1.0330	1.0310	1.0300	1.0300	1.0310
1.0380	1.0340	1.0330	1.0310	1.0300	1.0300	1.0310
1.0370	1.0340	1.0320	1.0310	1.0300	1.0300	1.0310
1.0370	1.0340	1.0320	1.0310	1.0300	1.0300	1.0310
1.0370	1.0340	1.0320	1.0310	1.0300	1.0300	1.0310
1.0370	1.0340	1.0320	1.0310	1.0300	1.0300	1.0310
1.0370	1.0340	1.0320	1.0310	1.0300	1.0300	1.0310
1.0370	1.0340	1.0320	1.0310	1.0300	1.0300	1.0310
1.0370	1.0340	1.0320	1.0310	1.0300	1.0300	1.0310
1.0370	1.0340	1.0320	1.0310	1.0300	1.0300	1.0310
1.0370	1.0340	1.0320	1.0310	1.0300	1.0300	1.0310
1.0370	1.0340	1.0320	1.0310	1.0300	1.0310	1.0310
1.0370	1.0340	1.0320	1.0310	1.0300	1.0310	1.0310
1.0370	1.0340	1.0320	1.0310	1.0300	1.0310	1.0310
1.0360	1.0340	1.0320	1.0310	1.0300	1.0310	1.0310
1.0360	1.0340	1.0320	1.0310	1.0300	1.0310	1.0310
1.0360	1.0340	1.0320	1.0310	1.0300	1.0310	1.0310
1.0360	1.0340	1.0320	1.0310	1.0300	1.0310	1.0310
1.0360	1.0340	1.0320	1.0310	1.0300	1.0310	1.0310
1.0360	1.0340	1.0320	1.0310	1.0300	1.0310	1.0320
1.0360	1.0340	1.0320	1.0310	1.0300	1.0310	1.0320
1.0360	1.0340	1.0320	1.0310	1.0300	1.0310	1.0320
1.0360	1.0330	1.0320	1.0310	1.0300	1.0310	1.0320
1.0360	1.0330	1.0320	1.0310	1.0300	1.0310	1.0320
1.0360	1.0330	1.0320	1.0310	1.0300	1.0310	1.0320

1.0320	1.0330	1.0360	1.0340	1.0320	1.0310	1.0300
1.0320	1.0330	1.0360	1.0340	1.0320	1.0310	1.0300
1.0320	1.0330	1.0360	1.0340	1.0320	1.0310	1.0300
1.0320	1.0340	1.0360	1.0340	1.0320	1.0310	1.0300
1.0320	1.0340	1.0360	1.0340	1.0320	1.0310	1.0300
1.0320	1.0340	1.0360	1.0340	1.0320	1.0310	1.0300
1.0320	1.0340	1.0360	1.0340	1.0320	1.0310	1.0300
1.0320	1.0340	1.0360	1.0340	1.0320	1.0310	1.0300
1.0320	1.0340	1.0360	1.0340	1.0320	1.0310	1.0300
1.0320	1.0340	1.0360	1.0340	1.0320	1.0310	1.0300
1.0320	1.0340	1.0360	1.0340	1.0320	1.0310	1.0300
1.0320	1.0340	1.0360	1.0340	1.0320	1.0310	1.0300
1.0320	1.0340	1.0360	1.0330	1.0320	1.0310	1.0300
1.0320	1.0340	1.0360	1.0330	1.0320	1.0310	1.0300
1.0320	1.0340	1.0360	1.0330	1.0320	1.0310	1.0300
1.0320	1.0340	1.0360	1.0330	1.0320	1.0310	1.0300
1.0320	1.0340	1.0360	1.0330	1.0320	1.0310	1.0300
1.0320	1.0340	1.0360	1.0330	1.0320	1.0310	1.0300
1.0320	1.0340	1.0360	1.0330	1.0320	1.0310	1.0300
1.0320	1.0340	1.0350	1.0330	1.0320	1.0310	1.0300
1.0320	1.0340	1.0350	1.0330	1.0320	1.0310	1.0300
1.0320	1.0340	1.0350	1.0330	1.0310	1.0310	1.0300
1.0320	1.0340	1.0350	1.0330	1.0310	1.0310	1.0300
1.0320	1.0340	1.0350	1.0330	1.0310	1.0310	1.0300
1.0320	1.0340	1.0350	1.0330	1.0310	1.0300	1.0300
1.0320	1.0340	1.0350	1.0330	1.0310	1.0300	1.0300
1.0320	1.0350	1.0350	1.0330	1.0310	1.0300	1.0300
1.0330	1.0350	1.0350	1.0330	1.0310	1.0300	1.0300
1.0330	1.0350	1.0350	1.0330	1.0310	1.0300	1.0300
1.0330	1.0350	1.0350	1.0330	1.0310	1.0300	1.0300
1.0330	1.0350	1.0350	1.0330	1.0310	1.0300	1.0300
1.0330	1.0350	1.0350	1.0330	1.0310	1.0300	1.0300
1.0330	1.0350	1.0350	1.0330	1.0310	1.0300	1.0300
1.0330	1.0350	1.0350	1.0330	1.0310	1.0300	1.0300
1.0330	1.0350	1.0350	1.0330	1.0310	1.0300	1.0310
1.0330	1.0350	1.0350	1.0330	1.0310	1.0300	1.0310
1.0330	1.0350	1.0350	1.0330	1.0310	1.0300	1.0310
1.0330	1.0350	1.0350	1.0330	1.0310	1.0300	1.0310
1.0330	1.0350	1.0350	1.0330	1.0310	1.0300	1.0310
1.0330	1.0350	1.0350	1.0330	1.0310	1.0300	1.0310
1.0330	1.0350	1.0350	1.0320	1.0310	1.0300	1.0310
1.0330	1.0350	1.0340	1.0320	1.0310	1.0300	1.0310
1.0330	1.0350	1.0340	1.0320	1.0310	1.0300	1.0310
1.0330	1.0350	1.0340	1.0320	1.0310	1.0300	1.0310
1.0330	1.0350	1.0340	1.0320	1.0310	1.0300	1.0310
1.0330	1.0350	1.0340	1.0320	1.0310	1.0300	1.0310
1.0330	1.0350	1.0340	1.0320	1.0310	1.0300	1.0310
1.0330	1.0350	1.0340	1.0320	1.0310	1.0300	1.0310
1.0330	1.0360	1.0340	1.0320	1.0310	1.0300	1.0310
1.0330	1.0360	1.0340	1.0320	1.0310	1.0300	1.0310
1.0330	1.0360	1.0340	1.0320	1.0310	1.0300	1.0310
1.0330	1.0360	1.0340	1.0320	1.0310	1.0300	1.0310

1.0310	1.0310	1.0320	1.0330	1.0340	1.0350	1.0370
1.0310	1.0310	1.0320	1.0330	1.0340	1.0350	1.0370
1.0310	1.0310	1.0320	1.0330	1.0340	1.0360	1.0370
1.0310	1.0310	1.0320	1.0330	1.0340	1.0360	1.0380
1.0310	1.0310	1.0320	1.0330	1.0340	1.0360	1.0380
1.0310	1.0310	1.0320	1.0330	1.0340	1.0360	1.0380
1.0310	1.0310	1.0320	1.0330	1.0340	1.0360	1.0380
1.0310	1.0310	1.0320	1.0330	1.0340	1.0360	1.0380
1.0310	1.0310	1.0320	1.0330	1.0340	1.0360	1.0380
1.0310	1.0310	1.0320	1.0330	1.0340	1.0360	1.0380
1.0310	1.0320	1.0320	1.0330	1.0340	1.0360	1.0380
1.0310	1.0320	1.0320	1.0330	1.0350	1.0360	1.0380
1.0310	1.0320	1.0320	1.0330	1.0350	1.0360	1.0380
1.0310	1.0320	1.0320	1.0330	1.0350	1.0360	1.0380
1.0310	1.0320	1.0320	1.0330	1.0350	1.0360	1.0390
1.0310	1.0320	1.0320	1.0330	1.0350	1.0360	1.0390
1.0310	1.0320	1.0330	1.0340	1.0350	1.0360	1.0390
1.0310	1.0320	1.0330	1.0340	1.0350	1.0370	1.0390
1.0310	1.0320	1.0330	1.0340	1.0350	1.0370	1.0390
1.0310	1.0320	1.0330	1.0340	1.0350	1.0370	1.0390
1.0310	1.0320	1.0330	1.0340	1.0350	1.0370	1.0390
1.0310	1.0320	1.0330	1.0340	1.0350	1.0370	1.0390
1.0310	1.0320	1.0330	1.0340	1.0350	1.0370	1.0390
1.0310	1.0320	1.0330	1.0340	1.0350	1.0370	1.0390
1.0310	1.0320	1.0330	1.0340	1.0350	1.0370	1.0400
1.0310	1.0320	1.0330	1.0340	1.0350	1.0370	
1.0310	1.0320	1.0330	1.0340	1.0350	1.0370	

C.3 Rawdata Regulator, Vout Measured (Vin = 1.85V – 1.85V)

Columns 1 through 12
1.0086 1.0046 1.0063 1.0051 1.0085 1.0055 1.0086 1.0080 1.0077 1.0061
1.0071 1.0059
Columns 13 through 24
1.0045 1.0071 1.0037 1.0075 1.0064 1.0067 1.0037 1.0031 1.0018 1.0045
1.0037 1.0050
Columns 25 through 36
1.0014 1.0000 1.0031 1.0040 1.0031 1.0015 1.0007 1.0006 1.0040 1.0049
1.0006 1.0008
Columns 37 through 48
1.0008 1.0024 1.0012 1.0020 1.0010 1.0029 1.0018 1.0022 1.0013 1.0014
0.9994 1.0009
Columns 49 through 60
0.9980 0.9998 1.0017 1.0003 0.9981 0.9986 0.9980 0.9991 1.0005 0.9988
0.9974 0.9986
Columns 61 through 72
0.9975 0.9962 1.0002 0.9974 0.9996 0.9952 0.9955 0.9967 0.9966 0.9976
0.9963 0.9958
Columns 73 through 84
0.9952 0.9973 0.9993 0.9939 0.9989 0.9979 0.9948 0.9953 0.9931 0.9981
0.9968 0.9949
Columns 85 through 96
0.9959 0.9950 0.9990 0.9961 0.9943 0.9944 0.9971 0.9962 0.9971 0.9959
0.9992 0.9975
Columns 97 through 108
0.9946 0.9976 0.9963 0.9959 0.9960 0.9969 0.9966 0.9981 0.9988 0.9971
0.9949 0.9966
Columns 109 through 120
0.9967 0.9962 0.9954 0.9963 0.9976 0.9951 0.9970 0.9977 0.9969 0.9958
0.9990 0.9979
Columns 121 through 132
0.9955 0.9983 0.9954 0.9976 0.9942 0.9969 0.9967 0.9989 0.9969 0.9953
0.9971 0.9955
Columns 133 through 144
0.9968 0.9965 0.9964 0.9980 0.9946 0.9954 0.9947 0.9966 0.9986 0.9969
0.9955 0.9967
Columns 145 through 156
0.9972 0.9972 0.9994 0.9985 0.9970 0.9988 0.9946 0.9962 1.0001 0.9974
0.9976 0.9994
Columns 157 through 168
0.9954 0.9969 0.9994 0.9963 0.9954 0.9940 0.9992 0.9973 0.9965 0.9957
0.9977 0.9977
Columns 169 through 180
0.9994 0.9971 1.0008 0.9959 0.9971 0.9990 0.9968 0.9960 0.9961 0.9967
0.9954 0.9962
Columns 181 through 192

```
  0.9983    0.9969    0.9973    0.9963    0.9957    0.9959    0.9952    0.9979    0.9984    0.9954
0.9966    0.9984
 Columns 193 through 204
  0.9965    0.9973    1.0009    0.9988    0.9995    0.9990    0.9964    0.9961    0.9977    0.9976
0.9980    0.9973
 Columns 205 through 216
  0.9982    0.9959    0.9976    0.9978    1.0000    0.9999    0.9990    1.0010    0.9983    0.9967
1.0004    0.9985
 Columns 217 through 228
  1.0010    1.0004    0.9993    0.9998    0.9993    0.9982    1.0021    0.9971    0.9985    1.0010
1.0007    1.0004
 Columns 229 through 240
  0.9986    1.0012    0.9983    1.0003    0.9997    0.9983    0.9977    1.0005    0.9998    0.9985
0.9967    0.9983
 Columns 241 through 252
  1.0004    0.9985    1.0002    1.0001    0.9988    0.9989    0.9986    1.0002    0.9988    0.9993
0.9993    0.9981
 Columns 253 through 264
  1.0006    0.9975    0.9968    0.9959    0.9967    0.9977    0.9964    0.9964    0.9996    0.9976
0.9994    1.0005
 Columns 265 through 276
  0.9957    0.9981    1.0005    1.0018    0.9983    0.9977    0.9999    0.9992    0.9994    1.0001
0.9973    0.9995
 Columns 277 through 288
  0.9988    0.9951    0.9980    0.9994    0.9978    0.9979    1.0012    1.0023    0.9971    0.9975
0.9975    0.9968
 Columns 289 through 300
  0.9969    0.9958    0.9978    0.9990    0.9974    0.9996    0.9968    0.9958    0.9972    0.9973
0.9980    0.9965
 Columns 301 through 312
  0.9985    0.9972    0.9966    0.9985    0.9950    0.9973    0.9978    0.9978    0.9959    0.9957
0.9958    0.9977

Columns 313 through 324
  0.9960    0.9953    0.9958    0.9975    0.9949    0.9997    1.0000    0.9976    0.9975    0.9958
0.9970    0.9992
 Columns 325 through 336
  0.9987    0.9966    0.9986    0.9967    0.9995    0.9975    0.9969    0.9983    0.9947    0.9976
0.9978    0.9962
 Columns 337 through 348
  1.0010    0.9988    0.9982    0.9966    0.9968    0.9978    1.0003    0.9961    0.9988    0.9996
0.9958    0.9986
 Columns 349 through 360
  0.9999    0.9970    0.9959    0.9967    0.9979    0.9977    0.9977    0.9987    0.9972    0.9985
1.0007    0.9968
 Columns 361 through 372
  1.0004    0.9983    0.9994    0.9984    0.9987    0.9975    0.9995    0.9985    0.9969    0.9980
0.9995    0.9988
 Columns 373 through 384
  0.9979    0.9963    0.9969    0.9973    0.9974    0.9977    0.9983    0.9967    0.9963    0.9977
0.9970    0.9989
 Columns 385 through 396
```

0.9990 0.9958 0.9969 0.9985 1.0004 0.9999 0.9993 1.0001 0.9992 1.0010
0.9983 1.0000

Columns 397 through 408

1.0004 0.9997 0.9989 0.9991 1.0002 1.0011 1.0031 1.0001 1.0009 1.0008
0.9986 0.9979

Columns 409 through 420

1.0009 0.9994 1.0001 0.9988 1.0007 1.0023 1.0025 0.9990 1.0008 1.0000
1.0023 0.9995

Columns 421 through 432

1.0003 1.0019 1.0020 1.0047 1.0049 1.0011 1.0036 1.0010 1.0026 1.0034
1.0031 1.0027

Columns 433 through 443

1.0019 1.0045 1.0041 1.0047 1.0042 1.0050 1.0070 1.0032 1.0059 1.0059
1.0080

C.4 Measurement - Noise

Regarding noise: Display-readings from the regulator on oscilloscope showed none or small signs to noise in a degree as the measured curve in Figure 5.17 in chapter 5. Therefore, some investigations were done. First, 1V is placed across a 1KΩ resistance inside a Faraday cage at 0^{o}C and measurement was done. From the thermal noise expression, this would give rise to a noise equal to

$$v_{noise} = \sqrt{4k_B TR} = \sqrt{4 \times 1.38 \times 10^{-23} J/K \times 273.15K \times 1k\Omega} = 3.88nV/\sqrt{Hz}$$

where k_B is Boltzmann's constant, T is absolute temperature and R is the resistance value if the voltage source were noise free. The same script was used as for the readings from the regulator.

This investigation showed noise in the same degree as the noise appearing on the regulator readings. Although stable output was shown on the oscilloscope, noise was picked up and stored trough the MatLab script. Different pause times were also experimented without significantly changes in the resulting curve.

Secondly, the output from the source was connected directly to the input of the oscilloscope outside the Faraday cage with short coax cables. The same script was used and the results investigated.

All these experiments showed no signs of noise on the oscilloscope. Also, the noise appeared in the same way and with the same amplitude in all three cases. From this, it seems the Agilent HP 54622 oscilloscope trough the GPIB bus and the script used is not fully stable, and with a stable input voltage, it delivers different readings with about the same amount of AVVIK as shown in the regulator readings.

From this I conclude not all of the noise can be written to one part of the system alone, but it is clear that the regulator itself is not as noisy as it appears on Figure 5.17 in chapter 5.

C.5 Rawdata from temperature measurements

Measured:

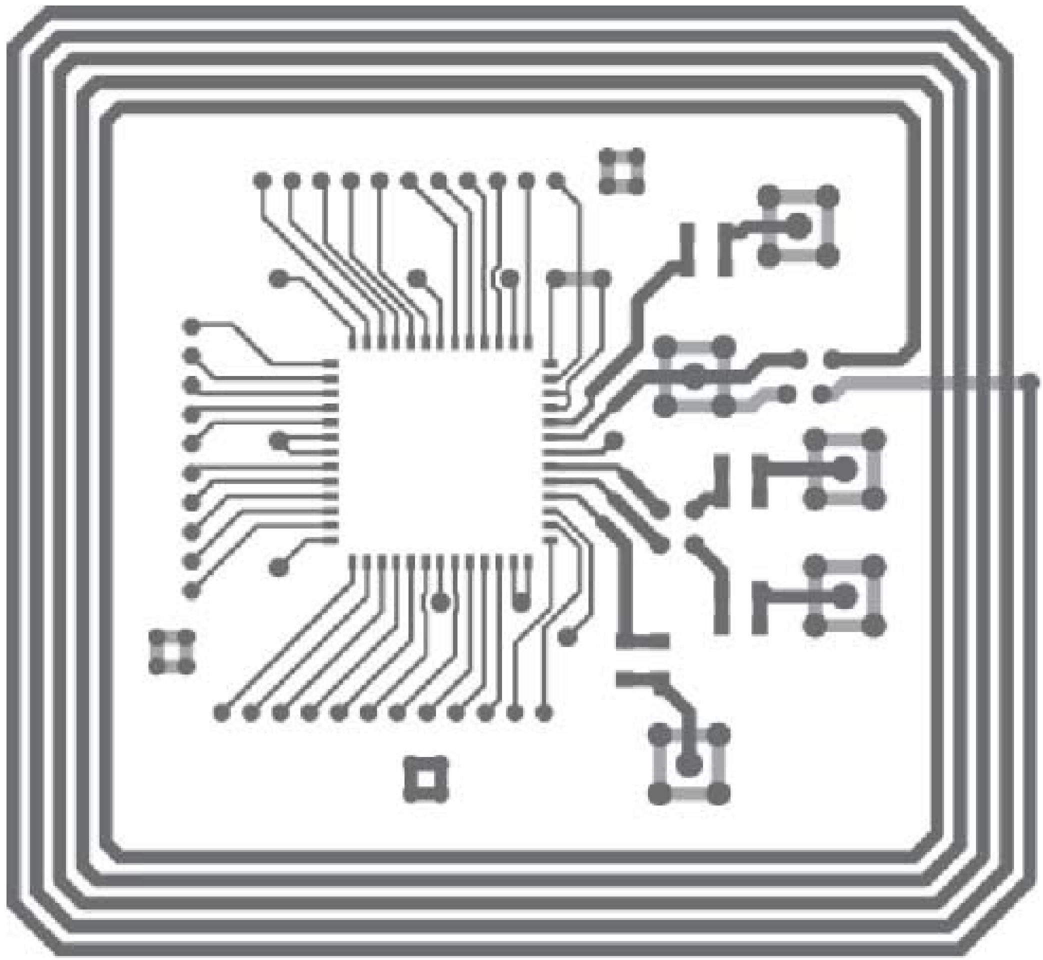
Temp	Output Voltage
2	1.1293
4	1.1269
6	1.1231
8	1.1179
10	1.1150
12	1.1112
14	1.1089
16	1.1033
18	1.1010
20	1.0955
22	1.0937
24	1.0897
26	1.0848
28	1.0772
30	1.0755
32	1.0680
34	1.0654
36	1.0631
38	1.0591
40	1.0531
42	1.0480
44	1.0458
46	1.0431
48	1.0380
50	1.0278
52	1.0211
54	1.0175
56	1.0142
58	1.0101
60	1.0093
62	1.0061
64	1.0042
66	0.9986
68	0.9962
70	0.9947

Simulated:

Temp	Output Voltage
-2.00000e-01	1.11085e+00
1.60000e+00	1.10732e+00
3.40000e+00	1.10378e+00
5.20000e+00	1.10024e+00
7.00000e+00	1.09669e+00
8.80000e+00	1.09315e+00
1.06000e+01	1.08959e+00
1.24000e+01	1.08604e+00
1.42000e+01	1.08248e+00
1.60000e+01	1.07892e+00
1.78000e+01	1.07536e+00
1.96000e+01	1.07179e+00
2.14000e+01	1.06822e+00
2.32000e+01	1.06464e+00
2.50000e+01	1.06106e+00
2.68000e+01	1.05748e+00
2.86000e+01	1.05389e+00
3.04000e+01	1.05030e+00
3.22000e+01	1.04671e+00
3.40000e+01	1.04311e+00
3.58000e+01	1.03950e+00
3.76000e+01	1.03590e+00
3.94000e+01	1.03228e+00
4.12000e+01	1.02867e+00
4.30000e+01	1.02505e+00
4.48000e+01	1.02142e+00
4.66000e+01	1.01779e+00
4.84000e+01	1.01416e+00
5.02000e+01	1.01052e+00
5.20000e+01	1.00688e+00
5.38000e+01	1.00323e+00
5.56000e+01	9.99579e01
5.74000e+01	9.95922e01
5.92000e+01	9.92260e01
6.10000e+01	9.88593e01
6.28000e+01	9.84921e01
6.46000e+01	9.81244e01
6.64000e+01	9.77562e01
6.82000e+01	9.73875e01
7.00000e+01	9.70183e01

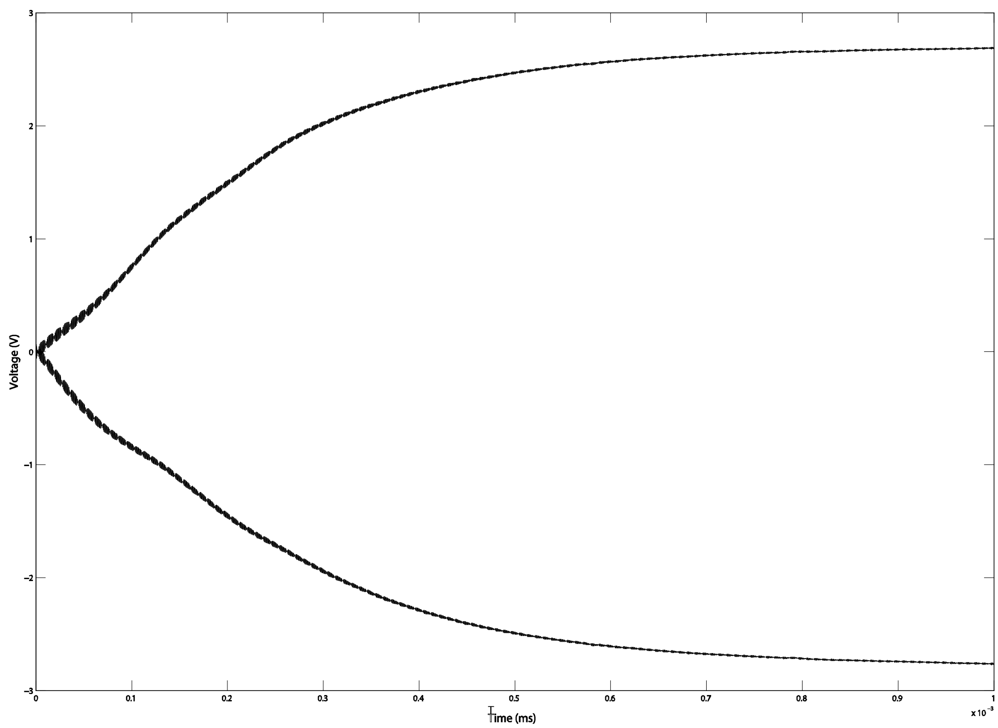
11 Appendix D

PCB-layout for chargepump testing:



The point where the ASIC docking is placed is the white square in the middle of the PCB. Different connectors to the ASIC are placed around depending on the circuitry it is connected to. In the outer ends of the board, a square inductor with 5 loops is placed. This is for first order testing of a large antenna. However, this PCB did not come in use.

12 Appendix E



The figure shows the output voltage from Chargepump Circuit two with a 1MΩ load. All other parameters are kept the same as before (basic setup). The total output voltage reaches 5.485V within 1ms from startup.