UNIVERSITY OF OSLO
Department of informatics

A 5-GHz RF Front-End for IEEE 802.11a and HiperLAN/2

Master (Siv.Ing.) thesis

Bartosz Uzieblo

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PREFACE

This thesis is submitted to the Department of Informatics at the University of Oslo in partial fulfillment of the Master of Science (siv.ing.) degree.

The thesis is done in cooperation with Chipcon AS (now Texas Instruments Norway).

I would like to take this opportunity to thank my supervisor, Tor A. Fjeldly at Department of Informatics and Øyvind Birkenes and Oddgeir Fikstvedt at Texas Instruments Norway for their skillful guidance, patience and support. I would also want to thank my family for their support and encouragement and my current employer for giving me possibility to finalize my studies.

Oslo, April 27, 2007
Bartosz Uzieblo

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CHAPTER 1

1.1 Introduction

Since 1997, when the new standard for wireless data communication emerged, it has been an explosive demand for wireless enabled products. Over time more and more devices get built-in wireless capabilities in connecting to internet or other devices. As well the amount of data to be transferred increases dramatically. The current marked situation for wireless enabled devices doesn't show any signs of slowing down. The strong and growing demand for high data rates/ better performance pushes forward new standards. One of the new promising standards for high speed networks is IEEE 802.11a from Institute of Electrical and Electronics Engineers Inc. (IEEE). This standard is designed to operate in the 5GHz radio band and can achieve transmission rate up to 54 Mbps.

This explosive development of wireless communication and its applications has created high demand for portable wireless devices that are smaller, lighter, and cheaper and of higher performance than ever. To be able to achieve those requirements new system architectures and circuit topologies need to be utilized. One of the factors that have been a driving force for new system architectures and circuit topologies has been development of integrated circuit (IC). Especially the development of CMOS, deep sub-micron technologies made possible higher level of integration and higher operating frequencies, resulting in improvements of performance, power consumption and cost. Higher frequency limits and improved performance of IC technologies also make it possible to transfer some of the signal processing that normally has been done in the analog domain to the digital domain.

1.2 Overview of the thesis

The main goal of this thesis is to give an overview of available techniques and to demonstrate its use in the design of a radio receiver front-end that covers the IEEE 802.11a and HiperLAN/2 RF requirements.

The thesis is divided in following parts:

- **Chapter 1** contains an introduction and an overview of this thesis.
- **Chapter 2** gives a general overview of different wireless communication standards and the differences between them.
- **Chapter 3** provides a short overview of RF building blocks and review of the different receiver architectures.
- **Chapter 4** provides an overview over selected articles. The different technical aspects presented in the articles are discussed.
- **Chapter 5** contains the base design, implementation and simulation results for the RF front end. The design trade-offs are discussed as well in this chapter.
- **Chapter 6** contains the conclusion for this thesis and further improvements are discussed.

CHAPTER 2

In this chapter I will present a short summary of the different short-range wireless communication standards and the differences between them. I will concentrate on the IEEE 802.11 and HiperLAN family of standards.

2.1 Wireless LAN: A short overview

In United States a decision by FCC (Federal Communication Commission) [1] in 1985 gave a start to a whole new industry, wireless data communication. FCC opened several radio bands for use without a government license. However those bands were already allocated to use by equipment such us microwaves ovens, cordless telephones, garage door openers, etc. Because of that, a special modulation technique was required to use those bands. That modulation technique is called spread spectrum technology. In this technology the signal is spread out over a wide range of frequencies, making the signal less susceptible to interference and more difficult to intercept. The advantage of the release of the 2.4 GHz band is that it is available worldwide. A disadvantage is that the frequencies in the 2.4GHz band tends to reflect off solid objects (walls/ buildings, etc.), causing delays/ disturbance in the delivery of data. The spread spectrum signal itself doesn't cause harmful interference, but it does accept any interference it receives. Bluetooth [2], microwave ovens, cordless telephones, ZigBee [3], HomeRF [4] and other 802.11b devices operate in this band, which increases the chance of interference. To deal with these problems, a second frequency band has been made available, 5GHz. The 5GHz band offers the advantages of higher data rates, far more available spectrum, less sharing with other users, and probably most important, an environment with much less noise and interferences from the existing devices. The band is also more or less globally available. Table 2.1 show an overview of different frequency bands in U.S., Europe and Asia.

Frequencies	**2.4 GHz band**	**5 GHz band**
U.S.	2.4 – 2.4835 GHz	5.15 – 5.35 GHz, 5.725 – 5.825 GHz
Europe	2.4 – 2.4835 GHz France: 2.4465 – 2.48835 GHz Spain: 2.445 – 2.475 GHz	5.15 – 5.35 GHz, 5.47 – 5.725 GHz
Japan	2.471 – 2.497 GHz	5.15 – 5.25 GHz

Table 2.1: Frequency allocations

Because of the lack of standard for wireless communication in this band, a committee by IEEE [5] was established in 1990. The committee was named 802.11. Several years later in 1997 a standard was established/ published, but already some pre-standard devices were available in the market. The first standard called 802.11 supported speeds up to only 2 Mbps and was based on modulation techniques called DSSS (Direct Sequence Spread Spectrum) [6] or FHSS (Frequency Hopping Spread Spectrum) [7]. The standard supported two entirely different modulation techniques, which led to incompatibility and confusion between various types of equipment. The standard suffered as well from poor handing of reflected signals. Over the next 2 years two new standards in addition to the 'original' standard 802.11 were developed, 802.11b and 802.11a, followed later by 802.11g. The 802.11b got increased range as well the speed from 2Mbps to 11Mbps. The DSSS was chosen as the preferred modulation techniques since it proved more reliable than FHSS.

The 802.11a was moved to the 5GHz frequency band from already overcrowded 2.4GHz band. The modulation was upgraded from DSSS to OFDM (Orthogonal Frequency Division Multiplexing) [8]. This modulation proved to give better performance in environments, where multipath propagation is a problem i.e. home and office environments. These made possible to achieve data rates of up 54 Mbps.

In 2003 802.11g was developed as an upgrade of already existing 802.11a using the 2.4GHz frequency band. But the modulation was changed to OFDM giving possibility for speed up to 54Mbps and to utilize OFDM modulation advantages.

In recent years a strong demand for higher data rates/ bigger range resulted in the development of the new standard 802.11n. The work on 802.11n is still in progress, but already some pre-standard devices are available. The new

802.11n is built on 802.11 by adding MIMO (Multiple-Input, Multiple-Output) [9] techniques. MIMO uses multiple transmitter and receiver antennas to allow for increased data throughput.

At the same time in Europe several research projects were started. The goal of those was to develop a common standard for wireless communication. That work lead to a standard named HiperLAN (HIgh PERformance LAN) [10][11][19][20]. The standard was released by a technical committee RES10 (Radio Equipment and Systems) of ETSI (European Telecommunications Standard Institute) [12] in 1996. HiperLAN provided features and capabilities to those of the IEEE 802.11 wireless local area network standards. It also provided data rates up to 20Mps in the 5GHz band. By early 2000 a new version of the HiperLAN was released. The new version is named HiperLAN/2 [11][19][20]. Unlike the HiperLAN, the HiperLAN/2 was specifically developed to mainly have a wired infrastructure providing a short range wireless access to IP, ATM and UMTS networks. For HiperLan/2 the data rate was increased to 54Mbps. The HiperLAN family of standards merely describes a common air interface and the physical layer for wireless communications equipment, thus ensuring compatible systems while leaving implementation of higher level function up to each manufacturer. The main advantages over the IEEE standard family are improved quality of service, increased throughput and less interference.

In Japan a third system for use in 5GHz was developed by Japanese counterpart of ETSI and IEEE, ARIB MMAC (Multimedia Mobile Access Communications group within the Association of Radio Industries and Broadcasting) [13]. The standard is named HiSWAN (High Speed Wireless Access Network) [14] and supports data rates up to 54 Mbps. I will not go into the details for this standard in this work.

A close cooperation between IEEE 802.11, ETSI and ARIB MMAC has ensured that the physical (PHY) layers of the various 5GHz wireless LAN standards are broadly harmonized [15][16]. This makes possible the low-cost production of devices that conforms to requirements for all three standards.

Table 2.2 shows a compilation of technical aspects of the various standards.

The further development of the wireless standards looks into new ways of transmitting data with even higher throughput and performance that those already available. One of the new techniques that has generated a considerable interest in wireless community is UWB (Ultra Wide-Band) transmission [17], [21]. UWB has its origin within military radar applications and has proved to provide good performance in multi-path environments such as inside buildings.

The recent development of IC and silicon technology has now made possible to built practical communications systems based on that technique. UWB transmitter works by sending billions of pulses across a very wide spectrum of frequency, several GHz in bandwidth. The corresponding receiver then translates the pulses into data by listening for a familiar pulse sequence sent by the transmitter. UWB's combination of larger spectrum, lower power and pulsed data improves speed and reduces interference with other wireless spectra. Pulse position modulation is employed with a low power, but a high processing gain, so that the data is recovered even in presence of high power levels from other services in one part of the spectrum. Because of the nature of a UWB signal the technology is not worldwide available as it still has an issue with current regulations around the world. In 2002 the FCC in the United States approved that UWB radio transmissions can legally operate in the range from 3.1 GHz up to 10.6 GHz, at a limited transmit power of –41dBm/MHz. However two competing standards make the situation still complicated. The UWB Forum [17] is promoting one standard based on DS-UWB (Direct Sequence-UWB) and the WiMedia Alliance [18] is promoting another standard based on OFDM. Both of the competing standards provide substantial increase in short-range channel capacity and limited interference. Because of the power limitation the UWB technology has a potential to be used in data links for high data rate wireless PAN (Private Area Network) connectivity (in excess of 100 Mbps) at ranges up to 10 m, particularly for in-home networking applications.

WLAN standard	***Released***	***Freq. band***	***Data rate***	***Typical Range***	***Modulation***
IEEE 802.11	1997	2,4 GHz	up to 2 Mbps	50-100m	DSSS, FHSS, IR
IEEE 802.11b	1999	2,4 GHz	up to 11 Mbps	50-100m	DSSS/ CCK
IEEE 802.11a	1999	5 GHz	up to 54 Mbps	50-100m	OFDM
IEEE 802.11g	2003	2,4 GHz	up to 54 Mbps	50-100m	OFDM/ PBCC
IEEE 802.11n	late 2006	5 GHz	200 Mbps+	up to 250m	OFDM
HiperLAN	1996	5 GHz	up to 23.5 Mbps	50m	GMSK
HiperLAN/2	2000	5 GHz	up to 54 Mbps	indoor 50m, outdoor 100m	OFDM
HiSWAN	1999	5 GHz	up to 27 Mbps	100-150m	OFDM

Where: DSSS = Direct Sequence Spread Spectrum, FHSS = Frequency Hopping Spread Spectrum, IR = Infrared, CCK = Complementary Code Keying, OFDM = Orthogonal Frequency Division Multiplexing, PBCC = Packet Binary Convolution Code, GMSK = Gaussian Minimum Shift Keying.

Table 2.2: Technical aspects of the various WLAN standards

2.2 References

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[2] Bluetooth, http://www.bluetooth.com

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[5] IEEE, http://www.ieee.org

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[10] HiperLAN, http://en.wikipedia.org/wiki/HIPERLAN

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CHAPTER 3

The basic function of a radio front-end is to take the weak modulated carrier signal from the antenna, apply amplification, perform down-conversion of the signal, select the wanted channel and finally extract the baseband information. There are several building blocks a receiver front-end can be based on. The main blocks are: low noise amplifier (LNA), mixer and an oscillator (not covered in this document). Each of them has specific function and requirements. This chapter gives a short overview of each of the building blocks and radio receiver architectures. More detailed information can be found in [1 - 11].

3.1 Building blocks

3.1.1 Low-Noise Amplifier (LNA)

Low-Noise Amplifier (LNA) is the corner stone in all RF front-end receiver architectures. The main function of the LNA is to amplify the very weak RF signal with minimum addition of noise and distortion. Design consideration such as gain, noise, input match and linearity must be taken into account when designing the LNA. For many applications the power consumption and die area need also to be taken into consideration.

The LNA should have a lowest possible noise figure (NF), since the weak RF signal coming from antenna is first amplified by the LNA and any noise

contribution from LNA is directly added to the system. According to the Friis formula (3.1) [12]:

$$F_{TOT} = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + ... + \frac{F_N - 1}{G_1 G_2 .... G_{N-1}} \qquad (3.1)$$

The total noise factor is the sum of contribution from all stages, where the noise factor of stage N is divided by the total gain from input to stage N. In case of radio receiver where the first stage is a LNA the formula (3.1) can be rewritten to (3.2), where F_{REST} is the noise figure of the subsequent stages.

$$F_{TOT} = F_{LNA} + \frac{F_{REST} - 1}{G_{LNA}} \qquad (3.2)$$

We can see from the formula (3.2) that if the gain is sufficient high the overall noise figure is dominated by the noise figure of the first stage, normally a LNA.

LNA should have a well defined input characteristic, so that the energy of the received signal is totally absorbed and not reflected back causing an ineffective reception. In most designs there is a passive filter between antenna and LNA. The performances of those filters are heavily depended on the correct termination [1]. In the case where the LNA is followed by a passive filter the LNA's output characteristic should also be well defined and adapt according to the filter characteristic.

Another vital parameter of the LNA is linearity. Although the main function of the LNA is providing maximum amplification without adding much noise, the LNA must remain linear, independent of the signal strength received. The linearity of the LNA plays a most important role in the case when receiving a weak signal in presence of a strong interfering one because the nonlinearities then will result in intermodulation distortion, desensitization (blocking) and cross-modulation [1]. The most common used measures for linearity are 1-dB compression point (P1dB) and third-order intercept point (IP3). Figure 3.1 and 3.2 show P1dB and IP3 graphic definition respectively.

1-dB compression point represents the point where the linear magnitude response of the LNA have has been reduced by 1 dB due to nonlinearities. 1-dB compression point is also a measure of the maximum signal input range of the circuit.

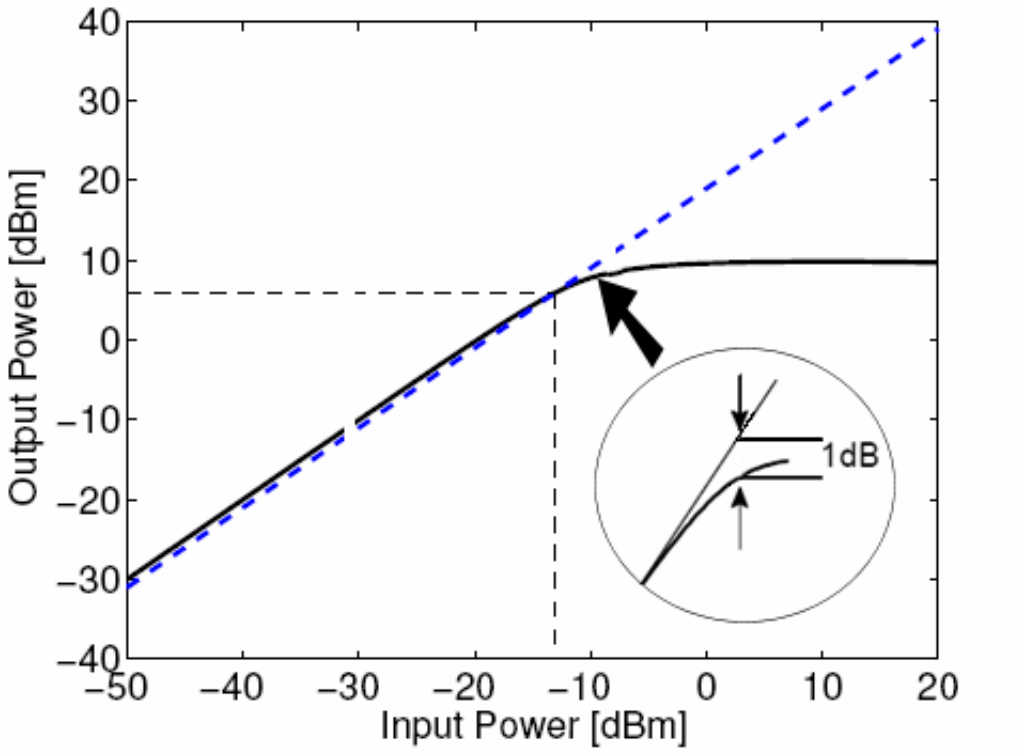

Figure 3.1: 1-dB compression point

Third-order intercept point is the measure of intermodulation products and indicates how well the receiver performs in the presence of strong interferers. The IP3 is important as third-order nonlinearity products tend to fall within wanted frequency band and interfere with the wanted signal. However in the direct-conversion receivers the second-order intermodulation products are equally important as third-order nonlinearities. The IP3 is often referred into as IIP3 (input-referred IP3) and OIP3 (output-referred IP3).

There is no fixed relationship between measures of P1dB and IP3 as they characterize linearity in two distinctive regimes [1]. However the IP3 or P1dB can be easily estimate by using following approximation [13]:

$$IIP\ 3 - P1dB = 9.6\,dB \qquad (3.3)$$

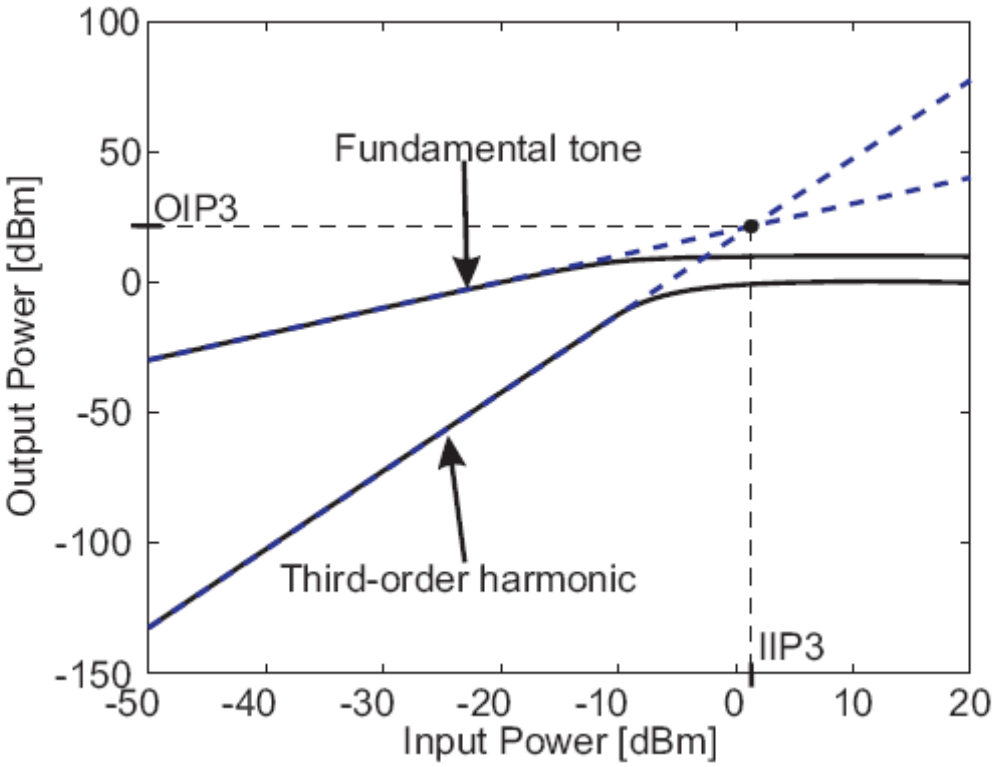

Figure 3.2: Third-order intercept point (IIP3 and OIP3)

3.1.2 Mixer

Mixer is used for frequency conversion and is a crucial circuit in the RF system. The main reason for using mixers and frequency conversion is that the signal processing can be then done in much lower frequency domain than RF, thus reducing complexity and cost of the circuits. An ideal mixer, shown in figure 3.3 is a device that multiplies to input signals, in this case f_1 which is incoming RF signal, f_2 which are the local oscillator signal LO and IF which is the complex output.

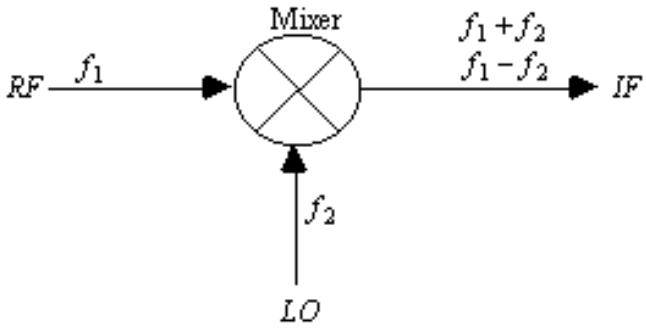

Figure 3.3: Schematic symbol of a mixer

If both signals are sinusoids the ideal mixer output will be the sum and difference frequencies given by formula 3.3 [1].

$$(A\cos\omega_1 t)(B\cos\omega_2 t) = \frac{AB}{2}\left[\cos(\omega_1 - \omega_2)t + \cos(\omega_1 + \omega_2)t\right] \quad (3.4)$$

$$\omega_1 = 2\pi f_1$$

$$\omega_2 = 2\pi f_2 \quad (3.5)$$

The amplitudes of the signals at the output are proportional to the product of RF and LO amplitudes.

However since the mixer is not ideal other spurious tones due to even and odd harmonics will be to find in the resulting frequency spectrum. A schematic plot of the spectrum of non-ideal mixer is shown in figure 3.4.

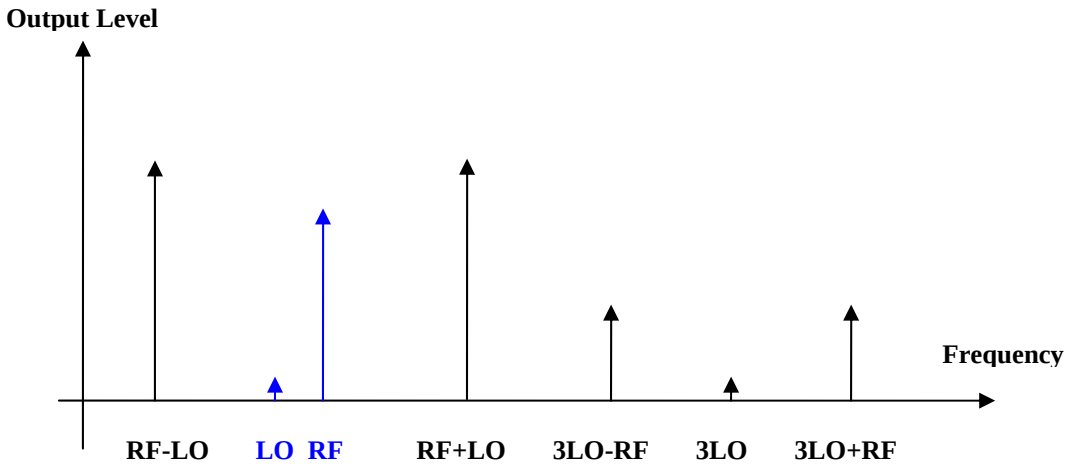

Figure 3.4: Schematic output frequency spectrum for a non-ideal mixer

The performance of the mixer is normally presented by conversion gain (conversion loss for passive mixers), noise figure and linearity. Conversion gain/ loss is defined as the ratio of amplitude of the IF signal to the amplitude of the RF signal. Noise figure tells us how much noise the mixer adds to the output signal. Linearity can be estimated on the basis of 1-dB compression point (P1dB) and third-order intercept point (IP3). Figure 3.1 and 3.2 show P1dB and IP3 graphic definition respectively.

If we summarized the performance requirements for a mixer, we can say that a good mixer requires: low conversion loss or high gain, a low noise figure, low VSWR [12, 17] (Voltage Standing Wave Ratio) for the RF, IF and LO ports,

good isolation between any two of the RF, IF and LO ports, good dynamic range, a high 1-dB compression point and low intermodulation [8].

Mixers can be categorized according to functionality, power consumption and topology. According to the functionality mixers can be classified into two groups: up converting and down converting mixers. In down converting mixers the output is difference between LO and RF, also called IF (Intermediate Frequency). The process can be described by following numerical expression:

$$f_{IF} = f_{RF} - f_{LO} \qquad (3.6)$$

As distinct from down converting mixers, in up converting mixers the output is a sum of IF and LO, ref. equation 3.7.

$$f_{RF} = f_{IF} + f_{LO} \qquad (3.7)$$

Mixers can be categorized according to power consumption as active and passive mixers. The passive mixers are also known as switching mixers. Passive mixers as the name indicates doesn't consume any DC power and their conversion gain is always less than 1 compared to active mixers who have conversion gain usually larger than 1. However, the passive mixers have better distortion performance than the active mixers. The non-existing DC current in passive mixers implies the absence of 1/f noise [1]. This property is particularly valuable in direct conversion receiver architectures.

Mixers are also classified according to topology. Most common are: unbalanced, single balanced and double balanced mixers.

Unbalanced mixers are the simplest kind of mixers. However because of the simplicity of unbalanced mixer it has the lowest noise figure [14]. Figure 3.5 shows a single transistor unbalanced mixer.

The unbalanced mixers have very poor port to port isolation due to their structure. Because of the poor isolation a fraction of the RF signal will appear at the IF port and also a fraction of the LO signal will appear both at IF and RF port. This phenomenon is undesirable and need to be taken care by additional filters.

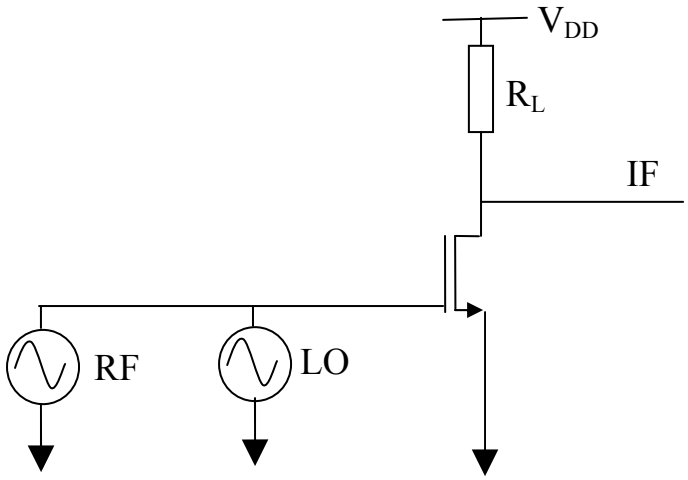

Figure 3.5: Unbalanced mixer

An improved design of the unbalanced mixer is single balanced topology show in figure 3.6.

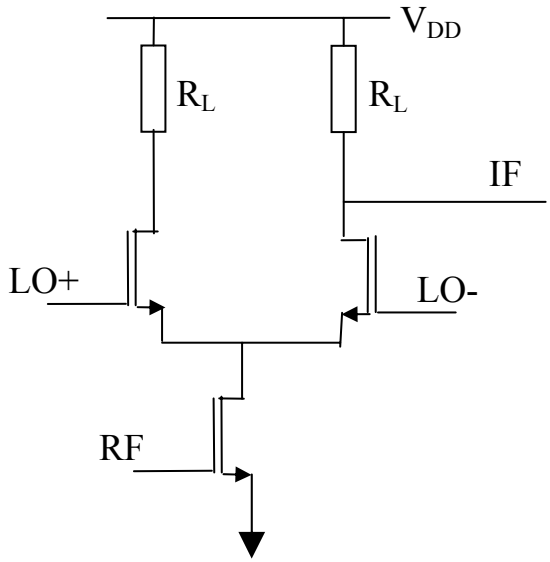

Figure 3.6: Single balanced mixer

Since the IF signal is taken out differentially the undesirable RF feedthrough is cancelled [1]. However the undesirable LO feedthrough still exists.

A third type of mixers is the double balanced, show in figure 3.7. The double balanced mixer is also called the Gilbert mixer or quad mixer and it is the most commonly used topology. The main advantage over the unbalanced and single balanced topologies are that it rejects both RF and IF frequency components at

the output. However because of more noise contributor devices it has highest noise figure [14].

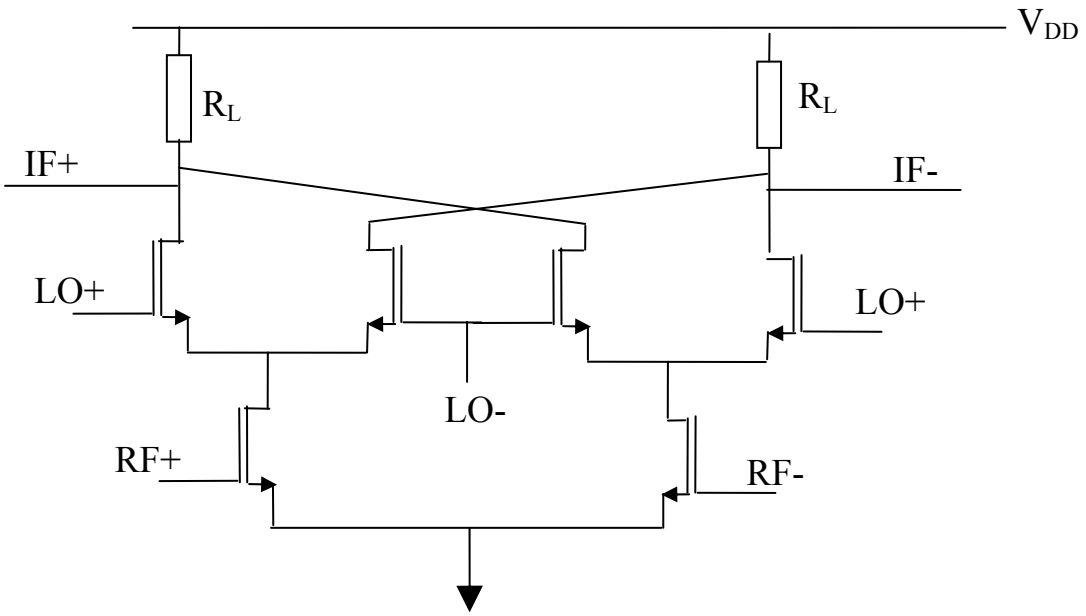

Figure 3.7: Double balanced mixer

3.2 Receiver architectures

As the main part of a WLAN front-end implementation consists of a radio receiver we need to be able to understand different topologies that can be used in its implementation and trade-offs. The function of the receiver is to successfully demodulate a desired signal in the presence of strong interference and noise. The receiver must be able to process the desired channel while sufficiently rejecting strong neighboring channels.

3.2.1 Radio receiver performance measure

To be able to understand the design choices made in RF receiver system, some standard parameters must be utilized to evaluate the performance of the receiver. The performance of the receiver depends on the system design, circuit design and working environment [8]. The key parameters are sensitivity, selectivity, dynamic range, blocker immunity and power consumption.

Sensitivity

Sensitivity is a receiver's ability to receive and demodulate weak signals. Sensitivity is defined as the minimum "available" signal power at the input terminal of the receiver such that there is an adequate signal-to-noise ratio (SNR) at the output of the receiver.

"Available" signal power means the signal power at the input or output terminal of a block under matched impedance conditions.

For a system in the digital domain such as WLAN with a digital modulation schema, the specified SNR is corresponding to the minimum bit error rate (BER).

Another used measure of sensitivity is the MDS (Minimum Detectable Signal).

Selectivity

Selectivity is defined as the ability of a receiver to satisfactorily extract the desired signal in the presence of strong adjacent frequency interference.

Dynamic range

The dynamic range defines the receiver's ability to detect a weak signal above the noise floor and process the strong signal with no distortion. The ratio of the maximum signal to minimum signal at the receiver's input defines its dynamic range.

Blocker immunity

Interfering RF signals together with receiver nonlinearities can generate intermodulation products that fall into frequency spectrum of the channel of interest. The receiver linearity is usually specified through the IP3 and 1-dB compression point.

Power consumption

The growing popularity of portable wireless devices demands radio transceivers with low power consumption. The optimization of the power consumption of a portable transceiver requires close collaboration between network architecture and transceiver design in order to realize the best performance [15]. However design trade-offs need to be made to achieve best performance.

3.2.2 Receiver topologies

There are several receiver architectures developed, each having advantages and drawbacks. The most common topologies are super-heterodyne, homodyne and various-IF configuration. These have different advantages/ disadvantages that need to be taken into consideration when designing a circuit.

Super-Heterodyne architectures

The super-heterodyne architecture was invented by Edwin H. Armstrong in 1918 and was and still is viewed as the most reliable receiver topology since excellent sensitivity and selectivity can be achieved by proper choice of IF and filters. In the super-heterodyne receiver the RF signal is down-convert to baseband in at least a two-step process. Figure 3.8 shows a simplified block diagram of a super-heterodyne receiver. The incoming RF signal is first processed trough a band-pass filter (BPF1) that selects the desired frequency channel. The filter is centered at the RF carrier frequency. This filter is also called band select filter. Then the selected frequency channel is amplified in a low-noise amplifier (LNA). The output from the LNA is then again filtered in a band-pass filter (BPF2) to remove the image, which has an offset of twice the intermediate frequency from the desired channel signal. This filter is also called the image rejection filter. Later the RF signal is translated by a mixer to a lower frequency, know as the intermediate frequency (IF). The process is also called down-conversion. Mixers are commonly used to multiply signals of different frequencies in an effort to achieve frequency translation, here the RF signal and a local oscillator (LO1) is mixed together. The IF signal is next filtered by a band pass filter (BPF3) centered at the IF frequency. This filters out all bands except the one of interest, and is typically called the channel filter. The filtered signal is then again amplified and mixed together with a local oscillator (LO2) centered at IF frequency. The signal coming out from the output is now at baseband.

Advantages of the heterodyne architectures are:

- Excellent performance with respect to selectivity and sensitivity
- Reduced baseband filtering needs

Disadvantages of the heterodyne architectures are:

- It can’t be fully integrated
- It requires expensive off-chip components

- It is a hard-wired implementation that is fixed for a single radio standard
- The off-chip components require design trade-offs that increase power consumption and reduce system gain
- Image rejection is limited by the off-chip components
- The LNA must drive a 50 Ω load because the image-reject filter is placed off-chip.

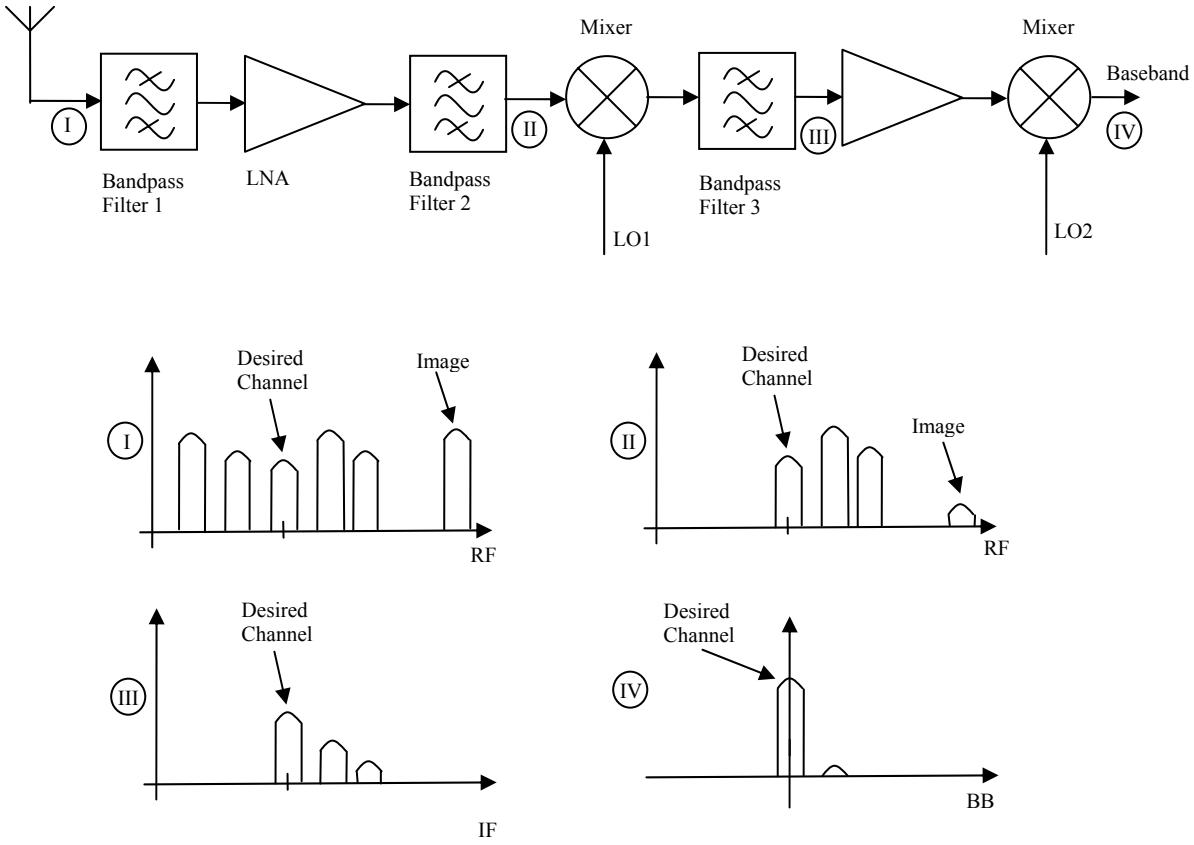

Figure 3.8: Super-heterodyne receiver

Homodyne architectures

The homodyne architecture was first described in 1924 by F.M. Colebrook in his attempt to improve on the Armstrong's super-heterodyne receiver. This architecture also known as "direct-conversion" or "zero-IF" performs the RF to base-band down-conversion in a single step. Figure 3.9 shows a simplified block diagram of a homodyne/ direct-conversion receiver. The incoming RF signal is first processed trough a band-pass filter that selects the desired frequency channel. The filter is centered at the RF carrier frequency. Then the selected frequency channel is amplified in a low-noise amplifier (LNA). Then the RF signal is mixed with a local oscillator (LO). The LO is tuned into the

incoming carrier frequency. The RF signal is down-converted to the base-band. Next the baseband signal is filtered using a low pass filter. Finally the signals then can be processed to the required format.

In a homodyne receiver, all the channels are down-converted to zero-IF before any channel filtering is performed. This allows the possibility of on-chip programmable filter structures to accommodate the variable channel bandwidth.

This makes it possible to use homodyne receivers in multi-mode or/ and standard radio receiver systems.

Advantages of the homodyne architectures are:

- Higher level of integration compared to super-heterodyne architecture.
- No needs for image rejection filter, less off-chip components.
- Less number of off-chip components compared to heterodyne architecture.
- The LNA doesn't need to drive a 50Ω load because no image rejection filter is required.
- Easily adaptable channel bandwidth. Multi-mode and standard operation possible.

Disadvantages of the homodyne/ direct-conversion topology are:

- As the local oscillator (LO) is at the same frequency at RF carrier, the possibility of LO leakage to mixer input or to the antenna exists. Then the leaked signal can be down-converted to base-band and creates a DC offset.
- The conversion process creates "noise" near the base-band, called 1/f, which can corrupt the RF signal.
- Second order distortion error can also occur, where any large unwanted RF signals or other signals can corrupt the desired radio signal.
- Phase and gain mismatch introduced by the mixers can be a problem, as it is not possible to achieve even phase and gain trough both mixers.
- Requires a high frequency, low phase-noise, channel-select frequency synthesizer.

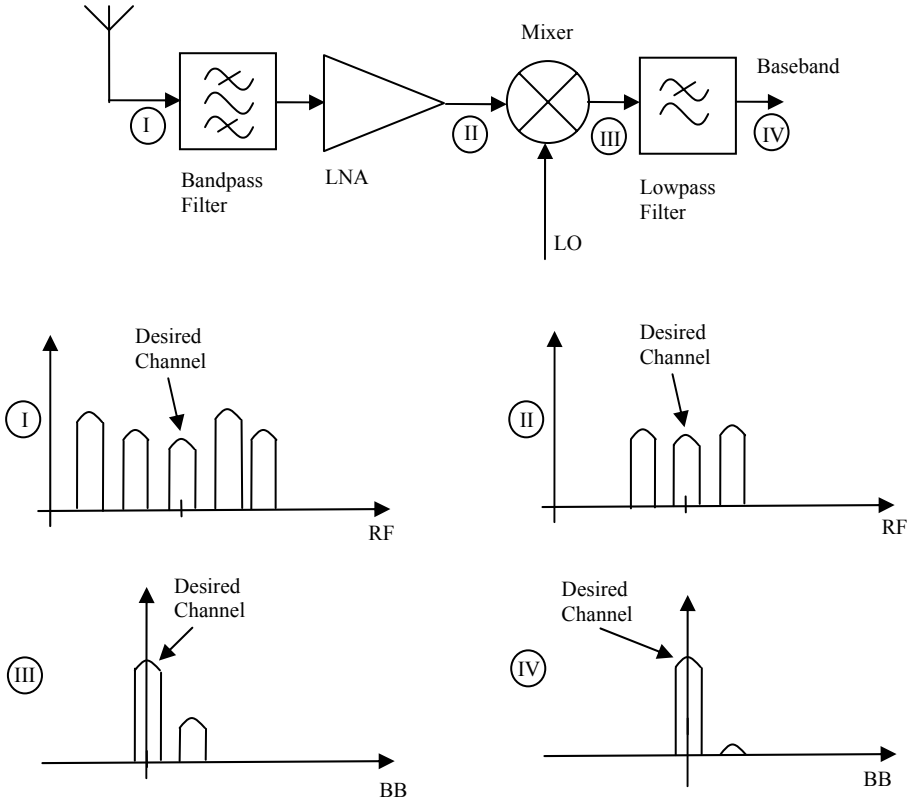

Figure 3.9: Homodyne/ direct-conversion receiver

Low-IF architectures

The low-IF architecture is similar to the direct conversion architecture, where a single mixer stage is used to frequency translate all of the desire channels to a zero intermediate frequency (IF). In low-IF receiver the down-conversion is done to a low-IF instead a zero-IF. Typically the low-IF is in range of one or two channel bandwidths. In that way we avoid the problem with DC offset that normally plague the direct-conversions receivers. Figure 3.10 shows a simplified block diagram of a low-IF receiver.

Advantages of the low-IF architectures are:

- DC offset and LO leakage is no longer a problem compared to direct-conversion architecture.
- Higher level of integration compared to super-heterodyne architecture.

Disadvantages of the low-IF architectures are:

- Requires that some variant of image-rejection must be done. Can be accomplished by using an image-rejection mixer in signal path. Thus more components and higher power consumption are introduced.

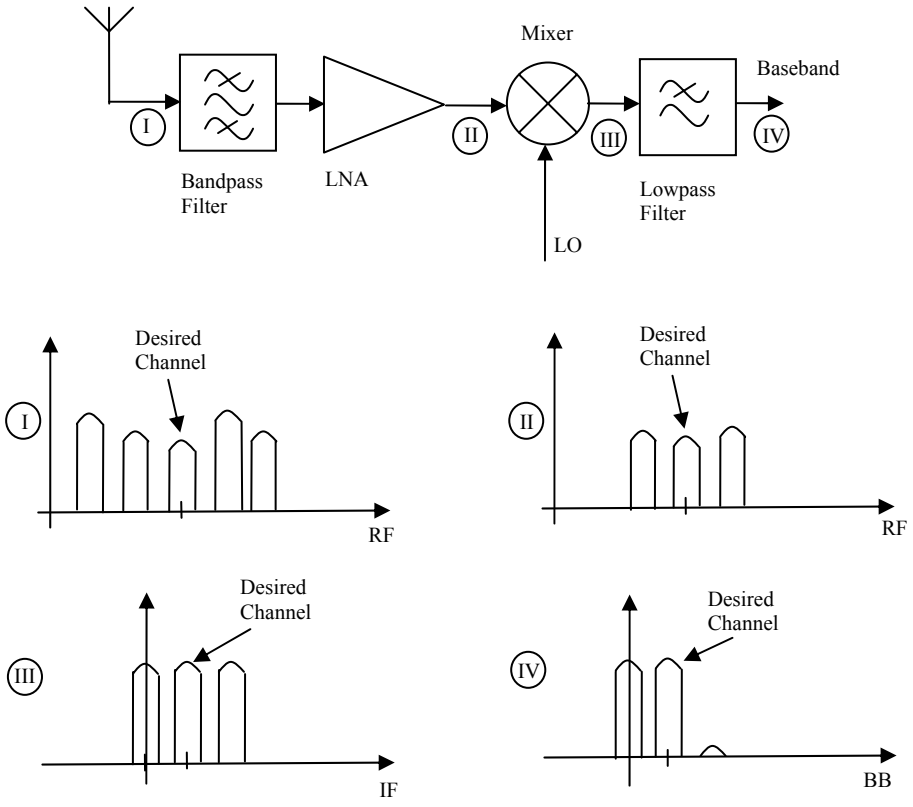

Figure 3.10: Low-IF receiver

Wide-band double-IF architectures

This architecture was presented by a group of researchers from UC Berkley. It combines the zero-IF and heterodyne architecture. This architecture is well suited for integration as it requires a minimum of off-chip components and the filtering can be made on-chip. Figure 3.11 shows a simplified block diagram of a wide-band double-IF receiver. The incoming RF signal is down-converted first to high intermediate frequency (IF) using a mixer with fixed frequency (LO1). A low-pass filter is then use for filtering the IF signal for up-converted frequencies. The filter will allow the desire channel to pass to second mixer stage. The second mixer has an adjustable local frequency (LO2) and it performs the down-conversion from the first IF to zero-IF (DC). The channel selection is done in the second mixer.

Advantages of the wide-band double-IF architectures are:

- Well suited for integration of the entire receiver.
- No local oscillator (LO) operating at the same frequency as incoming RF carrier frequency.
- Simplifies the design of the frequency synthesizer, as the highest frequency (LO1) is a fixed frequency and the tuning frequency (LO2) can be a lower frequency.
- Channel filtering can be done at baseband, enabling multi-standard capabilities.

Disadvantages of the wide-band double-IF architectures are:

- Image-rejection is realized by use of mixers. Thus more components/ higher power consumption.
- It can suffer from signal cross talk between IF and RF.

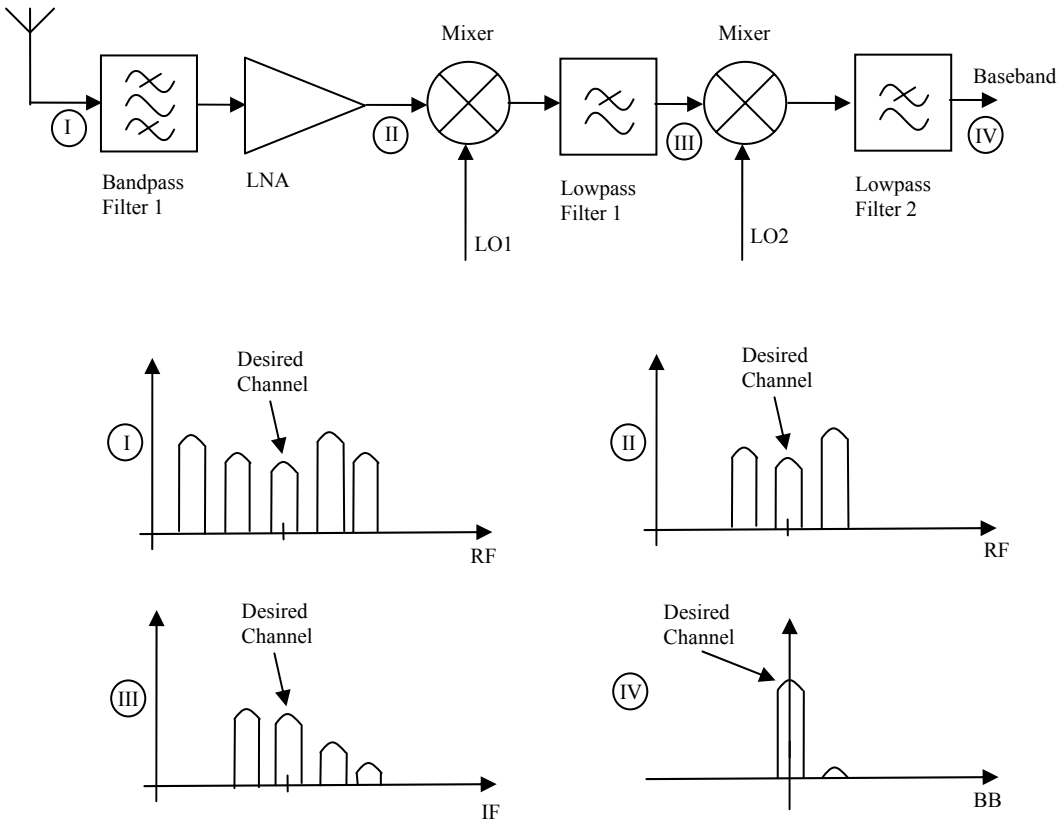

Figure 3.11: Wide-band, double-IF receiver

Other architectures

The radio receiver architectures and circuit topologies are under continued development; however the main principles of operation remain. As the CMOS technology evolves and the availability of high-speed CMOS processes increases, some of the analog IF processing has been moved over to the digital domain. An example of those architectures is the sub-sampling [3] and digital-IF architecture [3].

The sub-sampling architecture is based on the zero-IF topology, where the mixers have been replace by a sampling circuit. The RF signal is sampled at the Nyquist rate [16] of the baseband signal. It results in a spectral image that first is filtered and then converted by ADC (Analog to Digital Converter). The architecture is well suited for integration, because the complex down-conversion process is reduced to a simple sampling operation. Unfortunately the architecture still suffers from some drawbacks that make it unsuitable for higher frequency use. Figure 3.12 shows a simplified diagram of a sub-sampling receiver.

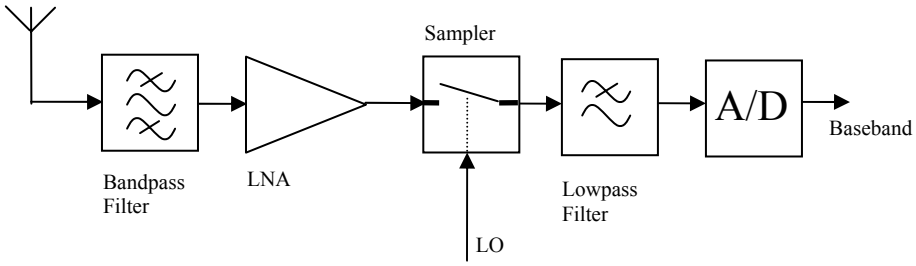

Figure 3.12: Sub-sampling receiver [3]

Another promising topology is the digital-IF architecture. In digital-IF architecture the final mixing and filtering is done in the digital domain, utilizing the fact that low-frequency operation such as the second set of mixing and filtering can be performed more efficiently in the digital domain. However the architecture requires use of high performance ADC, thus increasing the overall power consumption. The future development of this architecture depends on the development of fast, low-power and accurate ADC. Figure 3.13 shows a simplified diagram of a digital-IF receiver.

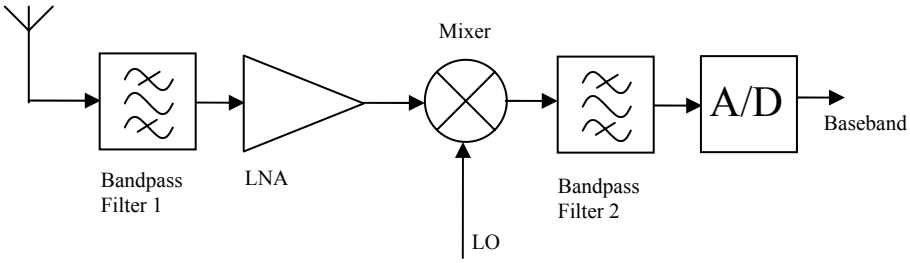

Figure 3.13: Digital-IF receiver [3]

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CHAPTER 4

4.1 Circuits, classic single band receivers

There are a number of papers published, which deal with the subject of a CMOS transceiver operating in 5GHz band and complying with both IEEE 802.11a and its European counterpart, the HiperLAN/2 standard. Both standards, even though they have a different media access control (MAC) layer approach, they share some similar requirements for theirs physical layer (PHY) [1]. This makes it possible to design transceivers that cover both standards. Physical layer standards describe the requirements for the protocol at the air interface. The protocol needs to be very resilient to cope with high level of interference, which will occur from other WLAN systems and other users of the band. The PHY standard specifies also the lowest signal level that the receiver must be able do receive and the highest level at which a transmitter can transmit.

4.1.1 A 5 GHz CMOS transceiver for IEEE 802.11a wireless LAN system

In ref. [2] the authors present an implementation of a transceiver that covers the IEEE 802.11a standard requirements. The design has been implemented as a two-chip solution in a standard 0.25μm CMOS technology where the first chip consist of an RF receiver, a frequency synthesizer and an RF transmitter. The other chip consists of an integrated base band and a MAC processor. The

transmitter, the frequency synthesizer and the second chip, will not be covered here. Fig 4.1 shows the system architecture for the proposed design.

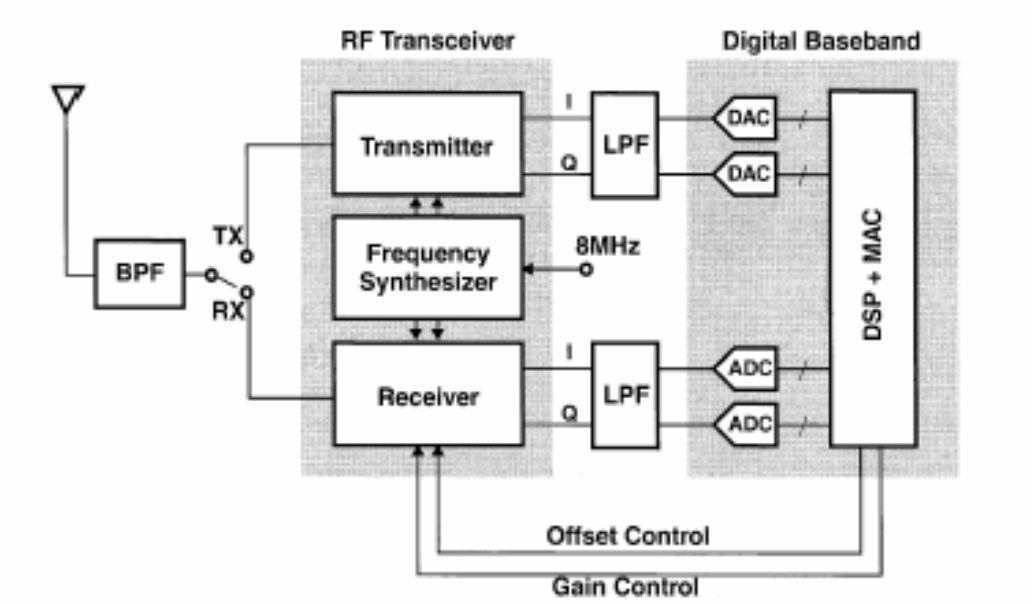

Figure 4.1: A 5-GHz CMOS transceiver for IEEE 802.11a wireless LAN system [2]

The authors have chosen dual conversion architecture for their receiver, with an intermediate frequency (IF) at 1 GHz. The local oscillator (LO) frequency has been chose to 4GHz in the first stage and 1 GHz in second. Figure 4.2 shows a simplified block diagram of the receiver part of the design.

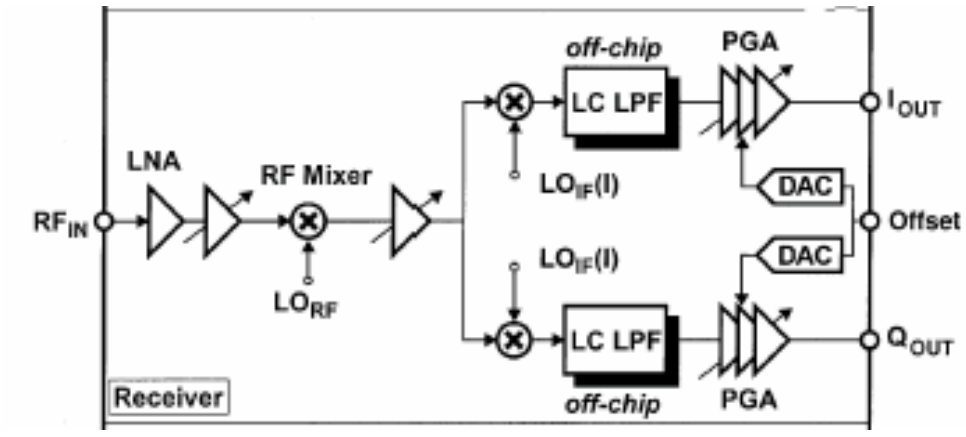

Figure 4.2: Simplified block diagram of the receiver [2]

The incoming RF signal is first mixed down to 1 GHz and then down converted to the base band. During down conversion several unwanted signals are created and need to be filtered away. During down mixing from 5GHz to 1 GHz an

image signal located at 3GHz is created and a spurious signal at 9GHz. The choice of a 1 GHz IF provides a 2GHz frequency separation between the incoming RF signal and the image. The image signal is taken care by a narrow-band on-chip tuning elements used in the RF and IF amplification stages. The image signal is suppressed by -23dBc. The high frequency spurious signal is attenuated by the inherent bandwidth limitation of the circuit. Using this technique and by correct frequency planning the authors avoid using any external IF filtering.

The receiver operates at 2.5V and consumes 250mW. The overall noise figure (NF) for the entire receiver chain has been measured to 8dB, sensitivity to -81.9dBm and maximum input signal to -19dBm.

4.1.2 5 GHz CMOS Wireless LANs

As in the previous article [2] the authors of ref. [3] have also chosen to use the dual conversion approach in their design. However their design covers both IEEE 802.11a and HiperLAN/2 physical layer requirements. The chip has been implemented in standard 0.25μm CMOS technology, however lower operational voltage and power consumption have been achieved compared to design [2]. As the local oscillator frequencies for the first and second down-conversion, they have chose 16/17 and 1/17 of the RF input, respectively. That gives approximately for a 5GHz input signal, first LO at 4.705GHz and second at 0.295GHz. After first down-conversion the IF will be at 0.295GHz. Figure 4.3 shows the architecture of the receiver. The authors have chosen a different approach in image rejection. Because of the chosen mixer architecture an additional image rejection is required. That is done by using a notch filter that is fully integrated / merged together with the low noise amplifier (LNA). A notch filter is more easily integrated than a conventional band pass filter, however the notch filter requires tuning. In the circuit presented an automatic tuning technique of the notch filter is used.

The receiver operates at 1.8V and consumes 24.7mW. The achieved overall noise figure has been measured to 7.2dB. The required sensitivity is -85dBm and maximum input signal -25dBm. The results for P1dB and IIP3 are -18dBm and -7dBm respectively.

As we can see, compared to ref. [2] the authors of ref. [3] have achieved better circuit performance using the same CMOS technology. Moreover, they have covered the requirements for both standards for the PHY.

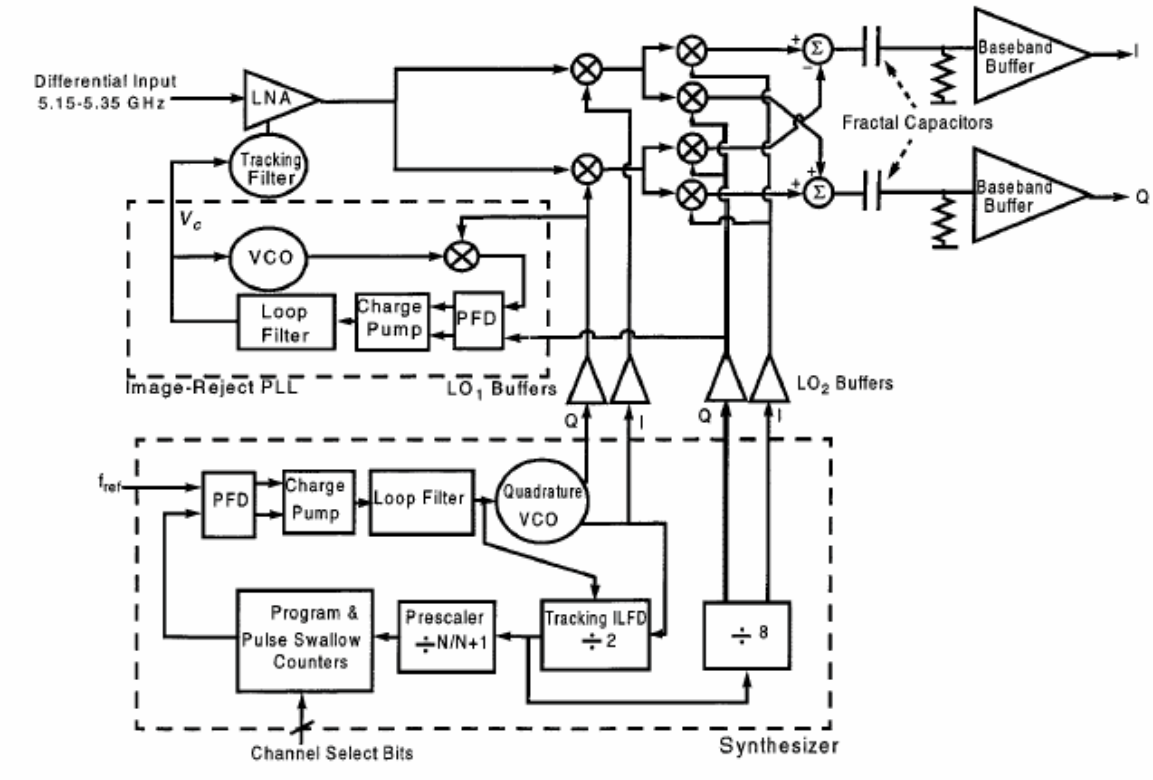

Figure 4.3: System architecture for proposed receiver [3]

4.1.3 A 5.25-GHz image rejection RF Front-End receiver with polyphase filters

In ref. [4] the authors has proposed a double conversion receiver based on high-IF topology and the double quadrature architecture. Figure 4.4 shows the proposed front-end architecture. The proposed circuit has been implemented in standard 0.18µm CMOS technology.

The RF signal is first amplified by a LNA and then transformed to quadrature RF signals by the three-stage RF polyphase filter. The quadrature RF signals are then down converted by double quadrature mixers to 1st IF at 1 GHz. Next, the down converted signals and its images at 3.25 GHz are then passed trough an IF polyphase filter. The function of this filter bank is to reject unwanted image signals. The 2nd IF amplifier compensate for the insertion-loss of the IF polyphase filter and also suppressed unwanted common-mode signals from double quadrature mixers. After the 2nd stage the IF signal can then be down converted again from 1 GHz to base band.

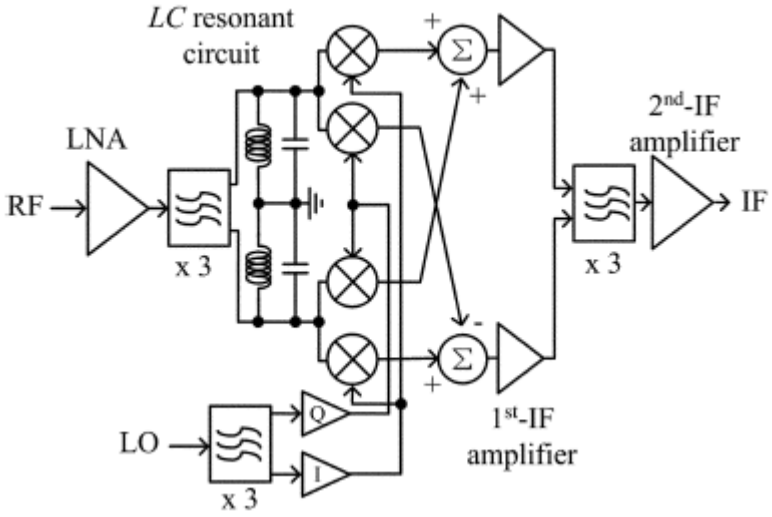

Figure 4.4: Proposed front-end architecture [4]

The proposed front-end operates at 1.8V and consumes 57.6mW. The achieved overall noise figure is 7.9dB at an overall conversion gain of 14 dB and image rejection ratio of 40 dB. The results for P1dB and IIP3 are -18dBm and -8dBm respectively.

4.1.4 Low power consumption direct conversion CMOS transceiver for multi standard 5-GHz WLAN systems

In ref. [5] the authors selected the direct-conversion architecture for their design of the receiver opposed to refs [2], [3] and [4]. However they have achieved better performance with regard to noise figure and power consumption. The advantage of their design is that it is not locked to a specific frequency band, which provides opportunity for a worldwide multi-standard operation. The frequency range for the receiver is 4.9-5.96 GHz and it can be operated in multiple-channel bandwidth systems since the bandwidth can be controlled in the range 5-20 MHz. Figure 4.5 show a block diagram of the proposed architecture. The signal path for the RF signal consists of a LNA circuit, a mixer and channel selection low-pass filters. The down-converted RF signal feeds directly to a set of analog-to-digital converters (ADC) for baseband processing. The authors chose to use a dual stage LNA arrangement where the second stage of the LNA can be switched off in the presence of strong signals, thus reducing the power consumption.

The transceiver has been designed and manufactured in standard 0.18μm CMOS technology and achieves a noise figure of 4.4dB. At the supply voltage of 1.8V it consumes 60mA.

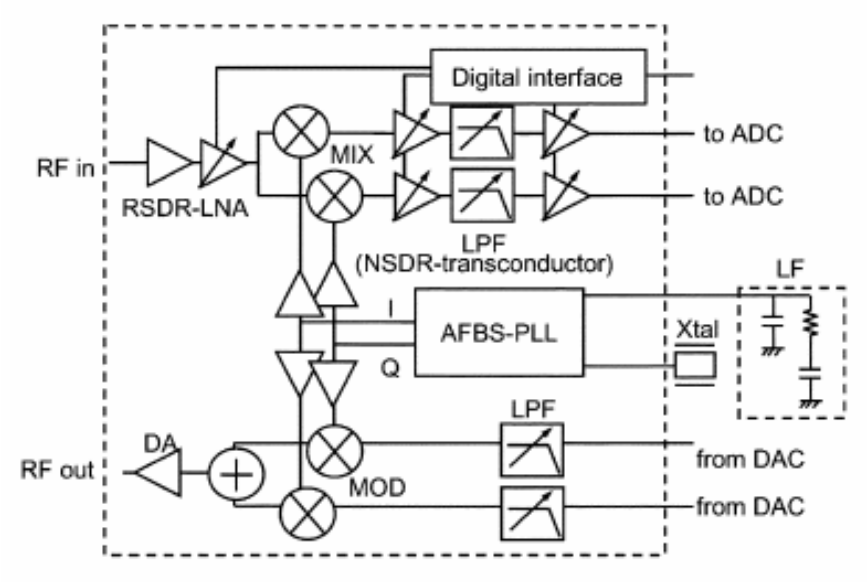

Figure 4.5: Proposed transceiver architecture [5]

4.1.5 Conclusion

There are a great number of published designs for IEEE 802.11b/g circuits operating in 2.4 GHz band, but for IEEE 802.11a/ HiperLAN operating at 5 GHz band the number is limited. One of the reasons has been that in past the right CMOS technology has been not available. With modern submicron CMOS technologies it is no longer an issue whether CMOS is capable of operating with high performance at radio frequencies. The authors of proposed circuits [1-5] show that it is possible to achieve high level of integration and low power consumption utilizing standard radio architectures.

4.2 Circuits, multi-band receivers

Growing demand for a wireless single device that covers all the different standards pushes forward development of multi-band transceivers. The standards not only differ between themselves in terms of operation (e.g. modulation, coding), but also they operate in different frequency bands, e.g. IEEE802.11a and IEEE802.11b/g respectively in 5GHz and 2.4GHz band. While the demodulation and decoding of the base band signals can be done by a

single digital signal processor (DSP) or software regardless of standards, the RF signal processing will differ. For some devices, switching between bands is a fully acceptable solution, where RF signals have multiple independent signal paths. The drawback is that the solution inevitable increases the power consumption, the area of the chip and the cost. Figure 4.6 shows a block diagram of a dual band receiver with independent RF signal paths.

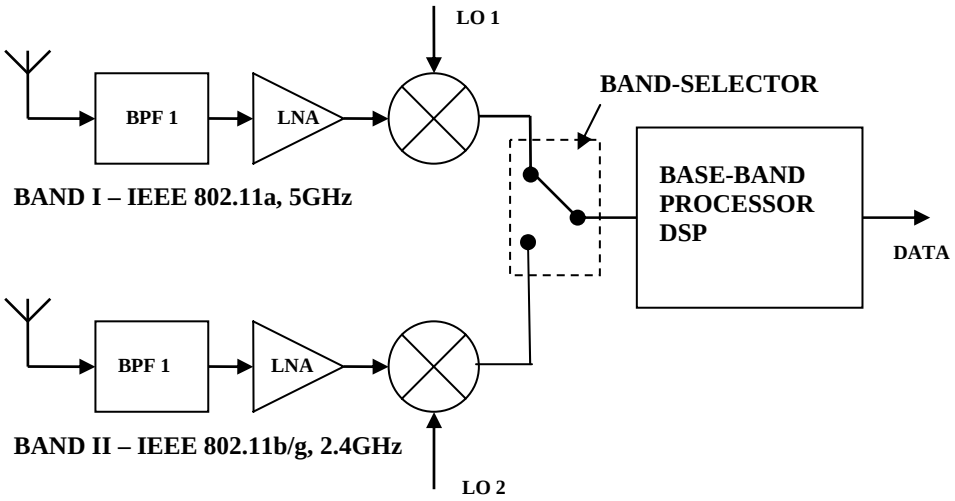

Figure 4.6: Dual band receiver with independent RF processing

In some cases however the need for switching between bands and one band at time operation is not sufficient. This is the case in multifunctional transceivers where more that one band needs to be received simultaneously. Also as a result of requirements for the lower power consumption and lower cost, single receiver circuits that can cover both frequency bands are desirable. Figure 4.7 show a block diagram of a dual-band receiver where receiver processes both bands simultaneously. This approach is also called concurrent architecture.

The main difference between the concurrent and non-concurrent approach is that in the in conventional architectures only one of the single-band LNAs is selected according to the desired frequency band of operation. Each of the LNAs can then be designed to have high selectivity and sensitivity according to the RF requirements. However this is accomplish by narrowing the bandwidth of the LNAs, thus making them useless for simultaneous operations in different frequency bands, thus requiring use of a separate circuit for each frequency band. This results in higher power consumption and larger die area.

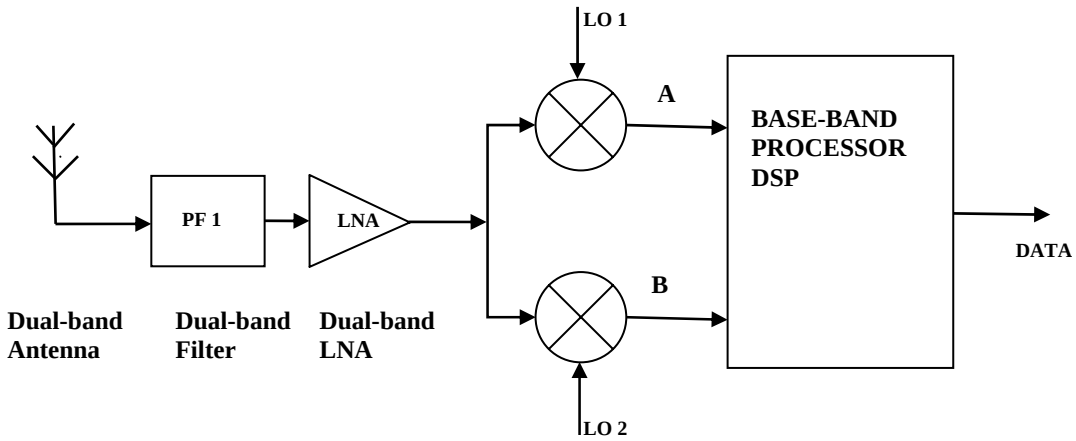

Figure 4.7: Concurrent dual-band receiver

In the concurrent approach it has been proposed to replace several LNA circuits with one wide-band LNA that can cover both of the bands. But simultaneous with the desired signals, strong unwanted signals are amplified, thus significantly degrading the receiver's selectivity and requires high level of filtration. The solution to this problem is to use a multi-band LNA where the LNA circuit is designed to give amplification to only desired bands.

There are several papers published regarding the subject of multi-band operation, see refs. [6-9].

4.2.1 A CMOS direct conversion transceiver for IEEE 802.11a/b/g

The authors of ref. [6] have presented a typical multi-band transceiver where each frequency bands has a separate signal path. Figure 4.8 shows the proposed architecture. The circuit has been manufactured in 0.18um standard CMOS process.

The authors have adopted the direct conversion receiver architecture in their design where the RF signal is down-converted directly into the baseband. The transceiver consists of two separate signal paths. One is designed for 5 GHz IEEE 802.11a operations. The other one is for 2.4GHz IEEE 802.11b/g. The common part for both is the frequency synthesizer circuit. The main advantage of such architecture is that each of the signal paths can be designed and optimized strictly according to given PHY requirements. The main drawback is that the design requires twice the amount of components, thus a large die area and higher power consumption.

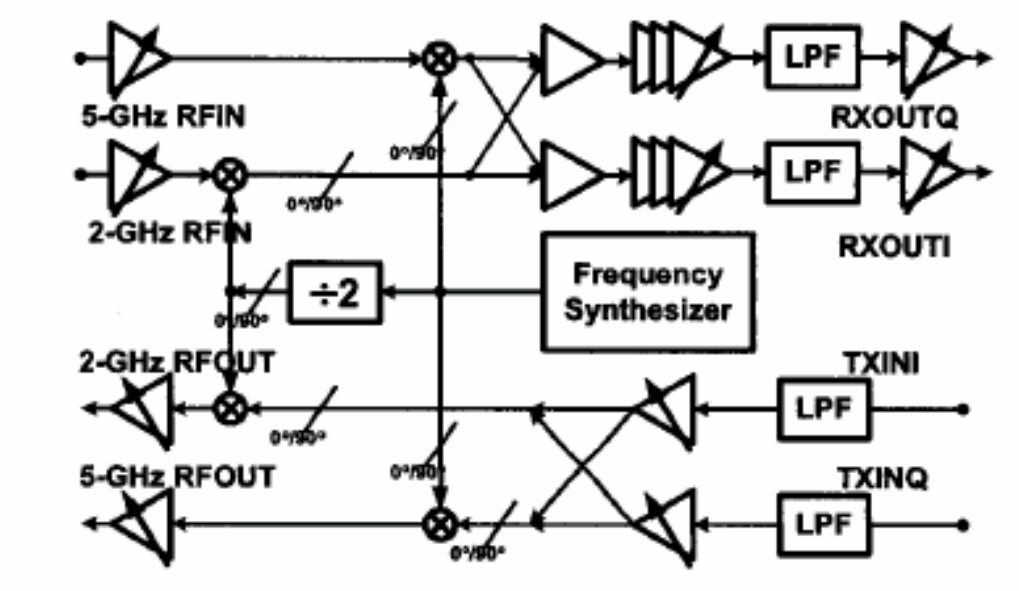

Figure 4.8: Dual band transceiver for IEEE 802.11a/b/g [6]

4.2.2 Concurrent multi-band LNA – Theory, design and application

In ref. [7] the authors have approached the problem of multi band operation from a different angle than [6]. Instead of using a separate path for each band, the authors have proposed a concurrent dual-band receiver. That means that both bands are processed by a single receiver circuit simultaneously. Figure 4.9 shows the proposed architecture. The RF signal is feed trough a dual-band LNA and then down-converted to IF by a common mixer set for both bands. To be able to eventually convert both bands from IF to separate baseband signals, a separate set of mixers and local oscillators are needed. By thorough frequency planning of IF, a high grade of image rejection is achieved.

Compared to architecture [6], the proposed architecture eliminates an extra antenna, a front-end filter, an LNA and a pair of mixers, resulting in power and die area savings. It also provides a simultaneous processing of both frequency bands that can be useful in some applications.

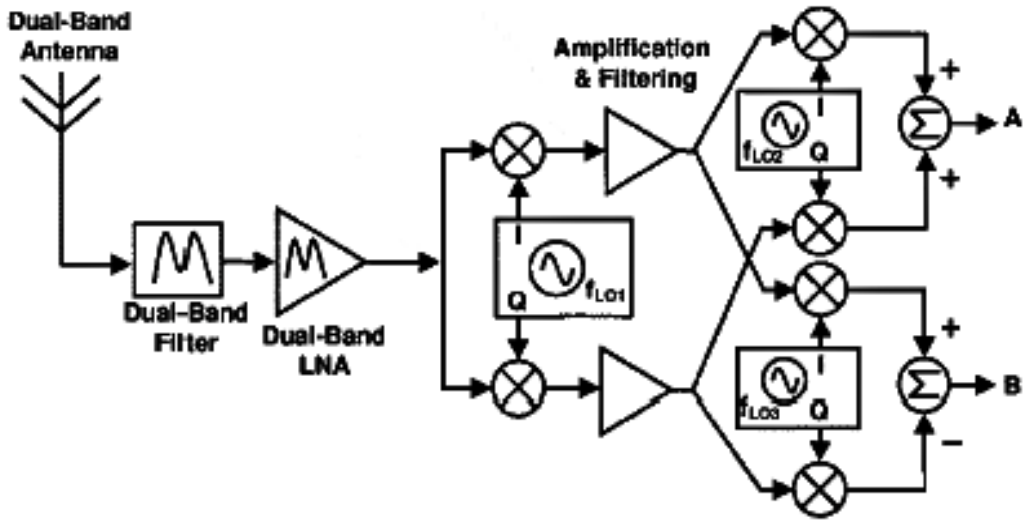

Figure 4.9: Concurrent dual-band receiver architecture [7]

4.2.3 A multi-band multi-standard RF Front-End for IEEE 802.16a and IEEE 802.11a/b/g applications

In ref. [8], the authors have chosen to use the concurrent approach presented in [7] for their design. However their design only operates in one frequency band at the time. The advantage of this design compared to the standard approach presented in [6] is that they maximize the level of hardware sharing as both the LNA and mixer circuits are shared for all the standards. Figure 4.10 shows the proposed architecture. The selection of the frequency band is done by switching the load inductor. In that way the LNA's resonance frequency can be changed according to required operation mode. Figure 4.11 shows a simplified schematic of the proposed LNA circuit.

The receiver is based on a combination of dual-conversion and Zero-IF architecture, where Zero-IF is adopted for IEEE 802.16a and the dual-conversion for IEEE 802.11a/b/g. The mixer is a wide-band type that covers all the bands. The authors have by thorough frequency planning managed to achieve multi-band operation by using only one local oscillator that can operate from 3.4GHz to 4.37GHz. Their proposed design shows a highly integrated circuit with low power consumption and small die area, which is well suitable for multi-band multi-standard operation when the simultaneous reception is not necessary.

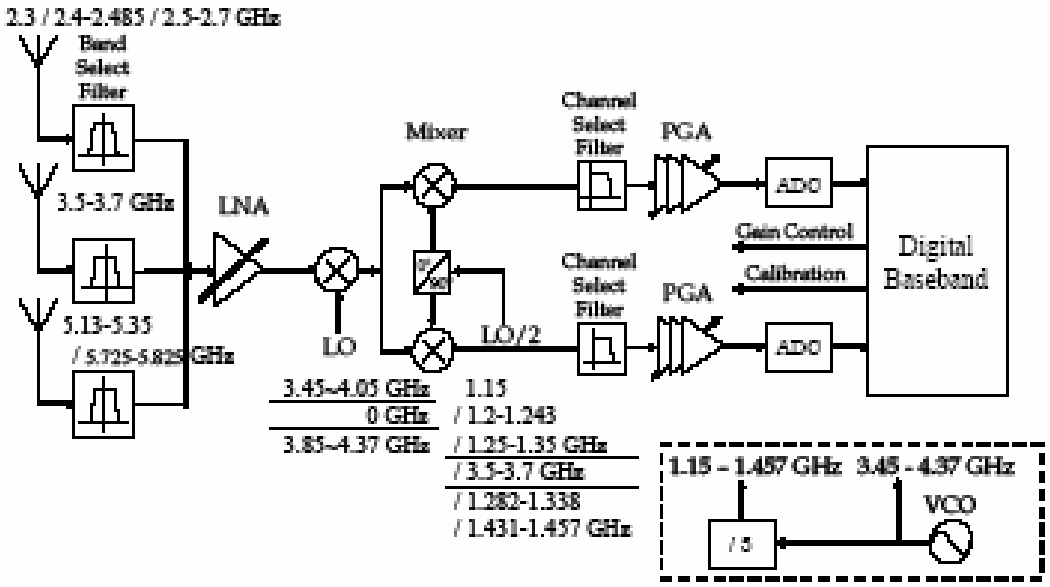

Figure 4.10: Proposed receiver architecture [8]

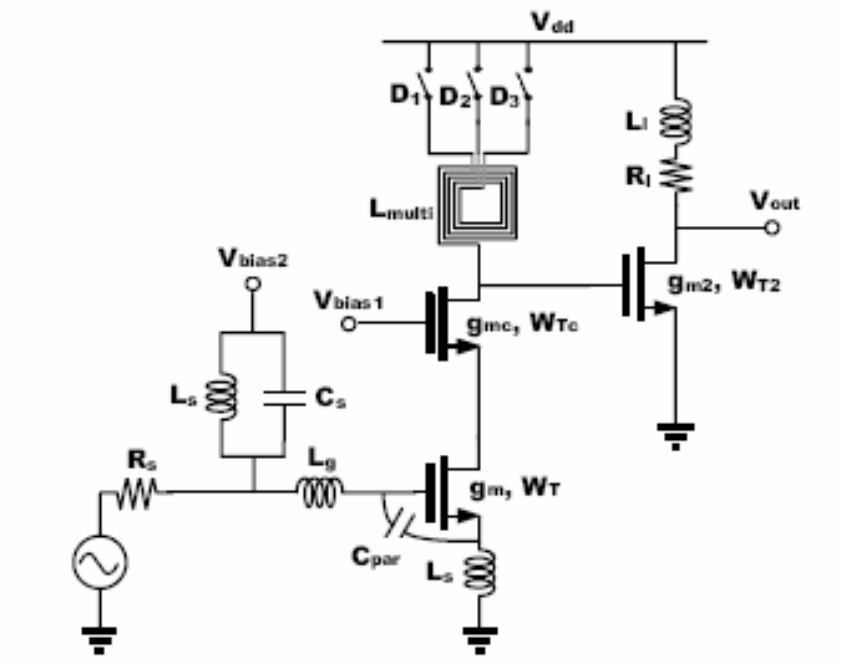

Figure 4.11: Simplified schematic of the proposed multi-band LNA [8]

4.2.4 A single-chip CMOS transceiver for IEEE 802.11a/b/g wireless LANs

In ref. [9] the authors has presented a single-chip solution for a triple standard operating transceiver for wireless LANs. The authors have taken similar approach as in [6], where each of the bands has separate LNA circuit. However

the processing after LNA is shared for both bands. The transceiver covers the 802.11a, b and g standards where 802.11a operates in 5 GHz band and 802.11b and g in 2.4GHz band. The receiver architecture shown on figure 4.12 is based on wideband IF topology.

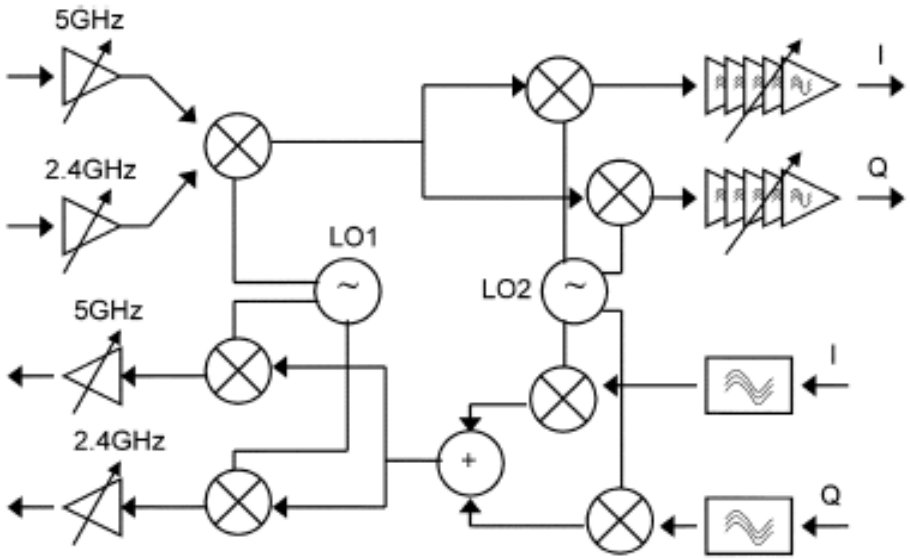

Figure 4.12: Proposed transceiver architecture [9]

The RF signals are first amplified by separate LNA circuits for each of the frequency bands. The advantage of this solution is that each of the LNA circuit can be optimized according to RF requirements. After amplification the signals are down-converted to a common high-IF frequency. Then the IF signal is down-converted again down to baseband by a complex I/Q mixer. In first down conversion the local oscillator runs on fixed frequency of 3840 MHz that cover both 2.4GHz and lower 5GHz band. The upper 5GHz can be covered by choosing a different LO frequency in the first mixer stage. In second down-conversion the LO frequency can be controlled according to desired channel reception. The mixer circuit is common for both bands, thus the receiver only operates in one frequency band at time. Figure 4.13 shows the proposed frequency plan for the transceiver.

The proposed circuit has been implemented in standard CMOS 0.18µm process. It requires 1.8V supply voltage and consumes in average 116mA for the receiver and 137mA for the transmitter part.

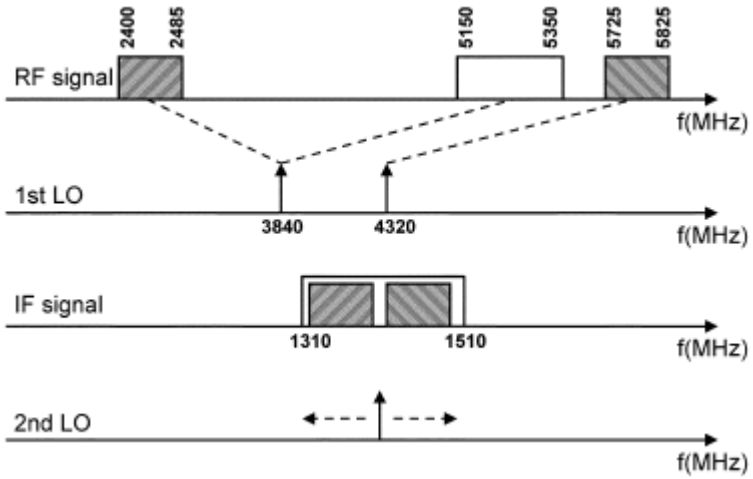

Figure 4.13: Frequency plan for the proposed transceiver [9]

4.2.5 Conclusion

The need for radio systems with more bandwidth and flexibility are increasing as the number of wireless communication standards operating in different frequency bands increases. The first solution to this challenge was to have a different chip for each of the bands. From the angle of the power consumption and cost, that solution was not very efficient. However a perfect RF requirements match was possible, as each of the chips was designed and made according to specific RF requirements. To cope with the drawbacks and increase integration, dual-band transceivers have been introduced [6-9]. The dual-band architecture made possible to share some of the circuits between the bands, thus increasing integration and reducing power consumption and cost. The future of the wireless communication receivers goes into direction multi-band multi-standard circuit. This multi flexible circuit can be then configured 'on the fly' and adopted to the desired application.

4.3 References

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CHAPTER 5

I have chosen to design a part of an RF receiver front-end that satisfies RF requirements for both IEEE 802.11a and HiperLAN/2 standards operating in the 5 GHz band. The proposed architecture is designed in the Cadence environment using 90 nm CMOS process from STMicroelectronics. The simulations are performed using Cadence simulator *Spectre*. In this chapter I will present the design of the circuit and its simulation results.

5.1 The receiver architecture

The proposed receiver architecture shown in figure 5.1 is based on the homodyne architecture describe in sec. 3.2.2. This architecture, known also as 'direct-conversion' or 'Zero-IF' topology, performs the down-conversion from RF to baseband in one single step. The architecture provides a higher level of integration than super-heterodyne architecture as no off-chip components are required. Full integration is a very important factor for power consumption and cost reduction. The use of Zero-IF receivers was very limited in the past due to the poor performance compared to IF receivers. However in the receiver systems for digital communication lower performance can be accepted in exchange for higher degree of integration [1].

I have chosen to implement the low noise amplifier (LNA) and mixers in my design as indicated in figure 5.1.

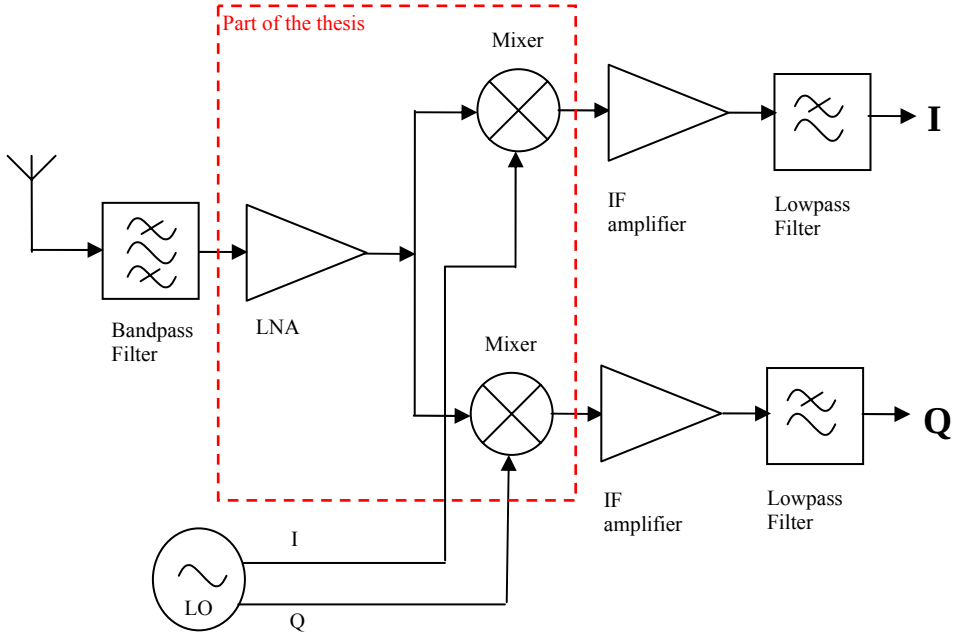

Figure 5.1: 'Zero-IF' receiver architecture

5.2 Specification

The first step in the design process is to establish target specification according to operating standards requirements, operating condition etc.

5.2.1 IEEE 802.11a and HiperLAN/2 RF specification

To be able to determine the RF requirements for the receiver both standards specification of the physical (PHY) layer need to be studied. The 802.11a standard specifies operation over a 300 MHz allocation of spectrum in the 5 GHz band [2], [3]. Of that 300 MHz allowance, there is a lower band located at 5.15 – 5.35 GHz and a separate upper band at 5.725 – 5.825 GHz, ref. sec. 2.1. The HiperLAN/2 standard specified operation in lower band located at 5.15 GHz – 5.35 GHz and an upper band at 5.47 – 5.725 GHz [4].

HiperLAN/2 has a different media access control (MAC) layer approach than 802.11a, but they share some similarities in the PHY layer [5], [6]. This result in that the performance requirements for the RF signal processing is quite similar [7] and a single receiver can cover both standards requirements.
First items that should be specified are the frequency range. As the upper band is not worldwide available and doesn't correlate for both of the standards, it is

often acceptable to only cover lower band [7]. Thus, the choice of frequency span for my design is 5.15 – 5.35 GHz.

To compile a common set of requirement for both 802.11a and HiperLAN/2 we need to take a look at each of those separately and then chose the most stringent one. Table 5.1 shows the RF requirements for both 802.11a and HiperLAN/2 separately [3], [4], [7], [8].

Parameter	IEEE 802.11a	HiperLAN/2
Frequency span	5.15 – 5.35GHz 5.725 – 5.825GHz	5.15 – 5.35GHz 5.47 – 5.725GHz
Noise Figure (NF)	< 10dB	< 18dB
P1dB	> -26dBm	> -21dBm
IIP3	> -16dBm	> -10dBm
Channel bandwidth	20MHz	20MHz

Table 5.1: RF requirements for 802.11a and HiperLAN/2 [3], [4], [7], [8]

When summarized table 5.1 gives us our target RF specification as shown in table 5.2.

Parameter	IEEE 802.11a/ HiperLAN/2
Frequency span	5.15 – 5.35GHz
Noise Figure (NF)	< 10dB
P1dB	> -21dBm
IIP3	> -10dBm
Channel bandwidth	20MHz

Table 5.2: Target RF requirements.

5.2.2 Operating requirements

Target power consumption and input characteristic requirements are shown in table 5.3.

Parameter	Value
Power supply	1.2 V
Power consumption	< 5mA/ 6mW
Input impedance	50Ω

Table 5.3: Target power consumption

5.3 LNA design

The LNA is very important component in the front-end of an RF receiver. Usually, it is the first active block in the receiver signal path. Therefore, it has a large impact on the system noise figure and determinates the overall input characteristic, ref. sec. 3.1.1. A good LNA should exhibit low noise figure (NF), have high gain and well defined input characteristic.

The LNA used in my design is based on single stage cascode common source topology. This topology is widely used and has proven to perform very well [9], [10] and [11]. Figure 5.2 shows a principal schematic of a single stage cascode common source LNA. Cascode configuration offers best isolation, low-to-moderate noise, easy matching, good linearity and high gain. However, because of two transistors stacked on each other, the configuration requires higher supply voltage compared to single transistor configuration. Cascoding transistor M_2 is used to reduce the interacting of the tune output with the tuned input and to reduce the effect of gate-drain capacitance C_{gd} of transistor M_1. Transistor M_2 also improves the amplifiers reverse isolation and reduced signal leakages from the output back to the amplifier e.g. LO leakage from the mixer back to the LNA. The inductors L_s and L_g are chosen to provide together with gate-source capacitance C_{gs} of transistor M_1 the desired input characteristic. The inductance L_d together with the load capacitances and capacitances of M_2 form a LC tank circuit tuned to operating frequency. Transistor M_3 together with resistors R_{B1} and R_{B2} forms the biasing network for transistor M_1 where M_3 form a current mirror with M_1. Capacitors C are DC blocking capacitors. The LNA has been design as a narrowband LNA tuned to the center frequency at 5.25 GHz with inductive source degeneration.

5.3.1 Transistor sizing

First step in the design process is to decide proper transistor size, according to required power consumption/ bias condition. Transistor size has direct influence on power consumption and noise figure of the circuit. In case of cascode topology, transistor M_1 will have biggest impact on the overall noise figure. By using power-constrained noise optimization method described in [12], [9] an optimal transistor size can be establish. The equation 5.1 [12] gives us optimal transistor width W_{opt} which would provide the minimum noise figure for set power dissipation.

$$W_{opt} \approx \frac{1}{3\omega L C_{ox} R_s} \qquad (5.1)$$

A common practice regarding the width of transistor M2 is to select same width as M1, but this is not necessarily best choice. However, this choice allows the drain of the input transistor and the source of the cascode transistor to be merged in the layout of the chip. [12]

The length L of the transistors are kept to theirs process minimum to maximize ω_T and g_m.

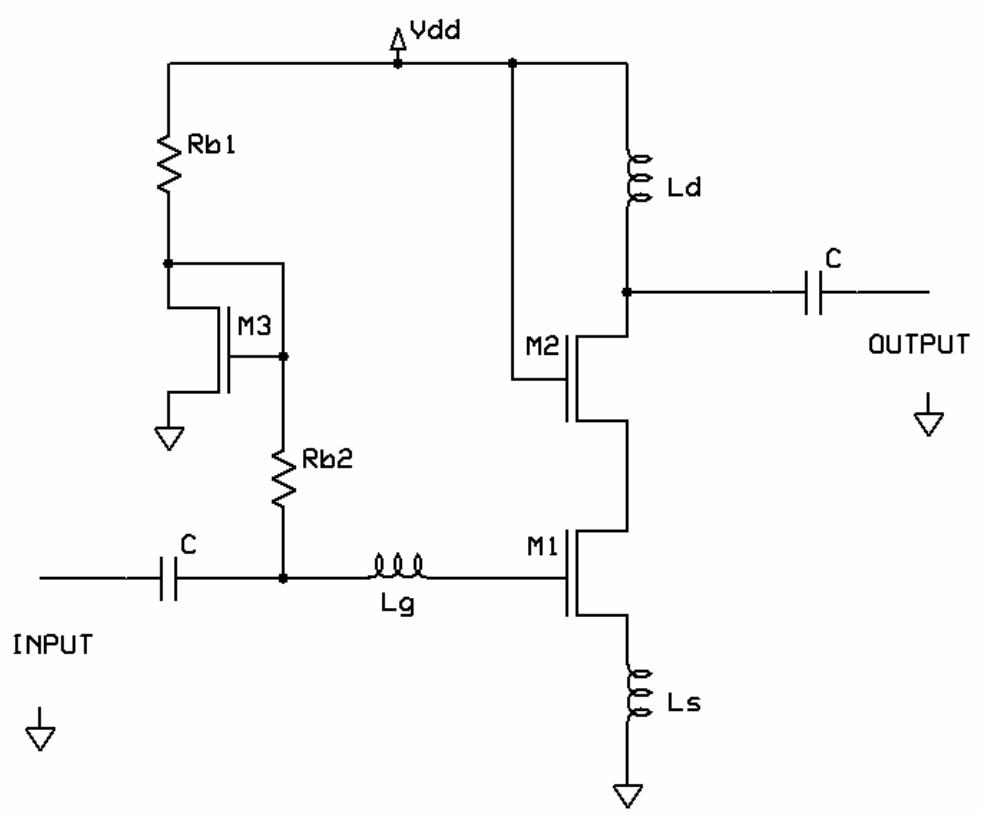

Figure 5.2: Single stage cascode amplifier with inductive source degeneration

5.3.2 Impedance matching

Ref. sec. 3.1.1 the LNA should have a well defined input characteristic. In this case the input impedance of 50Ω is required to limit the reflections of the signal from a band-select filter or an antenna. In a fully integrated front end, LNA output matching is often not required, as the LNA is going to be connected on-chip to the next stage in the receiver chain [13].

There are several methods [9], [12] of achieving the correct input characteristic.

The simplest method is to put a 50Ω resistor across the input terminals as shown in figure 5.3. This method provides a good broadband matching. Unfortunately

the thermal noise coming from the resistor tends to degrade the noise figure of the system and it act as an attenuator [12]. Therefore this method is not usually used.

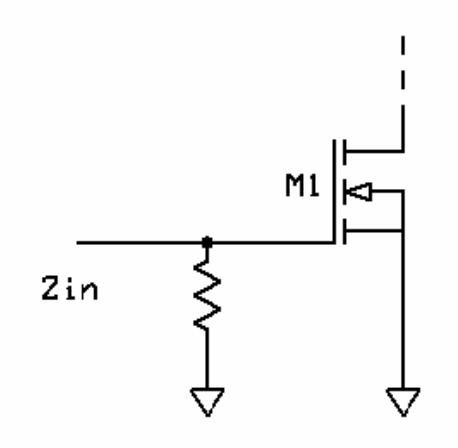

Figure 5.3: Resistive input matching

The second method is to use a shunt-series amplifier configuration as show on figure 5.4. This configuration has slightly better noise performance and suffers from fewer problems than the previous method. The noise figure is much better than in previous method, but still it is not at its minimum [12]. However because of the broadband capabilities the circuit can be often found in many LNA applications [14].

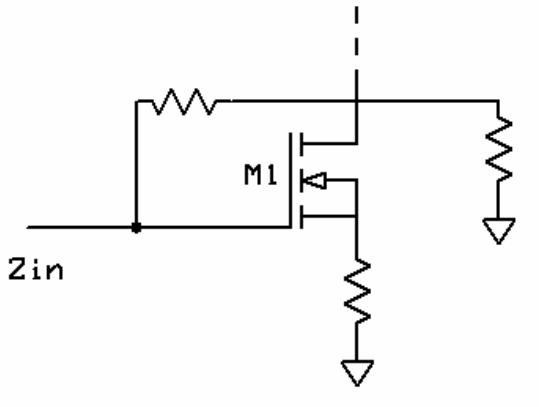

Figure 5.4: Shunt-series amplifier

Third method is to use a common-gate configuration as shown in figure 5.5. Utilizing the fact that the resistance looking into source terminal is $1/ g_m$, a proper selection of device size and bias current can provide the desired input characteristic. However the lowest noise figure that can be achieved is about 2.2 dB and 4.8 dB for respectively long- and short-channel devices [12]. The noise figure will significantly degrade at high frequencies. However the method has been successfully used in some LNA applications [15].

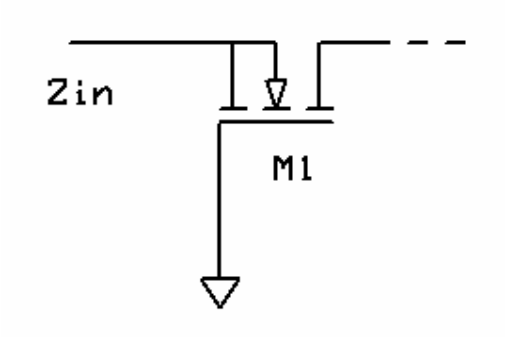

Figure 5.5: Common-gate termination

Fourth and most used method for input matching is inductive source degeneration as shown in figure 5.6. By using an inductance L_s, a real term in the input impedance can be achieved without need for a real noisy resistance. Gate inductance L_g provides an additional degree of freedom in the design phase to achieve the correct resonance frequency giving the purely resistive input impedance. It is concluded in [9] that by using the inductive source degeneration, the best noise figure can be achieved. However, matching trough inductive degeneration will only create a narrow-band match.

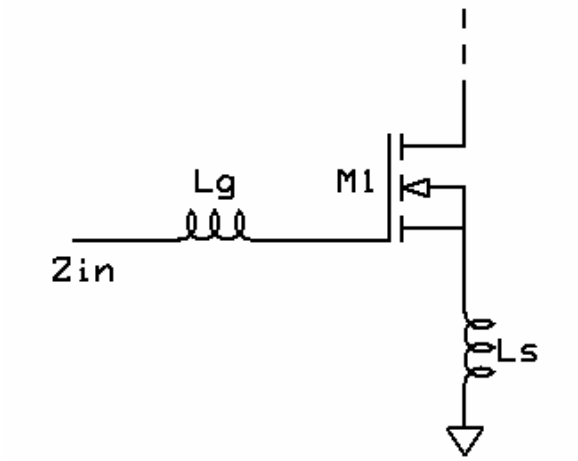

Figure 5.6: Inductive source degeneration

Studying the cascode amplifier with inductive source degeneration shown in figure 5.2 we can see that the input impedance of the LNA can be expressed by equation 5.2.

$$Z_{in} = \frac{1}{j\omega C_{gs}} + j\omega(L_s + L_g) + \frac{g_m L_s}{C_{gs}} \qquad (5.2)$$

Since Z_{in} in our case is to be matched to be R_s=50Ω and at the resonance we can rewrite 5.2 in to following equations:

$$L_s = \frac{g_m R_s}{C_{gs}} \qquad (5.3)$$

$$L_g = \frac{1}{\omega_0{}^2 C_{gs}} - L_s \qquad (5.4)$$

5.3.3 Initial calculations

I have chosen I_D current for the amplifier to be 1mA. Using the equation 5.1 and known process parameters, the optimal transistor width for M_1 can be found, ref. equation 5.5.

$$L = 0.1\mu m$$

$$C_{ox} = 17.745 \cdot 10^{-3} \frac{F}{m^2}$$

$$R_s = 50\Omega$$

$$\mu_n = 0.05 \frac{m^2}{V} s \qquad [16]$$

$$f_o = 5.25GHz$$

$$I_D = 1mA$$

$$W_{opt} \approx \frac{1}{3\omega_o L C_{ox} R_s} \approx 114\mu m \qquad (5.5)$$

The width of transistor W_1 and W_2 is then set to 115 µm. The length L of all transistors is kept to minimum process length. The minimum transistor length for the STMicroelectronics 90nm CMOS process is 0.1 µm.

Knowing the size of the input transistor M_1 the gate-source capacitance C_{gs} can be obtained by using (5.6), [16] and g_m by using (5.7), [16].

$$C_{gs} = \frac{2}{3} C_{ox} WL \approx 136 fF \qquad (5.6)$$

$$g_m = \sqrt{2\mu_n C_{ox} \frac{W}{L} I_D} \approx 45mS \qquad (5.7)$$

Using those key parameters an initial value for source degeneration inductance L_s and gate inductance L_g can be calculated by using (5.3) and (5.4).

$$L_s = \frac{g_m R_s}{C_{gs}} \approx 0.2nH \qquad (5.8)$$

$$L_g = \frac{1}{\omega_0^{\,2} C_{gs}} - L_s \approx 5.6nH \qquad (5.9)$$

The value of $L_{d,}$ that forms a LC tank together with parasitic capacitances and the input capacitance of the next stage e.g. mixer is calculated according to (5.11). The total output capacitance C_o (5.10) has been set to 600fF.

$$C_o = C_{db} + C_{dg} + C_L \qquad (5.10)$$

$$L_d = \frac{1}{\omega_o^{\,2} C_o} \approx 1.5nH \qquad (5.11)$$

The values obtained from (5.5-11) don't take the parasitic capacitances and other undesired products that influence the performance into consideration, but gives us a starting point. The values need to be verified and adjusted during simulation phase.

5.3.4 The circuit

The LNA circuit as shown in figure 5.7 has been designed and simulated. The transistors have been implemented as multi finger transistors to reduce gate resistance. By using narrow finger width, the effect of the gate resistance can be made small compared to the other parasitic resistors [17]. The optimal finger width has been determined by simulation. Further to be able to use the cascode configuration with low supply voltage the low-threshold voltage transistors available in the process are used.

The function of the capacitor C_{ex} is together with L_d, C_L and parasitic capacitances to tune the resonance frequency of the output LC tank circuit.

The design has been first simulated with ideal inductances and the values have been tuned to the best performance. In the next step of the design process all the inductors was realized as on-ship inductors and the ideal model has been replaced by physical π-model [18], [19] shown in figure 5.8. The inductors have been modeled using ASITIC [20] tool. The ASITIC has been set up with a technology file that describes the substrate and metal layer of the process. The inductors are constructed in the top metal layer of CMOS process and are of square type. The layout of on-chip inductor L_g is shown in figure 5.9. The final design parameters of the on-chip inductors are presented in the appendix. However the on-chip spiral inductors can be partly replaced by bonding wires or a combination of bonding wire and on-chip inductor. That will lead to a better design, because the quality factor Q of bondwires is much higher then on-chip spiral inductors [21].

The other passive components such as resistors and capacitors are modeled with models provided in the design library for 90nm process. Resistors are of poly P+ non-silicided type and capacitors are of MIM (Metal-Insulator-Metal) type.

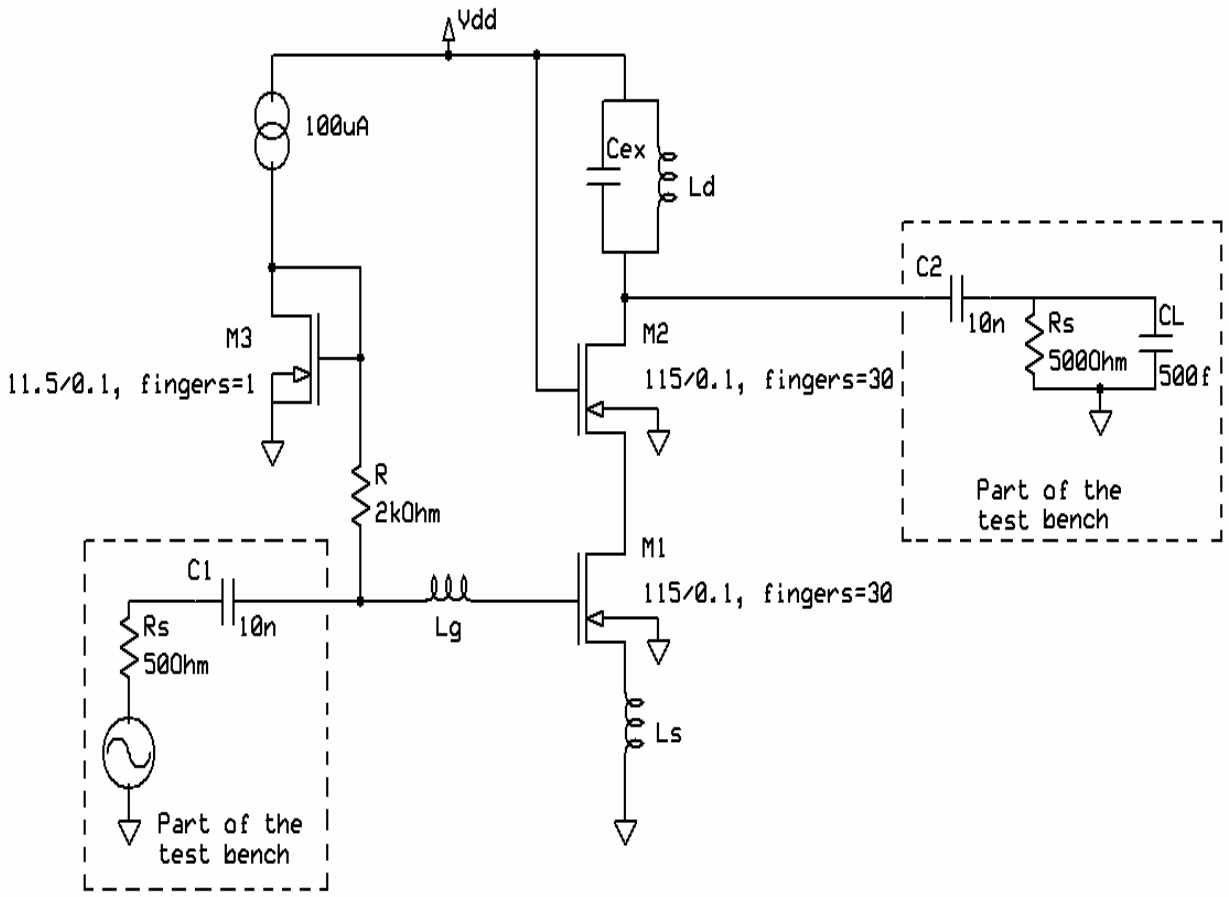

Figure 5.7: The schematic of the LNA incl. test bench and bias components

Table 5.4 shows the final component values.

Component	Value
M1 & M2	W=115µm, L=0.1µm, fingers=30
M3	W=11.5µm, L=0.1µm, fingers=1
L_s	0.73nH
L_g	5.5nH
L_d	1.3nH
C_{ex}	85fF

Table 5.4: Final component values

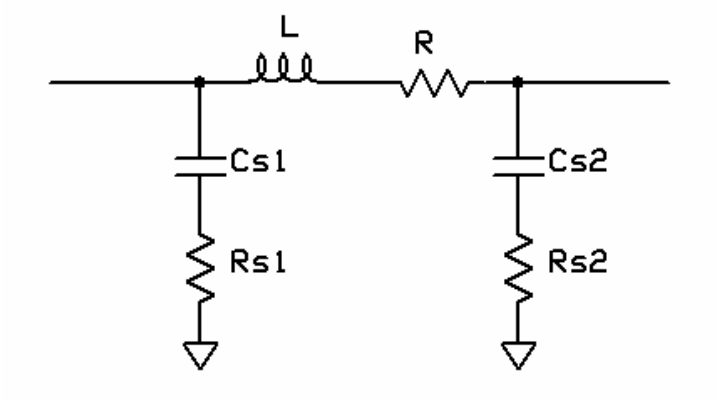

Figure 5.8: π-model of a spiral inductor

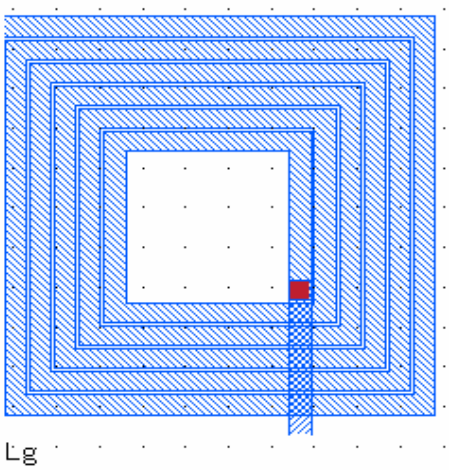

Figure 5.9: On-chip inductor L_g

In my design I have chose to not take the parasitic capacitances and inductances associated with chip package into consideration as this thesis didn't aim at creating the physical chip layout. However those parasitics will influence on the

LNA's input match and can cause variations on the supply and ground nodes of the final chip and need to be taken into consideration during design phase. One of the improvements to get more accurate simulation is to include a model for the connection pads [21]. Such model can consists of an inductor with a series resistor representing bonding wire and a capacitor representing capacitance from connection pad to the ground, as shown on figure 5.10.

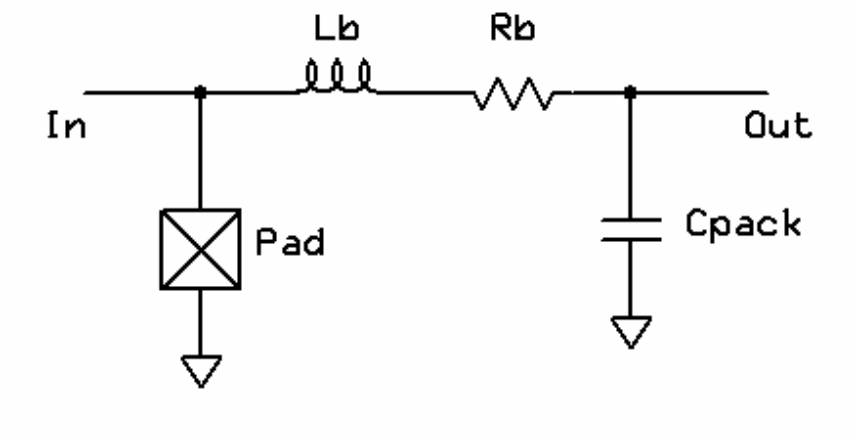

Figure 5.10: The model of the connection pad

Another item that needs to be taken into consideration before the design can be implemented into physical chip is ESD (Electro-Static Discharge) protection, as their implementation will also have impact on the LNA's performance. There are several methods of implementing ESD protection [22], however not all methods are suitable to use at high frequency applications [23].

The simulation result and performance summary of the LNA circuit are presented in the section 5.3.5. The detail schematic and test bench used in the simulation can be found in the appendix.

5.3.5 Simulations results

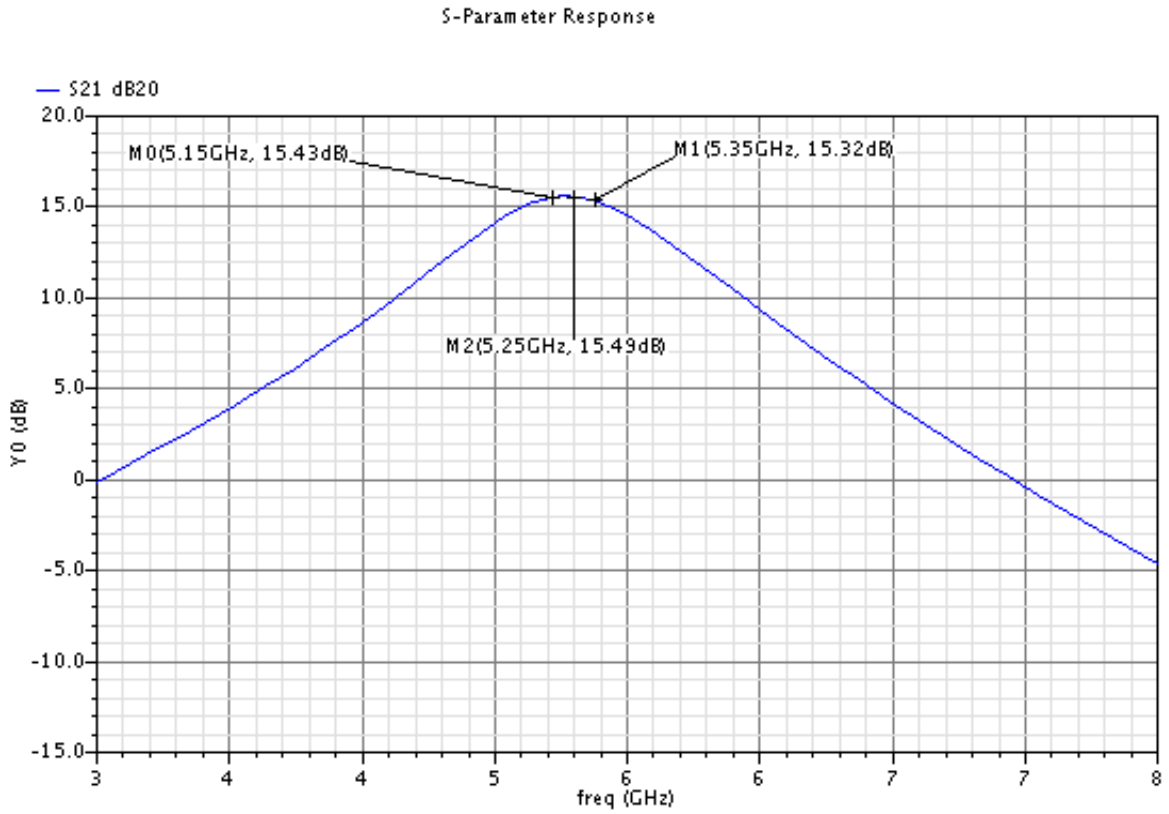

Figure 5.11: Forward gain of the LNA, S21

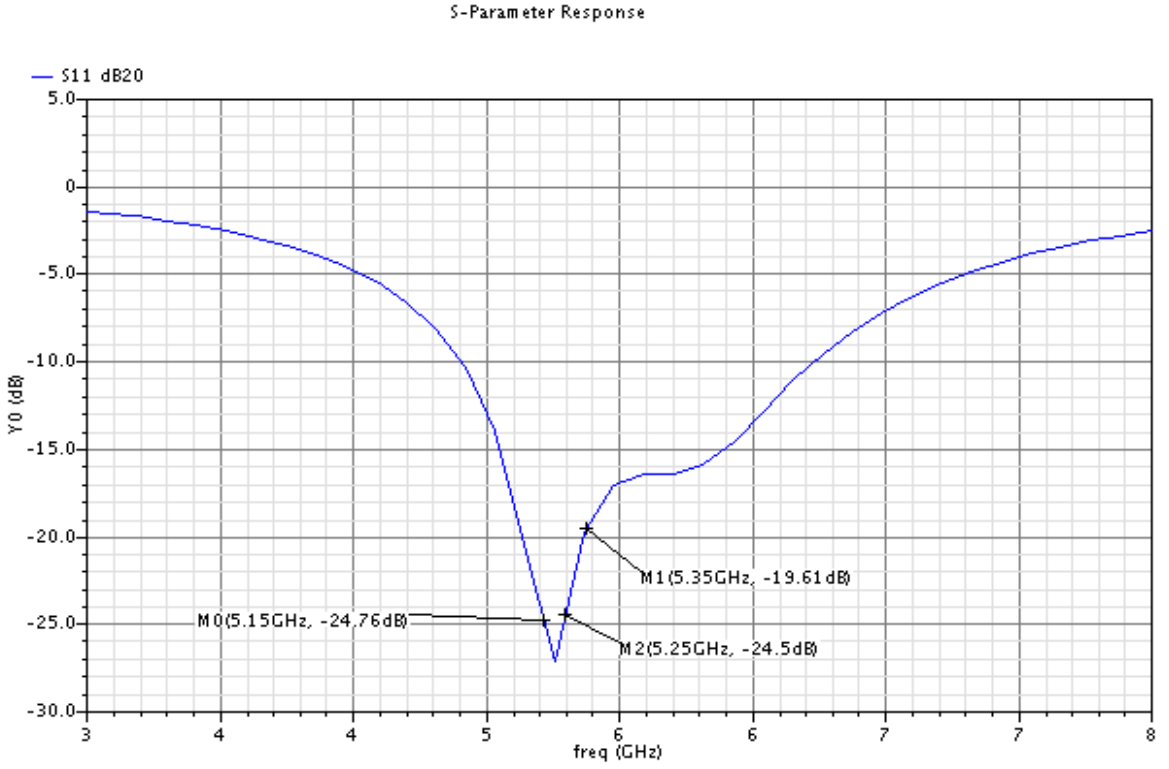

Figure 5.12: Input matching of the LNA, S11

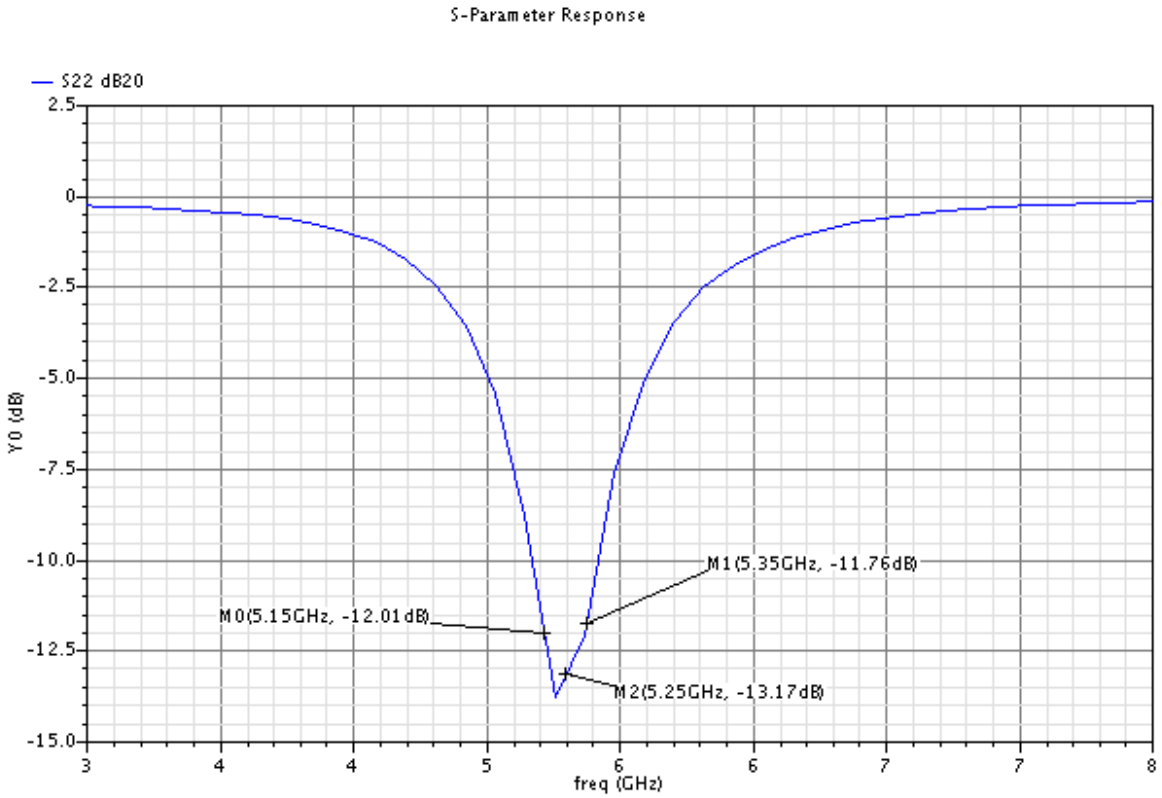

Figure 5.13: Output matching of the LNA, S22 @ 500Ω/ 500fF load

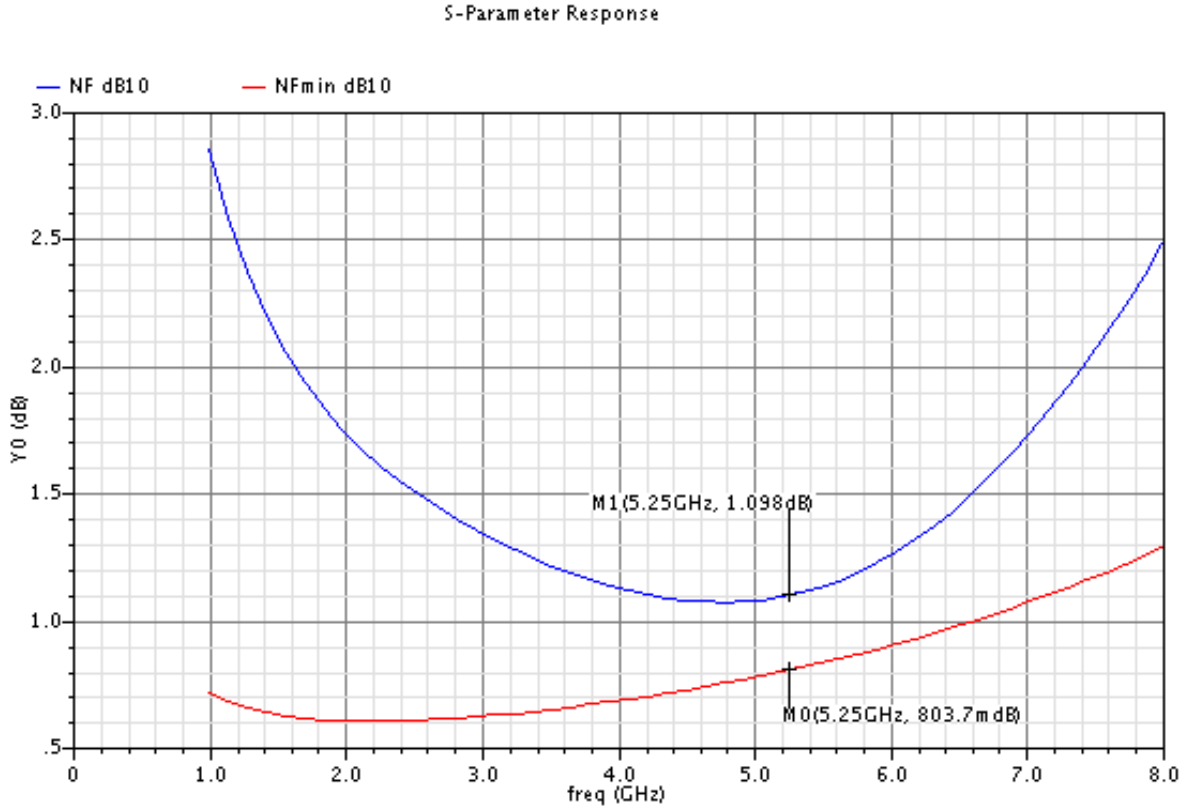

Figure 5.14: Noise figure (NF) and minimum noise figure (NFmin) of the LNA

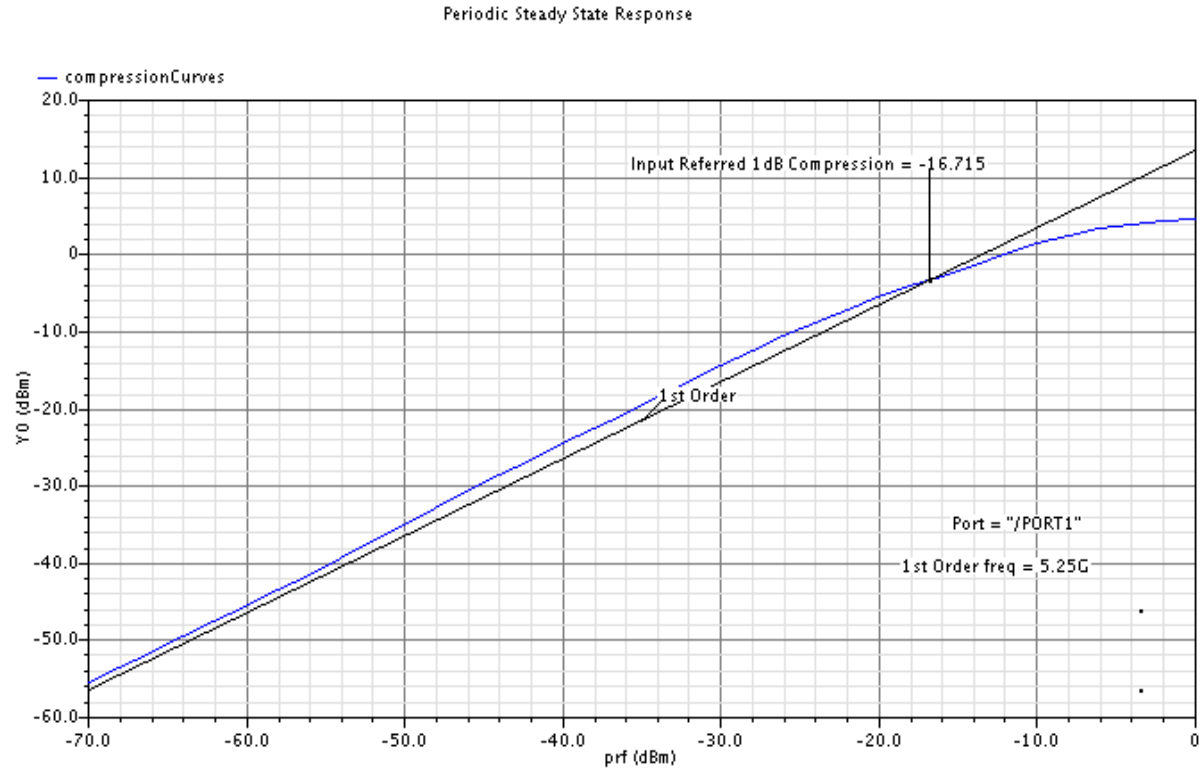

Figure 5.15: 1-dB compression point of the LNA, P1dB

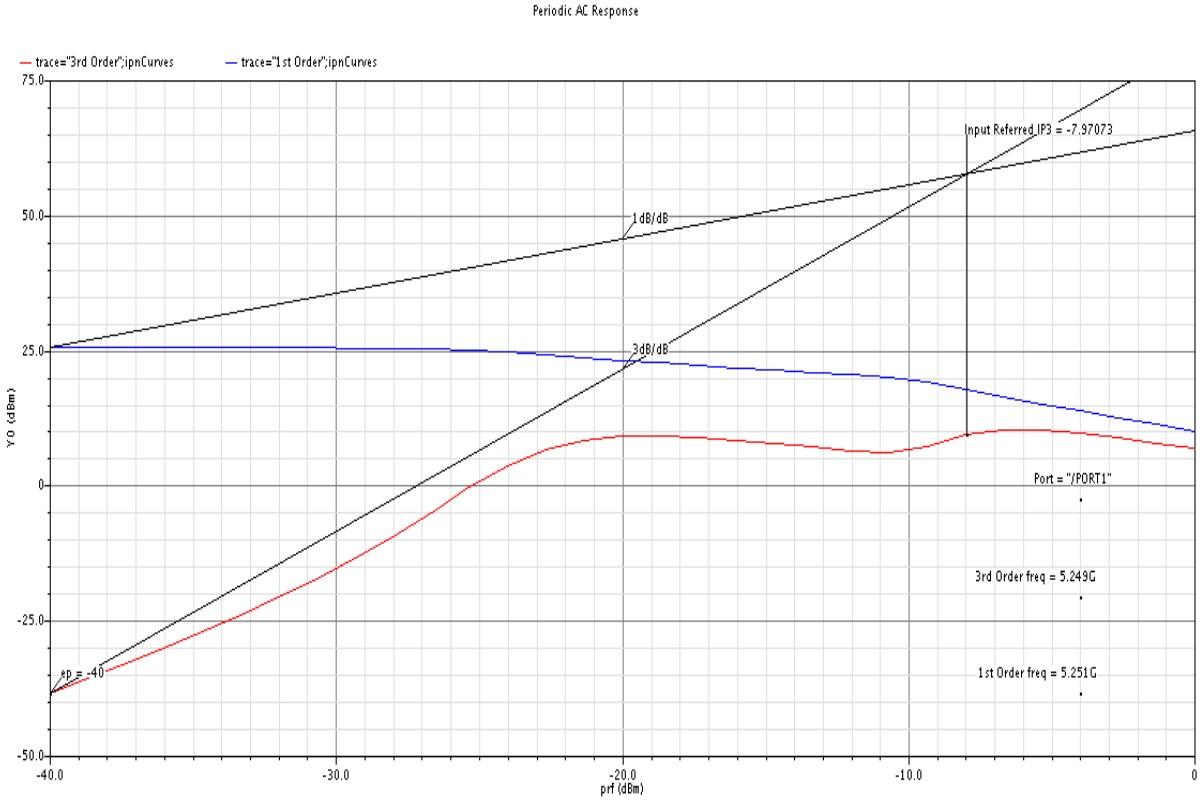

Figure 5.16: Input referred third-order intercept point, IIP3

Parameter	Value
Forward gain, S21 @ 5.25GHz	15.5dB
Δ |S21| @ 5.15-5.35GHz	0.17dB
Input match, S11 @ 5.25GHz	-24.5dB
Output match, S22 @ 5.25GHz, 500Ω/ 500fF load	-13.17dB
Noise figure, NF @ 5.25 GHz	1.1dB
P1dB	-16.7dBm
IIP3	-8dBm
Power consumption	1.1mA
Power supply	1.2V

Table 5.5: Performance summary for the LNA

5.4 Mixer design

A direct conversion architecture is specially exposed for 1/f noise as the noise is located very close to the base band and can corrupt the IF signal. The 1/f noise is also a generally the dominant contributor to the front end flicker noise [12]. Other factors as the linearity and power consumption should also be taken into consideration when selecting the circuit topologies for the mixer. That is why the passive voltage switching mixers should be considering for use in the direct conversion receivers. The passive mixers allow a drastic reduction of the 1/f noise of the mixer switching pair as there is no DC current flowing trough switching transistors. Secondly, no DC current results in zero-DC power consumption. However, the main drawbacks of the passive mixers are that they don't provide gain and require a relative large LO drive. The conversion loss needs to be compensated in the LNA and/ or the IF buffer stage.

5.4.1 The circuit

In my implementation I have chosen to use a double-balanced passive mixer, presented in [12]. The schematic is shown in figure 5.17. The circuit consists of four switching transistors (M1 – M4). The switching transistors are driven by differential LO signal. When M1 and M4 are on, output "IF+" is connected to "RF+" and output "IF-" is connected to "RF-". When M2 and M3 are on, output "IF+" is connected to "RF-" and output "IF-" is connected to "RF+". As indicated earlier the main drawback of the proposed topology is the negative conversion gain. The theoretical conversion gain is -2.1 dB and -3.92 dB with respectively sinusoidal and square-wave LO drive for this type of mixers [12]. The conversion loss can be optimized by selecting optimal transistor width. The

conversion gain given by (5.14) is related to the transistors r_{ds} (5.12). That indicates that large transistor will give us low conversion loss. However as the size of the transistor increases, the parasitics capacitances of the transistor increase as well. As the result of it will degrade performance of the mixer.

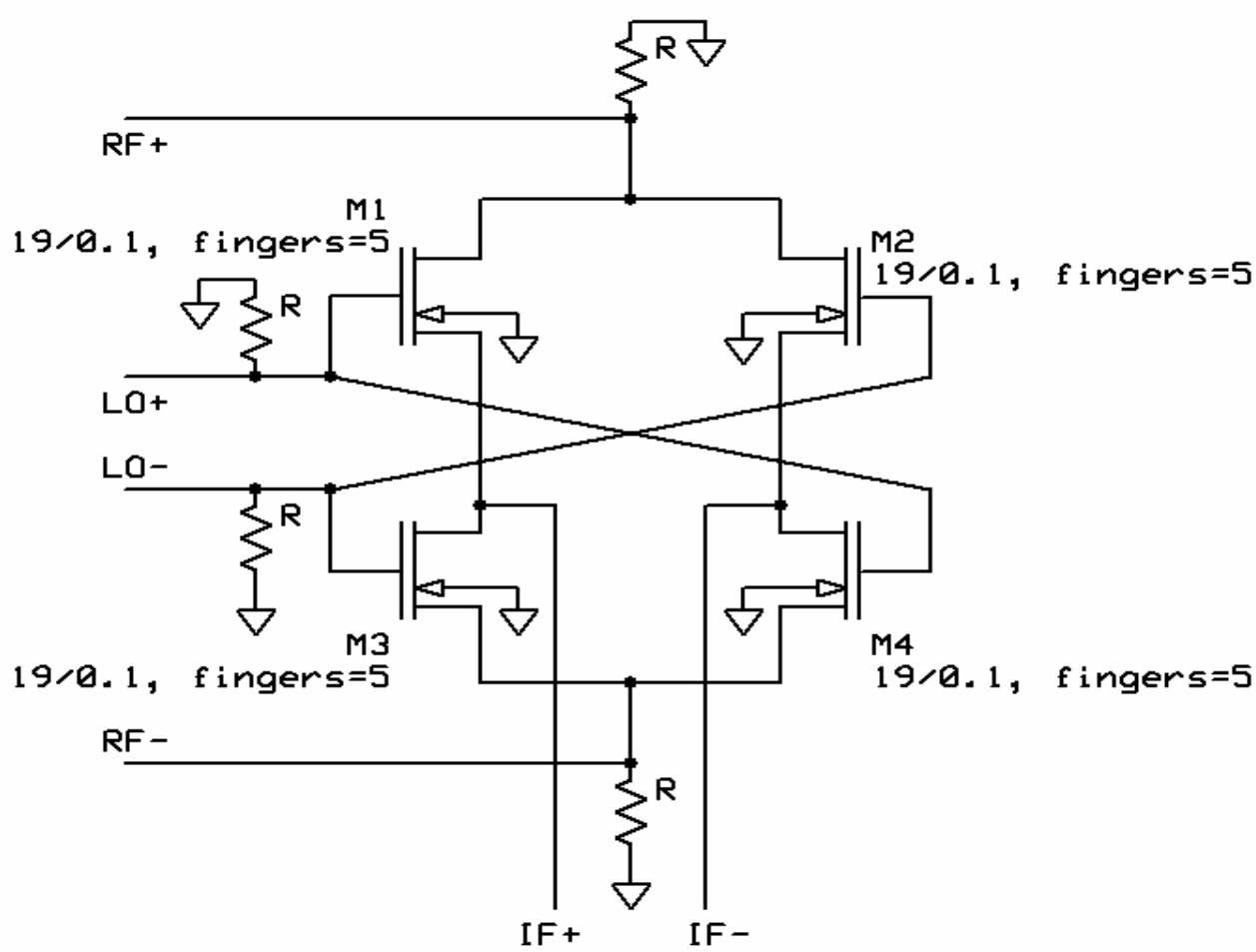

Figure 5.17: Double-balanced passive mixer

The size of the transistor and amount of fingers for my implementation has been decided according to simulation results for the conversion gain versus transistor width shown in figure 5.18. In the plot we can see at minimum gain loss can be found when the width W is approximately 19µm. The noise figure of the mixer is depending on the transistor size as well. Plot in figure 5.18 shows simulated noise figure for different transistor width. From 5.18 we can se that 19µm is an optimal choice for lowest conversion loss, but it is not optimal for noise figure in figure 5.19. However a compromise between conversion loss and noise figure must be made. The switching transistors are a low V_T (threshold voltage) type available in the process.

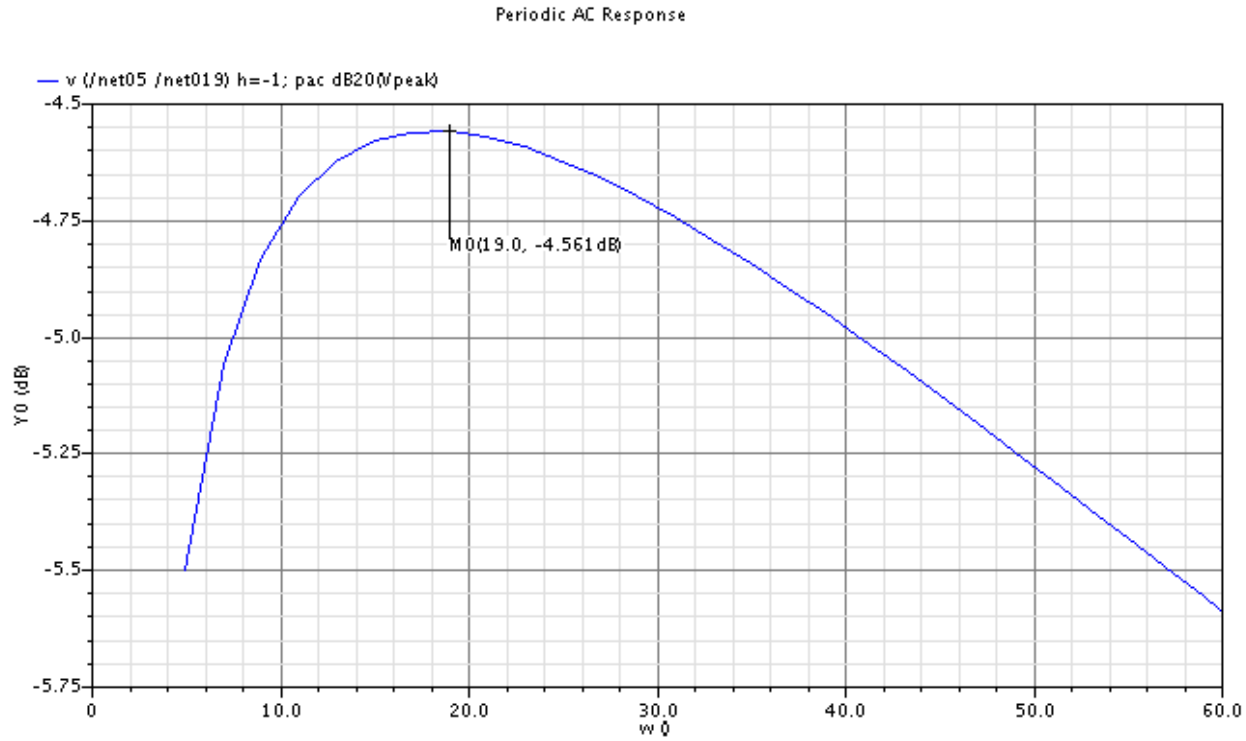

Figure 5.18: Conversion gain versus transistor width w (µm)

The available LO drive is set to 0dBm, which results in LO voltage of $0.707V_{rms}$ at 500Ω input impedance.

Using process parameters from section 5.3.3 and new values for W and R_S, the conversion gain can be estimated by using equations 5.12 [16], 5.13 and 5.14 [24].

$$W = 19\mu m$$

$$R_S = 500\Omega$$

$$V_{eff} = 0.707V_{rms} \quad (0dBm\ LO\ at\ 500\Omega)$$

$$r_{ds} = \frac{1}{\mu_n C_{ox}\left(\frac{W}{L}\right)(V_{GS} - V_t)} \approx 11.8\Omega \qquad (5.12)$$

$$A_0 = \frac{R_S}{R_S + 2r_{ds}} \qquad (5.13)$$

$$G_C(dB) = 20\log\frac{2}{\pi}A_0 \approx -4.3dB \qquad (5.14)$$

The functions of resistors R are to set correctly the potential for the input circuit.

The bias of the LO signal should be very close to the bias voltage of the RF input plus V_T (threshold voltage of the transistor). In our case the bias of RF input equals 0V, so the LO bias should equal V_T. However, it was determined by simulation that the LO bias when applied cause degeneration of the conversion loss, therefore no DC bias was applied to the LO signal in the final circuit.

The simulation results and performance summary (table 5.6) of the mixer circuit are presented in the section 5.4.1. The detail schematic and test bench used in the simulation can be found in the appendix.

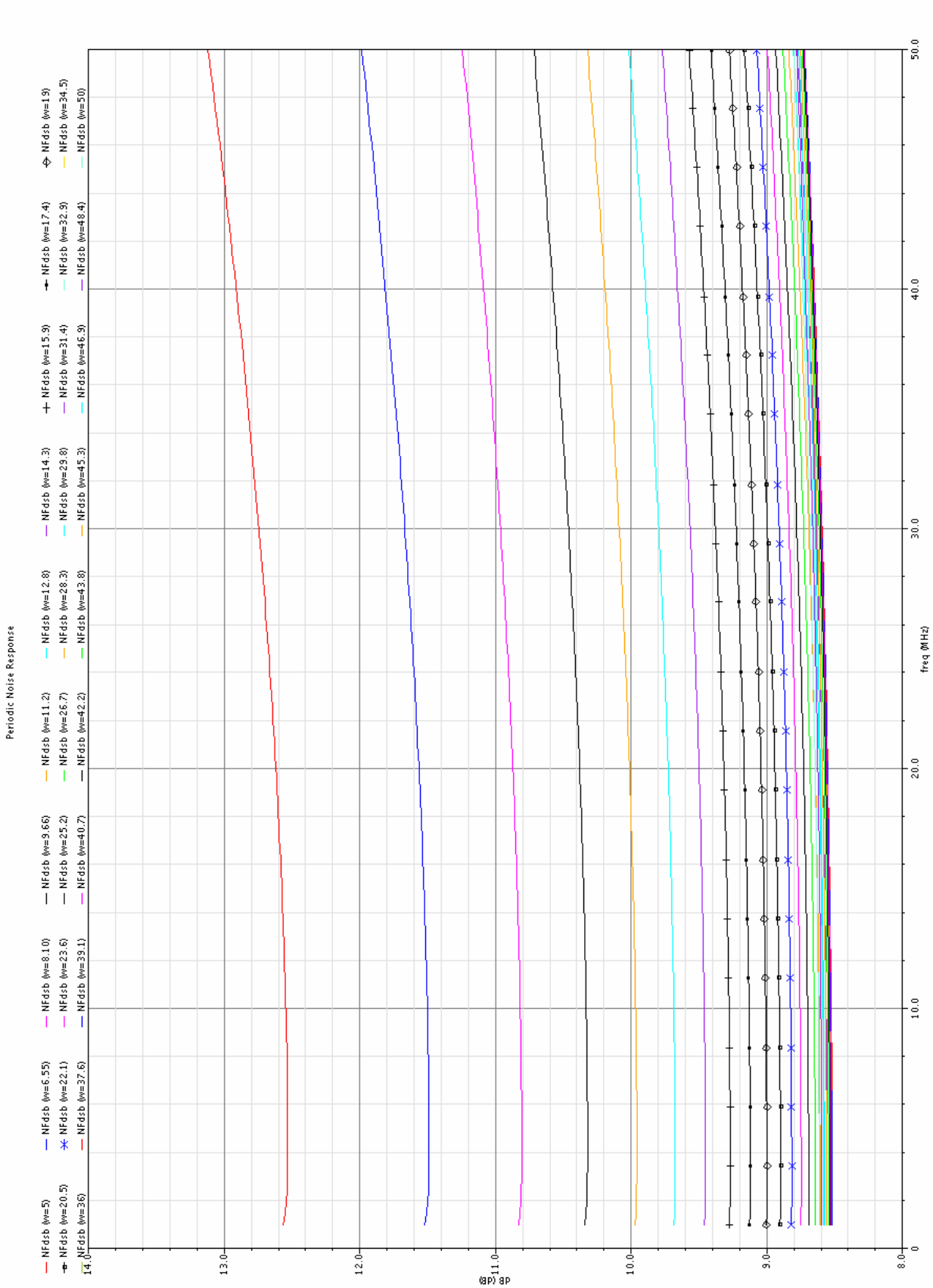

Figure 5.19: Double sideband noise figure (NFdsb) for different transistor width w (μm)

5.4.1 Simulation results

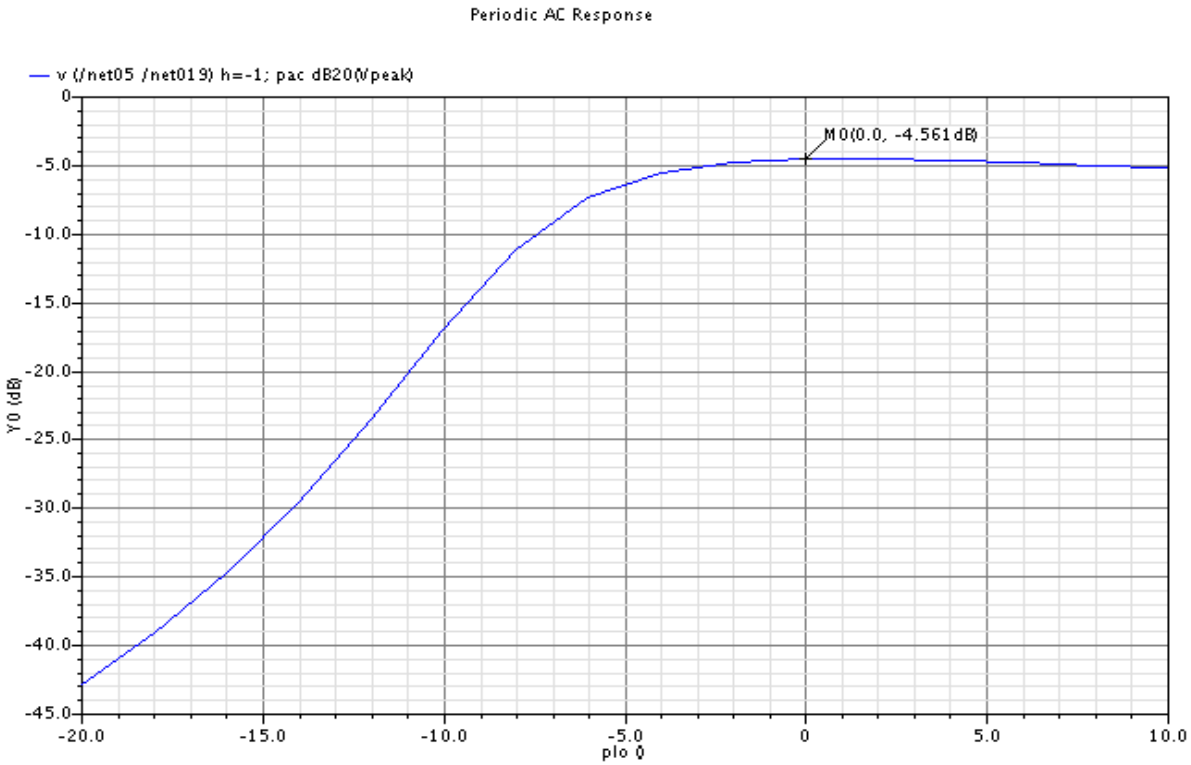

Figure 5.20: Conversion gain versus LO power (dBm)

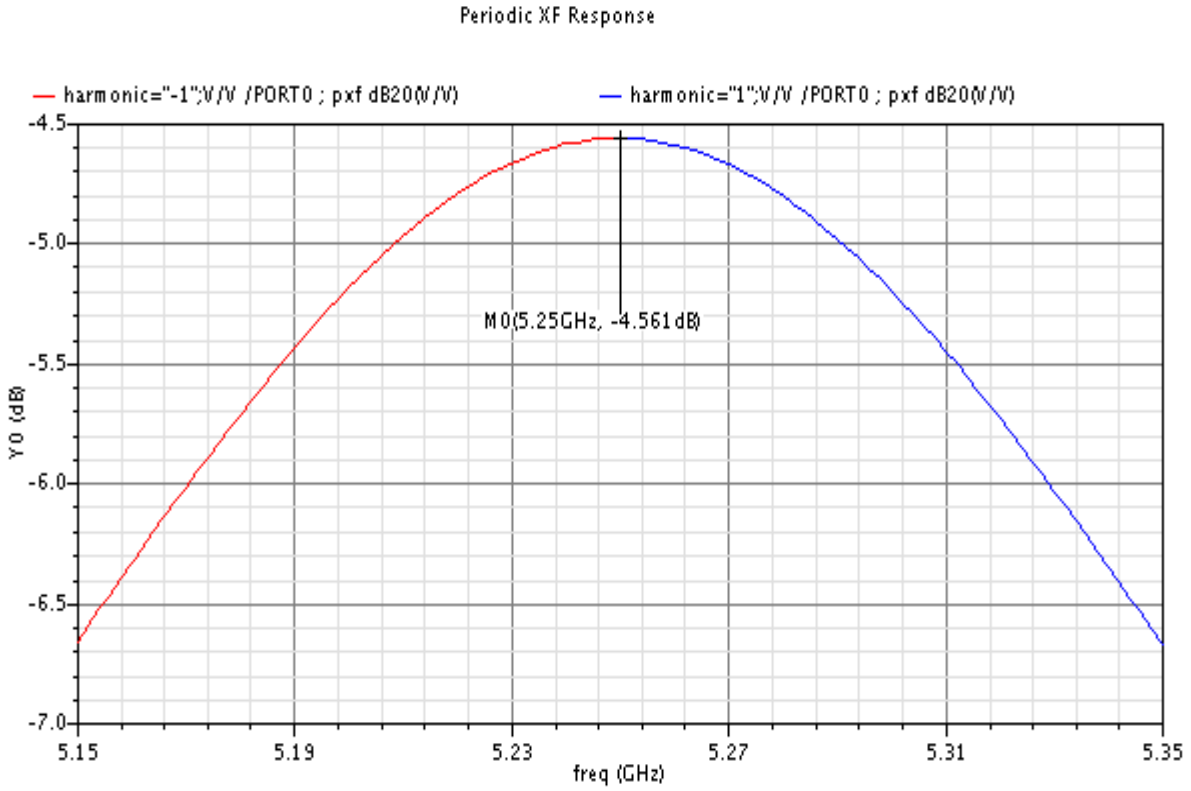

Figure 5.21: Conversion gain versus RF frequency

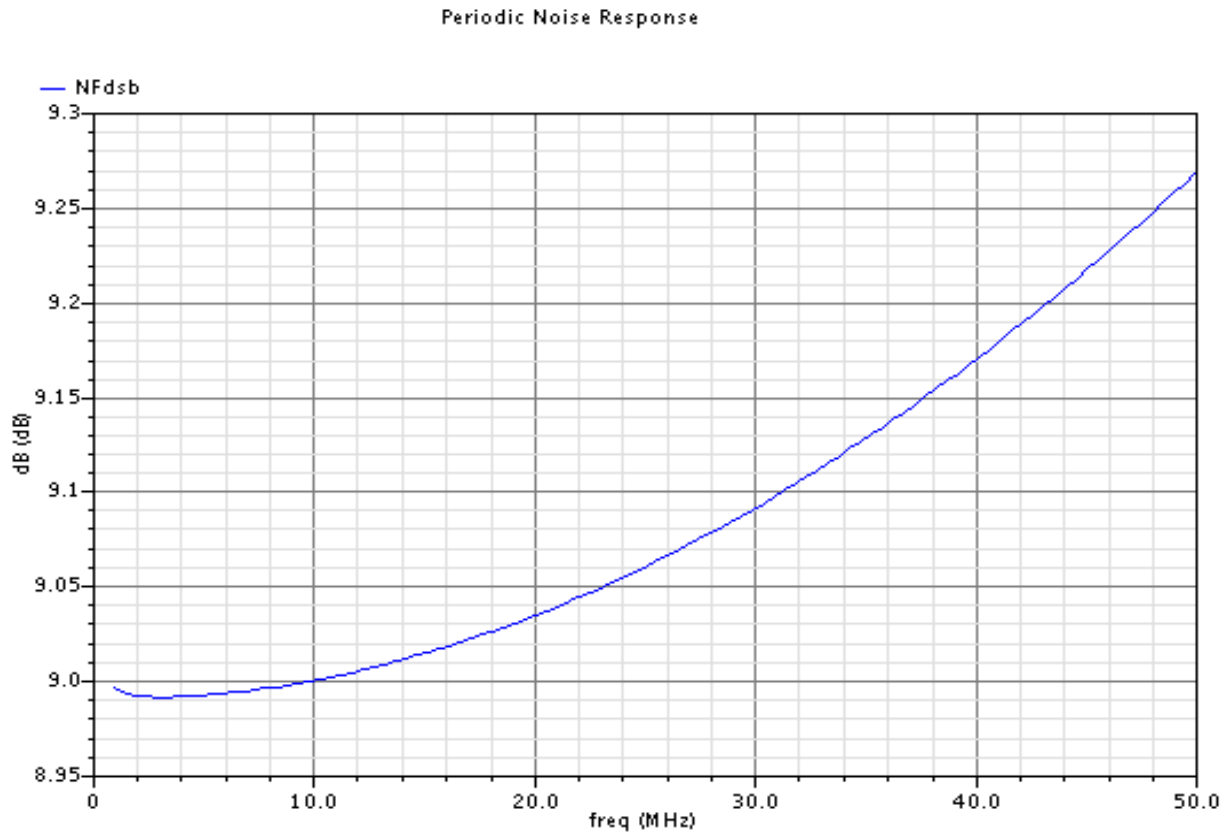

Figure 5.22: Double sideband noise figure, NF_{dsb}

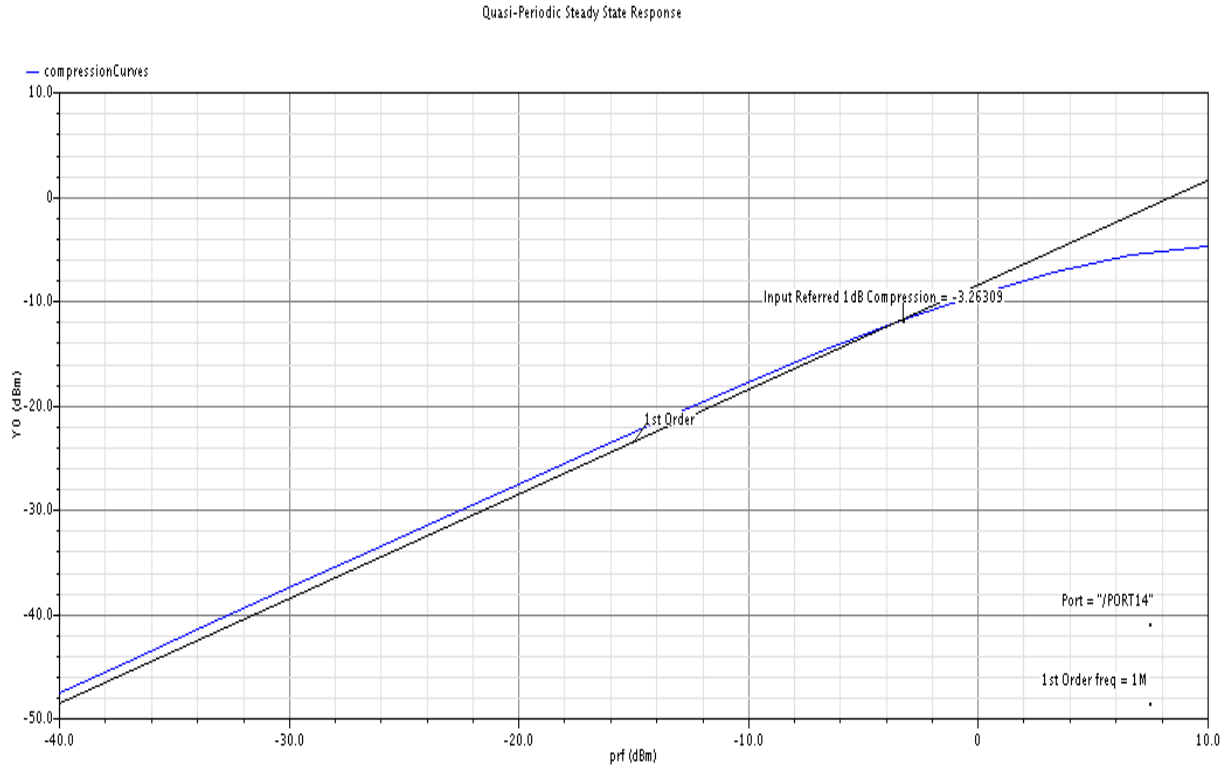

Figure 5.23: 1-dB compression point, P1dB

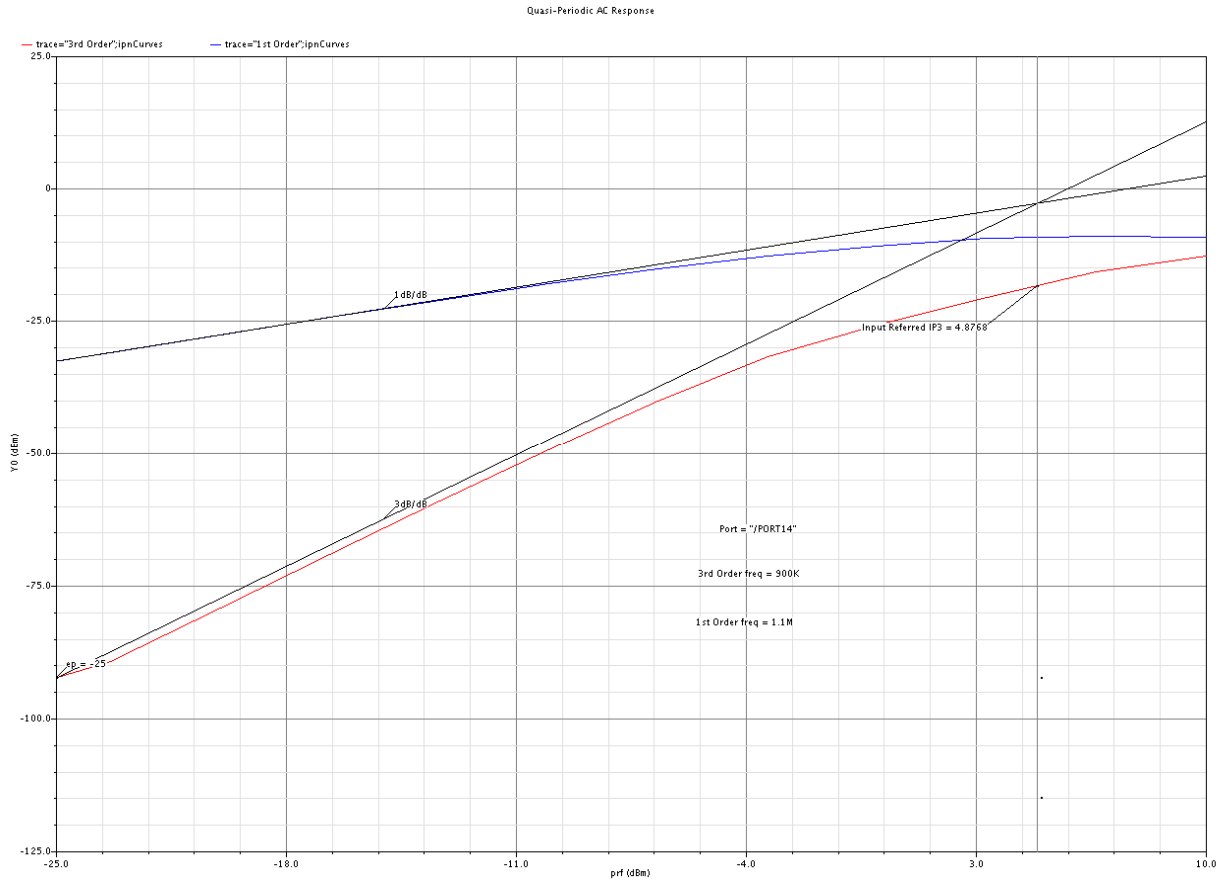

Figure 5.24: Input referred third-order intercept point, IIP3

Parameter	Value
Conversion gain	-4.5dB
Double sideband noise figure NF_{dsb} *(1MHz-20MHz average)*	≈ 9dB
P1dB	-3.3dBm
IIP3	4.8dBm
DC power consumption	0
Power supply	0

Table 5.6: Performance summary of the mixer

5.5 Front-End Integration

In the preceding sections each part of the proposed receiver front-end illustrated in figure 5.25 has been simulated separately and results were presented. However to evaluate and compare the performance of the receiver to our target requirements presented in section 5.2 we need to simulate the complete front end as well.

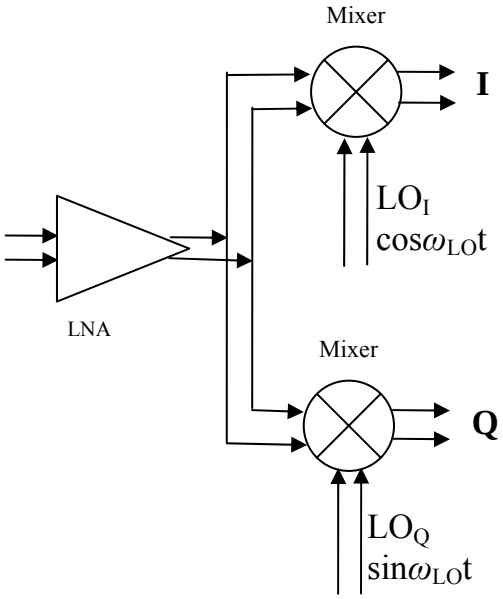

Figure 5.25: Part of the receiver to be implemented

As the mixer presented in section 5.4 is based on balanced topology the LNA presented in section 5.3 needs to be set-up in differential configuration as illustrated in figure 5.26.

The mixers receives a differential input from the LNA and drives estimated 3pF loads which represent the capacitive input of the baseband amplifier stage.

The lower path mixer functions only as a dummy load to the LNA. All simulations are performed on the upper path mixer.

The value of capacitor C_{ex} has been adjusted according to the capacitive load that mixers present to the LNA to keep the resonance frequency at 5.25GHz for the LC tank consist of L_d, C_{ex}, C_L and parasitic capacitances.

The value of resistors R (ref. figure 5.17) has been adjusted to provide correct impedance between LNA and mixers.

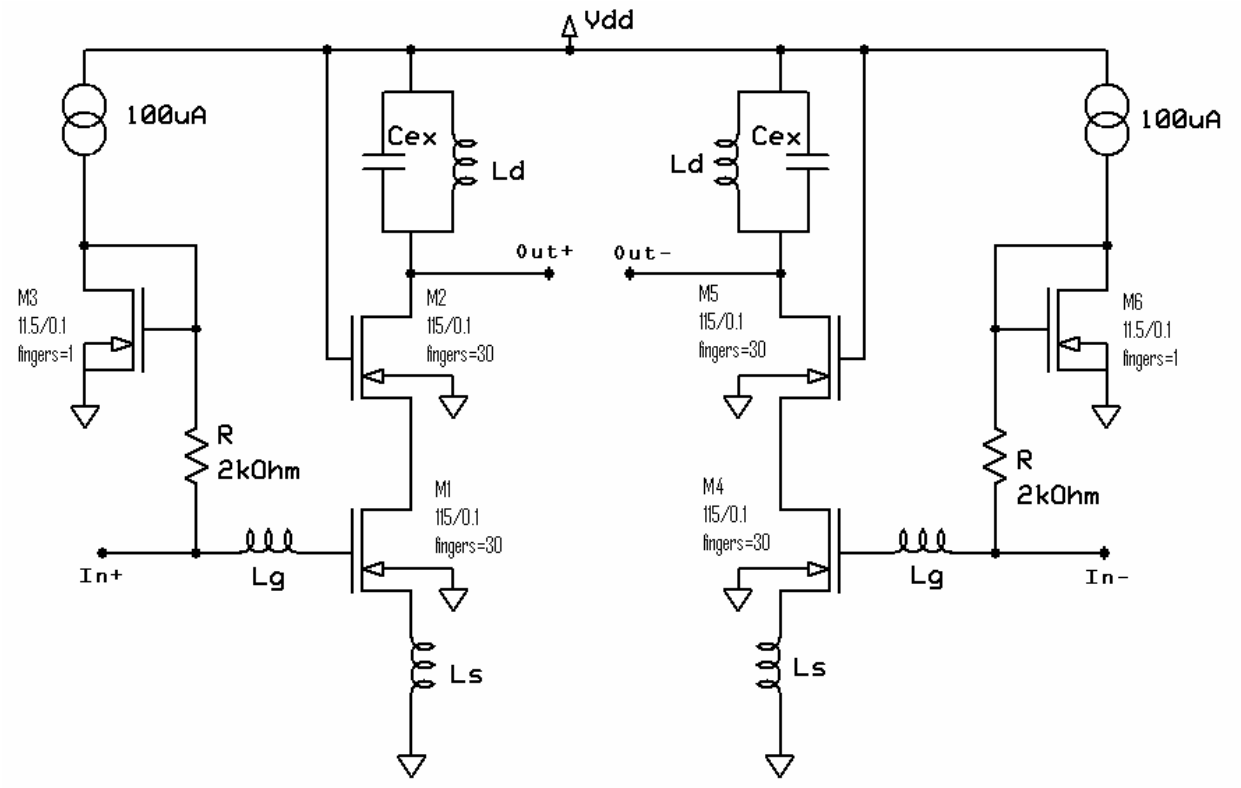

Figure 5.26: Differential LNA

The completed zero-IF down-conversion receiver front end has been simulated and the simulation results obtained are presented in section 5.5.1 and discussed in section 5.5.2. The details schematic and test bench used in the simulations can be found in the appendix.

5.5.1 Simulation results

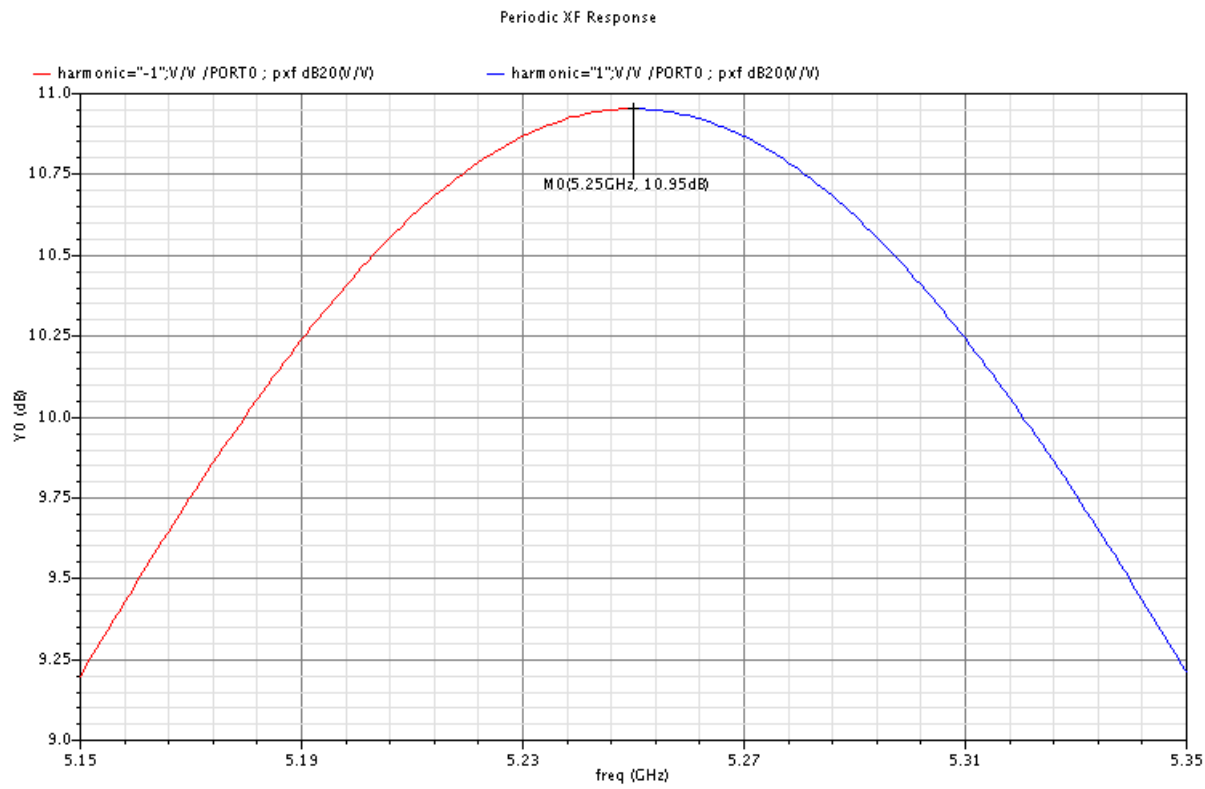

Figure 5.27: Conversion gain versus RF frequency for the front-end

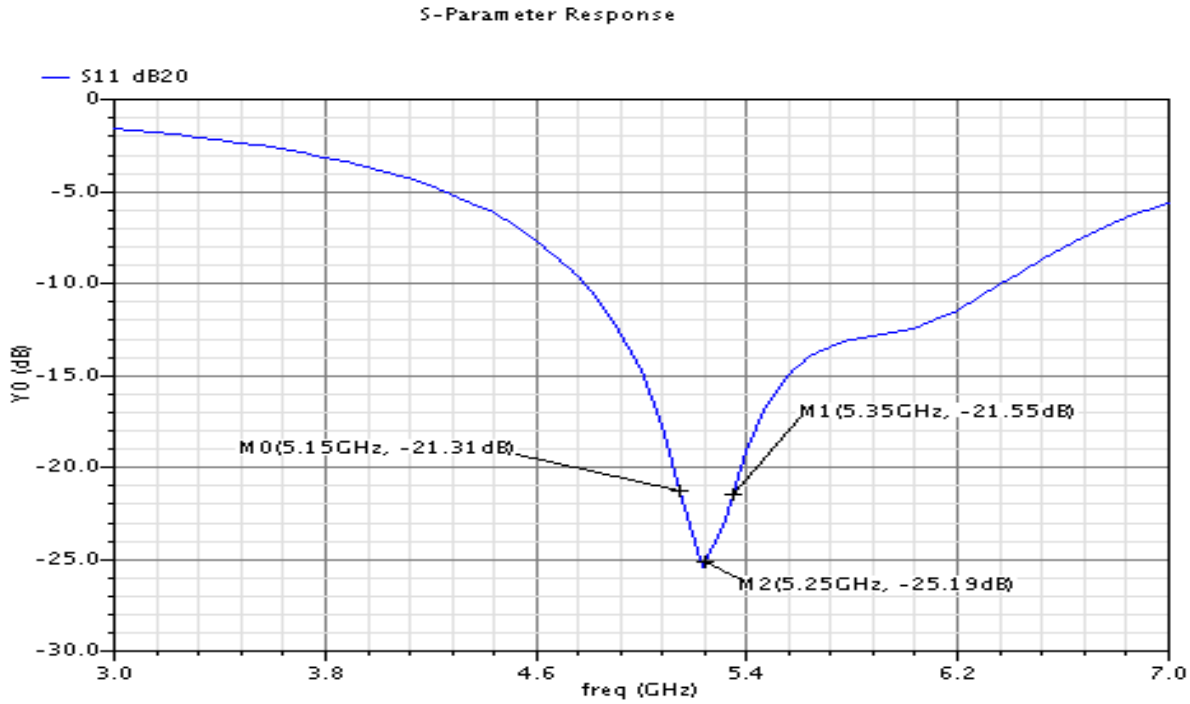

Figure 5.28: Front-end input characteristic match, S11

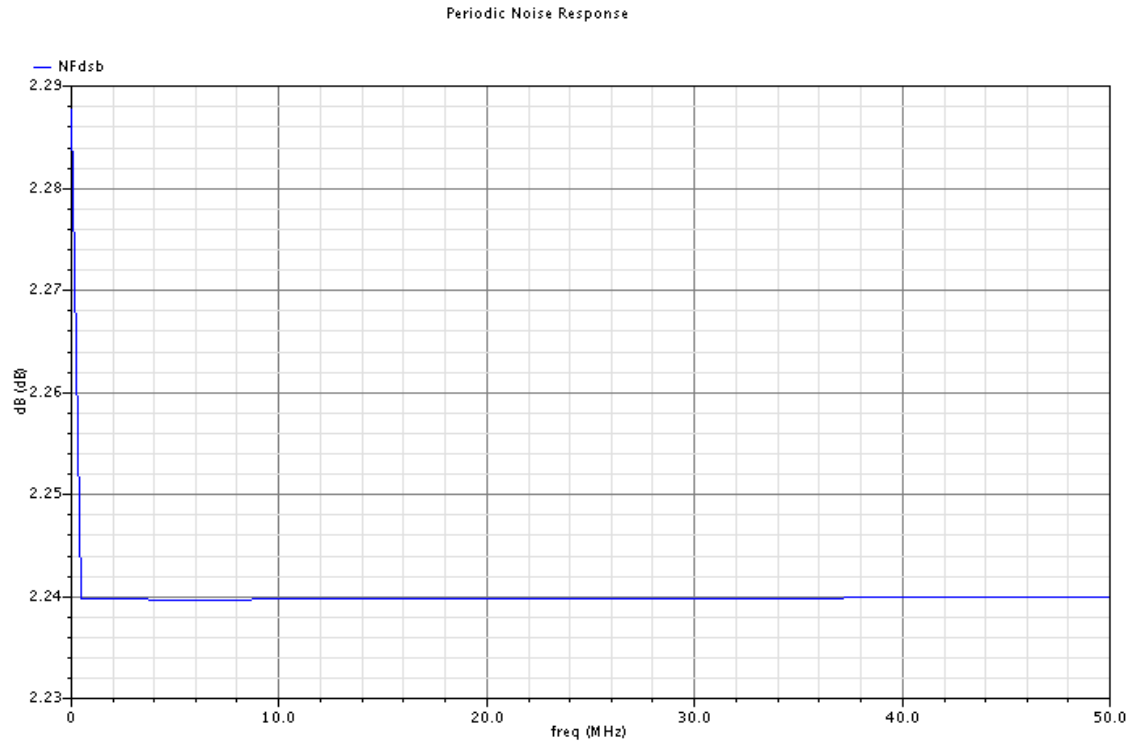

Figure 5.29: Double sideband noise figure, NF_{dsb} 1kHz-50MHz

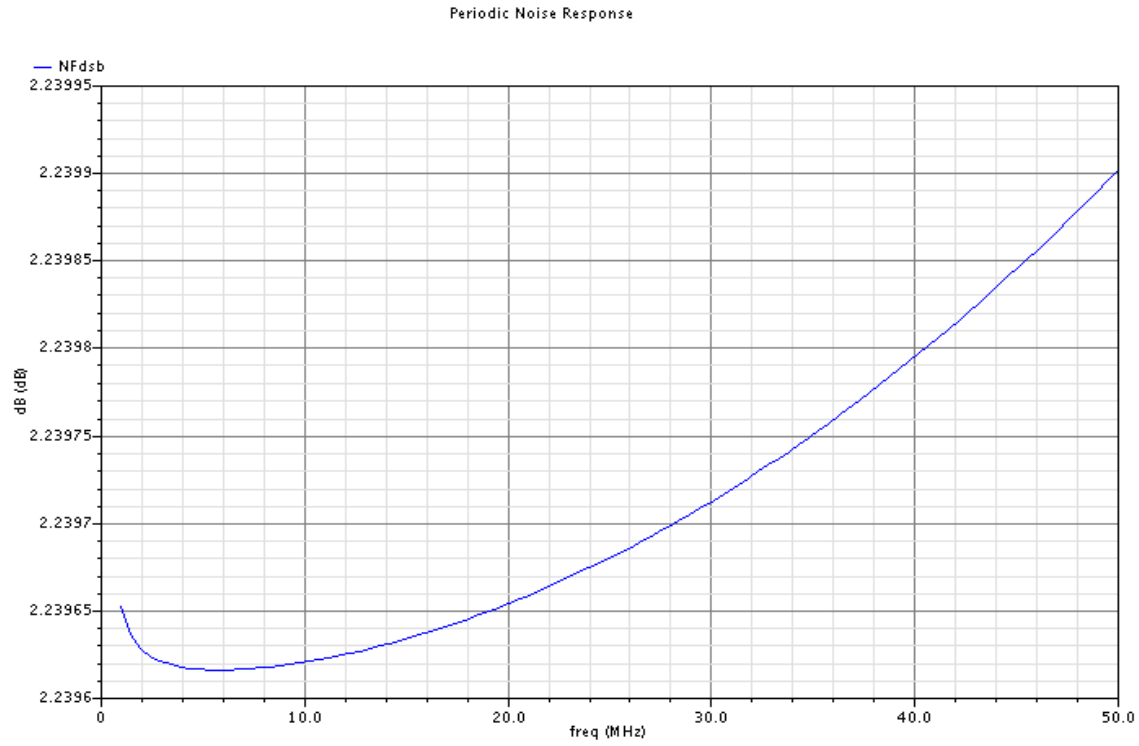

Figure 5.30: Double sideband noise figure, NF_{dsb} 1MHz-50MHz

Figure 5.31: 1-dB compression point of the front-end, P1dB

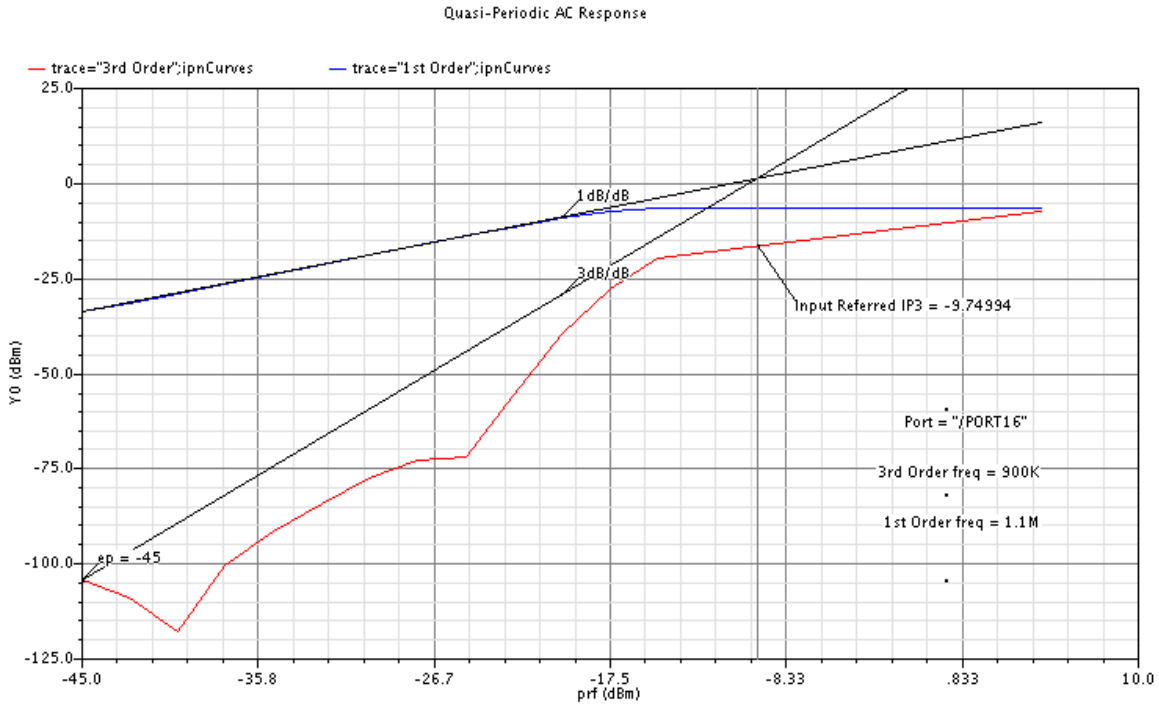

Figure 5.32: Input referred third-order intercept point, IIP3

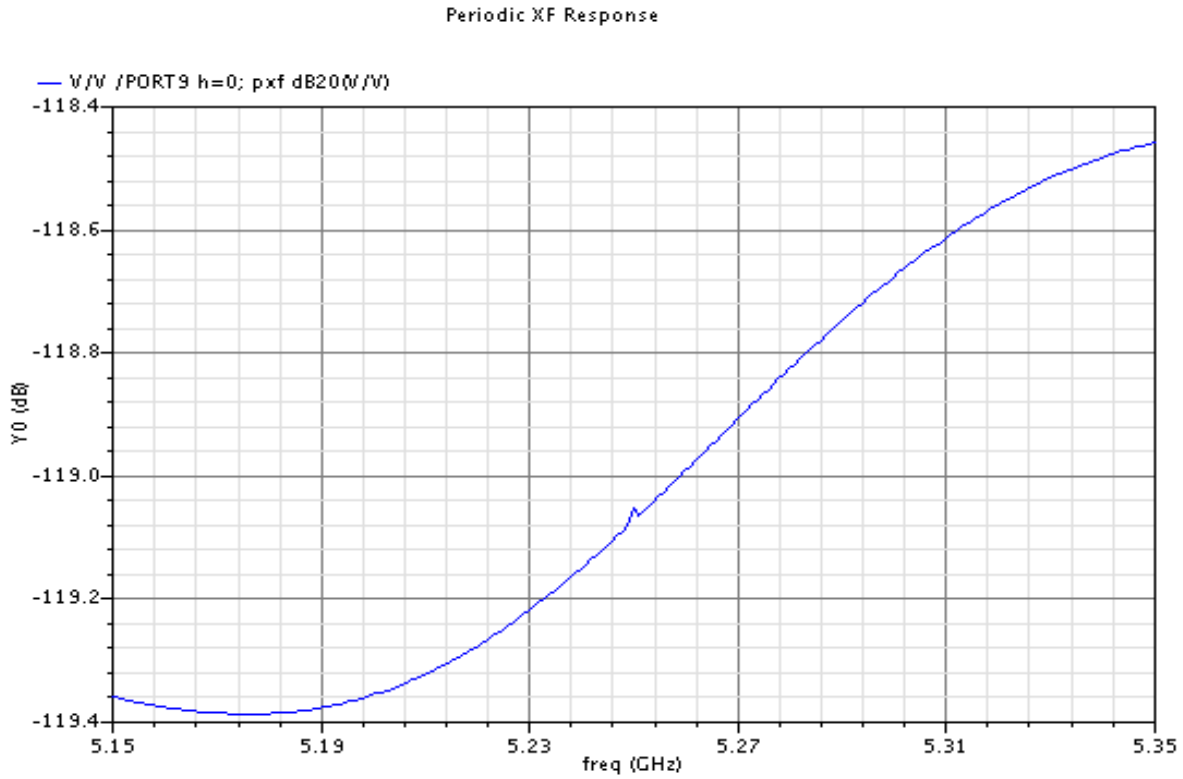

Figure 5.33: LO-to-IF feedthrough

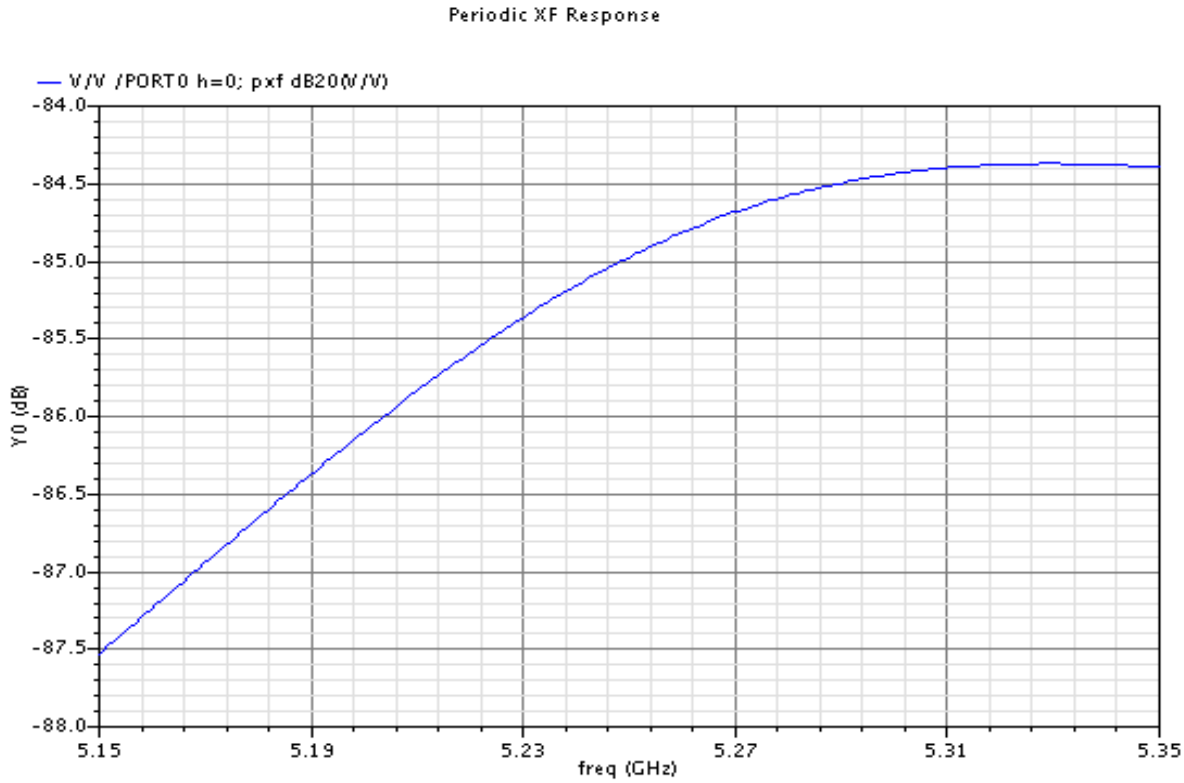

Figure 5.34: LO-to-RF feedthrough

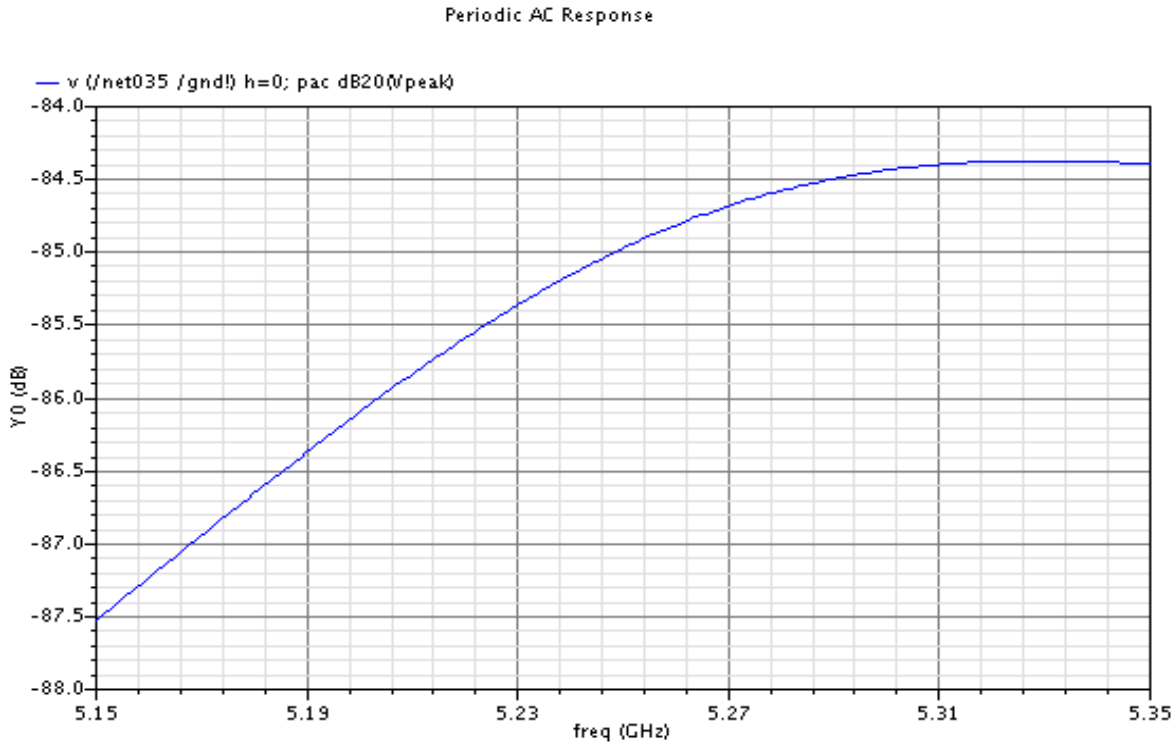

Figure 5.35: RF-to-IF feedthrough

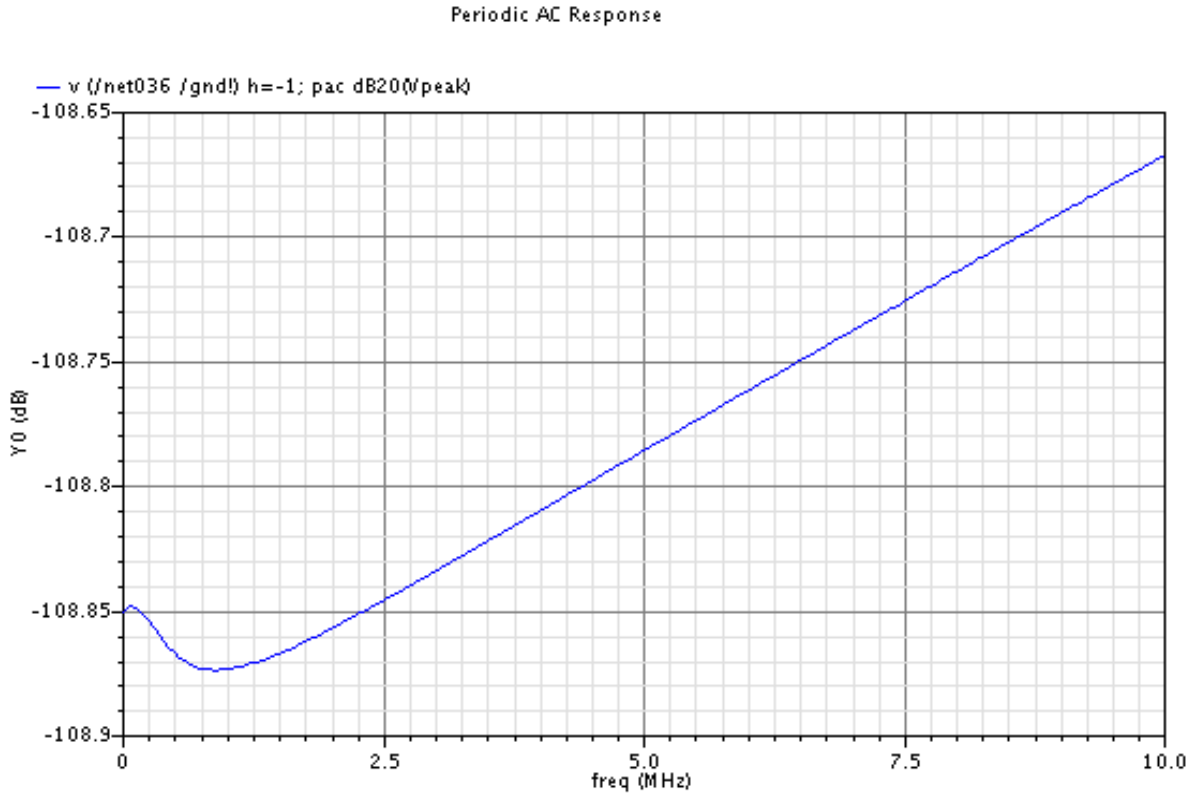

Figure 5.36: RF-to-LO feedthrough

5.5.2 Summary

When summarized, the simulation result presented in 5.4.1 gives a set of final results for the front-end as shown in table 5.7.

Parameter	Value	Target
Conversion gain, S21 @ 5.25GHz	10.95dB	-
Double sideband noise figure NF_{dsb} (1MHz-20MHz average)	2.24dB	< 10dB
Input match, S11 @ 5.15-5.35GHz	< -20dB	-
P1dB	-15.1dBm	> -21dBm
IIP3	-9.7dBm	> -10dBm
LO-to-IF feedthrough @ 5.15-5.35GHz	< -118dB	-
LO-to-RF feedthrough @ 5.15-5.35GHz	< -84dB	-
RF-to-IF feedthrough @ 5.15-5.35GHz	< -84dB	-
RF-to-LO feedthrough @ 0-10MHz	< -108dB	-
Total DC power consumption	2.2mA/ 3.4mW	< 5mA/ 6mW
Power supply	1.2V	-

Table 5.7: Final simulation results for front-end

Conversion gain, shown in figure 5.27 gives a peak value of 10.95dB at 5.25GHz which are according to the expectation. The total gain is given in our case by equation 5.16.

$$G_{TOTAL} = G_{LNA} + G_{MIXER} \qquad (5.16)$$

The conversion gain varies with about 1.7dB within the 5.15-5.35GHz band. This variation is caused by mixer as the variation of the LNA is less than 0.17dB.

The input impedance match given by reflection coefficient S_{11} is given in figure 5.28. The value is better than -20dB in the band of interest, hence the LNA provides very good 50Ω input match. However, the match is very narrow, as expected for the inductively degenerated LNA.

The double sideband noise figure, NF_{dsb} for the front end is in average 2.25dB within the 1-20MHz range of the IF output. That is well below the target value of 10dB. Even so the noise figure of the mixer is about 9dB, it only contributes with about 1.3dB to the front-end total noise figure. That is according to the Friis formula (3.1) and (3.2). In the figure 5.29 a spike near DC can be

observed. This spike is cause by the 1/f noise mostly contributed by the LNA transistors.

The P1dB and IIP3 are both inside target requirements. The overall performance is mainly set by the performance of the LNA. An increase in the linearity of the LNA will unfortunately result in the increase of the power consumption, thus a compromise between power consumption and linearity must be made.

The feedthrough parameters (Port-to-Port isolation) are not specified as target requirements, but they are critical for the mixer to function properly. These parameters should be as high as possible to avoid unwanted mixer products. Good port-to-port isolation will help to reduce self-mixing and reradiation which are very important in especially 'Zero-IF' receivers.

The overall power consumption is low, thanks to the use of passive mixer. However, additional gain stages to compensate for the conversion loss of the mixer will be required in final design, thus increasing the overall power consumption.

5.6 References

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CHAPTER 6

6.1 Conclusion

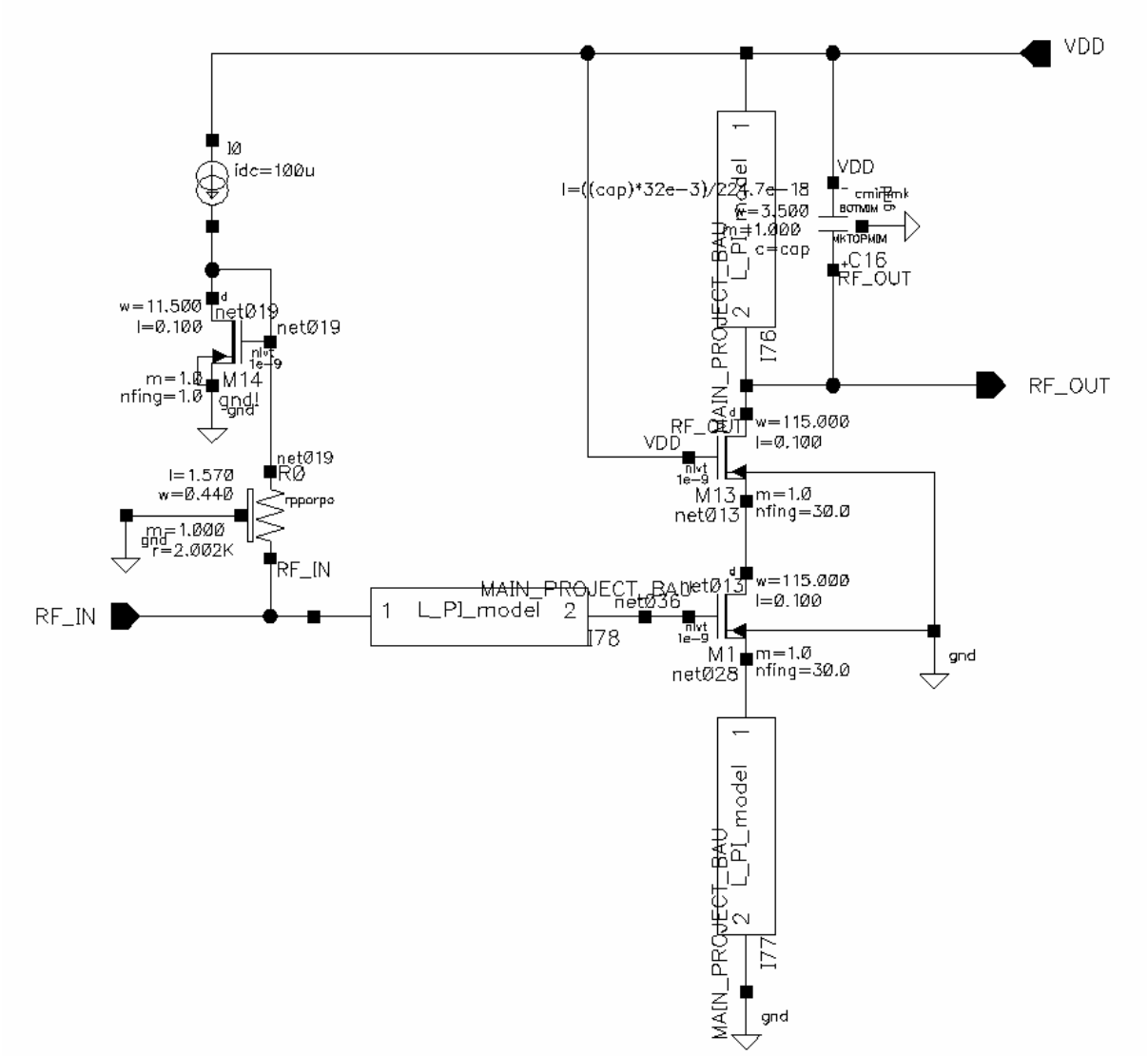
The main goal of this thesis has been to design an RF front-end compatible with IEEE 802.11a and HiperLAN/2 standards. The theoretical background and steps need to design such circuit are given in the foregone chapters. Finally, a receiver front-end consisting of a LNA and two mixes suitable for use in a 'Zero-IF' receiver has been designed and simulated. The results obtained satisfy the target requirements for operation under both IEEE 802.11a and HiperLAN/2 standard.

6.2 Further work

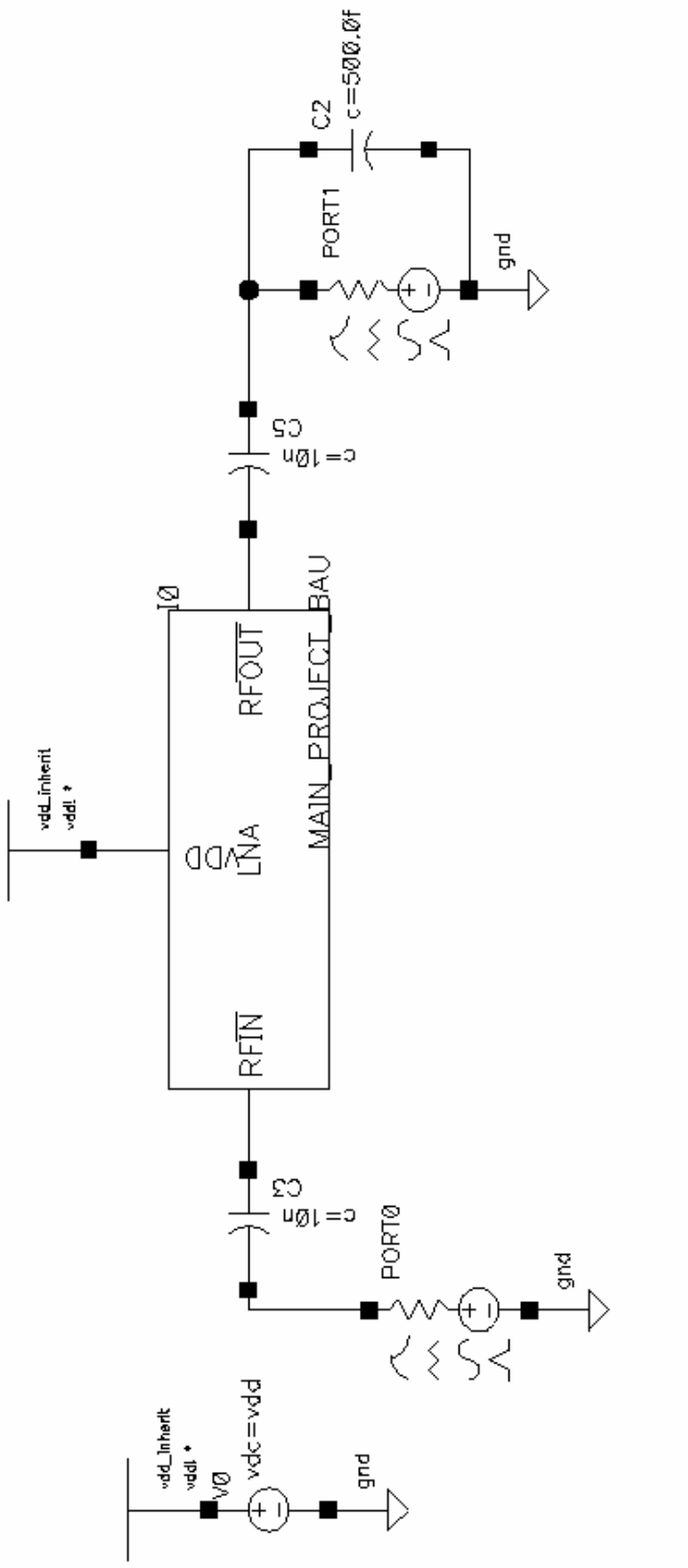
The design of the front-end is still not optimal and has a room for improvements before it can be implemented in silicon. Further work would include:

- Replacing the component models with more accurate RF models. However, RF library has not been made available for me at the time of my work.
- Adding and simulating package parasitics.
- Substituting whole or part of the on-chip inductors with bondwires.
- Adding and simulating ESD protection.
- Simulating mismatch in nominally matched pairs.
- Simulating the front-end with OFDM signals.

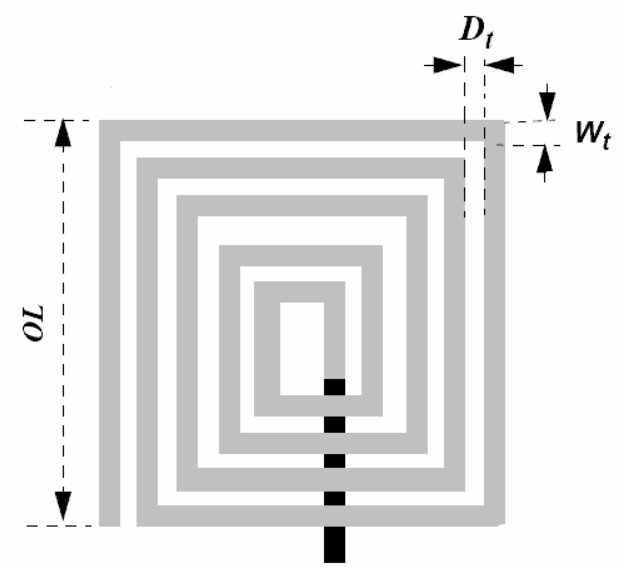
APPENDIX



Appendix 1: Schematic of LNA



Appendix 2: Test bench for LNA simulation



Appendix 3: Square type on-chip inductor

L_g, target inductance 5.5nH, result DC inductance 5.55nH	
width (OL) = 200μm, metal width (W_t) = 10μm, distance between metal (D_t) = 1.5μm, turns = 5.5	
L = 4.64nH	R=8.014Ω
C_{s1} = 96.86fF	R_{s1} = 5.191Ω
C_{s2} = 89.83fF	R_{s2} = 9.644Ω
Q ≈ 8.5	

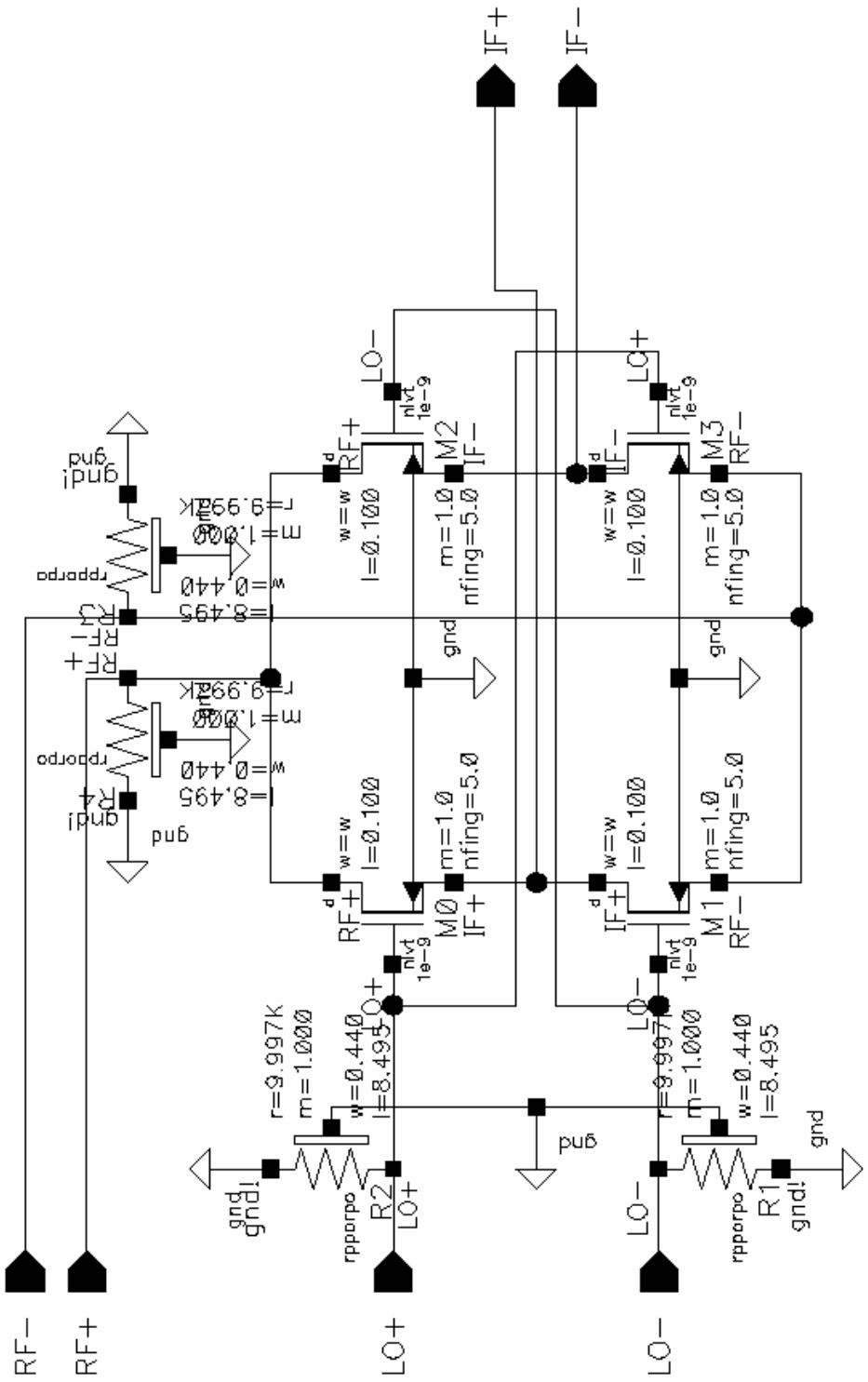
Appendix 4: Model parameters for on-chip inductor L_g

L_s, target inductance 0.7nH, result DC inductance 0.73nH	
width (OL) = 100μm, metal width (W_t) = 10μm, distance between metal (D_t) = 1.5μm, turns = 2.75	
L = 702.3pH	R=2.64Ω
C_{s1} = 25.44fF	R_{s1} = 4.17Ω
C_{s2} = 22.93fF	R_{s2} = 30.93Ω
Q ≈ 8.6	

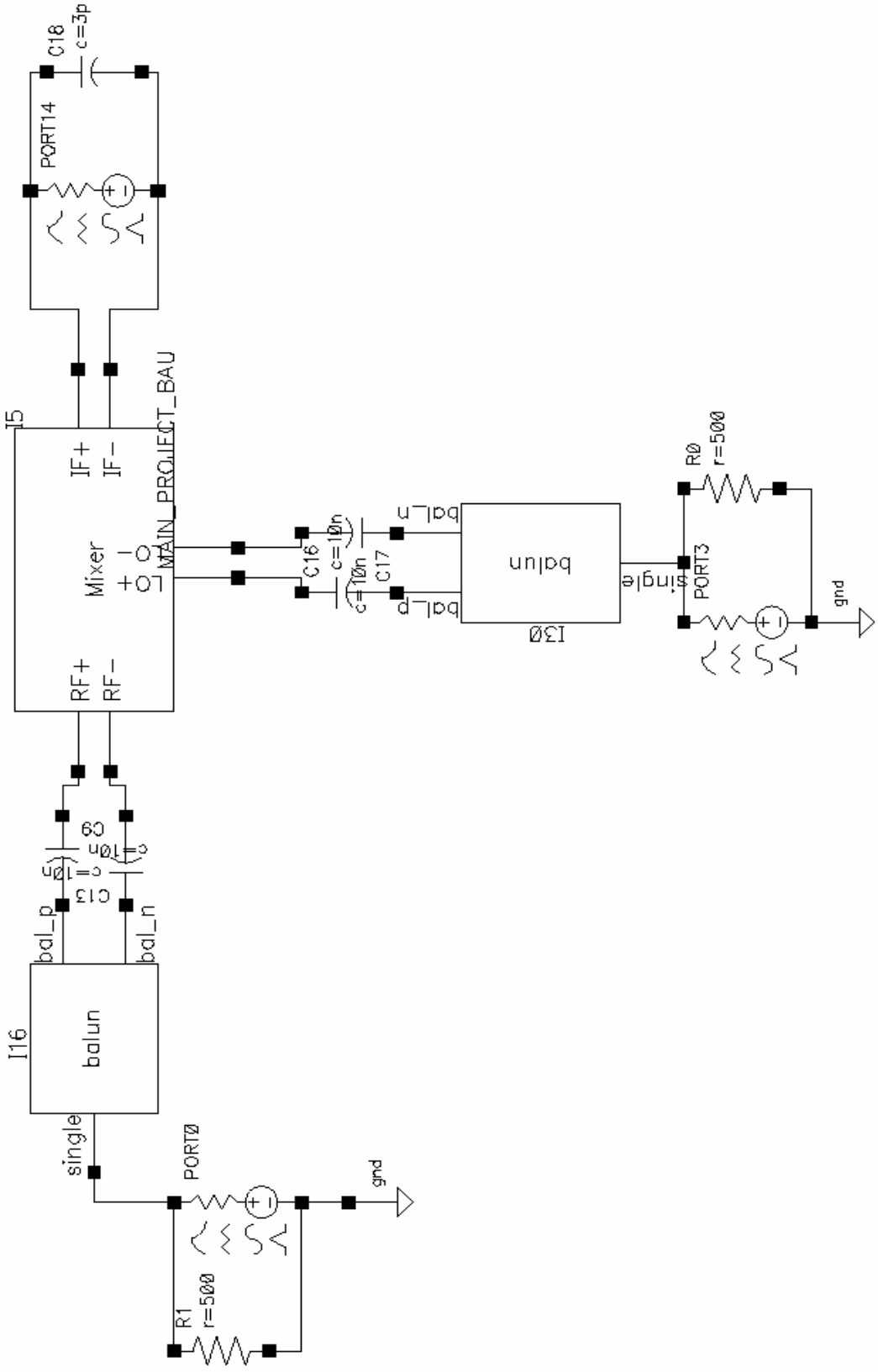
Appendix 5: Model parameters for on-chip inductor L_s

L_d, target inductance 1.3nH, result DC inductance 1.3nH	
width (OL) = 140μm, metal width (W_t) = 10μm, distance between metal (D_t) = 1.5μm, turns = 2.5	
L = 1.264nH	R=3.383Ω
C_{s1} = 37.23fF	R_{s1} = 5.661Ω
C_{s2} = 34.48fF	R_{s2} = 17.35Ω
Q ≈ 11.5	

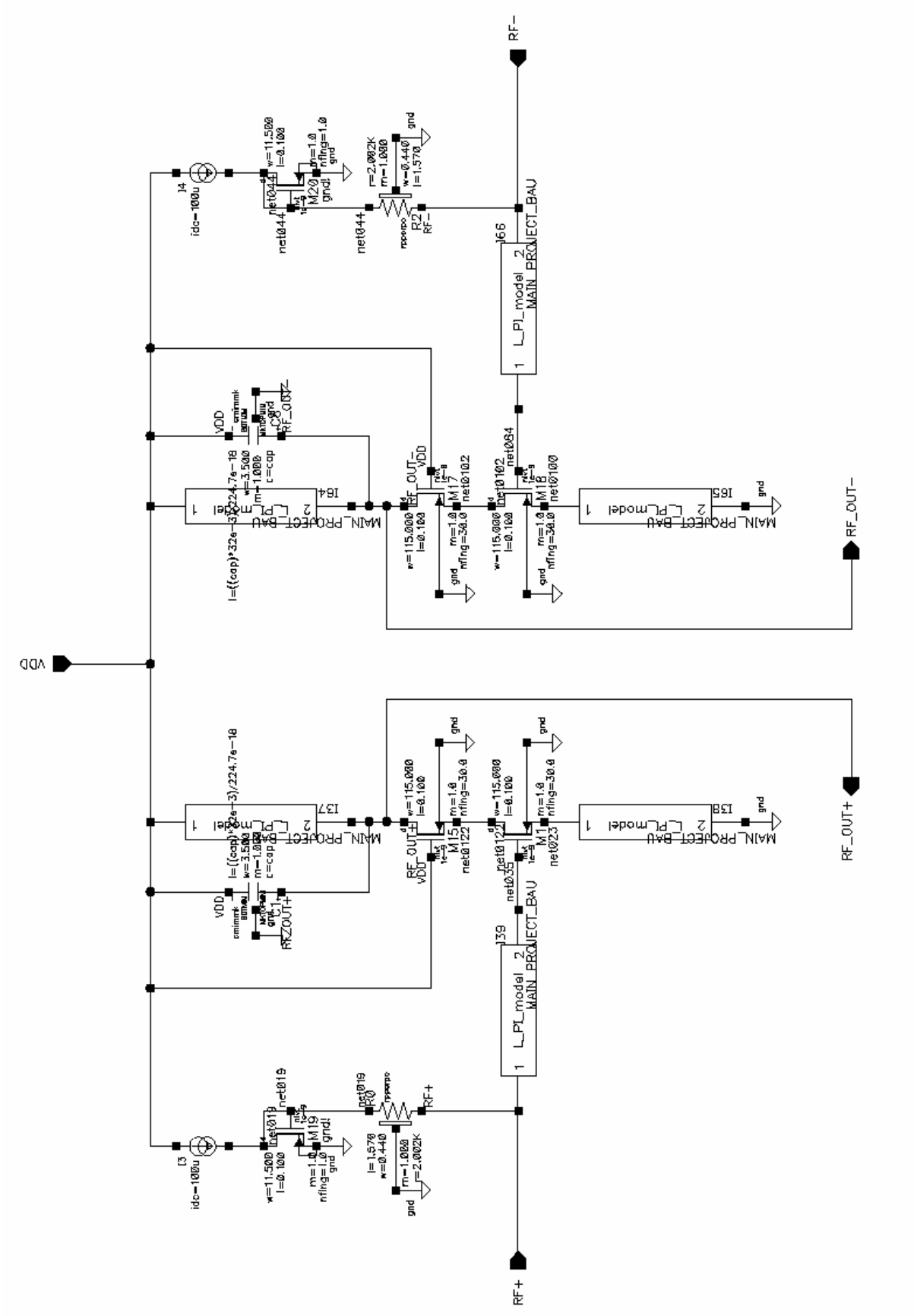
Appendix 6: Model parameters for on-chip inductor L_d



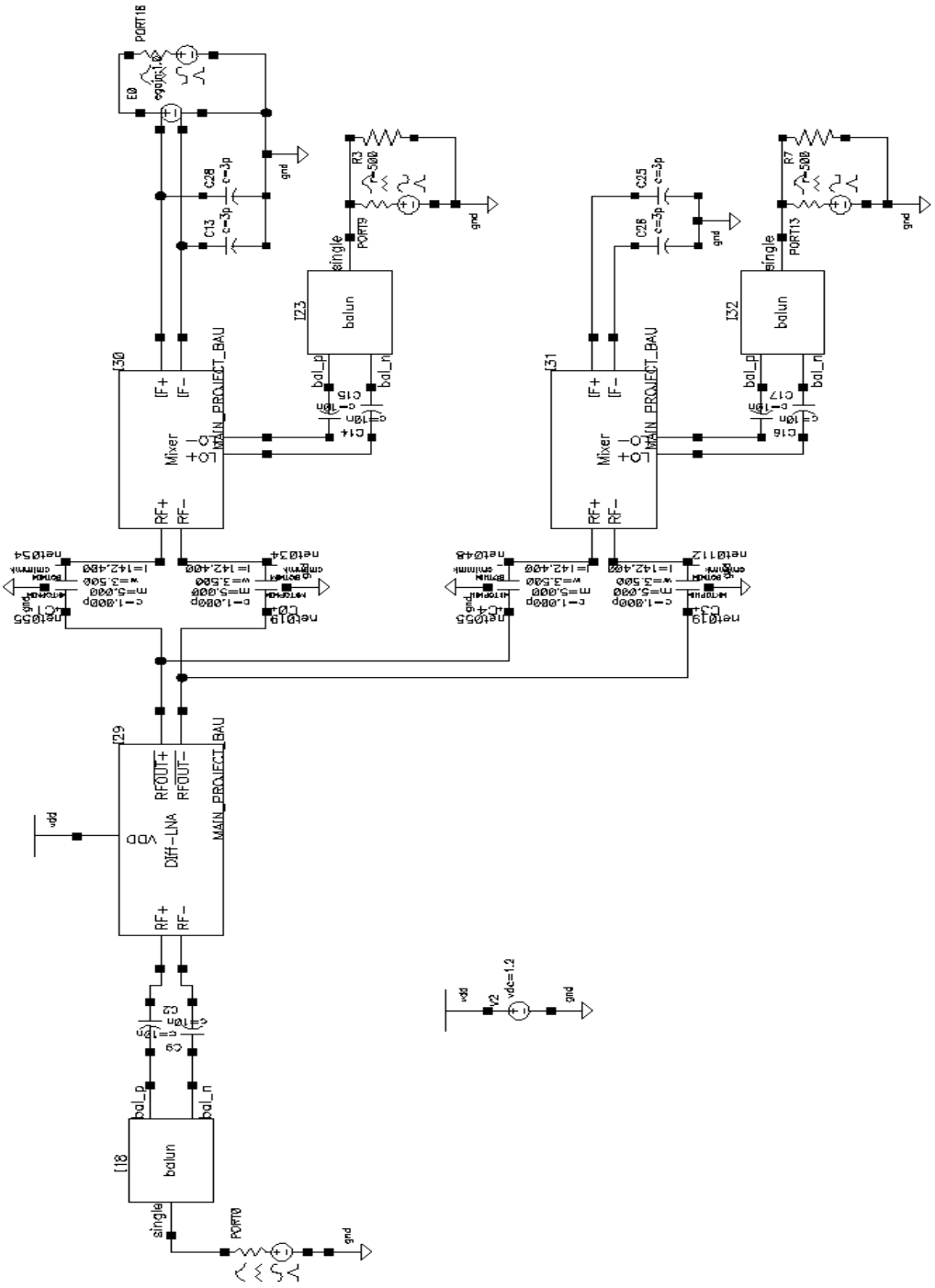
Appendix 7: Schematic of the mixer



Appendix 8: Test bench for simulation of mixer



Appendix 9: Schematic of differential configured LNA



Appendix 10: Test bench for simulation of the completed front-end