Parasitic’ Photo Diodes in General Purpose 180nm CMOS

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Abstract

Modern CMOS image sensor (CIS) are realized in highly specialized semiconductor production processes that provide microscopic photo pixels allowing extremely high-quality photo-sensing. However, these production processes are generally a well-guarded secret, costly, and not easily available for academic research groups. Thus, for some time a general-purpose CMOS process has been used to make experimental image sensors. This is possible because basically any PN-diode on a CMOS chip is sensitive to light and can be repurposed as a light sensor.

When working with analog circuits in common design software like Cadence, the multidimensional aspect is missing in the design process. Designers have no control over depths of the different implants, and the doping gradient is “hidden” from the designers in fabrication process parameters and in the world of TCAD tools. When it comes to photodiodes, the depths, and the concentration doping in the p-n junctions are critical for performance and limitations. It is therefore important to have an understanding and simulate these behaviors.

The goal of this project is to characterize candidates for ’parasitic’ photodiodes in the general purpose TSMC 180nm CMOS process that our group has access to, for a reasonable cost and production time cycle. The project was extended to not just characterize photodiodes, but also to build an PD 2D array, i.e., image sensor with the use of the photodiode candidates simulated in TCAD. FPGA control signal generation for the image sensor and Interfacing was done together with Emil Hultin, with his thesis project on test setups for future image sensors using the Digilent Nexys Video Artix-7 Development Board.

This thesis includes designs and TCAD simulations of photo-pixel variants, schematic and layout of pixel array, row/column decoders, readout circuitry, before a tape-out is made and design is sent for fabrication. Circuit boards were designed and produced to be used for supplying the chip with power and connecting pins to connectors for testing. A lens mount was 3D printed to fit the circuit boards.
Due to over three months production delays, the finished image sensor was not delivered in time for performing measurements. Some quick surface validation work was done when the chip arrived under a week before deadline. The finished Image sensor was supposed to be tested for noise, sensitivity, linearity and comparing the quality of the photodiode variants.

The image sensor's control signals were to be generated by a FPGA that also samples, analog to digital converting and stores the values from the sensor.

Future projects will benefit from finding one or several good photodiode solutions that can be used in different image sensor applications based on specification needs.

Preface

The work of this thesis and project has been done to complete my M.Sc. Degree in Microelectronics and sensor technology at the University of Oslo. During this project I have had a great opportunity to learn and get some hands-on experience working with the steps of designing, simulating, and producing an integrated circuit combined with digging deep into the world of TCAD simulations for the photodiodes. Debugging and analyzing has been present throughout this whole project.

The project started in the spring 2021 and is concluding in the fall 2022.
I want to thank my supervisors Philipp Dominik Häfliger and Johannes Sølhusvik for guiding me and keeping me on the right track throughout this project and connecting me to people with the right knowledge when I needed assistance. Also, thanks to Emil Hultin for working together on the FPGA part of this project even though we did not have time to test our systems together for now due to the substantial chip delay.

Abbreviations

TCAD	Technology Computer Aided Design
FPGA	Field-programmable gate array
CMOS	Complementary Metal Oxide Semiconductor
CIS	CMOS Image Sensor
TSMC	Taiwan Semiconductor Manufacturing Company
PD	Photodiode
QE	Quantum Efficiency
FWC	Full Well Capacity
CCD	Charge-coupled device
ADC	Analog to Digital Converter
CFA	Color Filter Array
FPN	Fixed Pattern Noise
BLC	Black level subtraction
CDS	Correlated Double Sampling
DDS	Differential Delta Sampling
GUI	Graphical User Interface
SWB	Sentaurus workbench
SDE	Structure generation
Sprocess	Sentaurus Process
Sdevice	Sentaurus Device
Svisual	Sentaurus Visual
NMOS	N-channel metal-oxide semiconductor
PMOS	P-channel metal–oxide–semiconductor
EQE	External Quantum Efficiency
DRC	Design Rule Check
LVS	Layout Versus Schematic
PCB	Printed Circuit Board
SMD	Surface Mount Device
IMEC	Interuniversity Microelectronics Center
M.O.D	Minimum distance to the object
VDMA	Video Direct Memory Access

List of figures

Figure 1 PN-junction with depletion region 13
Figure 2 Cross-section NMOS PMOS 13
Figure 3 Micro lens array of photodiode 15
Figure 4 SWB Tools 18
Figure 5 180nm PMOS and NMOS Transistor TCAD 21
Figure 6 Photodiode variants 22
Figure 7 Depletion Region PD1 24
Figure 8 Depletion Region PD2 24
Figure 9 Depletion Region PD3 24
Figure 10 Depletion Region PD4 25
Figure 11 Breakdown voltage PD1 26
Figure 12 Breakdown voltage PD2 26
Figure 13 Breakdown voltage PD3 26
Figure 14 Breakdown voltage PD4 27
Figure 15 Applied voltage, Electric field distribution 27
Figure 16 Light IV curves 29
Figure 17 Dark IV curves 30
Figure 18 PD2 Dark IV curves, 323kelvin 30
Figure 19 Current Density and Current flow lines PD1 32
Figure 20 Current Density and Current flow lines PD2 33
Figure 21 Current Density and Current flow lines PD3 33
Figure 22 Current Density and Current flow lines PD4 33
Figure 23 6µm and 60µm substrate 35
Figure 24 Reflectance Spectra 6µm substrate 35
Figure 25 Reflectance Spectra 180µm substrate 36
Figure 26 Energy Band Diagram 38
Figure 27 Top level design Image sensor 39
Figure 28 3T pixel 40
Figure 29 a,1 to 2 demultiplexer implemented using NAND b,1 to 2 demultiplexer implemented using NOR 41
Figure 30 4-bit demultiplexer 42
Figure 31 Schematic current source 43
Figure 32 Voltage readout path 44
Figure 33 Input output readout path linearity 44
Figure 34 Pixel layout PD1&PD2 46
Figure 35 Pixel layout PD3&PD4 46
Figure 36 Photodiode variants reminder 47
Figure 37 Pixel array layout 48
Figure 38 Column decoder layout 48
Figure 39 NOR AND NAND gate demux variant layout 49
Figure 40 NOR gate demultiplexer variant layout 49
Figure 41 NAND gate demultiplexer variant layout 50
Figure 42 Inverters for select signal layout 50
Figure 43 Full column amplifier layout 50
Figure 44 Column amplifier layout 51

Figure 45 Column amplifier and output current source layout ... 52
Figure 46 Test pixel layout ... 52
Figure 47 Full chip layout ... 53
Figure 48 Design in focus layout ... 54
Figure 49 Bonding diagram ... 55
Figure 50 Second PCB schematic ... 57
Figure 51 Image sensor symbol ... 58
Figure 52 Assembled PCBs ... 59
Figure 53 Second PCB layout ... 60
Figure 54 Power layer layout ... 61
Figure 55 Ground layer layout ... 61
Figure 56 Lens mount design ... 63
Figure 57 FPGA Frame buffering flow ... 63
Figure 58 Bonding IC ... 66
Figure 59 Fabricated IC ... 66
Figure 60 Fabricated IC close up ... 67

List of tables

Table 1 Estimated doping profiles 21
Table 2 Values light simulation 2V reverse bias, 293kelvin 31
Table 3 Reverse resistance of zero biased photodiodes 37
Table 4 Pixel transistor dimensions 40
Table 5 Dimensions column amplifier transistors 43
Table 6 Image sensor pin location 58
Table 7 Lens parameters 62

Contents

Abstract

Preface

Abbreviations

List of Figures

List of Tables

I Theoretical background 12
1.1 Photodiodes 12
1.1.1 MOSFET 13
1.1.2 CMOS Structures 14
1.1.3 Quantum efficiency 14
1.2 Image Sensor 15
1.3 Pixels 16
1.4 Noise 16
1.4.1 Fixed pattern noise 16
1.4.2 Temporal noise 17
1.5 Sample and hold 17
1.6 TCAD - Sentaurus Workbench 17
1.6.1 TCAD tools 18
II Design 20
2.1 TCAD - Photodiodes 20
2.1.1 Estimating process parameters of TSMC 180nm 20
2.1.2 Photodiode Structures 21
2.1.3 Simulations 23
2.1.3.1 Punch-through 23
2.1.3.2 Breakdown voltage 25
2.1.3.3 I-V characteristics 27
2.1.3.4 Light IV 28
2.1.3.5 Dark current 29
2.1.3.6 Current density 31

2.1.3.7 Absorbance, transmittance, and reflectance 34
2.1.3.8 Reverse resistance 36
2.1.3.9 Bandgap energy 37
2.2 Cadence 180nm Design and Implementation 38
2.1 Pixel 39
2.2 Decoders 41
2.3 Column amplifier 42
2.4 Voltage readout path 43
III Layout 45
3.1 Pixels 45
3.2 Pixel array 47
3.3 Decoders 48
3.4 Column amplifier 50
3.5 Readout 51
3.6 Extra Testability 52
3.7 Pad Frame 53
3.8 Package 54
IV Printed circuit board 56
4.1 Schematic 56
4.2 Image sensor 57
4.3 PCB Layout 60
4.3.1 Power and ground layers 60
4.4 PCB assembling and Testing 62
4.5 Lens and lens mount 62
5.6 FPGA 63
4.7 Timing 64
V Testing 65
Future work / Improvements 68
Conclusion 70
Bibliography 71
Appendix 72
A1 Doping estimates 72
A2 SDE 72
A2.1 PD1 72
A2.2 PD2 73
A2.3 PD3 74

A2.4 PD4 75
A3 SDEVICE 76
A3.1 Parameter file 76
A3.2 Breakdownvoltage 77
A3.3 DepletionRegion 79
A3.4 Light simulation 79
A3.5 Current density 82
A4 SVISUAL 82
A4.1 Light and dark IV/Cathode applied voltage vs cathode total current 82
A4.2 Band diagram 82
A4.3 Current density 83
A4.4 Reflectance 84

I Theoretical background

1.1 Photodiodes

A photodiode (PD) is a semiconductor device with a PN junction that converts signal from the optical domain over to the electrical domain. During this process the electromagnetic radiation is what is converted into electrical current. When electromagnetic radiation is absorbed in a semiconductor material, it can generate electron-hole pairs. The electron-hole pair is generated when an electron has been moved into the conduction band from the valence band. The free electron is what contributes to the conductivity of the semiconductor. When generating an electron-hole pair, the energy level of an electron needs to rise to equal or larger than the energy difference between the valence band and conduction band. This energy difference is what is known as the band gap energy [1].

The following formula describes the relation between the photon energy and the band gap energy:

$$\frac{h * c}{\lambda} > E_g$$

h is Planck's constant, c is the speed of light, λ is the wavelength of the electromagnetic radiation and E_g is the bandgap energy of the semiconductor. From the formula, the incident photons need to have a minimum energy equal to the band gap energy to be able to create an electron-hole pair. A typical semiconductor material used in integrated circuits is silicon. Due to its semiconductor properties and the abundant amount of silicon on Earth, silicon is extremely affordable and appealing in the industry [2]. The band gap energy of silicon is 1.12eV at 300 kelvin [3].

Combining this information together with the previous formula, we get a wavelength of $\cong 1.1\mu m$, which is very close to the infrared spectrum. Wavelengths below this value, possess the energy required to generate electron-hole pairs in silicon. Silicon is therefore favorable for detecting photons within the electromagnetic spectrum because it covers the visible light spectrum wavelengths with its range of 200–1100nm.

Electromagnetic waves will gradually be absorbed as it is penetrating the semiconducting material. Longer electromagnetic wavelengths tend to get absorbed deeper in the material and the shorter wavelengths will get absorbed closer to the surface. When the wavelengths are above 1100nm, the absorption coefficient is so low that these photons travel through the silicon material without being significantly absorbed [2]. The photocurrent of the diode mainly

depends on the intensity of incident radiation. Conversion gain is the term used to describe the change on voltage by a single electron at the conversion node.
The general structure of a photodiode consists of two differently doped semiconductor types, p- and n-type in a junction as mentioned. The forming of the n and p regions can be made by epitaxial growth, diffusion, or ion implantation. A result of the different doping is that the semiconductor regions achieve an excess of electrons and electron holes. When placed together they will flow towards the opposite type while leaving behind positive donor ions and negative acceptor ions. Diffusion occurs, and a PN junction is created. An example of this junction is shown in Figure 1. The junction will have an electric field that is called the depletion area. In this area no more electrons can travel to the other side without having the sufficient energy.

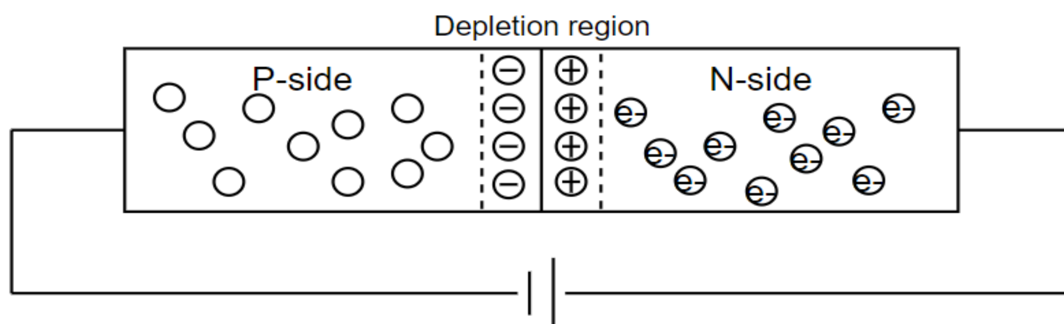


Figure 1 PN-junction with depletion region

1.1.1 MOSFET

The structures of NMOS and PMOS transistors can be viewed as the inter-connecting diodes across their PN junction. The diodes are from the source to bulk and from the drain to bulk. These are parasitic devices that add undesired parasitic capacitance and leakage. One needs to keep these junctions reverse biased to minimize any leakage currents through the diodes [4].

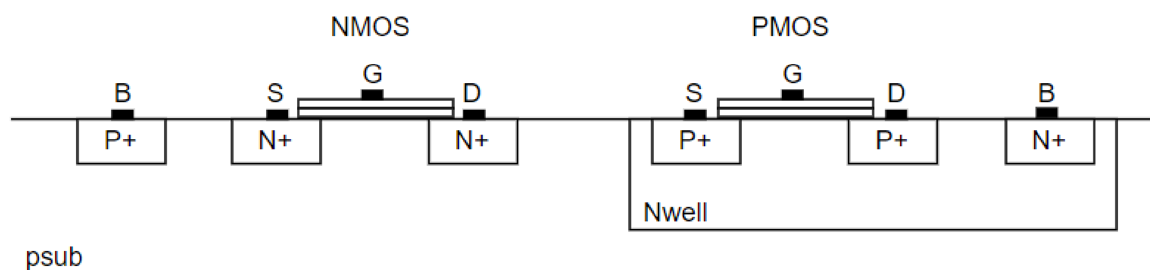


Figure 2 Cross-section NMOS PMOS

1.1.2 CMOS Structures

In the CMOS process, basically any PN-diode is sensitive to light and can be repurposed as a light sensor. Some of the simplest structure is created by combining a N+ region in a P-substrate (N+/P-sub) or placing a N-well in the P-substrate (N-well/P-sub). Another approach is to create a PN photodiode using P+/N-well. Also, If the substrate is grounded in the former mentioned diode, it creates a double junction diode (P+/N-well/P-sub).

The N+/P-sub diode is made with the high doping concentration for the N+ implant, thus resulting in a small width of the depletion region. This reduces collection efficiency compared to other structures. Since depletion width is small, the junction capacitance is large. The N+ region is created by ion implantation, which makes that the junction is close to the surface. This results in reduction in collection efficiency for the longer wavelengths [5].
The N-well/P-sub uses a lighter doped N-well to create the junction to the P-sub. The lower doping concentration increases the depletion width and junction capacitance decreases. However, the N-well diffusion is deeper than the N+. This increased depth creates depletion regions along the sidewalls of the junction that increase the overall junction capacitance. The collection efficiency is increased especially for higher wavelengths [5].
The P+/N-well/P-sub photodiode is like the N-well/P-sub diode but with an added P+ implant covering parts of the N-well. This structure has two PN junctions, the P+/N-well and the N-well/P-sub. This results in an even larger depletion region and should lead to the highest collection efficiency among the structures. The two junctions add capacitance in parallel, lowering charge to volt conversion. Since the P+ layer has a high hole concentration, we expect this photodiode to have lower dark current than the N-well/P-sub structure where the surface layer does not have a high free carrier concentration [5].

1.1.3 Quantum efficiency

Quantum efficiency (QE) is defined as the probability that an incident photon will generate an electron-hole pair that contributes to the detection signal. QE determines the light sensitivity. An ideal QE would be of a 100% for all wavelengths where every incident photon is converted into charge. The QE is affected by reflections from surfaces such as micro lens and silicon oxide. Photo-generated charges outside of the depletion layer do not experience any electric field and tend to diffuse in all directions and get lost through recombination. Photons can also go several micrometers deep into the substrate before being absorbed. The larger the depletion region width, the better for having a high QE. Decreasing the doping concentration can also increase the QE in some cases [6].

1.2 Image Sensor

The purpose of an image sensor is to convert incoming light into an electrical signal that can be viewed, analyzed, or stored [7]. There are two different image sensor technology types in use: charge-coupled device (CCD) and complementary metal–oxide–semiconductor (CMOS). CMOS technology has an edge over CCD in the sense that the area occupied by transistors can be significantly reduced and gives the possibility to implement more components like noise reduction circuits, ADCs, more pixels, and amplifiers in the same area. CMOS also requires less current and voltage to operate. All this combined with CMOS' high speed, made it grow in popularity for image sensor use in recent years. Making designs more compact is a development that can be explained by Moore's law. Moore's Law refers to Gordon Moore's perception that the number of transistors on a microchip doubles every two years, though the cost of computers is halved [8].

Often one uses micro lens array where small lenses are placed on the surface of the image sensor like the one shown in Figure 3. This results in focusing the light onto the photosensitive part of the sensor that increases the sensitivity. Using a color filter array (CFA), information about the amount of RGB light present in the scene can be measured. The CFA is a mosaic of color filters that allows red, green, and blue light to pass through over each pixel. To get a colored image, interpolation is used to create an RGB value of each pixel.

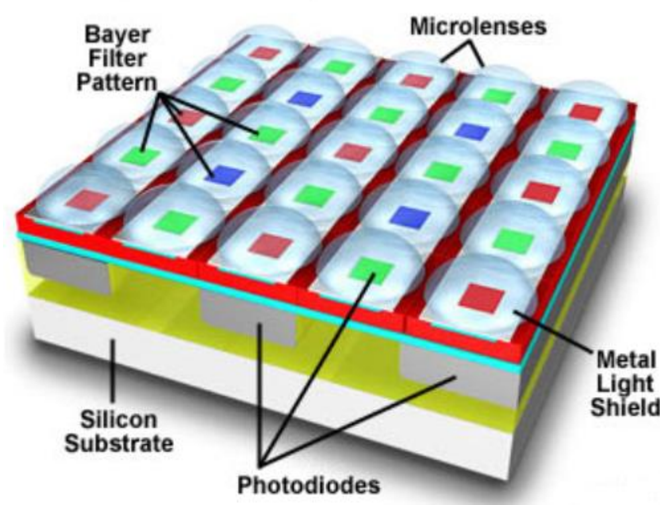


Figure 3 Micro lens array of photodiode [9]

1.3 Pixels

On an image sensor chip the pixels are the circuitry that often occupies the most area. They typically consist of a photodiode and several transistors. In some architectures the pixel can contain several photodiodes, capacitors along with noise reduction circuitry.
The different pixels used in this project are built up by three transistors together with one of the photodiode structure variants.
The fill rate of a pixel is the percentage of the pixel space that is allocated by the photodiode. 50% fill rate means the photodiode allocates 50% of the pixel space. One of the advantages of using CMOS technology compared to CCD explained earlier is that the transistors can be even smaller than before, and the photodiode fill rate can increase. Another method to increase fill factor is by using back side illumination instead of front side illumination. With back side illumination, the substrate is flipped during fabrication making it possible to place wiring behind the photodiode, thus increasing the fill factor.
Full well capacity (FWC) is the amount of charge that can be stored within an individual pixel without the pixel becoming saturated. It is the maximum amount of charge that can be accumulated in the photodiode [10]. The FWC plays a part in determining the dynamic range of an image sensor.

1.4 Noise

Noise will always be present and limit performance when talking about analog circuitry such as image sensors and photodiodes. The image sensor captures light information and represents it as a 2d image. Here the noise will reduce the quality of the representation of the signal.
There are two main noise categories. Noise that is fixed in a spatial position is called fixed pattern noise (FPN). This noise appears at fixed positions. FPN can, in theory, be removed either through signal processing or noise reduction circuits. The other type of noise is a time dependent random noise called temporal noise. Temporal varies in time and is frozen when an image is captured.

1.4.1 Fixed pattern noise

FPN are usually perceived as vertical stripes in the image superimposed on some salt and pepper noise. FPN’s main components are dark current non-uniformity, performance variations in the pixel source follower and offset found in the columns [10].

These vertical stripes arise due to mismatches of components that are common to each column that cause the noise pattern. The general salt and pepper noise is due to the pixels. Dark current is treated as an offset between pixels and is apparent during no illumination. Dark current is proportional to the integration time and is dependent on the temperature, PN junction area, and operating criteria, amongst other things.
As mentioned, FPN can be reduced or removed. Black level correction (BLC) is an effective technique. BLC works by first capturing an image in total darkness, then removing the values captured to the image taken which should result in an improved image.

1.4.2 Temporal noise

Thermal noise is random and varies over time. There are three fundamental temporal noise components in optical systems: thermal noise, shot noise and flicker noise [10].
Temporal noise can be caused by photon shot noise, dark current shot noise, thermal noise, reset noise and pixel source-follower noise. As mentioned, this noise is random and will be different each time an image is captured.

1.5 Sample and hold

A sample and hold circuitry are designed to hold and sample an analog signal for further processing. This allows the signal to be independent of time and prevents any further influence. In an image sensor this is useful to keep the stored analog values before converting them to the digital domain. A typical sample and hold circuit consist of a switch, capacitor, and an amplifier. A more advanced setup can perform noise reduction operations like Correlated Double Sampling (CDS) and Differential Delta Sampling (DDS).

1.6 TCAD - Sentaurus Workbench

Technology Computer-Aided Design (TCAD) refers to the use of computer simulations to develop and optimize semiconductor process technologies and devices. Synopsys TCAD offers industry-leading process and device simulation tools, as well as a powerful graphical user interface (GUI) driven simulation environment. Synopsys TCAD provides tools for interconnect modeling and extraction, providing critical parasitic information for optimizing chip performance [11].

TCAD can give insight in device design and behaviors of components. Sentaurus workbench (SWB) is well suited for testing out different structures of photodiodes based on CMOS 180nm process parameters. The main benefit of doing semiconductor simulations is that it is possible to get expected electrical and optical characteristics and confirm the working principles of a product before production.
SWB is a graphical front end that integrates TCAD Sentaurus simulation tools into one environment. SWB is used throughout the semiconductor industry to design, organize, and run simulations. (For future students wanting to learn this software, I recommend this site to read [12], as well as looking at the example projects and going through the training folder in SWB.)

1.6.1 TCAD tools

In SWB there is a large variety of different tools. For this project, the tools can be broken down to Structure generation, Sentaurus Process, Sentaurus Device Simulation, and Sentaurus Visualization optimization. These tools are described below. All the available tools can be seen in Figure 4.

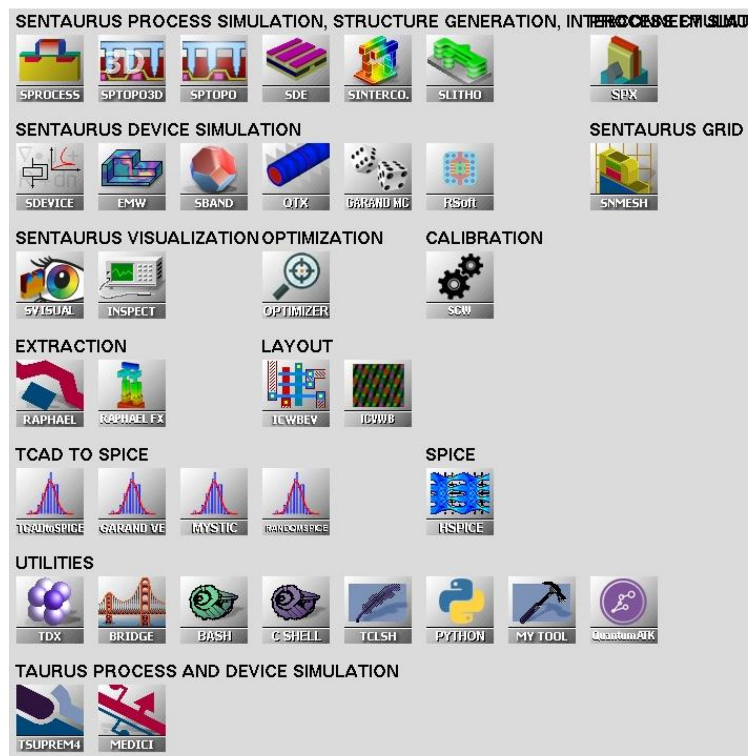
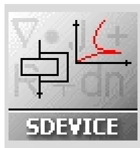


Figure 4 SWB Tools

Sentaurus Structure Editor (SDE) is a tool where the structural design of the device is defined. When using SDE, it is possible to work both in text and graphical views to define materials, regions, and structure contacts for the device. Here the evaluation windows for doping and meshing are defined followed by placing doping and mesh strategies. Meshing defines the fineness of the grid. The finer the meshing, the more points will be generated and increase simulation time. When working in the graphical view, the text script will be generated. It is also possible to edit and create the script without the use of the graphical view.

Sentaurus Process (Sprocess) is an advanced multidimensional process simulation. Sprocess is a highly flexible multidimensional process modeling environment for developing and optimizing silicon semiconductor process technologies. In this tool it will be possible to work with a broad range of technologies as well with specifications for 180nm CMOS. In Sprocess the specific processing steps are defined e.g., ion bombardment.



Sentaurus Device (Sdevice) is a semiconductor device simulator. Sdevice is an advanced multidimensional device simulator capable of simulating electrical, thermal, and optical characteristics of silicon-based and compound semiconductor devices.

Sentaurus Visual (Svisual) is a plotting tool for visualizing data from TCAD simulations and experiments. It enables users to work interactively with data using a user interface and to automate tasks with scripting.

II Design

2.1 TCAD - Photodiodes

The focus of the TCAD simulation chapter is about proving the working concepts of the designs rather than going into detail on the simulation results values. There will be parameter differences from the simulations to the parameters used in fabricating the IC.

2.1.1 Estimating process parameters of TSMC 180nm

The production processes are generally a well-guarded secret, costly, and not easily available for academic research groups. Specific process parameter estimations had to be made to define the implants and wells to be used in simulations.

From studying structures of 180nm NMOS and PMOS transistors generated in Sprocess shown in Figure 5 where the net active is shown, a manually matching and converting of the "tdr" file from Sprocess with the doping profiles, over to Sdevice was made. These structures are standard templates for 180nm generation MOSFET process simulation where the NMOS contains information about N+ and P-sub, and PMOS sits on a N-well and having P+ implants for the source and drain. With this information it was possible to make estimates of depth and grading for the N+, P+ and N-well implants as well as defining the doping for the P-substrate. This was done by looking at the boron and phosphorus concentrations through the material together with the net active properties and resulted in a realistic parameter estimate for the 180nm process.

The main reason for converting over to Sdevice from Sprocess is for the increased user friendliness and working speed in Sdevice. Working in Sdevice also makes design customizations easier together with the ability to work in a graphical view to write the SDE code.

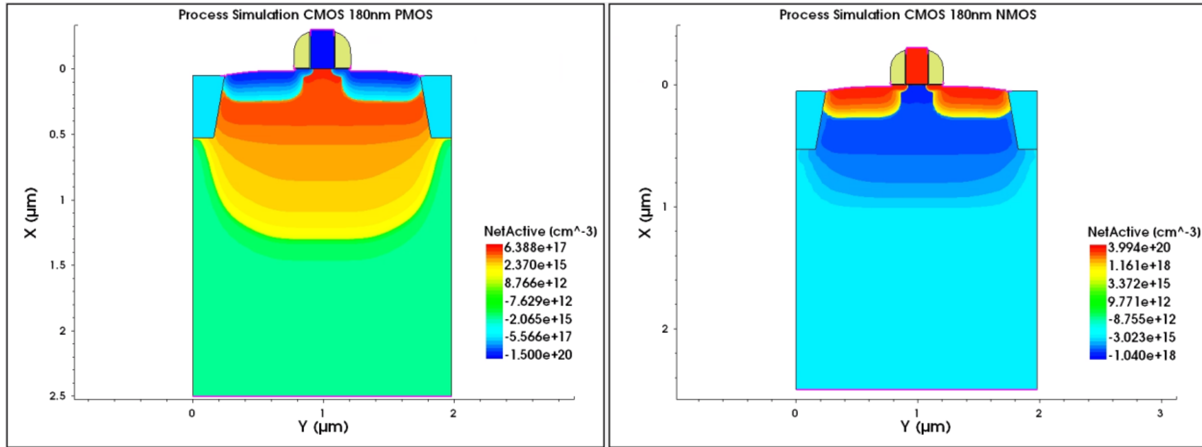


Figure 5 180nm PMOS and NMOS Transistor TCAD

Estimating the doping profiles for silicon 180nm are shown in the Table 1. It is worth noticing that the N-well depth is over three times of the N+. P substrate has a constant doping profile, where the other layers follow a gaussian profile. The gaussian profiles have the peak value on the surface and a lower doping value at the defined depth.

The SDE code is shown in the appendix.

Table 1 Estimated doping profiles

Layer	Distribution profile	Doping	Value	Peak value	Value at Depth	Factor	Depth(µm)
P+	Gaussian	Boron	*	5e+20	5e+16	0.8	0.4
N+	Gaussian	Phosphorus	*	5e+20	5e+16	0.8	0.4
N-well	Gaussian	Phosphorus	*	5e+17	5e+14	0.8	1.3
P-sub	Constant	Boron	5e+11	*	*	*	180

2.1.2 Photodiode Structures

Four different CMOS photodiode structures were created and simulated in TCAD. The structures are shown in the Figure 6 and are possible to design in Cadence 180nm layout. PD1 is a P+/N-well/P-sub, PD2 is a N+/P-sub, PD3 is a N-well/P-sub and PD4 is a P+/N-well diode. PD4 has been simulated with a floating substrate. However, on the produced IC, the substrate will always be grounded from the NMOS transistor bulk’s being connected to ground. PD4 should therefore perform close to PD1 on the produced IC if the substrate has good ground connections.

It is expected that PD2 and PD4 that are not using the N-well/P-sub junction will have less collection efficiency for longer wavelengths. This is because of the small depth of the N+ implants compared to the N-well for absorption as mentioned in a previous chapter.

For the project, it would have been beneficial to experiment with different doping and well types. It was later discovered that it was difficult to use these in cadence, and difficult to make an estimate on the concentrations and profiles without additional information from the manufacture.

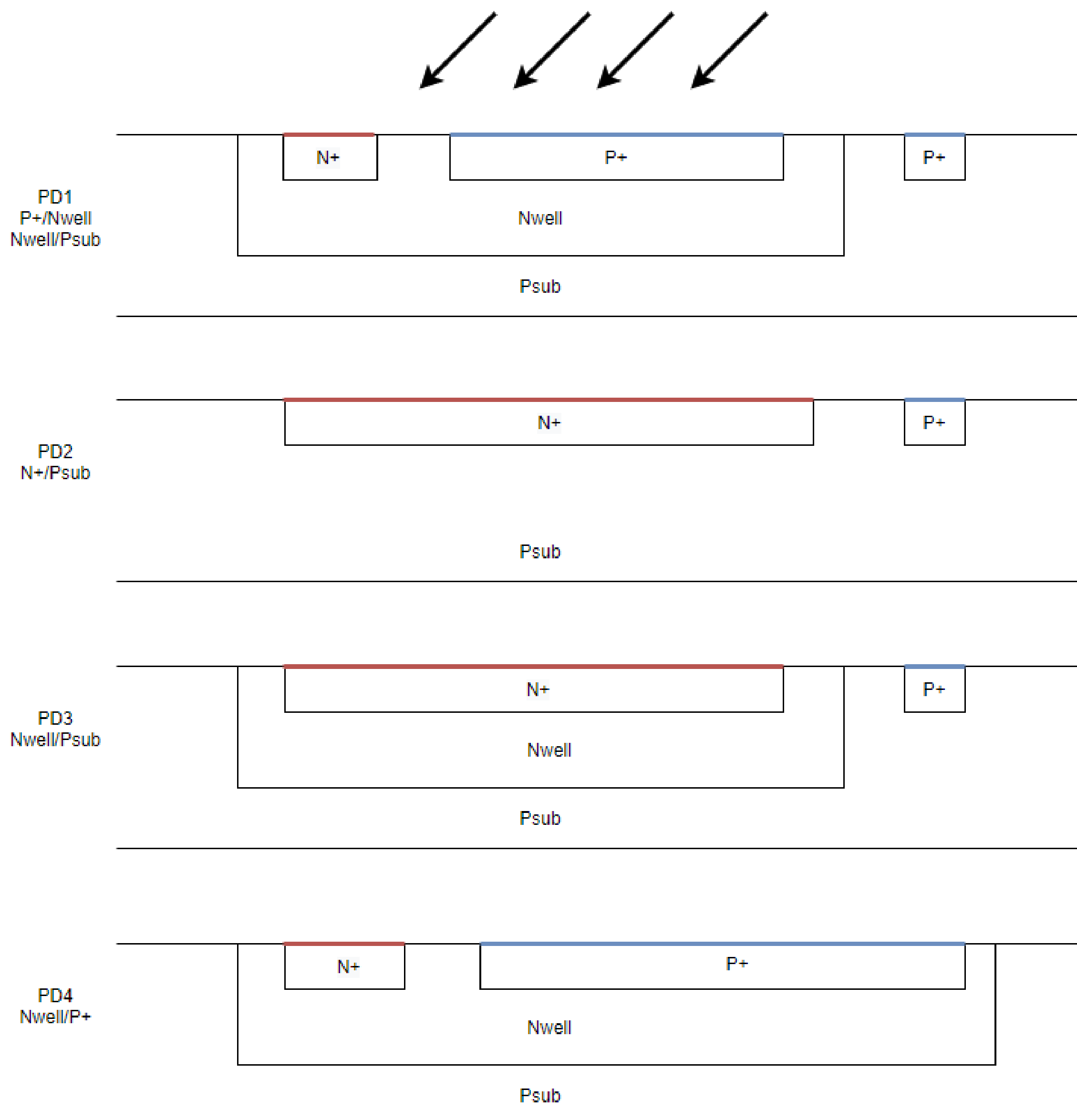


Figure 6 Photodiode variants

2.1.3 Simulations

2.1.3.1 Punch-through

When designing PN structures, it is important to be careful to avoid unwanted PN junctions and make sure the spacing between the implants is sufficient. To make sure there is no punch-through between the photodiode and the surrounding electronics, quasistationary simulations were run. Punch-through is when depletion regions from two different devices overlap. This spacing is generally sorted in the DRC of IC layout design. Since the photodiodes are not defined as a “component in a library”, it is possible some of the DRC checks are avoided. For safety reasons, these simulations were run, and they provide important information about distancing between devices.

From the quasistationary simulation it is possible to inspect how a device’s depletion region changes based on the voltage applied to the contacts. Different scenarios were simulated and checked that there is sufficient distance between the components to get no punch-through. From increasing the distances between photodiodes and transistors, some of the fill factor is lost from the pixels, but it reduces the risk of suffering from punch-through which could spoil the work, potentially resulting in defect components.
Shown in Figure 7 is the depletion region for PD1 with 1.5V reverse biased. The white lines represent the depletion region and can be seen at the P+/N-well junction, N-well/P-sub junction and around the anode. The depletion region is changing with the applied voltage. From studying the graph, the depletion region is extending a few micrometers beyond the structure to the right. This is important to make sure this region does not overlap with the depletion region from another device. Figure 8, Figure 9, Figure 10 shows the other PD variants with the same reverse biasing.

The way in which the depletion region is defined in Synopsys Sentaurus and the main TCAD competitor Silvaco Atlas are different. Therefore, there can be some differences from TCAD software to software.

For SDE parameters and Sdevice, see appendix.

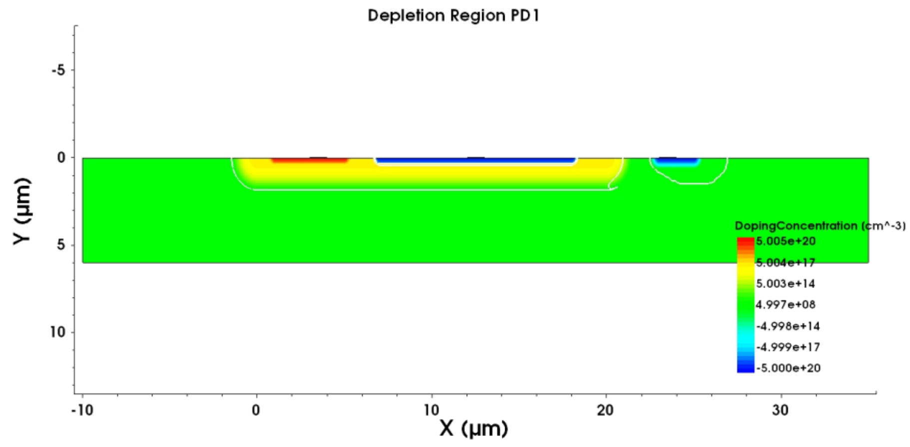


Figure 7 Depletion Region PD1

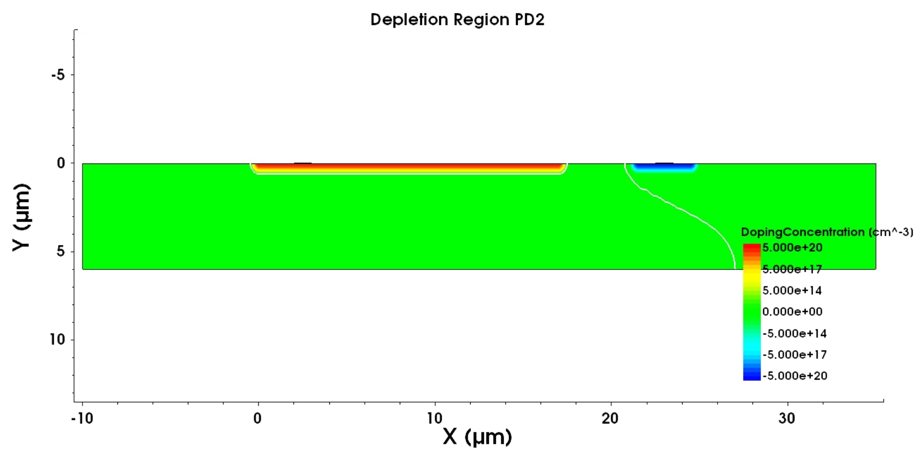


Figure 8 Depletion Region PD2

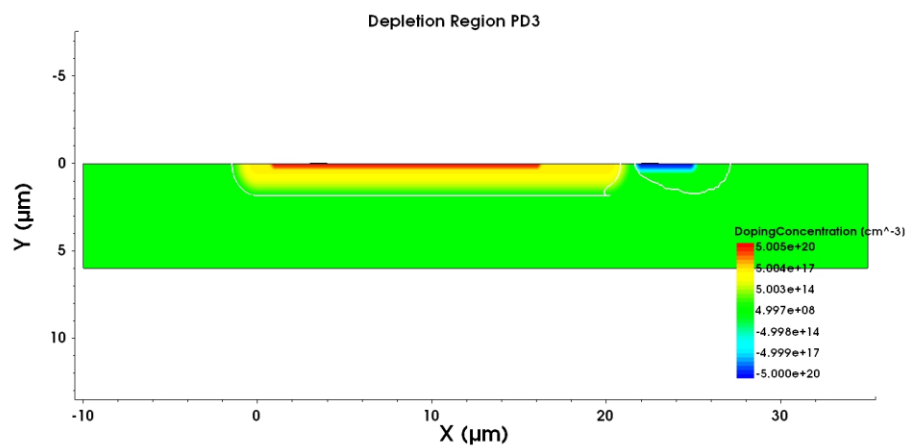


Figure 9 Depletion Region PD3

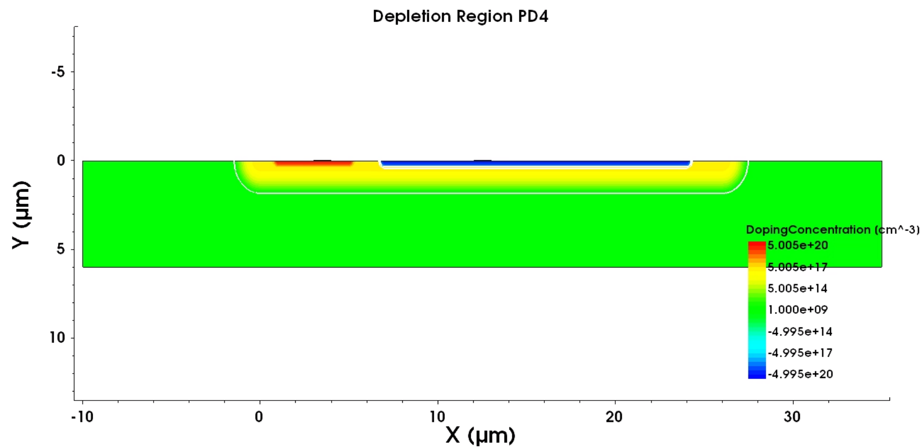


Figure 10 Depletion Region PD4

2.1.3.2 Breakdown voltage

Breakdown voltage defines the largest reverse voltage that can be applied to the photodiode without causing an exponential increase in the leakage current. In other words, breakdown voltage is the voltage that causes a portion of an insulator to become electrically conductive. To simulate breakdown voltage for the photodiodes, another type of Quasistationary simulation was defined together with ramping applied voltage.

From the simulation results, only PD1 and PD4 were sensitive for low voltage breakdowns at 8V as seen in Figure 11 and Figure 14. This breakdown is between the P+/N-well junction. This junction will break down before the N-well/P-sub junction and is the one that shows up in the graph. However, this should not be a concern since the core VDD is set to 1.8V and the photodiodes will never be exposed to these voltage levels. PD2 had a very high breakdown voltage of almost 80V is shown in Figure 12. PD3 broke down at 58V the simulation and is shown in Figure 13. It is expected that the structures with the highest doping difference between the junctions will have the lowest breakdown voltage. This is because higher doping gives smaller depletion region width and results in a larger electric field. This high electric field will exert a force on the electrons and holes and cause them to move across the junction by breaking the bond. It was therefore expected PD3 would have the highest breakdown of the structures. From the simulation PD2 had the highest breakdown voltage. This is likely due to variation in area between the structures during simulation and maybe missing simulation parameters, making it the most robust.
Usually, the manufacturer provides this kind of information with their process design kit, but to verify the result through these simulations is important to learn about the safety margins in the design.

The cmd. file for this simulation can be found in the appendix.

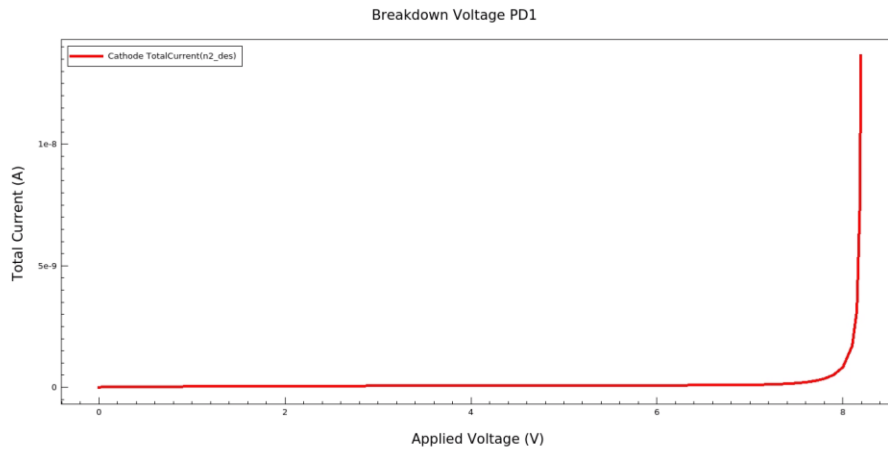


Figure 11 Breakdown voltage PD1

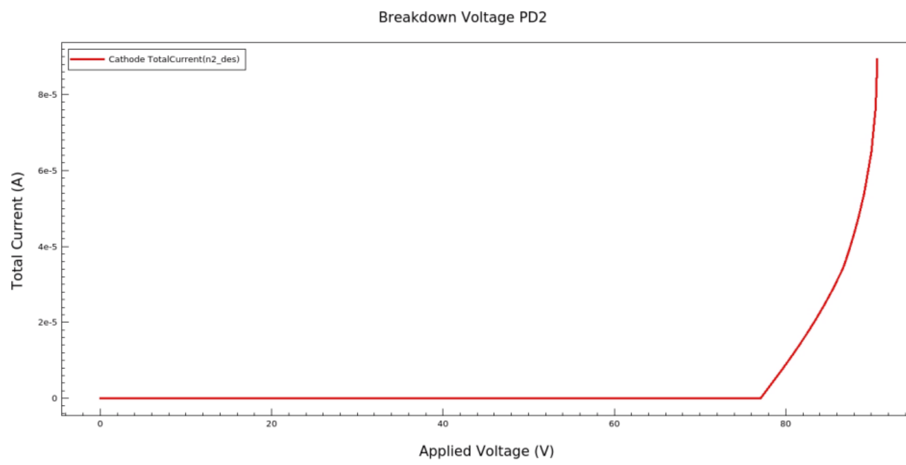


Figure 12 Breakdown voltage PD2

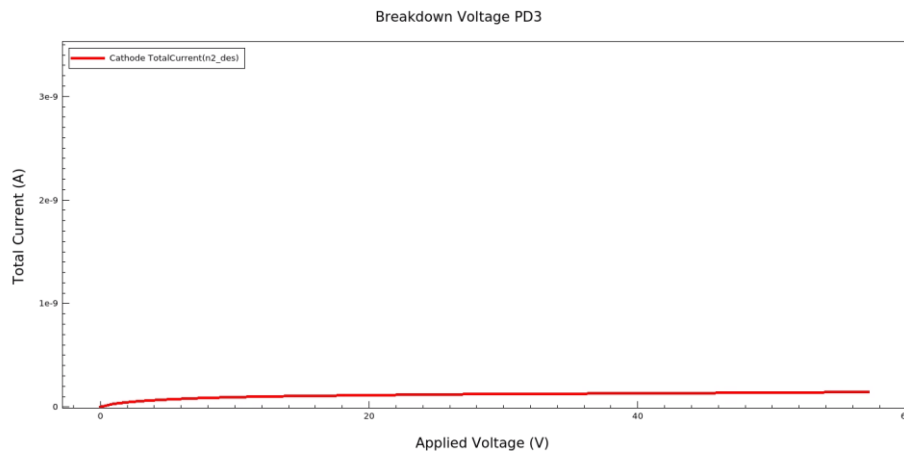


Figure 13 Breakdown voltage PD3

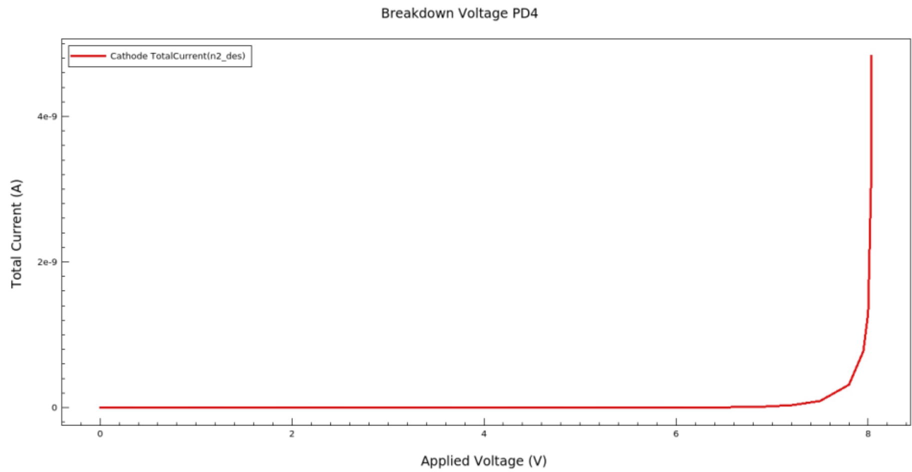


Figure 14 Breakdown voltage PD4

Additionally, when applying voltages to a thin substrate structure it is important to look at the generated TDR file after simulating. The electric field distribution over the structure needs to be inspected to see that voltages are applied correctly, and that the substrate is grounded correctly. An example of this is shown in Figure 15. In the first structure only the top anode contact is grounded resulting in no grounding on the left part of the structure. In the second structure the bottom of the substrate is grounded as well as the anode contact. This results in a much better grounding of the substrate and should represent a real-life substrate better for the simulations with a thin substrate defined.

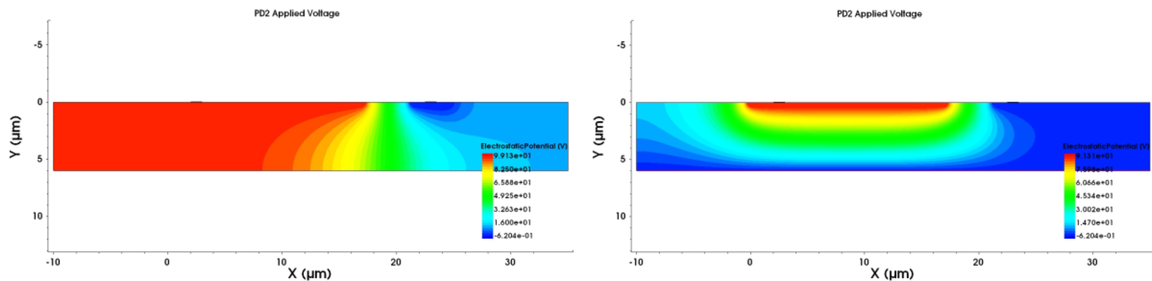


Figure 15 Applied voltage, Electric field distribution

2.1.3.3 I-V characteristics

With Sdevice, it is possible to use the optical generation rate to compute the light I–V characteristics of the illuminated structure. The optical generation function activates the computation of the optical generation rate. It also is used to specify the type of illumination source as well as optional parameters such as the quantum yield. For this simulation, additional contacts at each side of the end points of structure were defined. These are the

limits for the simulation along with reflectivity of the contacts. Voltage was ramped on the cathode from 0 to 2V.

The optical generation were defined with the following parameters:

- Type of illumination source is specified as a monochromatic source
- Temperature of 293 kelvin
- Wavelength of 500nm (for IV curves)
- Incident light intensity of 0.00855 [W/cm2]
- Polarization = 0.5
- Direction of the incidence of light Theta = 0 (in y direction)

The origin of the illumination is defined to be 1 um above the photodiodes surface and the window the illumination covers was a total of 35um. The rest of the test setup's cmd. file is found in the appendix.

During these simulations the photon absorption rate is defined as the rate at which photons are absorbed by the photodiode and is given with the following formula:

$$N_{abs}(\lambda) = \int_{\Omega} G_{abs} \mathrm{dV}$$

$G_{abs}(x, y, z, \lambda)$ $(cm\ s^{-1})$ is the photon absorption rate per unit volume or the absorbed photon density at each point inside the photodiode.

The optical generation rate G_{opt} $(cm^{-3} s^{-1})$ is at what rate the electron–hole pairs are generated due to absorption of photons and is calculated by the following formula:

$$G_{opt}(\lambda) = \eta_{QT} * G_{abs}(\lambda)$$

Where the quantum yield, η_{QT}, is defined as the ratio of the number of electron–hole pairs generated per absorbed photon.

2.1.3.4 Light IV

The Light I-V graph for photodiodes is shown in Figure 16 where we look at the cathode's outer voltage vs the cathode's total current. Looking at the graph, the current is increasing with the increasing applied voltage. This is expected behavior from a reverse biased photodiode. The depletion region should be widening with the increase in applied voltage and increasing the area for absorption. The total current in the cathode is a combination of dark current and light current. The total current would increase if the dark current were increasing with the applied voltage, but from looking at the dark current graph seen in Figure 17, the dark current remains the same value after roughly 250mV at room temperature.

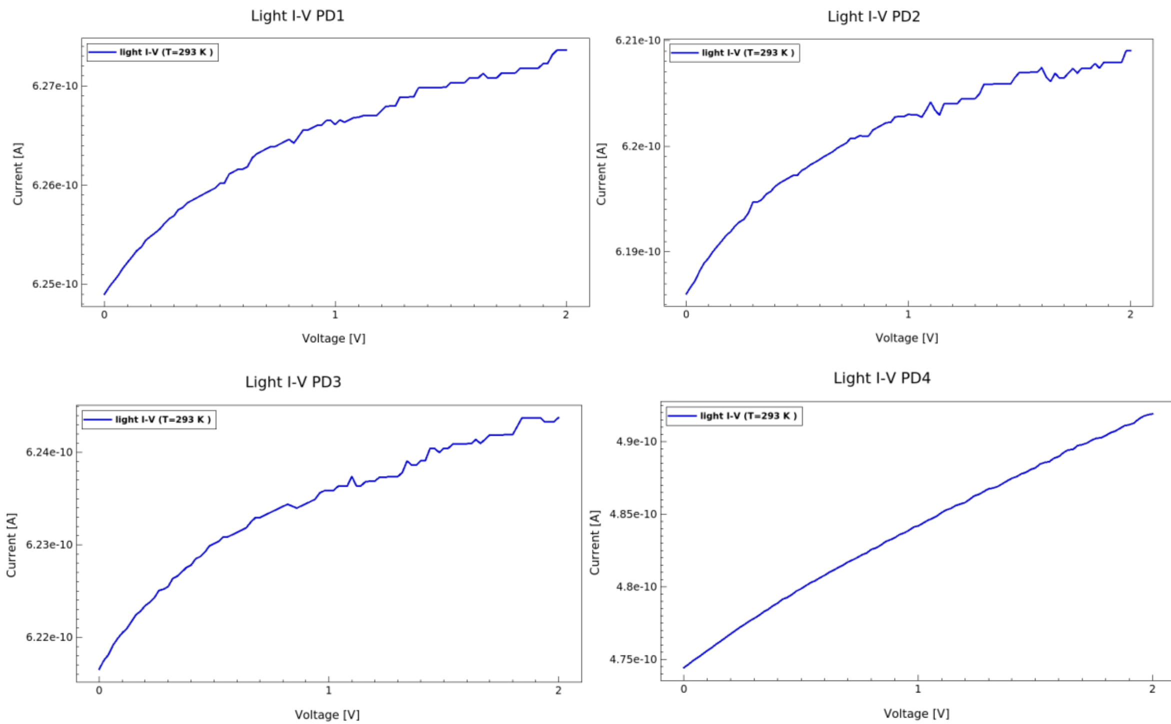


Figure 16 Light IV curves

2.1.3.5 Dark current

The rate of dark current generation depends on the active area of the PN junctions, but also on the temperature, on the band gap energy of the material and how the photodiode is being operated (near breakdown voltage etc.) [13].

From the dark currents graphs shown in Figure 17, one can see that the structures that have an N-well have the highest dark current (PD1, PD3, PD4). The generation of dark current in the P+/N-well does contribute, but the dark current from the N-well/P-sub is dominating. This is likely due to the large area the N-well occupies. This is most visible when looking at the PD1 compared to PD3 that have about the same dark current in the simulation. The photo- and dark current is shown in Table 2. It is however expected that PD1 and PD4 should have lower dark current than PD3. This is because the P+ layer has a high hole concentration close to the surface as mentioned in a previous chapter. Since the P+ layer has a high hole concentration, we expect this photodiode to have lower dark current than the N-well/P-sub structure where the surface layer does not have a high free carrier concentration light current is substantially larger than the dark current IV.

However, in real life scenarios there can often be a mismatch in the silicon/silicon dioxide crystals that can lead to interstitial energy levels that electrons use as steppingstones to reach conduction band energy, thus resulting in more dark current noise. This mismatch is

not included in the simulations due to the simulations coming a bit short and not performing as wanted when using this interfacing. The real dark current will therefore most likely be higher than simulated. There are also other currents that play a part in the dark current like tunneling currents, surface leakage current and generation-recombination current [14].

From looking at the graph for high temperature dark current PD2 shown in Figure 18, we see that the dark current is increasing with temperature and with applied voltage as we expect. The simulated dark current is almost multiplied by 10 when increasing the temperature by 30 degrees for PD2.

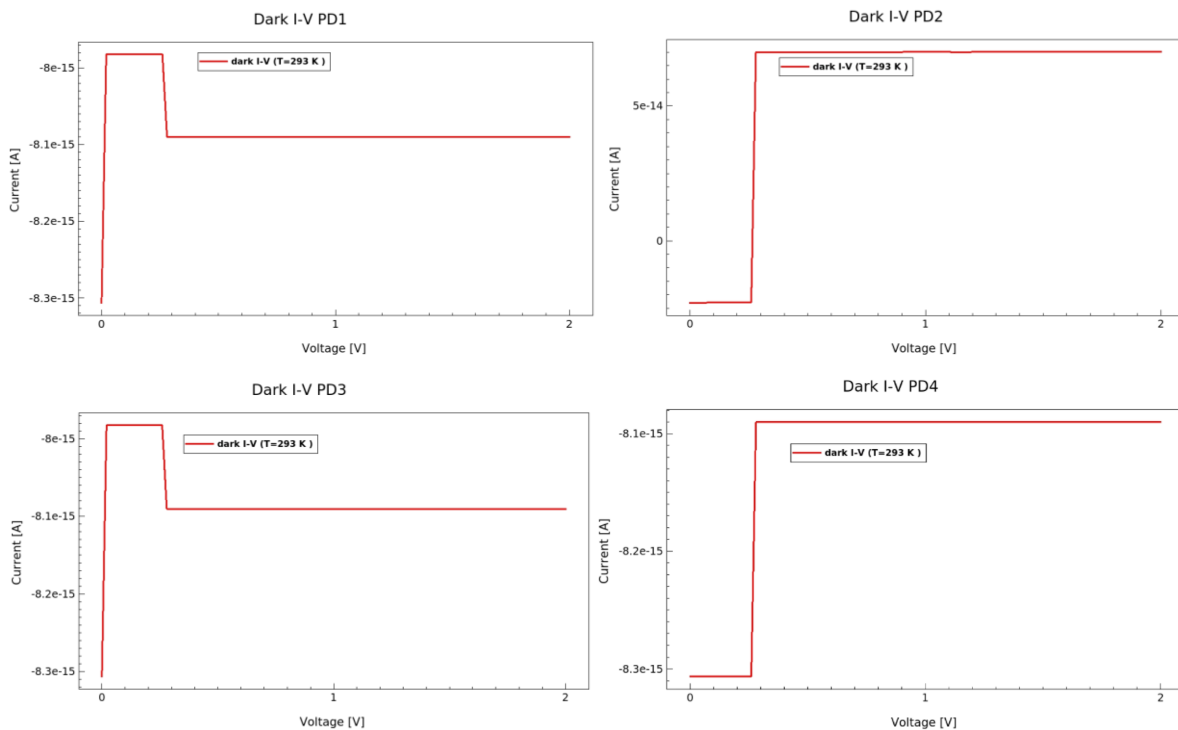


Figure 17 Dark IV curves

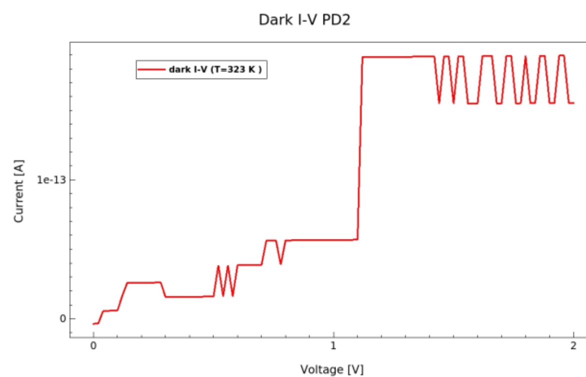


Figure 18 PD2 Dark IV curves, 323kelvin

Table 2 Values light simulation 2V reverse bias, 293kelvin

	Wavelength	Dark Current A	Photo Current A
PD1	500nm	-8.09e-15	6.249e-10
	700nm	-8.09e-15	7.59e-10
PD2	500nm	7.01e-15	6.186e-10
	700nm	7.01e-15	7.771e-10
PD3	500nm	-8.09e-15	6.217e-10
	700nm	-8.09e-15	7.758e-10
PD4	500nm	-8.09e-15	4.744e-10
	300nm	-8.09e-15	1.035e-10

2.1.3.6 Current density

The current density is measured at the last bias point (2V). Current density is related to electromagnetism and is defined as the amount of electric current flowing through a unit cross-sectional area [15].

Computing current density from current.

The current I in units of A is related to I' in the following formula:

$$I = I'L_z$$

Where the current I' is in units of A/µm. L_z is the width of the structure in the z-direction. For 2D structures, the default value for L_z is 1 µm. The current density is then defined as:

$$J = \frac{I}{A_{surf}}$$

A_{surf} is the surface area of the structure. If w_{tot} is the width in x-direction of the structure, we can say:

$$A_{surf} = w_{tot}\ L_Z$$

From combining these equations and since L_z is 1 µm, the current density is then calculated as following:

$$J[A/\mu m^2] = \frac{I'[A/\mu m]}{w_{tot}[\mu m]}$$

Visualizing all the current density vectors for each plot in one picture is difficult while keeping the fineness of the vectors visible. Shown in Figure 19, Figure 20, Figure 21, and Figure 22 are the vector lines uniformly scaled. If the vectors are scaled to the grid, it gives an unreadable plot for such a large structure without zooming in and out all the time. In this simulation only the anode contacts of the photodiodes are grounded and not the bottom part of the substrate. This simulation uses the same SDEVICE file as the light IV simulation. From the plots one can see that the majority of the total current density vectors is close to the surface of the structures. In PD2 almost all current is flowing at the top due to the shallow N+ compared to the deeper N-well in the other structures. The current density looks as expected. PD4 has the floating substrate, and this changes the current density and current potential quite a bit compared to the other structures. The current potential contours to visualize the current flow lines at the last bias point. This makes up the color part of the plots. Plots containing only the current potential are shown in the appendix.

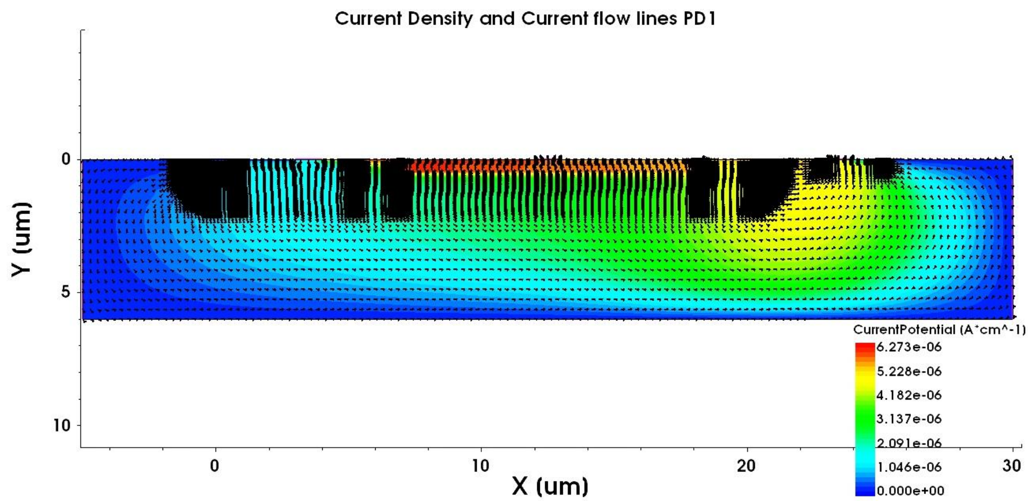


Figure 19 Current Density and Current flow lines PD1

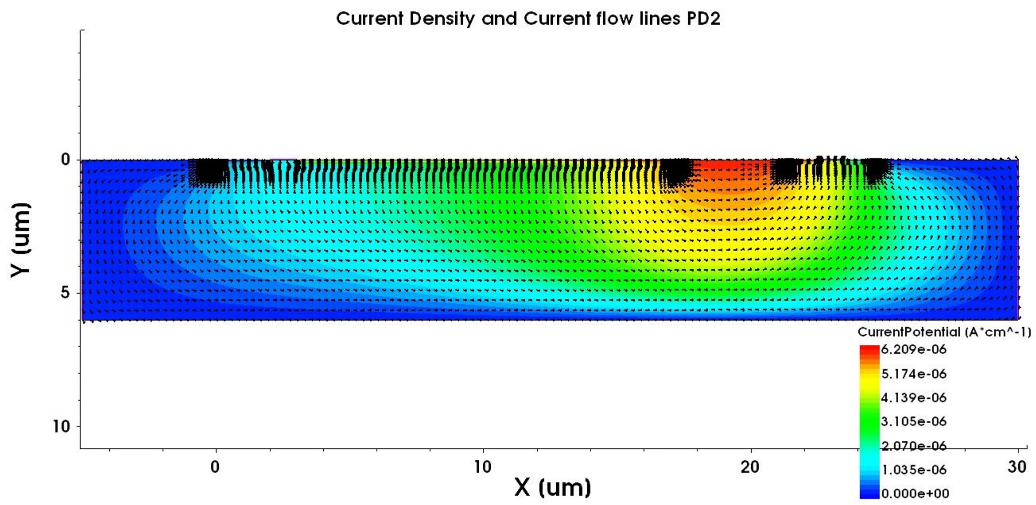


Figure 20 Current Density and Current flow lines PD2

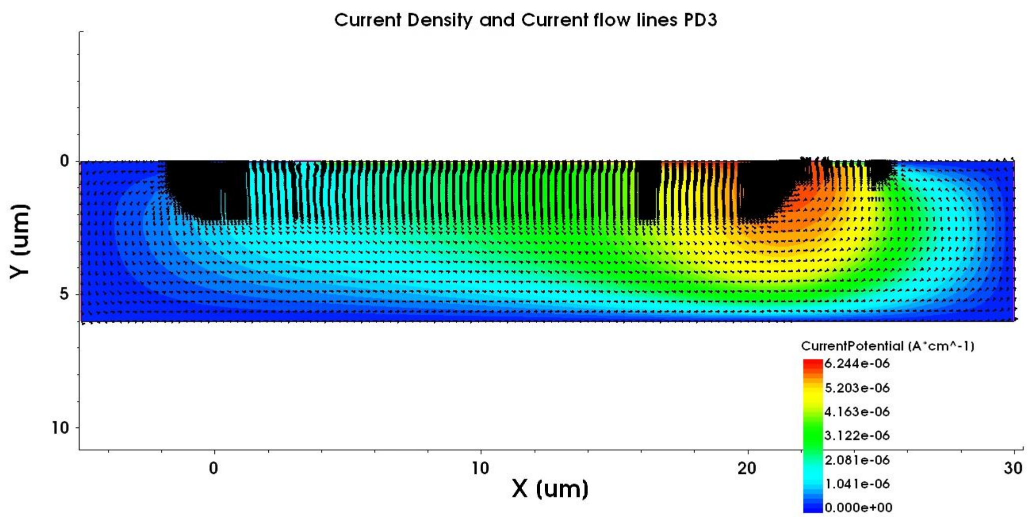


Figure 21 Current Density and Current flow lines PD3

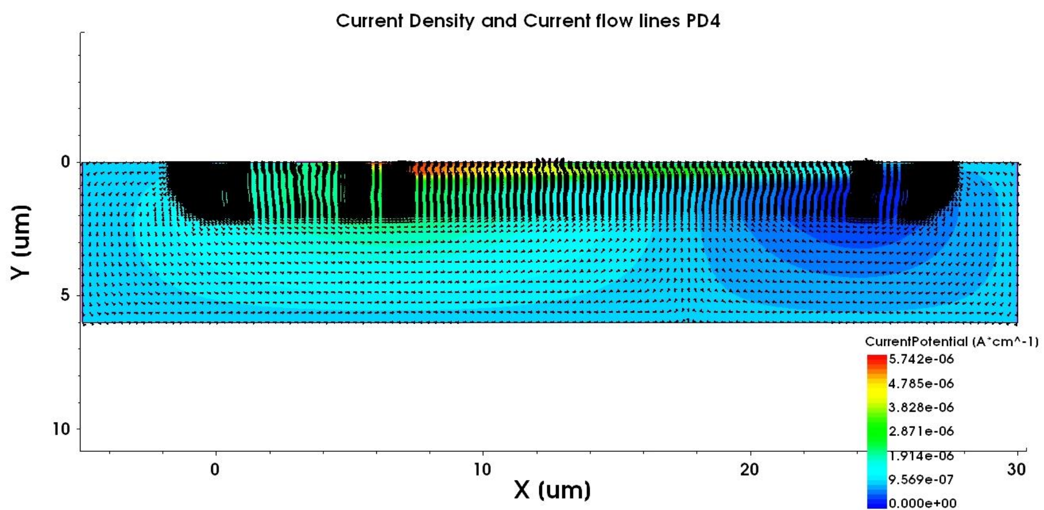


Figure 22 Current Density and Current flow lines PD4

2.1.3.7 Absorbance, transmittance, and reflectance

At the time the simulations were set up, it was unclear what die thickness the IC would end up with after fabrication. To make sure the simulations would finish in “workable” times and not spend a couple days each computing the results, the simulated substrate thickness was substantially thinner than what it would be in real life. The processing power and performance on the university workstation computers used for simulation, were limited. The die thickness for the IC ended up at almost 180μm and would be extremely time consuming to complete all previous and later simulations without adulterating the quality of meshing and structures.

The graphs in Figure 24 show the reflectance spectra for the optical generation simulations discussed in the last chapters. The graph shows that a factor of photons is reflected by the top surface of the photodiode and from the contacts. The remaining photons are transmitted into the photodiode. Some of these photons are absorbed by the photodiode, and the remaining photons are transmitted out of the bottom surface of the photodiode. The longer wavelengths tend to go deeper into the substrate before being absorbed. With the thin substrate simulated (6μm), the absorbance quickly drops for the higher wavelengths.
When the absorbance drops, we expect the transmittance to increase for the higher wavelengths. The simulation shows that the reflectance is increasing when absorbance goes down, and this is most likely artificially made up so that the combined factor of reflectance, transmittance, and absorbance equals “1”. During the simulation, the power reflectance, $R(\lambda)$, from the top surface of the photodiode is computed from the ratio of the photon flux reflected from the top surface of the photodiode, $N_{top}(\lambda)$, to the incident photon flux, $N_{in}(\lambda)$

$$R(\lambda) = \frac{N_{top}(\lambda)}{N_{in}(\lambda)}$$

It would be expected for reflectance to be quite similar for all structures and we would see the change in the absorbance and transmittance’s part of the graph. The reflectivity of a silicon wafer is determined from the complex refractive index. The reflectance is at highest for the short wavelengths, and at its lowest for the long wavelengths on a polished wafer [16]. This is opposite what the graph shows us, and again indicates that the reflectance is most likely artificially made up for the combined factor to equal “1” in our case.
From the previous light IV Table 2, one can see that the photocurrent for the photodiodes is quite similar for 500nm. The results from Figure 24 indicates that the photodiode structures have about the same absorbance for that specific wavelength thus resulting in similar photocurrents.

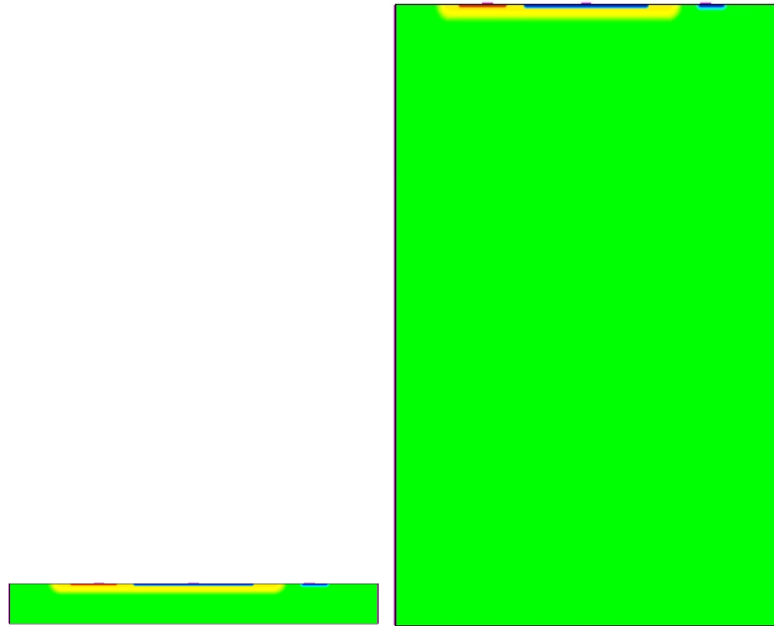


Figure 23 6µm and 60µm substrate

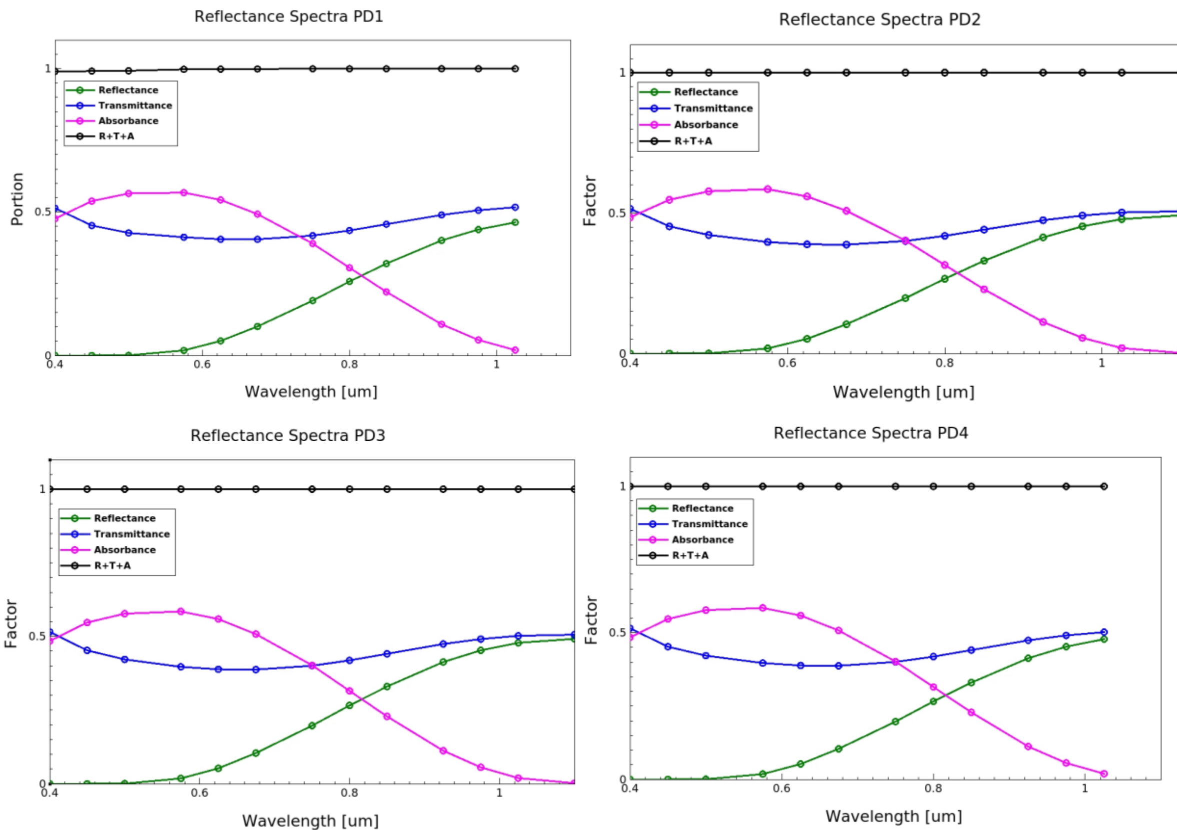


Figure 24 Reflectance Spectra 6µm substrate

When simulating with a thicker substrate (180µm) shown in Figure 25, it reveals that the photodiode structures taking advantage of the deeper penetrating N-well get a better absorbance rate for higher wavelengths. The absorbance factor is the same as the external

quantum efficiency (EQE) for the photodiode and is highest for PD1 and PD3 at 800-900nm with a EQE of 0.65 before approaching zero EQE for wavelengths over 1100nm.

The power absorbance, $A(\lambda)$ is given by the formula:

$$A(\lambda) = \frac{N_{abs}(\lambda)}{N_{in}(\lambda)}$$

Where $N_{abs}(\lambda)$ is the photon absorption rate in the photodiode and $N_{in}(\lambda)$ is the incident photon flux.

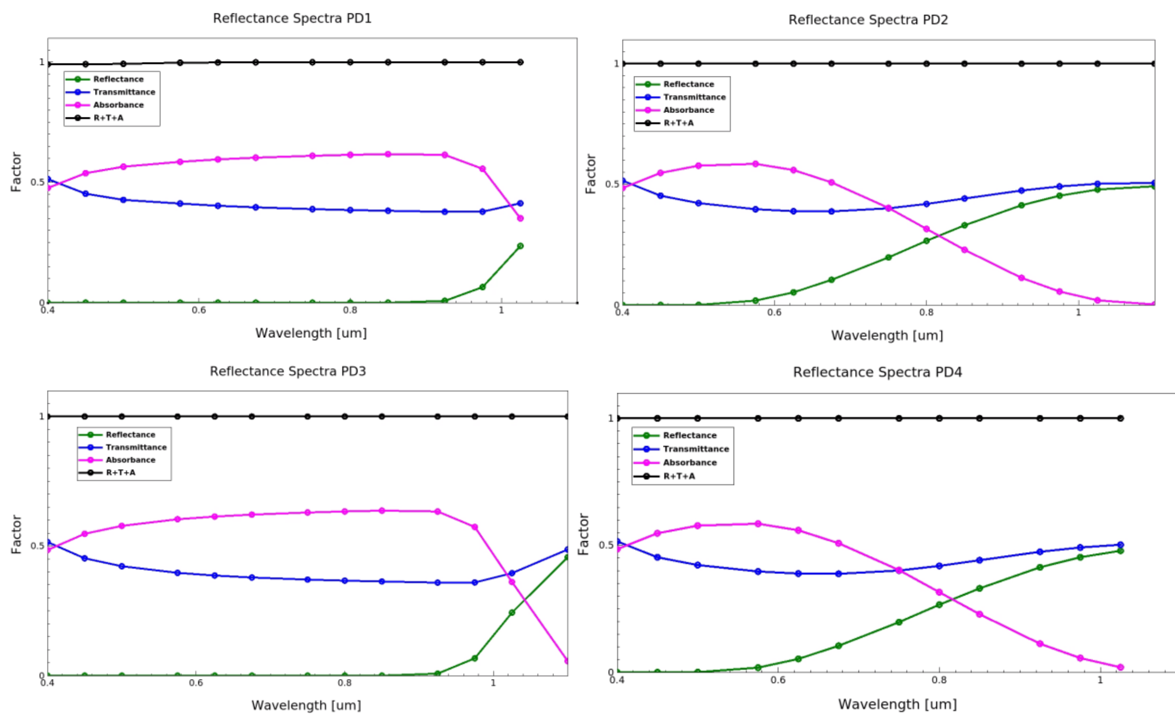


Figure 25 Reflectance Spectra 180µm substrate

2.1.3.8 Reverse resistance

The reverse resistance r_r of the photodiodes are calculated using the formula:

$$r_r = \frac{dV}{dI}$$

Ideally, the reverse resistance of a diode is infinite. However, in actual practice, the reverse resistance is not infinite because the diode conducts a small leakage current (due to minority carriers) when reverse biased [17]. This leakage current is a part of the factors making up the dark current.

The photodiodes are reverse biased, and the minority carriers present in the diode carry the electric current [18]. The reverse biased diode will give a large resistance to the electric

current. From the Table 3 all the photodiode variants have high resistance. PD4 stands out from the crowd with an even higher resistance with a resistance of 89 $E\Omega$. This high resistance is caused by the floating substrate in PD4 simulation.

Table 3 Reverse resistance of zero biased photodiodes

Photodiode variants	Reverse resistance
PD1 P+/N-well/P-sub	6.174e13
PD2 N+/P-sub	5.707e13
PD3 N-well/P-sub	6.174e13
PD4 N-well/P+	8.926e19

2.1.3.9 Bandgap energy

The energy band gap diagrams for the photodiodes are shown in Figure 26. One can see from the graphs that the energy difference between the valence band and conduction band gap energy is always about 1.1eV, as expected for silicon. Both the cathode and anode contacts are zero biased for the simulation.

PD1 and PD4 each have two different PN junctions where PD2 and PD3 only have one PN junction. For the structures with two junctions, it is expected to have two breaking points and for the structures with one junction we expect only one breaking point in the graphs. The breaking point is the potential difference between the p-side and the n-side of the semiconductor.
The figures for PD1 and PD4 tells us that the valence and conductor energy levels drop when we move 0.4μm into the substrate. This is where the PN junction between P+/N-well is located. The energy levels increase again when we move further into the material where the PN junction area between N-well/P-sub is located. The graph’s structure is as expected.

Looking at the graphs for PD2, the valence and conduction energy levels drop slightly when moving through the PN junction at 0.4μm. This drop is expected, but it would be more assuring to see a more “aggressive” jump through the junction when compared to PD1 and PD4’s band diagram.

The graph for PD3 is slightly declining throughout the structure. It would be expected to see something like the 2nd junction energy level shift of the PD1 and PD4 for this graph. At first it was assumed this problem was linked to low P-sub doping concentration or the structure not being grounded correctly. However additional simulations showed that this was not the reason for the unexpected result.

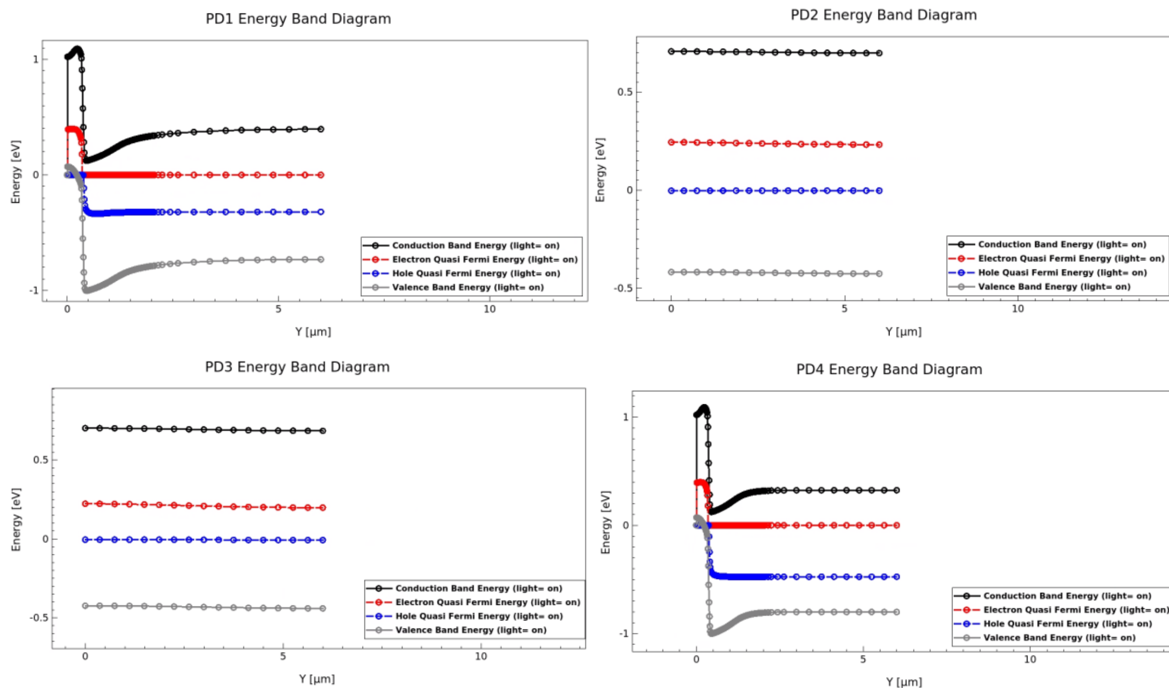


Figure 26 Energy Band Diagram

2.2 Cadence 180nm Design and Implementation

In this chapter the design of the image sensor will be discussed. The image sensor consists of four main components. The first component is the pixel array which consists of 16x16 pixels divided in four sections of 8x8 pixels with the four photodiode variants as previously simulated. In each pixel there is a NMOS source follower, reset transistor, and a select transistor. Selecting these pixels is done with the use of a row and a column decoder. Both decoders have 16 addressable outputs. The 16 column lines from the pixel array are connected to the column amplifier block at the bottom. This block contains the PMOS source follower needed to read out the pixel voltages. For reading out the voltages of the pixel array, an PMOS current source is added at the readout path. The output is analog and will be sampled and digitally converted on an FPGA. A top-level cadence diagram is shown in Figure 27.

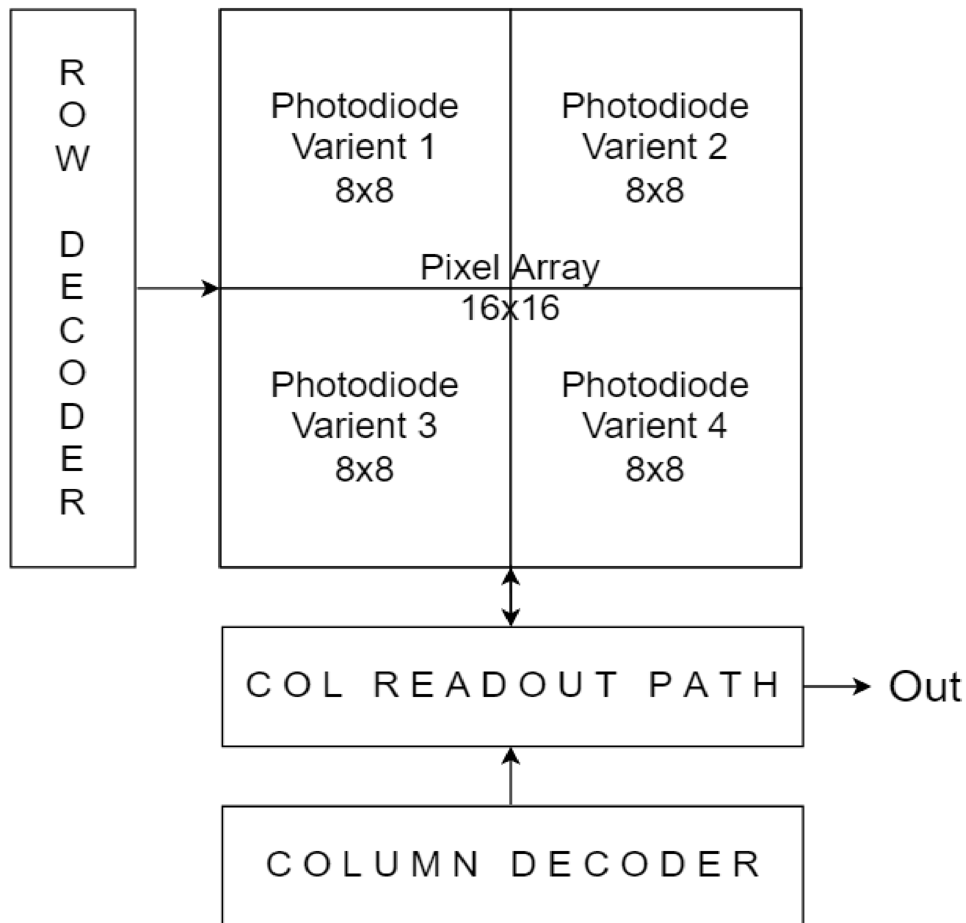


Figure 27 Top level design Image sensor

2.1 Pixel

The pixels designed are traditional three transistor (3T) active pixel sensors. This means there are no Tx or electrical shutters. The pixel does not consist of any PMOS transistors which would require more layout spacing for their separate N-wells to the photodiodes. The schematic of the 3T pixels is shown in Figure 28. The first transistor is the reset transistor (M1), the other one is the source follower transistor (M2), and the last one is the select transistor (M3). The last component is the photodiode that transforms the signal from light photons to electrons.

A “Reset” signal activates M1, which fills each pixel with energy (V_reset-Vth) that will be stored in a parasitic capacitor across the photodiode. The light that hits the photodiode will decrease the voltage stored in this capacitor. The lower the voltage across this diode, the brighter the pixel will look on the final photo. If the voltage stays high across this diode, the pixel will appear dark. When voltage across the photodiode is high, the gate voltage on the source follower will also be high. When “ROW_SEL” is high on the select transistor, the same current will flow through M3 and on to the readout circuitry.

Each pixel is relatively small but put together in an array they will fill most of the chip. It's important to occupy minimum transistor space to allow for a bigger photodiode and important to consider spacing between components as seen from the TCAD simulations.

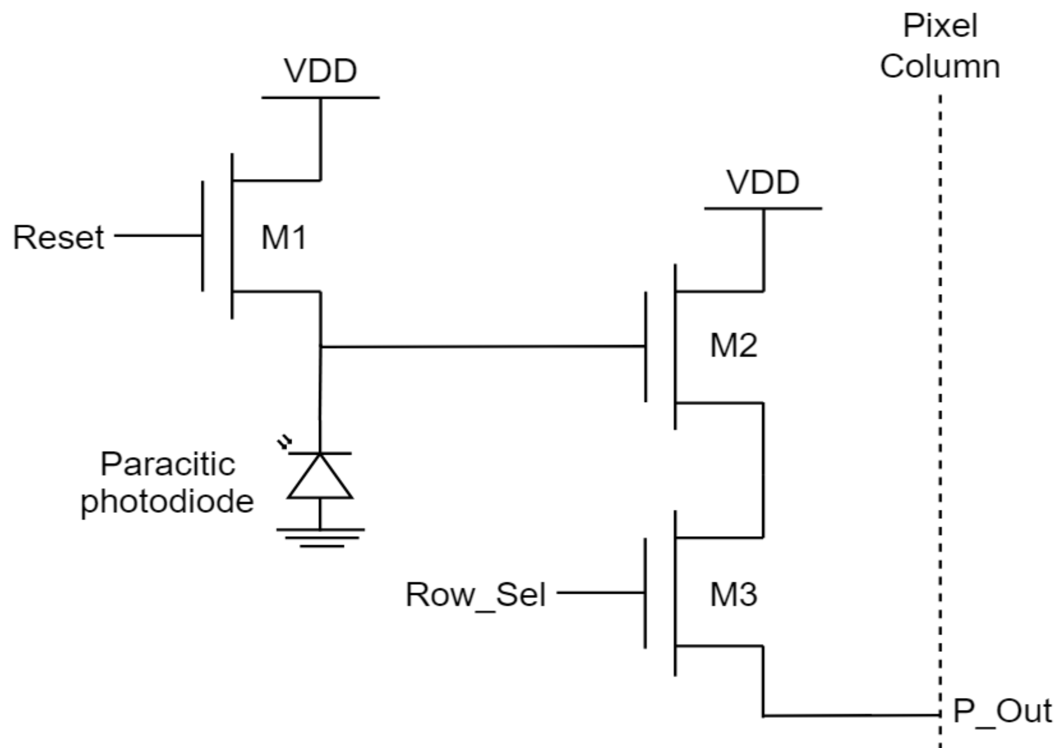


Figure 28 3T pixel

Table 4 Pixel transistor dimensions

Transistor	W/L (μ)
M1	2/0.18
M2	2/0.90
M3	2/0.18

Reasoning behind the transistor sizing in Table 4, is that the increased area for transistor M2 will give a higher transconductance and improve the linearity. Optimally the gain should be "1" and this is achieved by having high transconductance. However, when increasing the transistor area, 1/f noise will increase, and the potential photodiode fill factor of the pixel will decrease.

2.2 Decoders

The pixel array consists of 16x16 pixels; therefore a 4-bit row decoder and a 4-bit column decoder is needed to be able to select all pixels. Some of the design and layouts are based on the 3-bit decoders used in Magnus FD Drageseth's thesis [19].

The 4-bit demultiplexer in Figure 30 is created by using the demultiplexers from Figure 29 alternating between the variants for every row. The complete 4-bit demultiplexer outputs a single high signal out of the 16 outputs corresponding to the 4 bits selected "SEL_<0-3>" effectively making the circuit a decoder. The decoder is not a gray code decoder and there are a few glitches present when switching between states. Particularly when there are few bits in common between the switched states. The glitches last for a very short period (picoseconds) before it stabilizes. This should not lead to any problems in the system because there is no need to operate at that speed. A gray code decoder would not have had any speed advantage, but it would make the transitions smoother when going through the array in the predetermined order without the risk of short intermediate states.

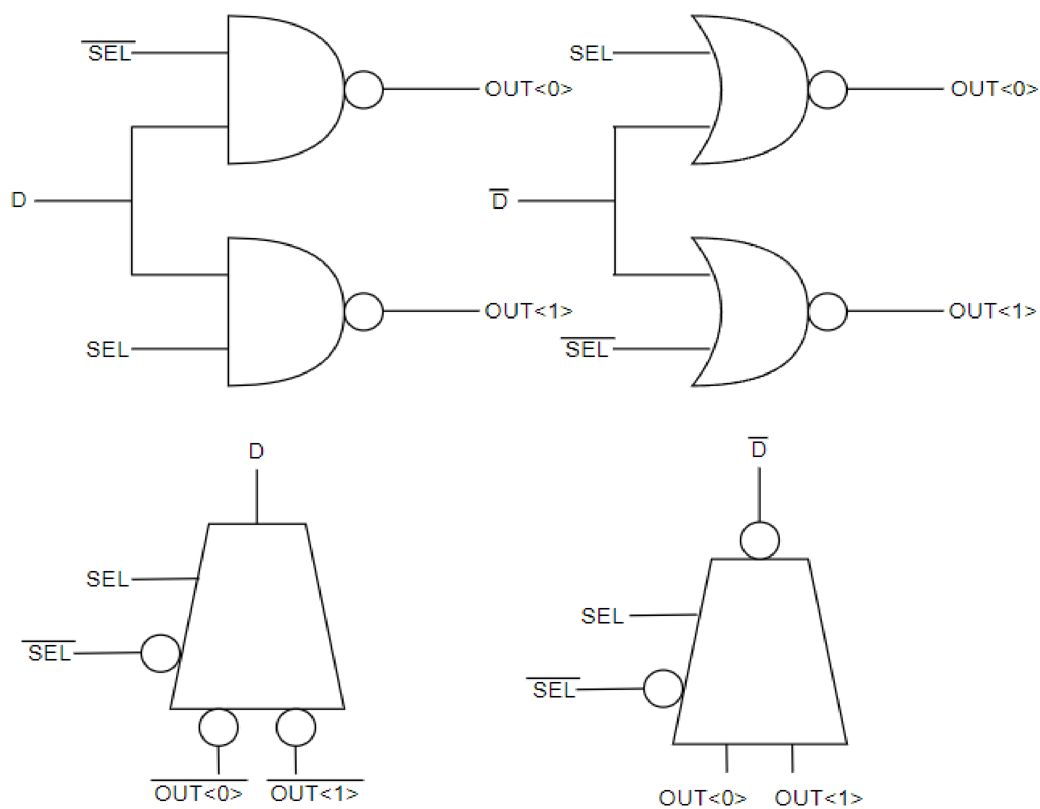


Figure 29 a,1 to 2 demultiplexer implemented using NAND b,1 to 2 demultiplexer implemented using NOR

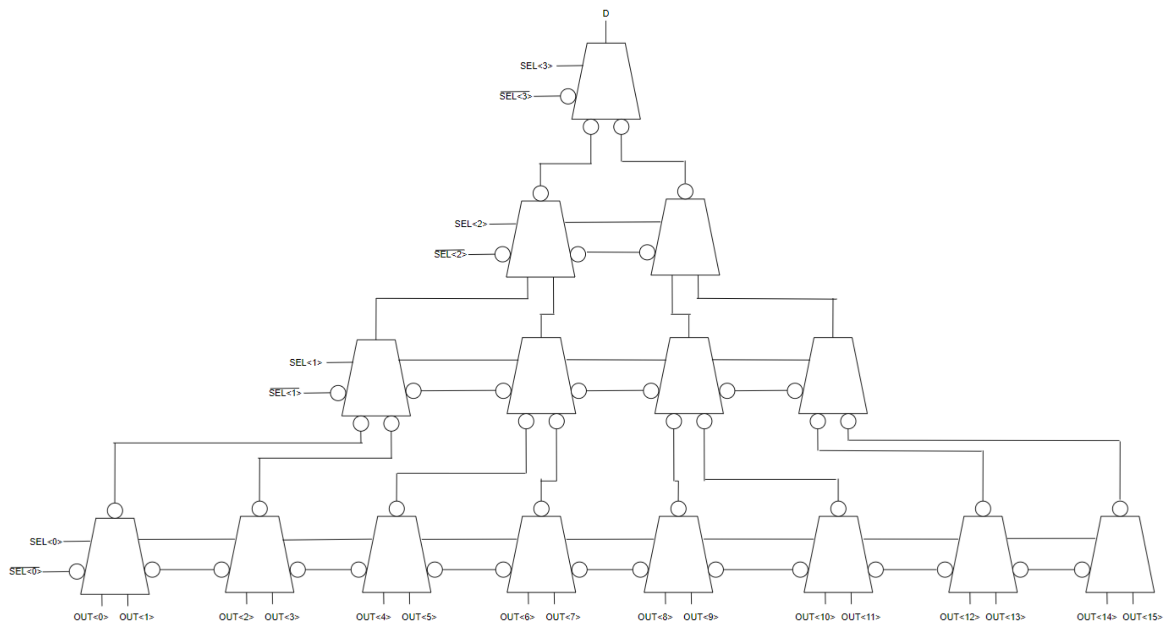


Figure 30 4-bit demultiplexer

2.3 Column amplifier

The column amplifier and the voltage readout in the next chapter is based on two former master theses. One made by Kristian Geli Nilsen with the title “Visible light communication CMOS image sensor for automotive applications” [20], and the other one is Magnus FD Drageseth’s thesis [18].
The schematic of the current source used at the bottom of every pixel column is shown in Figure 31. This circuitry consists of a NMOS current source M4, a PMOS source follower M5 and a column select transistor M6. P_Out is where the pixel column is connected to the current source and the PMOS source follower. The NMOS current source keeps the current constant while forcing the source of the source follower transistor in the pixel to follow the gate. The PMOS source follower is then connected to a column select transistor. C_out is connected to a horizontal output line that is connecting all the column amplifiers together.

The PMOS source follower is used mainly for its low output resistance. Usually, it also provides high current gain, but the current does not change much in this case. Connecting the bulk of the PMOS source follower to the source as seen in the figure will eliminate the body effect and increase the voltage gain closer to “1” but increase parasitic capacitance. Also, the large transistor widths chosen are less susceptible to process variations and mismatch.

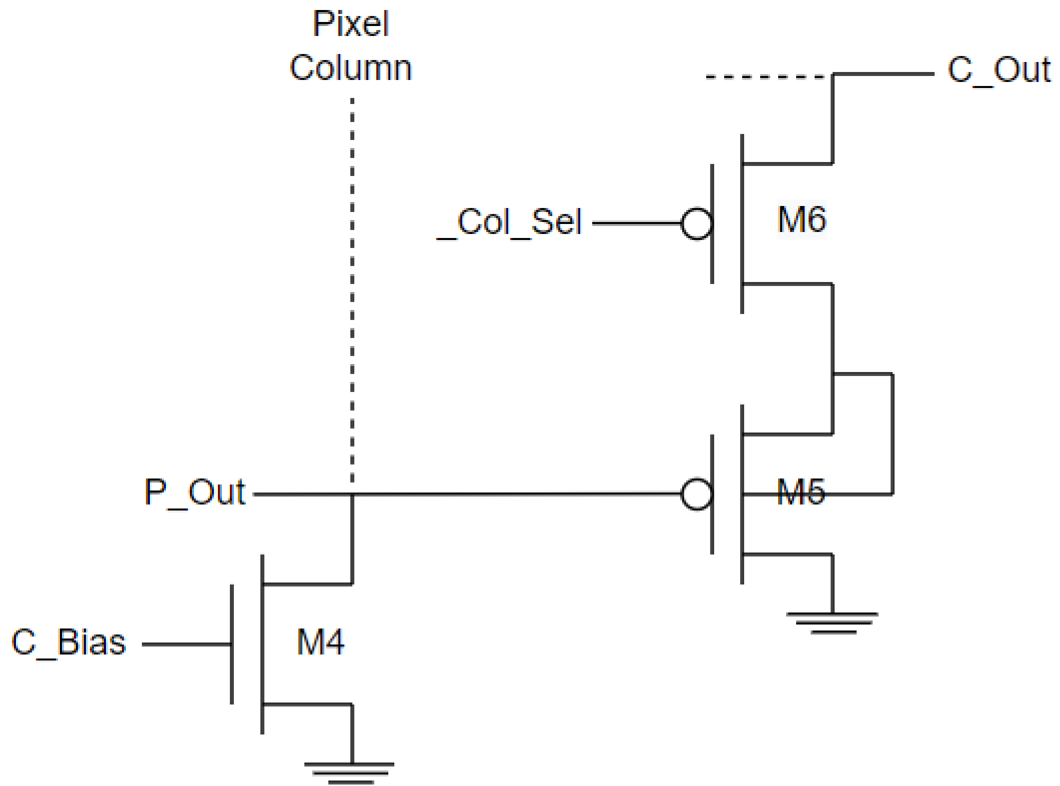


Figure 31 Schematic current source.

Table 5 Dimensions column amplifier transistors

Transistor	W/L (µ)
M4	2.6/0.18
M5	21/0.90
M6	7/0.18

2.4 Voltage readout path

The voltage readout path for the system is shown in Figure 32. M1, M2 and M3 are common for each pixel. M4, M5 and M6 which are common for each column amplifier and M7 is needed for the output signal. Together, the “column” and “output” shown in the figure make up the column readout path. As mentioned earlier, the NMOS source follower is used to route the signal from the selected row to the column line, and the PMOS source follower routes the signal from the selected column to the horizontal output line that is connected to

all the column selects. M7 is another current source for the output line that draws current from VDD.

C_ BIAS was set to 600mV and the OUT_BIAS was set to 1.1V. This gives a sufficient bandwidth with no overshoot. The input output graph for the readout path is shown in Figure 33 and is linear for the operating conditions between 0.4 - 1.2V input.

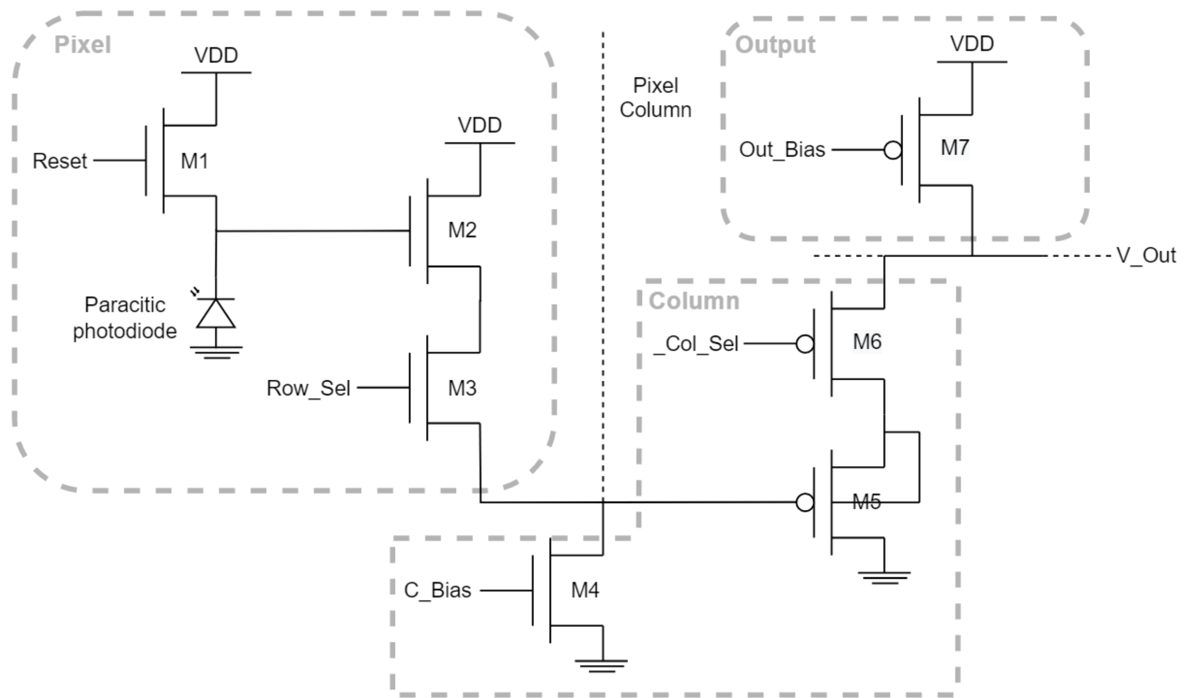


Figure 32 Voltage readout path

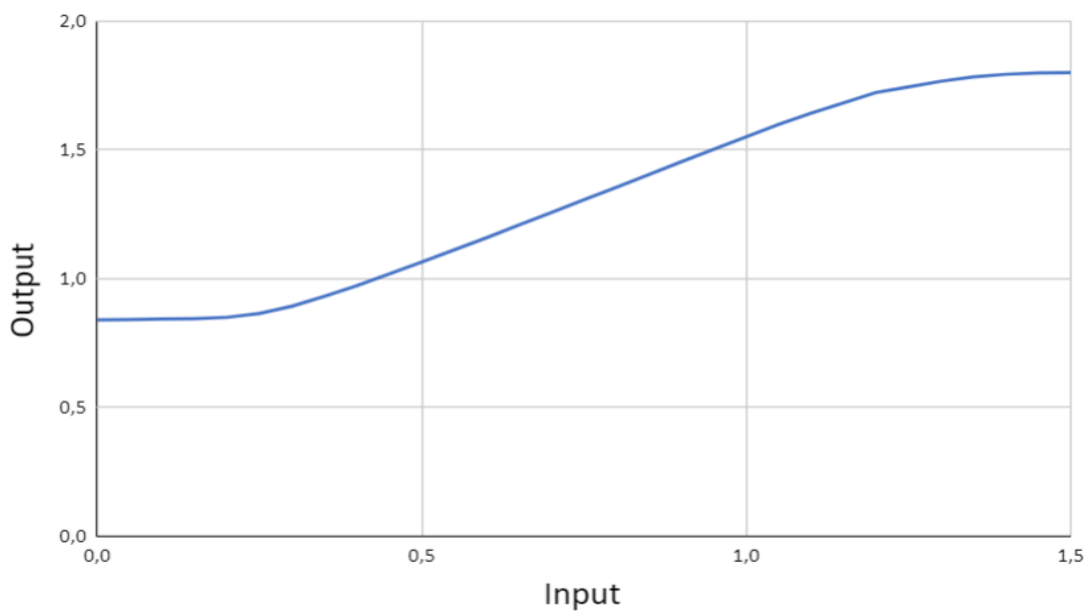


Figure 33 Input output readout path linearity

III Layout

3.1 Pixels

There are a total of 256 pixels in the pixel array. Every pixel has metal connections in horizontal and vertical lines to connect to neighboring pixels in most of the metal layers. This makes a good supply of VDD and GND for the pixel array, together with options for easy implementation of increasing the array size with more pixels.

A reminder on the photodiode structures can be seen in Figure 36. Each pixel layout consists of three transistors and one of the photodiode variants and can be seen in Figure 34 and Figure 35. The reset transistor is placed in the upper left corner, the source follower in the top right corner and the select transistor is beneath the SF. The photodiode is placed in the middle of the pixel and the area allocated is about 26μm x 26μm of area. The size of each pixel is 36μm x 36μm which makes the fill factor of the photodiodes to be about 52%. Looking at the photodiode layouts, the white layers are N+, the thicker white layers are the N-well, the purple layer is the P+ and the green layer is the salicide block. Other exclusions were made in top layer layout and discussed in the next chapter.

The reasoning for not putting a large metal layer over the grounding parts of the photodiode (bottom part) that would ensure better contact, is that from the TCAD simulations the depletion region extended to these grounding contacts for some of the simulations. If this part were covered, the active area of the photodiode would reduce. The photodiodes in layout were also kept as close to the photodiodes from the TCAD simulation for better comparison. The substrate is grounded in different places on the chip, so it is a possibility to skip using this extra grounding for each photodiode. This would increase the available space for the photodiode that could give a better fill factor. However, from the TCAD simulation it showed that sufficient and correct grounding of the substrate is important for performance. PD4 is similar to PD1 but without the extra substrate grounding contact. It will be especially interesting to compare these variants on the produced IC.

The pitch of the pixels matches the pitch of the column and row decoders of 36μm.

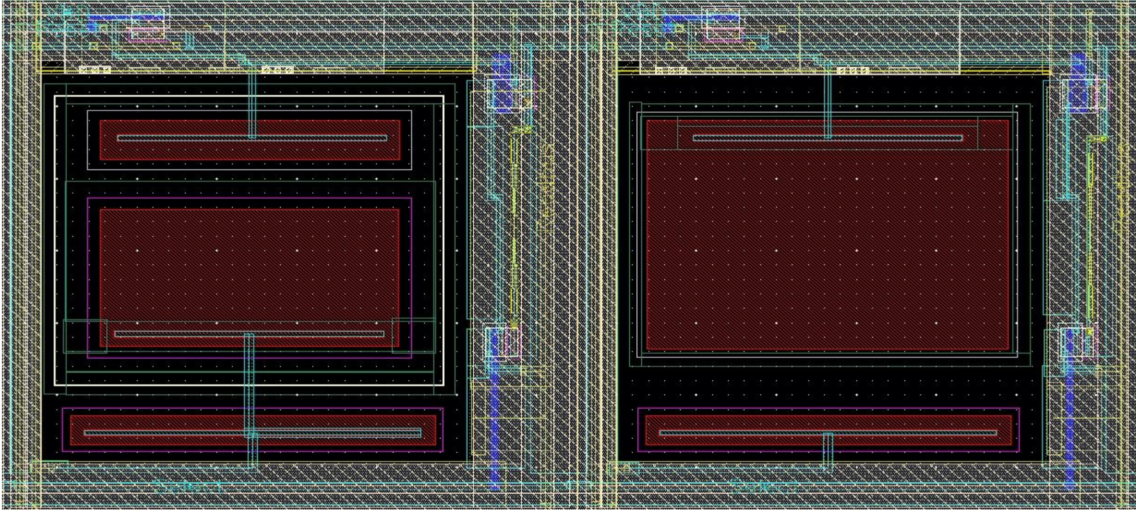


Figure 34 Pixel layout PD1&PD2

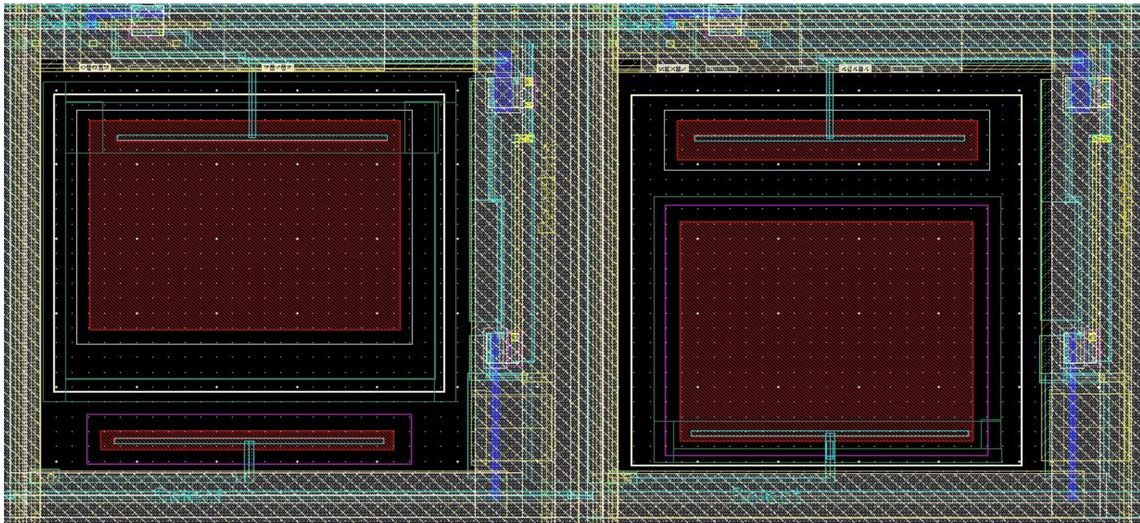


Figure 35 Pixel layout PD3&PD4

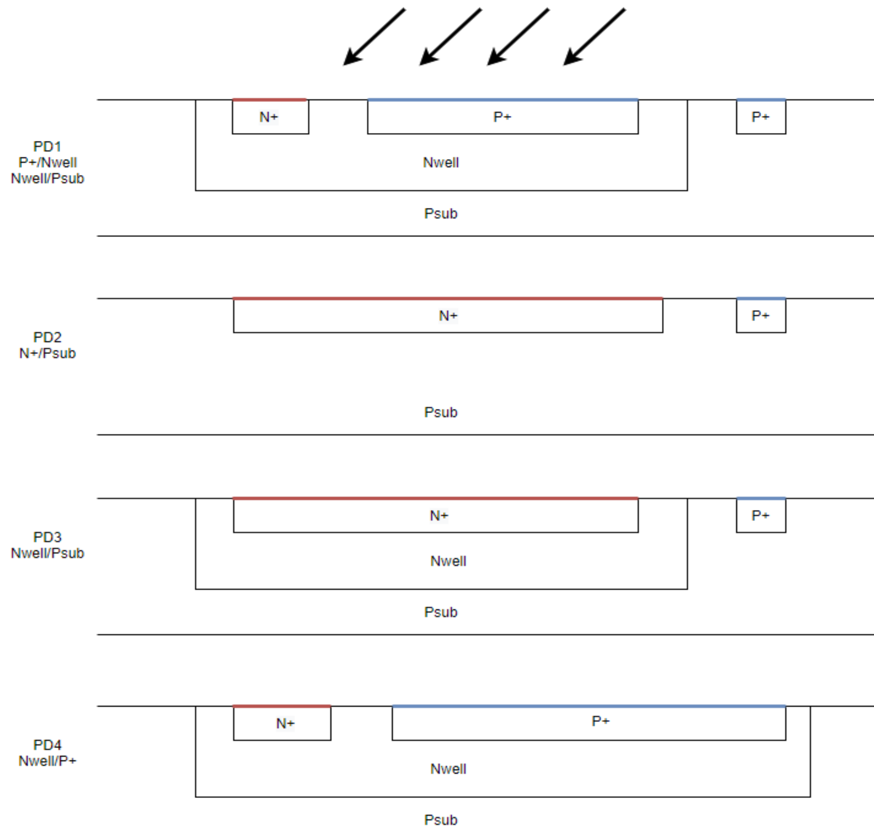


Figure 36 Photodiode variants reminder

3.2 Pixel array

The pixel array consists of 16x16 pixels. The array is built up by the four different photodiode pixels that each consist of 8x8 pixels and take up each corner of the design. They are horizontally and vertically stacked as shown in Figure 37.

Exclusion zones were created around the pixel array in top view layout to prevent this area over the photodiode to be filled with dummy metal. All other regions of the IC should be covered with salicide, and dummy metal to fulfill density rules.

The exclusion used over the pixel array were:

- ODBLK;drawing
- POBLK;drawing
- MDEXCL;dummy1-6
- Salicideblock RPO (over the photodiodes only)

With the exclusions over the array DRC density rules would have been a problem, but because of the additional metal 1-6 that was filled in the array to supply VDD and GND, the requirements were met. This metal also worked as a barrier to help prevent some of the light from shining through between the photodiodes.

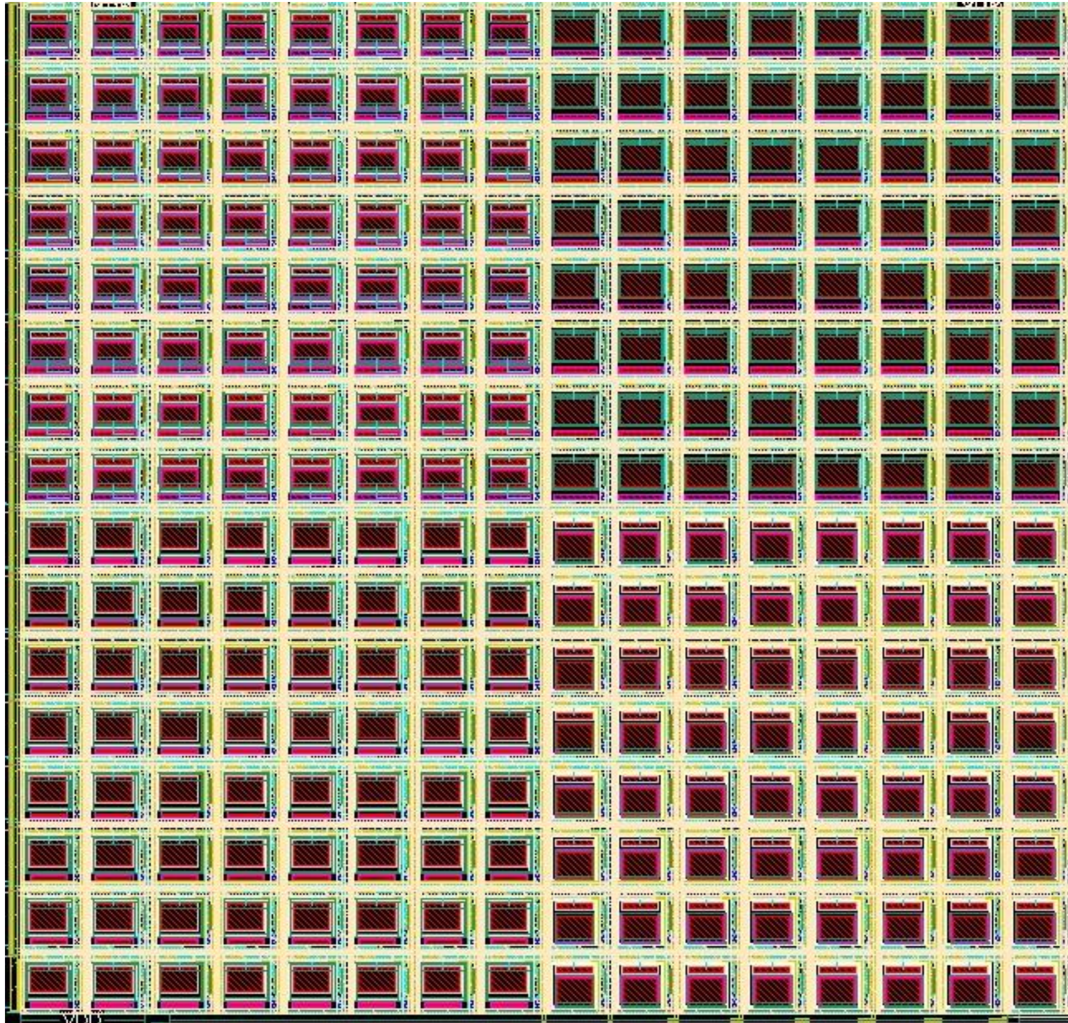


Figure 37 Pixel array layout

3.3 Decoders

The layout of a single 4-bit column demultiplexer is about 560µm x 17µm and shown in Figure 38. It is difficult to visualize the entirety due to its size. The layout for the row decoder is shifted 90° compared to the column decoder.

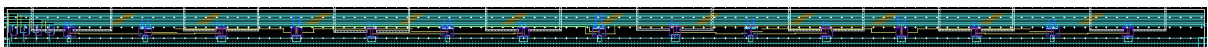


Figure 38 Column decoder layout

The NOR gate and NAND gate demultiplexer variants from the column decoder are shown in Figure 39. A more detailed figure of the demultiplexer variants is shown in Figure 40 and Figure 41. The NOR demultiplexer variant layout consists of two NOR gates combined, like shown in the schematic in Figure 29. And the NAND variant layout consists of two NAND gates combined.

The NAND and NOR demultiplexer requires both an inverted and non-inverted version of the select signal. The inverted "_SEL<0:3>" signals are created by using four inverters together with the SEL<0:3> signals as shown in Figure 42. The digital input lines SEL<0:3> and _SEL<0:3>, are routed horizontally in metal 1 layer. The outputs are routed in metal 5 out from the NOR demultiplexer with a pitch of 36µm to match the pixel pitch.

To pass the Antenna Design Rule Check, vias were made going between metal 1 and metal 2 on the input lines. The effect of charge accumulation in isolated nodes of an integrated circuit during its processing is known as Antenna effect. If a long route is connected to a MOSFET with a thin oxide, it might cause damage to the transistors and degrade its performance [21]. Therefore, it is beneficial to break up the long routes into shorter sections or use different measures that will help to discharge any significant potential buildup.
It would have been better to design the metal lines from the inverters to be wider. The thin lines might affect the inverted select signals from the inverter to be slow.

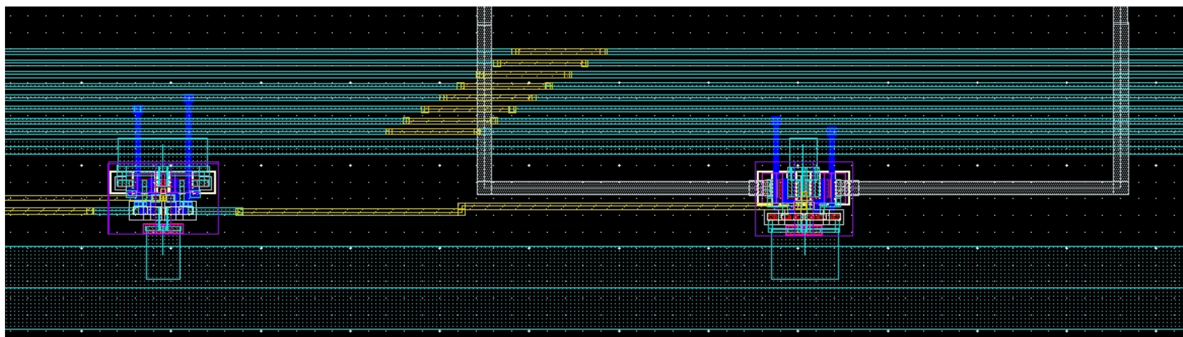


Figure 39 NOR AND NAND gate demux variant layout

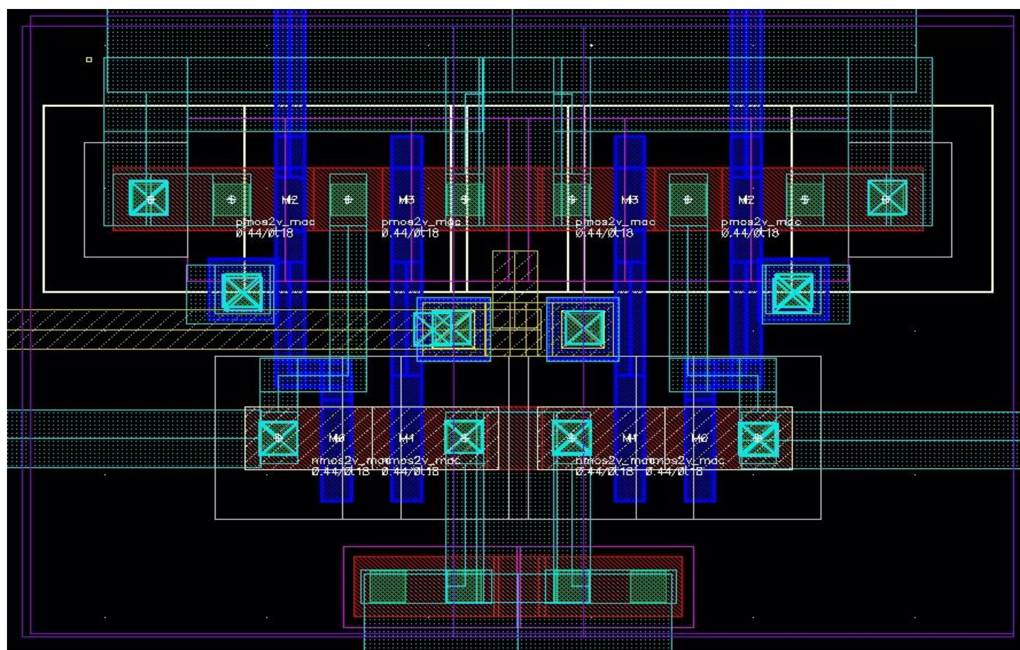


Figure 40 NOR gate demultiplexer variant layout

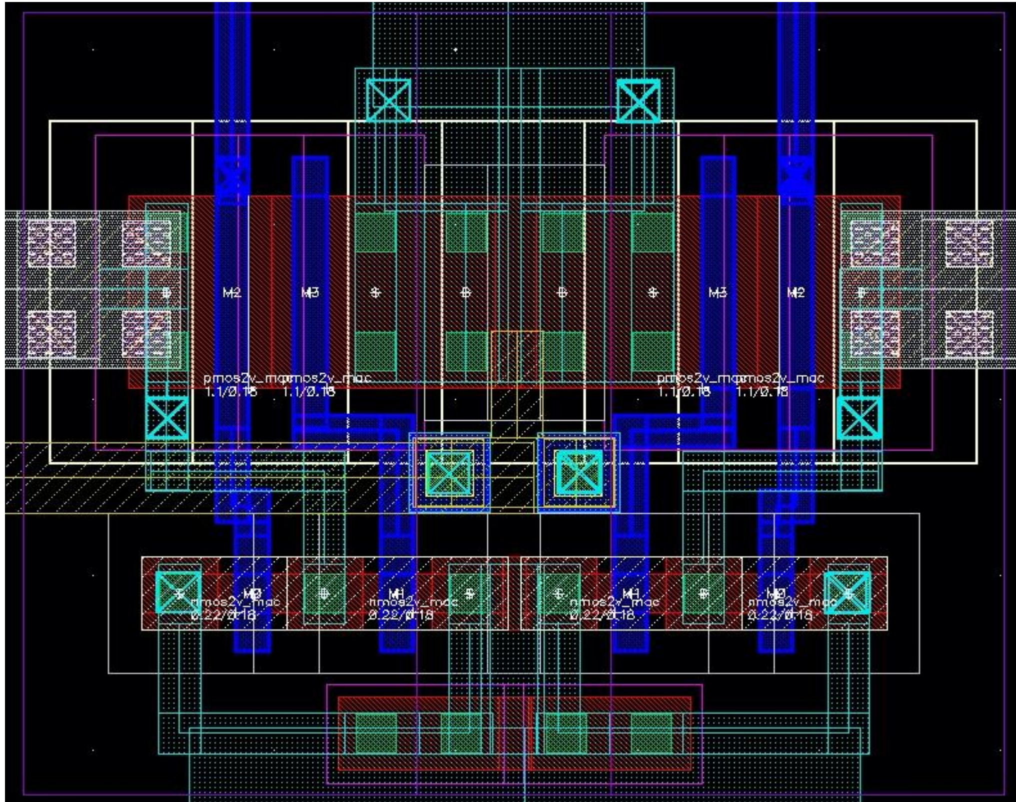


Figure 41 NAND gate demultiplexer variant layout

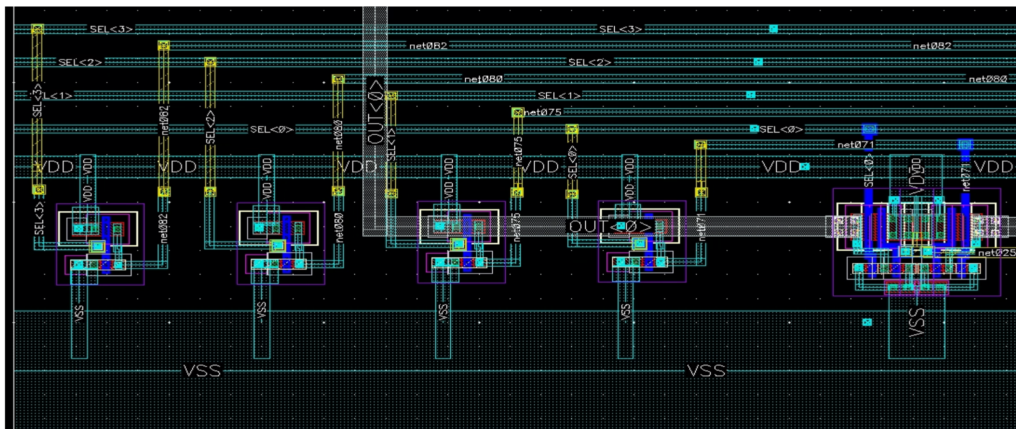


Figure 42 Inverters for select signal layout

3.4 Column amplifier

The layout for the column amplifier is shown on Figure 43 and consists of a current source, a PMOS source follower and a column select transistor. In Figure 44 the entirety of one column amplifiers is shown.

Figure 43 Full column amplifier layout

The supply for VDD, VSS, C_BIAS and V_OUT runs horizontally across the bottom or top of the column amplifier. C_BIAS is connected to the gate of the current source that is placed at the bottom left of every column amplifier. The pixel column line is connected to the drain of the current source and to the gate of the PMOS source follower. The PMOS source follower is connected to a PMOS column "_Select" transistor. The _Select signal comes from the column decoders combined with an inverter that is visible in the bottom of the figure, before connecting to the gate of the select transistors (net80).

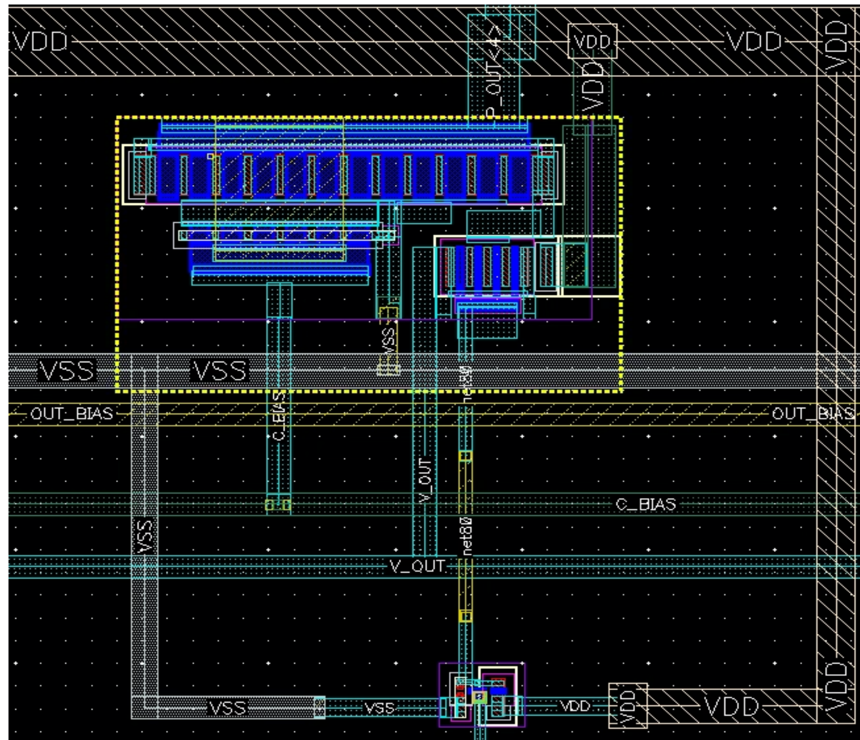


Figure 44 Column amplifier layout

3.5 Readout

Figure 45 shows the readout circuitry for the last column amplifier and the output current source. The large PMOS transistor on the right is the current source for the output line. The horizontal line in metal 2 connects the gate of the current source to the OUT_BIAS. VDD is connected to the drain of the current source. The horizontal output wire V_OUT is connected to the output current source and all the column amplifiers and then connected to a pad.

It would have been ideal to include an output buffer to drive the capacitive load of the pad. Time fell unfortunately short before the closing stages of tape out for this to be implemented. However, a larger bias current can be chosen for more drive but resulting in reduced gain.

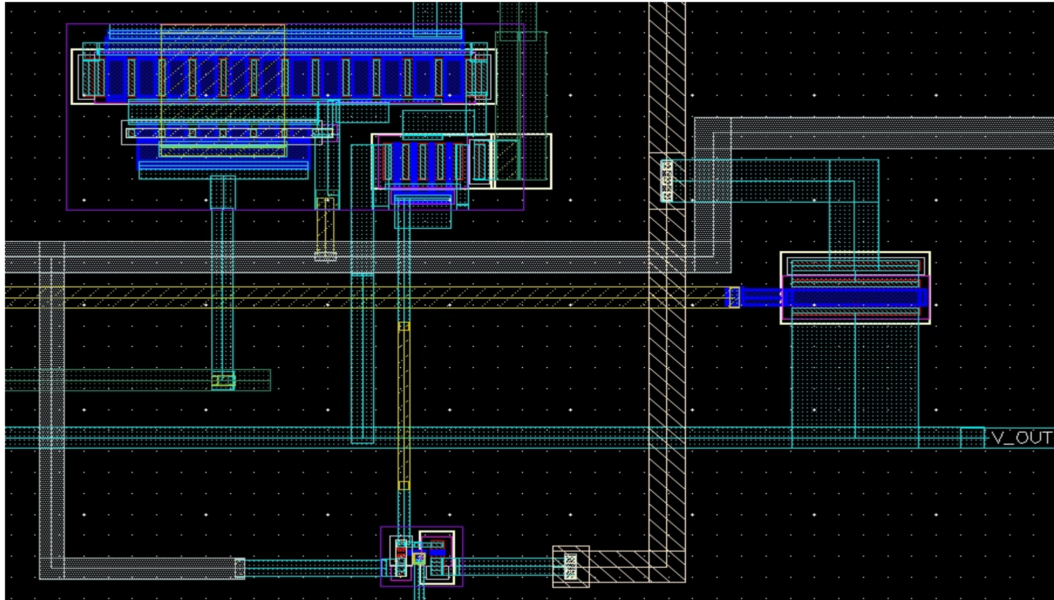


Figure 45 Column amplifier and output current source layout

3.6 Extra Testability

A separate single test pixel was included in the design for extra testability if there should be any problems with the decoders and/or the readout path shown in Figure 46. The test pixel has a separate reset, select and output from the rest of the array and is of the PD4 structure. Additionally, two points out from the pixel column lines (before the readout circuitry) was routed to pads for testability.

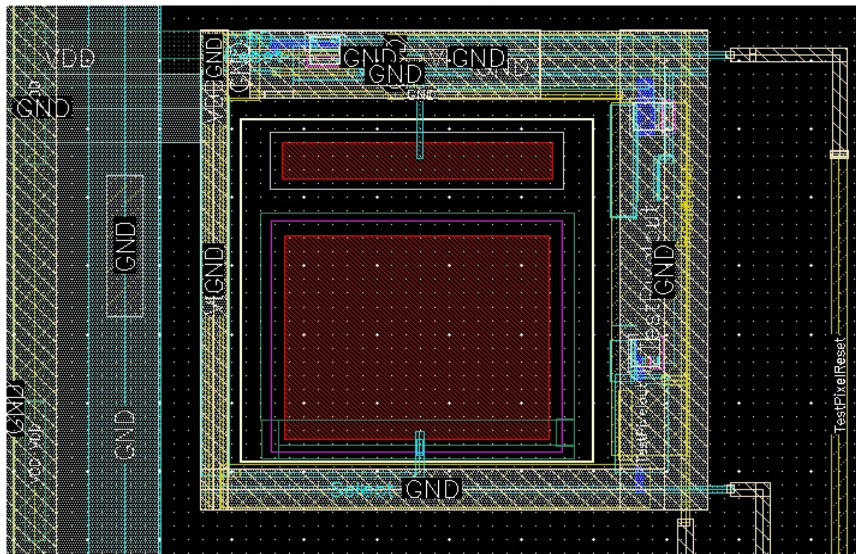


Figure 46 Test pixel layout

3.7 Pad Frame

The layout of the entire design on the pad frame is shown in Figure 47. The image sensor is placed in the bottom left corner surrounded by decoupling capacitors. The rest of the usable space on the pad frame was assigned to be used by another student. The pad frame consists of 78 usable pads, divided into VDD pads, ground pads, analog pads, and digital pads after demand. In Figure 48 the layout is shown in more detail. The pad frame has about 1620µm x 1540µm of usable area. TSMC is the producer of the chip.

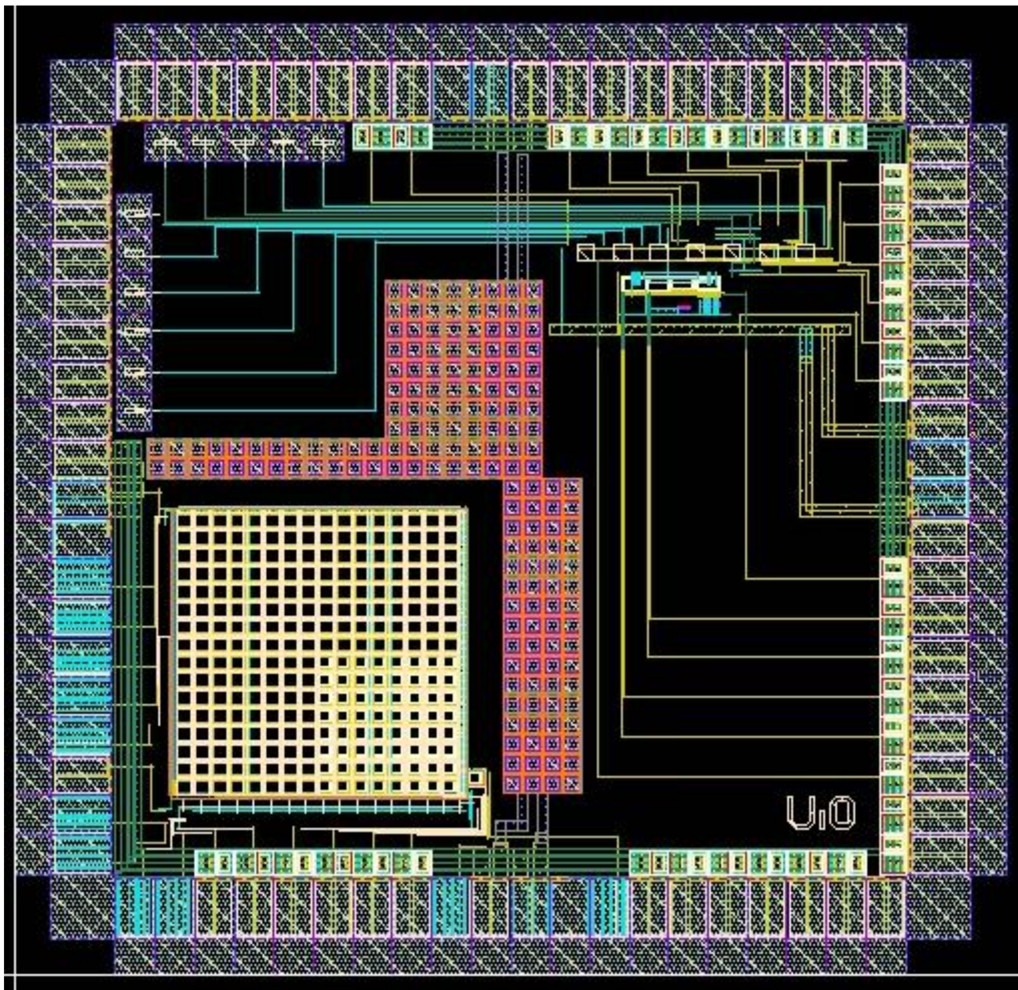


Figure 47 Full chip layout

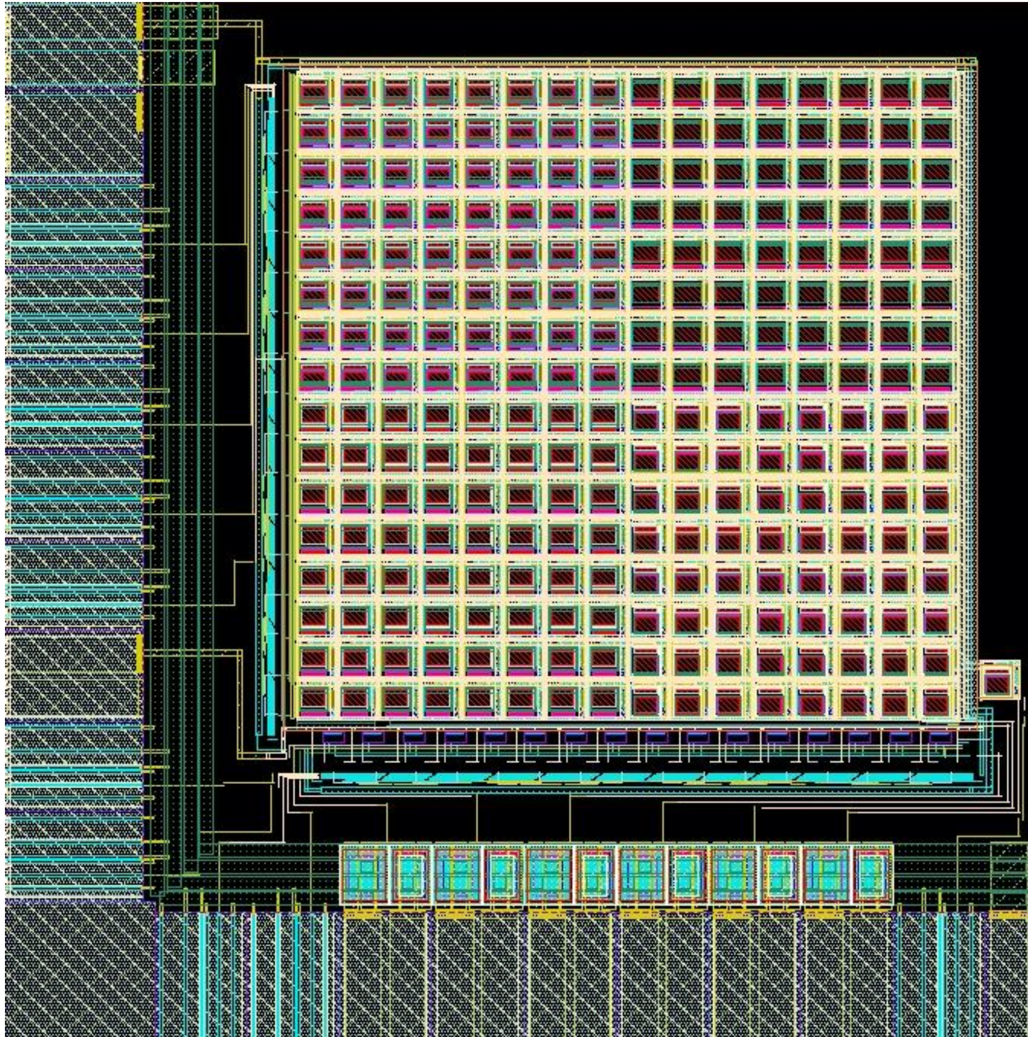


Figure 48 Design in focus layout

3.8 Package

The package used is a JLCC84. The bonding diagram between the pad frame and the package is shown in Figure 49 and the bonding is left to Interuniversity Microelectronics Center (IMEC) to do. The die thickness is 11 mils which is almost 280μm.

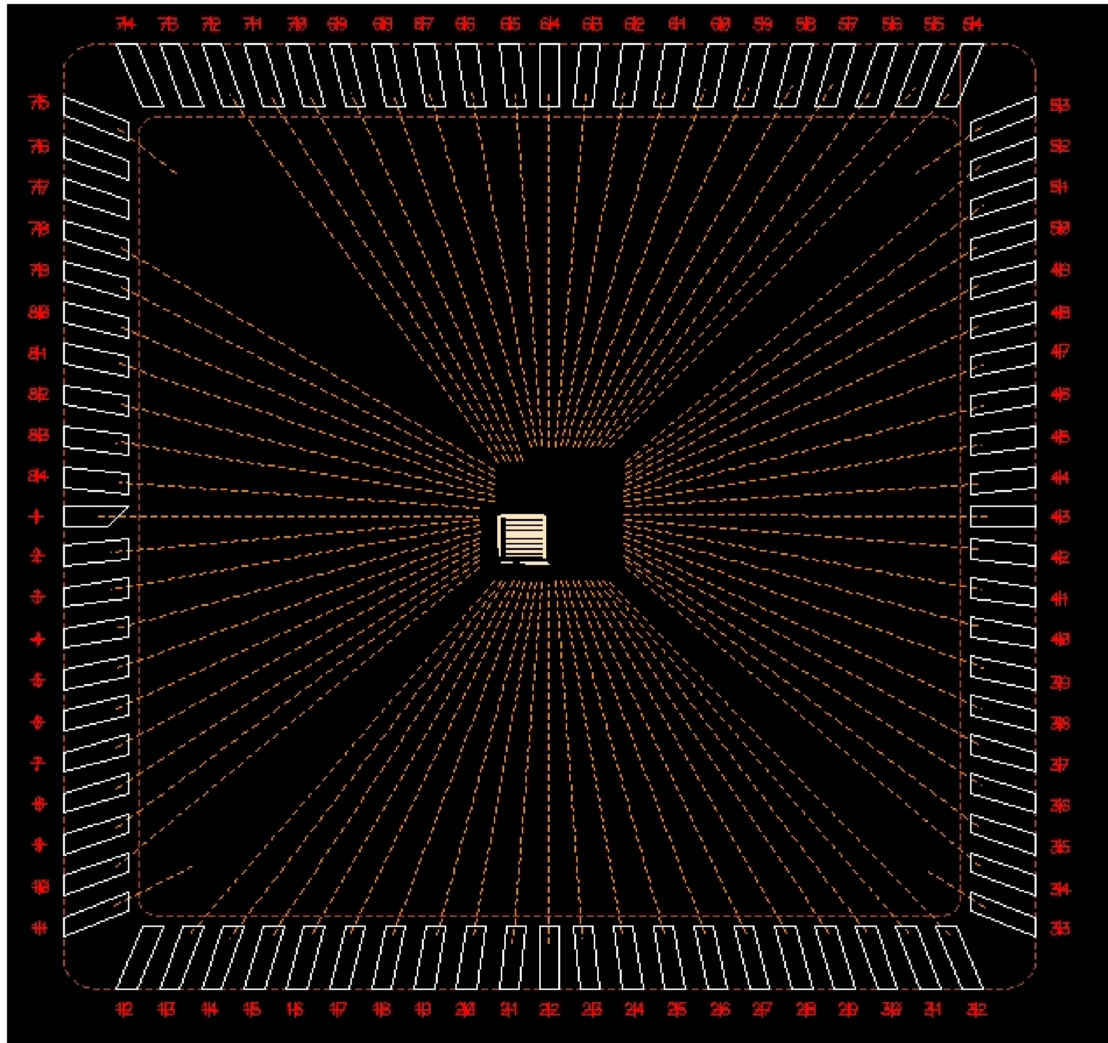


Figure 49 Bonding diagram

IV Printed circuit board

To interface and test the IC, custom PCBs were designed. Both schematic and layout were created with Eagle. The PCBs consist of 4 layers with power and ground in the inner layers and routing on the top layers. Both surface mount devices (SMD) and through hole components were used.
There were three versions of the PCB produced. On the first PCB some of the routing was incorrect and the board scraped. The second PCB was designed to be used together with the FPGA with the ability to slot connectors into the FPGA. On the third PCB, the digital signals can be switched manually without the need of an FPGA.

4.1 Schematic

The schematics for the second PCB are shown in Figure 50. Most of the components are placed on top of the circuit board. This includes a socket for the JLCC84 package, voltage regulators, potentiometers, passive components, test pins and decoupling capacitors. On the bottom of the board a 160 pins connector is placed to clip into the FPGA. This connector is swapped out with dip switches for the third PCB.
The voltage regulators used are the lm317. The regulators are connected to a ceramic and electrolytic capacitor on each side of the regulator to ensure stability. The voltage regulators generate analog VDD and ESD protection. On the third PCB an additional voltage regulator is added to generate digital VDD. The resistor values are calculated using the general equation shown below:

$$Vout = 1.25V(1 + \frac{R2}{R1})$$

The bias voltages are set using potentiometers connected between VDD and GND. The analog out signals is routed to a PMOD connector for all boards and the digital signals are routed to a 160-pin connector for the second board. Additionally, several decoupling capacitors were added for VDDs, 3.3V and bias voltages.

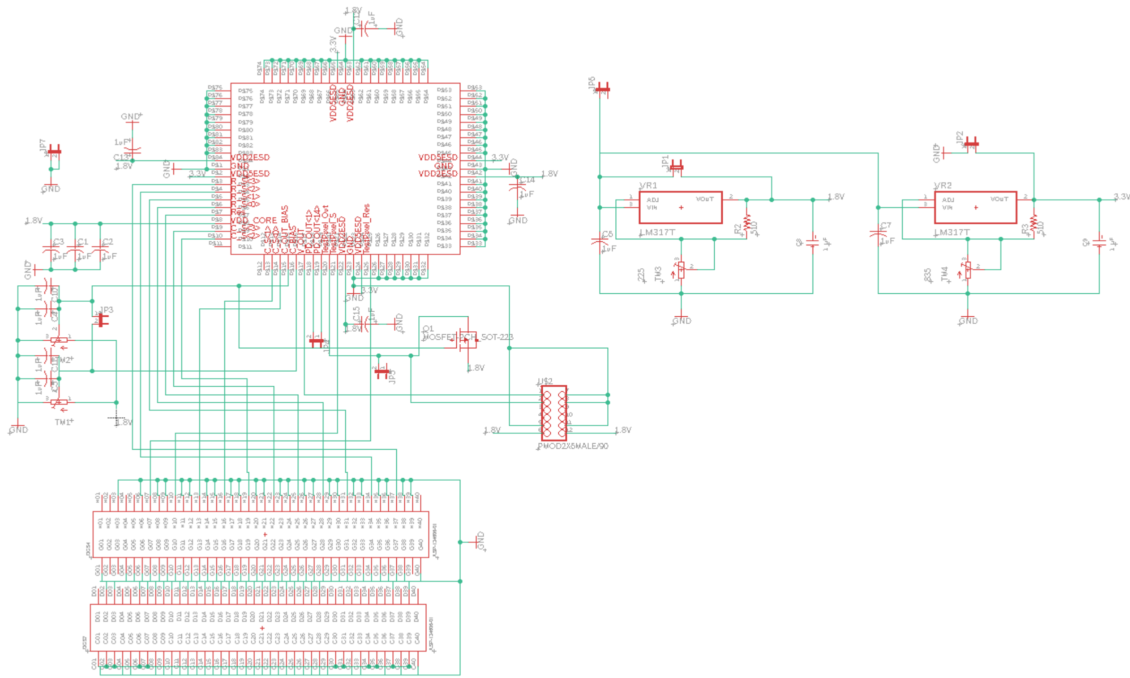


Figure 50 Second PCB schematic

4.2 Image sensor

The image sensor package is mounted in a JLCC 84 socket as shown in Figure 51. The pads allocated for the image sensor are on the left and bottom side of the package. The pads on the top and right side are allocated to another student's design. Not every pad allocated to the image sensor has been used. Pin location is shown in Table 6.

The package is to be supplied with a core VDD for 1.8V, ESD protection for 1.8V and 3.3V and bias voltages. The analog signals are connected to a PMOD connector, and the digital signals are routed to the 160-pin connector as previously mentioned. A lens on a mount will be fitted to the image sensor to focus the light onto the image sensor.

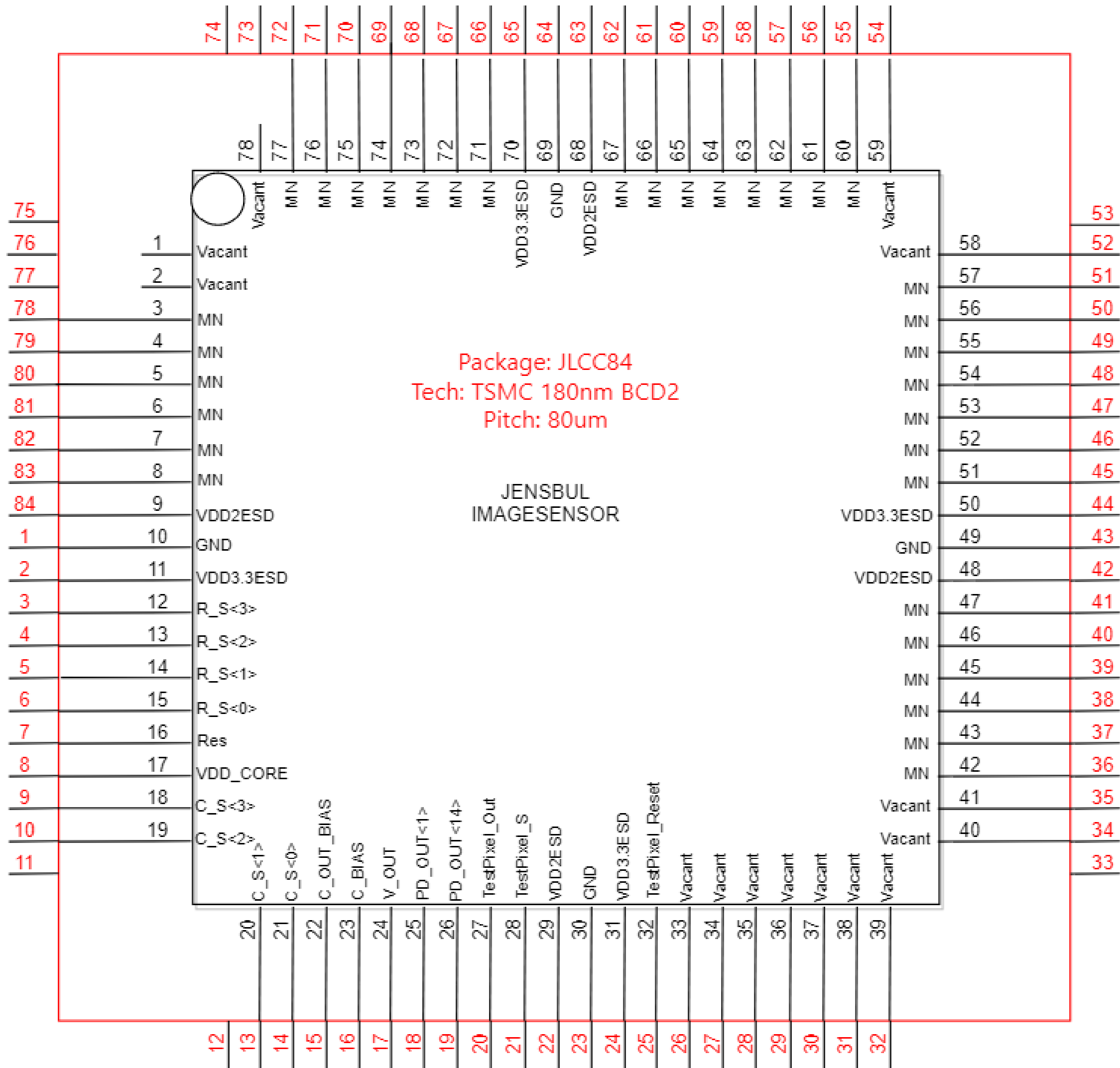


Figure 51 Image sensor symbol

Table 6 Image sensor pin location

Pin	I/O	Description
VDD2ESD	Input/Output	2V ESD protection for the pad frame
GND	Input/Output	GND
VDD3.3ESD	Input/Output	3.3V ESD protection for the pad frame
R_S<0..3>	Input	Digital Row select
Res	Input	Digital Global reset for the pixel array

VDD_CORE	Input/Output	VDD
C_S<0..3>	Input	Digital Column select
C_OUT_BIAS	Input	Out bias
C_BIAS	Input	C_bias
V_OUT	Output	Output for the image sensor
PD_OUT<1>	Output	“colum 1 Pixel array out”
PD_OUT<14>	Output	“colum 14 Pixel array out”
TestPixel_Out	Output	Output for the test pixel
TestPixel_S	Input	Digital Test pixel Select
TestPixel_Reset	Input	Digital Test pixel Reset

Two of the produced and assembled PCBs are shown in Figure 52. The one to the left is the third board (with lens and lens mount fitted) and on the right is the second board with the FPGA 160 pin connector on the opposite side of the board.

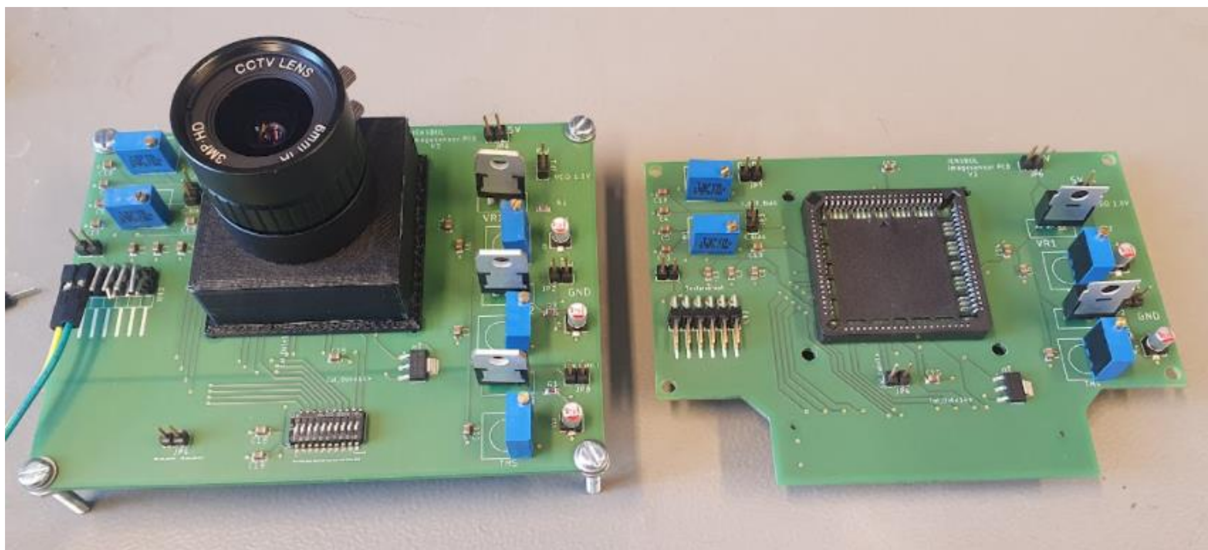


Figure 52 Assembled PCBs

4.3 PCB Layout

The layout for component placement and routing is shown in Figure 53 for the second board. Screw holes were added in the corners of the board and around the package for fixing the board securely and for mounting of the lens.

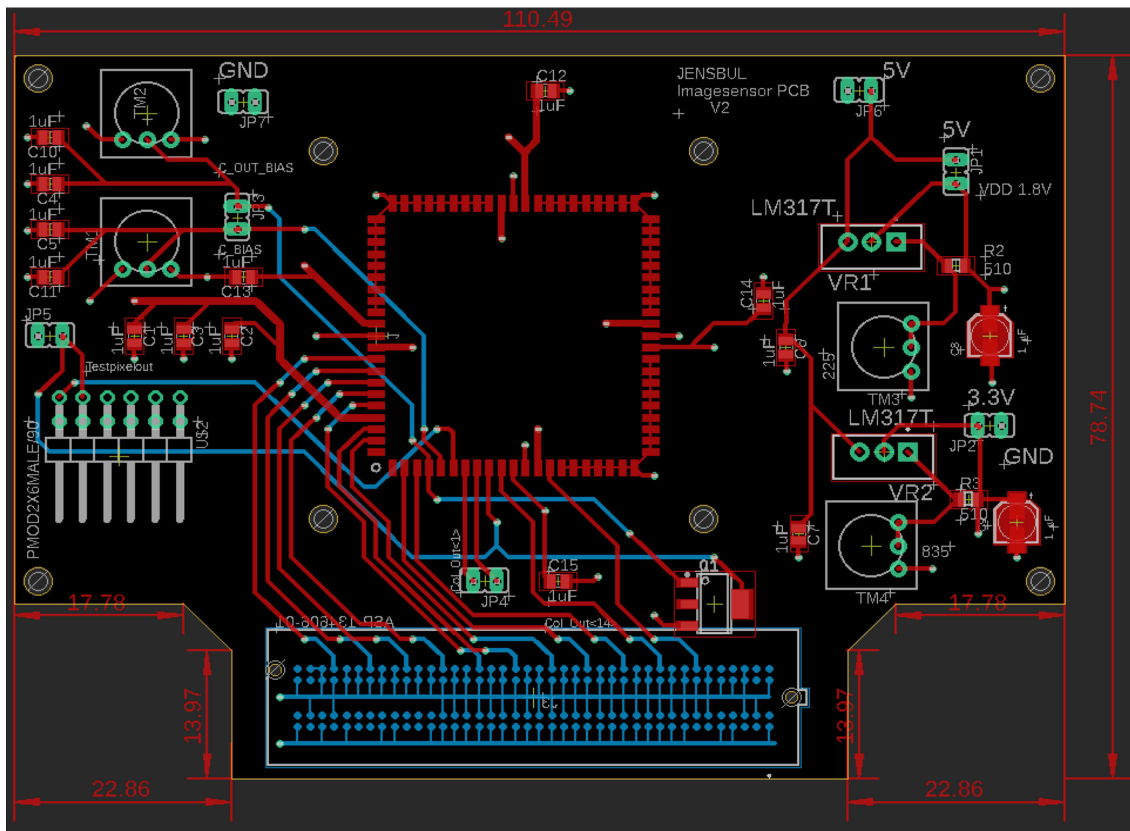


Figure 53 Second PCB layout

4.3.1 Power and ground layers

Eagle provides multiple layers PCB design with options of blind, buried or through vias. The two inner layers, 2 and 15, are dedicated to power and ground respectively,
see Figure 54 and Figure 55 for layout. The power layer is split into two parts for the board, 1.8V and 3.3V respectively. With this layer setup, we get a simple power and ground routing to the targeted areas compared to having them on the outer layers. For the third board this layer is split into three parts including 1.8V digital. The placement of SMD and wiring would need to be taken into consideration if the power and GND were on the outer layers. Another advantage with the current setup is that the power and ground planes create two plates with opposite voltage, which gives us a capacitive effect. This allows more current to be fed from the power plane without dropping voltage. This same effect can also be achieved by placing

decoupling capacitors. The inner layers work as an insulation between the two outer layers, so routing in the outer layers will not induce much field noise between the layers.

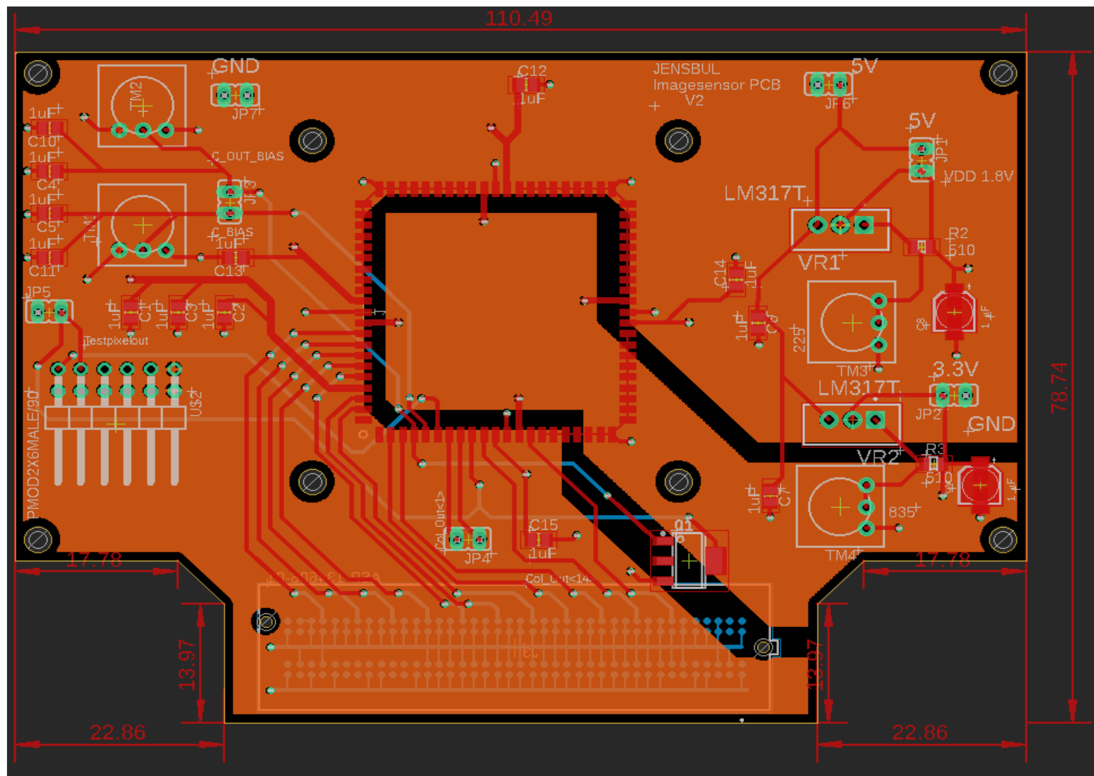


Figure 54 Power layer layout

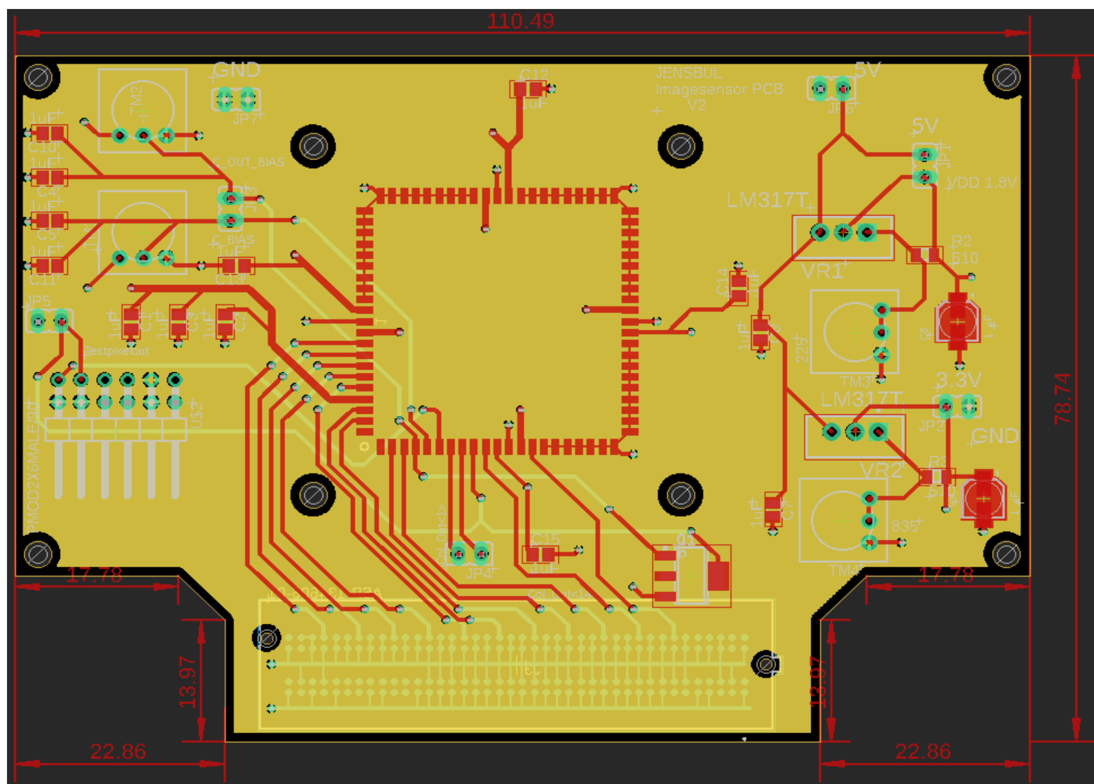


Figure 55 Ground layer layout

4.4 PCB assembling and Testing

The assembly and testing process were done at the University of Oslo department of informatics. The PCBs were ordered together with stencils and the required components for assembly.

The assembly process started with fixing the stencil on top of the board and applying solder paste on the SMD contacts. It was important to ensure that the solder paste was evenly and correctly distributed on the board to avoid unwanted tombstoning or shorting of the components. SMD components were then carefully placed, before the board went into a reflow oven for soldering. From inspecting the board under magnification, it was easy to check that the components had been soldered correctly. These steps were redone for the second PCB version with SMD components on both sides. The THT components were then manually soldered to the board finishing the assembly.

The testing process consisted of testing for shorts and correct connections before applying voltage to the board. Making sure the voltage regulators and bias voltages supply the board correctly before ensuring that the JLCC socket is supplied.

4.5 Lens and lens mount

The lens selected for this project is a PT361060M3MP12 and specifications can be seen in the Table 7.

Table 7 Lens parameters [22]

Model	PT361060M3MP12
Mount	CS-mount
Focal length	6 mm
Aperture	F1.2
M.O.D	0.2 m

The 3D printed CS mount has a flange focal distance of 12.526mm and a diameter of 25.4mm for mounting the lens. The design for the lens mount was drawn in Blender. Blender is a free and open-source computer graphics software toolset that can be used to create 3D models. The finished design was then exported as an STL file before being “sliced” in Ultimaker Cura and thereafter printed on a Ultimaker 3 Extended 3D printer.

On the PCB, screw holes were placed with 40mm distance from each other to fix the lens mount to the board. The footprint of the JLCC package used did not include the overhang from the package which meant the screw holes were too close to the package for the mount to cover the package and to fit screws. The lens mount was then instead printed with pins that fit into the holes securing the mount steady on the PCB. The lens mount design is shown in Figure 56 and is shown mounted on the PCB in Figure 52.

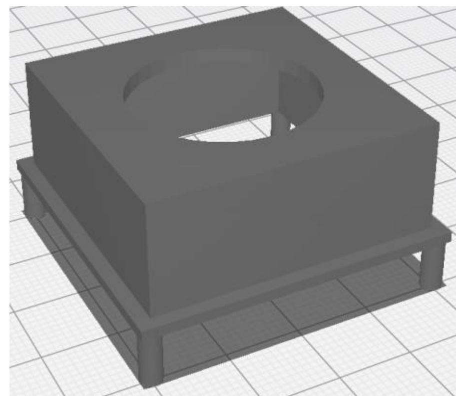


Figure 56 Lens mount design

5.6 FPGA

The FPGA selected for the project is Nexys Video Artix-7. The FPGA controls the timing and pixel selection for the sensor. An ADC is integrated on the board and the Nexys does the sampling and digital conversion of the image sensor's analog signals before interfacing this to a computer. To see the full working flow of the FPGA program, look at Emil's thesis with the title "Testbench System for Image Sensor Characterization" that have a planned publish 6 weeks from the date of this publication. The frame buffering flow for the FGPA is shown in Figure 57, where one picture is captured right after the pixel has been reset and the other picture is captured after exposure, before subtracting the frames for the final image to be displayed. "End Line" and "End Frame" signals that the row and frame is done. The Video Direct Memory Access (VDMA) is constantly outputting the frame to the HDMI before the next frame is ready.

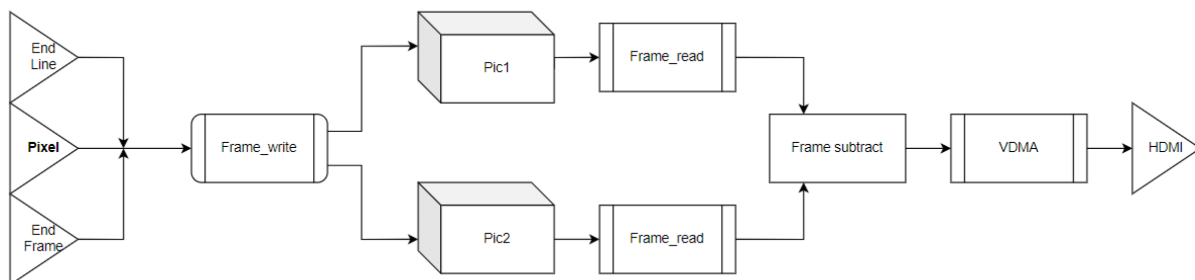


Figure 57 FPGA Frame buffering flow

4.7 Timing

The image sensor consists of 3t pixels. Usually, it is not optimal to do delta sampling on 3t pixels, because it would require a frame buffer to store all reset values for all pixels, and the CDS time becomes very long (=Tint) which increases 1/f-noise. But delta sampling is the preferred sampling method for this project. This is because the different photodiode variants will have different properties. When photodiodes have different structures, they will have different depletion regions. This will then give different junction capacitances that will again affect the speed of the photodiodes. Therefore, the photodiodes could get different reset values based on reset time, and delta sampling is necessary to get a correct reading after exposure. Since there is no physical shutter or Tx transistor, there will be a difference in integration time for the pixels under readout. The pixel array consists of a few pixels (16x16), and it should take relatively short time to read out the values, and the difference in integration time should be small. However, this difference can be adjusted digitally according to integration time for the pixel values. The exposure time should be easy and flexible to change in the FPGA code for later testing of linearity and sensitivity.
Delta sampling for a 3t pixel with global reset would start off by pulsing RST which resets all PDs to VRST-Vth. After waiting the integration time, each pixel would then be “selected” one after one where the signal level is sampled. When all the values after integration time have been sampled, the global reset is again pulsed. Then the reset value for each pixel is then sampled. The pixel value is then = reset value – integration value and we get delta sampling.

V Testing

Due to substantial production delays both from the manufacturer and the broker that were used for bonding, there was not sufficient time to test the IC before the deadline of this thesis. The plan for testing was to measure and look at the response and quality of the sensor. The tools planned to use for achieving the measurements was a fiber optic light source with changeable intensities, a monochromatic source with changeable wavelengths and a narrow band filter since the monochromatic source could have shown difficulty to center under testing. The IC is supplied by the PCB and together with the FPGA it would be possible to take images, change exposure times, look at linearity and noise such as FPN together and dark current. The goal would be to compare the photodiodes and confirm one or more good designs together with ensuring the image sensor design is working correctly.

The IC ended up arriving under a week before the project's deadline. A total of 9+1 chips were produced. A few pictures were taken to confirm the bonding and top surface manufacturing looks correct and promising. The bonding is shown in Figure 58 and the IC is shown in Figure 59 and Figure 60. The IC bonding matches the bonding diagram shown in Figure 49 and the bonds looks to be intact. The surface of the manufactured chip seems to match the design. The photodiodes are not covered in metal, and it looks like some of the decoder design has been covered with metal to fulfill density rules. It is not possible to see if salicide has been applied at this stage.
The student occupying the other part of the pad frame started testing the chip recently. The chip draws a lot of current when voltage is increased. It looks to be short between the pad frame ESD protection and ground on their part of the design. The other student's pad frame connection wires have sadly been drawn too far so that they enter the ESD protection circuitry (black box). The ESD pad frame is shorted to ground resulting in my part of the chip also being unreadable for testing in the current state. There is a small chance laser cutting action can burn down and remove her access M2 metal wires. But this comes with great risk of shorting other things.

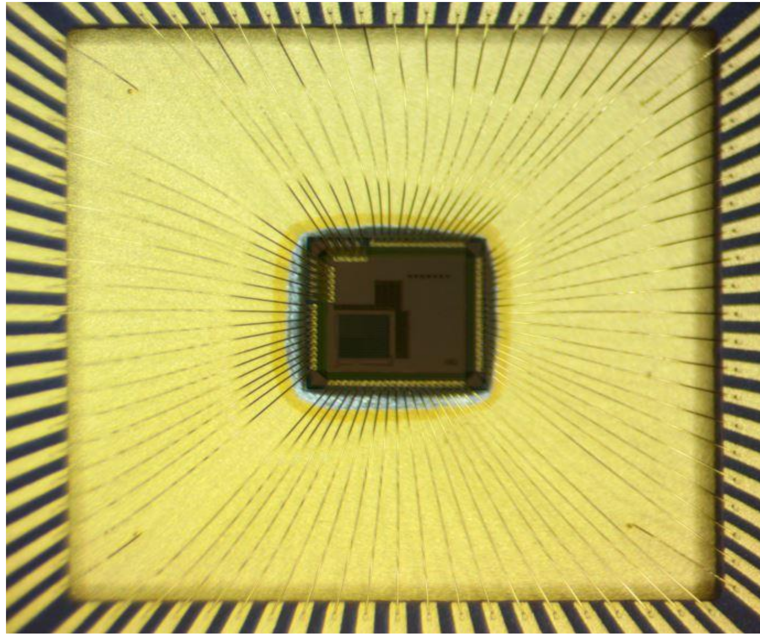


Figure 58 Bonding IC

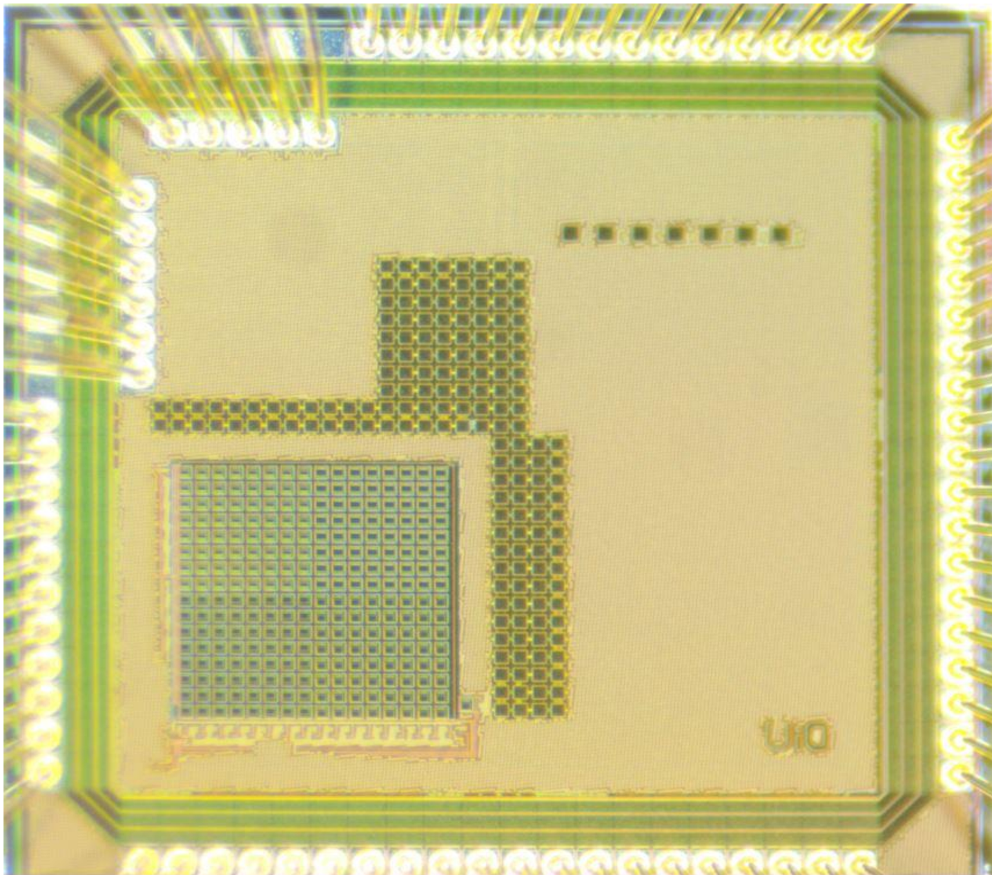


Figure 59 Fabricated IC

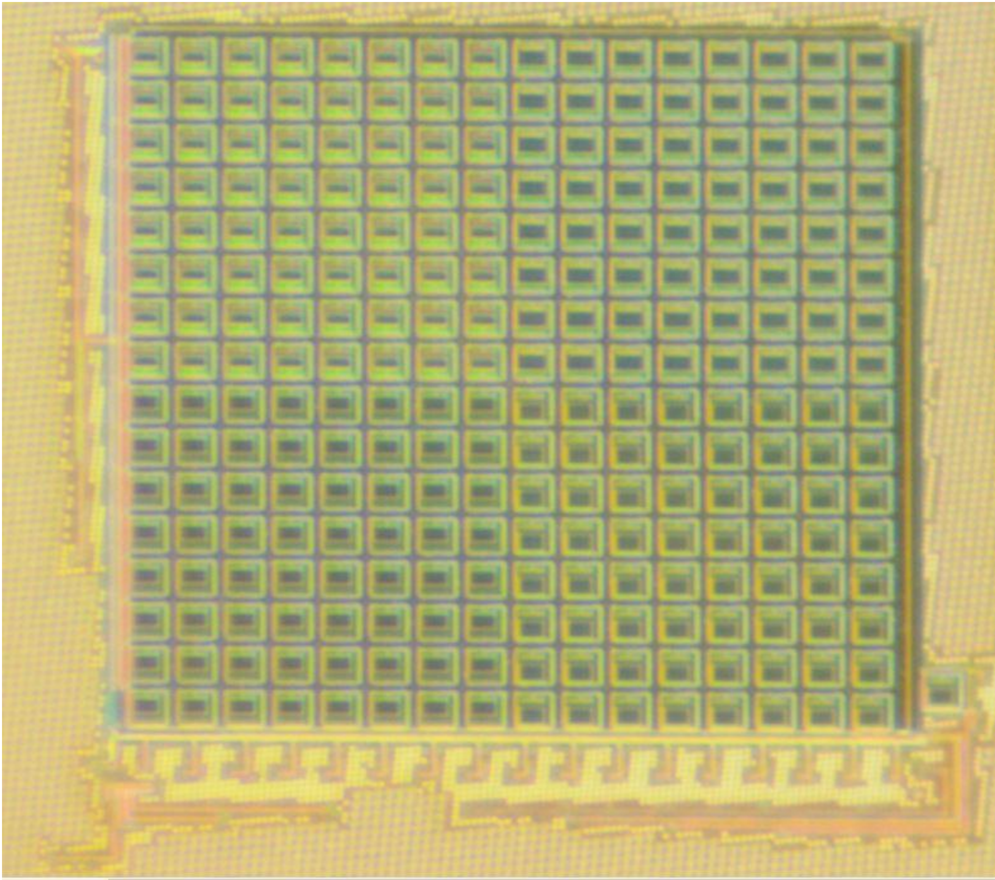


Figure 60 Fabricated IC close up

Future work / Improvements

The future work for this project is to do the verification and testing of the chip. This includes verifying the IC and the functionality together with Emil Hultin's FPGA. At this point, what is most questionable is if the chip is salvageable with the use of laser burning away the metal and leaving behind a mess. There is "danger" that along the sidewalls of the drill holes it might create shorts between the layers. Another approach is to use a focused ion beam. My supervisor Philipp have made contact to the Centre for Materials Science and Nanotechnology at Forskingsparken, Oslo that possesses one of these ion beams.

Improvements that can be done:
For the image sensor design in Cadence, it would have been beneficial to add dummy pixels around the array to reduce mismatch and make sure the pixels "see" the same surroundings for improved performance.
Changing the pixel design from a 3T to a 4T would make delta sampling easier with the ability to turn Tx off and have the exact same exposure time for all pixels without having to compensate for this in the digital domain.
Packing the transistors closer to each other and occupy less space of the pixel area would improve the fill factor. Making the overall layout more compact would also be beneficial.
To save space and increasing pixel fill factor, it would be possible to experiment with sharing the reset NMOS transistor's "N+ source" together with "N+ cathode" for the photodiodes.
If PD4 is performing equally or better than PD1, some areas can save space by not including the extra grounding of the substrate for each photodiode.
Experimenting with the use of deep N-well and different doping concentrations for P+ and N+ implants could result in better QE and performance.

With the TCAD simulations there were problems simulating the correct interface between Si/SiO2 material. This resulted in some inaccurate results when applying voltages. This interface would contribute to generation of dark current in the simulations among other things.
Gathering some expertise and redoing the energy band graph simulations for PD2 and PD3 for achieving more expected results would strengthen the report.
Experimenting with different doping concentrations in Cadence would create more photodiode variants but estimating these doping concentrations in TCAD would have been difficult without additional information from the fab.

The P-sub doping concentration used, is a bit lower than what is typically used in the industry. It would be beneficial to redo all simulations with a higher P-sub doping for more accurate results.
Creating simulations for measuring parasitic capacitance for the photodiodes would also be good to include as well as doing full three-dimensional simulations.

Conclusion

The focus of this thesis has been to characterize photodiode variants for the CMOS 180nm process to be used in future projects at the University of Oslo. Four 180nm CMOS photodiodes have been designed and simulated in TCAD. An image sensor was designed with these photodiodes and sent to production. Accompanying test PCBs have been produced and assembled. Two configurations of the PCB were produced and tested. One with the option to test the IC together with the FPGA, and one standalone version. A lens mount for the PCBs were designed and were 3d printed.

Due to production delays both at the manufacturer and broker, the image sensor was not delivered in time for testing before the deadline of this project. However, TCAD simulations show that all four photodiodes look promising for use in an image sensor application. Depletion regions look to be widening with the increase of applied voltage, increasing the photocurrent. Dark currents are generally low, and the “worst” breakdown voltages are for the P+/N-well junctions at 8V. From the simulations, PD1 and PD3 have better QE for longer wavelengths than the other structures. PD1 and PD4 could therefore be a good choice for a low voltage CMOS 180nm photodiode structure. PD2 and PD3 can be used in higher voltage applications but the bandgap energy diagrams result for these two structures were not exactly as expected. PD4 has been simulated with a floating ground and should perform close to PD1 on the produced IC where the substrate is grounded from NMOS bulks.

The simulation results indicated that the working principles of the structures are functioning, but specific simulated values are hard to justify for the produced IC since there are so many different influential parameters.

Since the pad frame on the IC is currently shorted, additional work must be done to the IC before any testing can be done.

Bibliography

[1] Tavernier, Filip, and Michiel Steyaert. *High-Speed Optical Receivers with Integrated Photodiode in Nanoscale CMOS*.

[2] “Why is Silicon Used for Electronic Devices?” *Wafer World*, 31 August 2016, https://www.waferworld.com/post/why-is-silicon-used-for-electronic-devices. Accessed 10 January 2022.

[3] “Semiconductor Band Gaps.” *Hyperphysics*, http://hyperphysics.phy-astr.gsu.edu/hbase/Tables/Semgap.html. Accessed 10 January 2022.

[4] “NMOS transistor: how does its structure relate to two interconnecting diode?” *Electrical Engineering Stack Exchange*, 25 September 2014, https://electronics.stackexchange.com/questions/130819/nmos-transistor-how-does-its-structure-relate-to-two-interconnecting-diode. Accessed 15 March 2022.

[5] K. Murari, R. Etienne-Cummings, N. Thakor and G. Cauwenberghs, "Which Photodiode to Use: A Comparison of CMOS-Compatible Structures," in IEEE Sensors Journal, vol. 9, no. 7, pp. 752-760, July 2009, doi: 10.1109/JSEN.2009.2021805.

[6] Saad Hamady, Sidi Ould. *A simulation of doping and trap effects on the spectral response of AlGaN ultraviolet detectors*. March 2012.

[7] “Introduction to Image Sensors.” *LUCID Vision Labs*, https://thinklucid.com/tech-briefs/understanding-digital-image-sensors/. Accessed 13 January 2022.

[8] Tardi, Carla, and Marguerita Cheng. “Moore's Law Definition.” *Investopedia*, https://www.investopedia.com/terms/m/mooreslaw.asp. Accessed 2 February 2022.

[9] Hamamatsu Learning Center: Microlens Arrays.” *Hamamatsu Learning Center*, https://hamamatsu.magnet.fsu.edu/articles/microlensarray.html. Accessed 15 April 2022.

[10] Nakamura, Junichi. *IMAGE SENSORS and SIGNAL PROCESSING for DIGITAL STILL CAMERA*.

[11] Moroz, Victor. “TCAD - Technology Computer Aided Design (TCAD).” *Synopsys*, https://www.synopsys.com/silicon/tcad.html. Accessed 24 November 2021.

[12] “TCAD Sentaurus Tutorial.” *TCAD Sentaurus Tutorial*, https://web.stanford.edu/class/ee328/swb/swb_menu.html. Accessed 26 November 2021.

[13] Paschotta, Rüdiger. “Dark current, explained by RP Photonics Encyclopedia; photodetector, photodiode, origins, thermal excitation, bias voltage.” *RP Photonics*, https://www.rp-photonics.com/dark_current.html. Accessed 7 January 2022.

[14] Titus, Albert H., et al. “CMOS Photodetectors.” *IntechOpen*, https://www.intechopen.com/chapters/17220. Accessed 6 October 2021.

[15] “What is a Current Density? - Definition from Corrosionpedia.” *Corrosionpedia*, 14 August 2018, https://www.corrosionpedia.com/definition/2066/current-density. Accessed 17 December 2022.

[16] “Optical Properties of Silicon.” PVEducation, https://www.pveducation.org/pvcdrom/materials/optical-properties-of-silicon. Accessed 9 May 2022.

[17] “Resistance of a Diode - Forward & Reverse Resistance.” *Circuit Globe*, https://circuitglobe.com/resistance-of-a-diode.html. Accessed 3 January 2022.

[18] “Diode resistance - Static, dynamic and reverse resistance.” *Physics and Radio-Electronics*, https://www.physics-and-radio-electronics.com/electronic-devices-and-circuits/semiconductor-diodes/dioderesistance-staticresistance-dynamicresistance.html. Accessed 24 April 2022.

[19] Drageseth, Magnus Flø. *Bioimpedance Microelectrode Array on ASIC*. Design of a Microelectrode Array Measurement System for Multi-Electrode Impedance-Sensing on Cell Cultures in 180nm CMOS Technology. 2020.

[20] Nilsen, Kristian Geli. *Visible light communication CMOS image sensor for automotive applications*. 2019.

[21] “Antenna Effect in 16nm Technology Node.” Design And Reuse, https://www.design-reuse.com/articles/48227/antenna-effect-in-16nm-technology-node.html. Accessed 6 April 2022.

[22] *镜头参数（Parameter of Lens） 型号（Model）：*, https://download.kamami.pl/p579418-20200408%20PT361060M3MP12.pdf. Accessed 13 April 2022.

Appendix

A1 Doping estimates

P+:
sdedr:define-gaussian-profile "guassian_P+" "BoronActiveConcentration" "PeakPos" 0 "PeakVal" 5e+20 "ValueAtDepth" 5e+16 "Depth" 0.4 "Gauss" "Factor" 0.8)
N+:
(sdedr:define-gaussian-profile "guassian_N+" "PhosphorusActiveConcentration" "PeakPos" 0 "PeakVal" 5e+20 "ValueAtDepth" 5e+16 "Depth" 0.4 "Gauss" "Factor" 0.8)
Nwell:
(sdedr:define-gaussian-profile "guassian_Nwell" "PhosphorusActiveConcentration" "PeakPos" 0 "PeakVal" 5e+17 "ValueAtDepth" 5e+14 "Depth" 1.3 "Gauss" "Factor" 0.8)
Psub:
(sdedr:define-constant-profile "constant_Psub" "BoronActiveConcentration" 5e+11)

A2 SDE

A2.1 PD1

```
; Reinitializing SDE
(sde:clear)

; set coordinate system up direction
(sde:set-process-up-direction "+z")

; Create material regions for Silicon and Oxide
(sdegeo:create-rectangle (position -10 0 0) (position 35 6 0) "Silicon" "region_Psub")
(sdegeo:create-rectangle (position 3 0 0)  (position 4 -0.01 0) "Gold" "oxide_N+")
(sdegeo:create-rectangle (position 12 0 0)  (position 13 -0.01 0) "Gold" "oxide_P+")
(sdegeo:create-rectangle (position 23 0 0)  (position 24 -0.01 0) "Gold" "oxide_P+2")

; Define the contacts
(sdegeo:define-contact-set "Anode" 4 (color:rgb 1 0 0) "##")
(sdegeo:define-contact-set "Anode2" 4 (color:rgb 1 1 0) "##")
(sdegeo:define-contact-set "Anode3" 4 (color:rgb 1 1 0) "##")
(sdegeo:define-contact-set "Cathode" 4 (color:rgb 0 1 0) "##")

; Set the contacts to the structure
(sdegeo:set-contact (list (car (find-edge-id (position 12.50 -0.01 0)))) "Anode")
(sdegeo:set-contact (list (car (find-edge-id (position 23.50 -0.01 0)))) "Anode2")
(sdegeo:set-contact (list (car (find-edge-id (position 12.50 6 0)))) "Anode3")
(sdegeo:set-contact (list (car (find-edge-id (position 3.50 -0.01 0)))) "Cathode")

; Define the evaluation windows for doping and meshing
(sdedr:define-refeval-window "global_ref_eval" "Rectangle"  (position -10 -0.01 0) (position 35 6 0))
(sdedr:define-refeval-window "n+_ref_eval" "Line"  (position 1.0 0 0) (position 5 0 0))
(sdedr:define-refeval-window "p+_ref_eval" "Line"  (position 7.0 0 0) (position 18 0 0))
(sdedr:define-refeval-window "p+2_ref_eval" "Line"  (position 23 0 0) (position 25.0 0 0))
(sdedr:define-refeval-window "nwell_ref_eval" "Line"  (position 0 0 0) (position 20 0 0))

; Define the doping profiles
(sdedr:define-constant-profile "constant_Psub" "BoronActiveConcentration" 5e+11)
(sdedr:define-gaussian-profile "guassian_P+" "BoronActiveConcentration" "PeakPos" 0  "PeakVal" 5e+20
"ValueAtDepth" 5e+16 "Depth" 0.4 "Gauss"  "Factor" 0.8)
```

```
(sdedr:define-gaussian-profile "guassian_P+2" "BoronActiveConcentration" "PeakPos" 0  "PeakVal" 5e+20
"ValueAtDepth" 5e+16 "Depth" 0.4 "Gauss"  "Factor" 0.8)
(sdedr:define-gaussian-profile "guassian_N+" "PhosphorusActiveConcentration" "PeakPos" 0  "PeakVal" 5e+20
"ValueAtDepth" 5e+16 "Depth" 0.4 "Gauss"  "Factor" 0.8)
(sdedr:define-gaussian-profile "guassian_Nwell" "PhosphorusActiveConcentration" "PeakPos" 0  "PeakVal"
5e+17 "ValueAtDepth" 5e+14 "Depth" 1.3 "Gauss"  "Factor" 0.8)

; Place the doping profiles
(sdedr:define-constant-profile-placement "Psub_placement" "constant_Psub" "global_ref_eval")
(sdedr:define-analytical-profile-placement "nwell_placement" "guassian_Nwell" "nwell_ref_eval" "Both"
"NoReplace" "Eval")
(sdedr:define-analytical-profile-placement "n+_placement" "guassian_N+" "n+_ref_eval" "Both" "NoReplace"
"Eval")
(sdedr:define-analytical-profile-placement "p+_placement" "guassian_P+" "p+_ref_eval" "Both" "NoReplace"
"Eval")
(sdedr:define-analytical-profile-placement "p+_placement2" "guassian_P+2" "p+2_ref_eval" "Both" "NoReplace"
"Eval")

; Define and place the mesh refinement
(sdedr:define-refinement-size "global_ref" 0.5 0.5 0 0.01 0.01 0)
(sdedr:define-refinement-placement "global_ref_placement" "global_ref" (list "window" "global_ref_eval" ) )
; Automatic adaptation of the grid with doping variation
(sdedr:define-refinement-function "global_ref" "DopingConcentration" "MaxTransDiff" 0.1)
; Automatic refinement of the mesh at the Si/Gold interface
(sdedr:define-refinement-function "global_ref" "MaxLenInt" "Silicon" "SiO2" 0.001 0.12 "DoubleSide")

; Save the structures and mesh creation
(sde:save-model "n@node@")
(sde:set-meshing-command "snmesh")
(sde:build-mesh "" "n@node@")
```

A2.2 PD2

```
; Reinitializing SDE
(sde:clear)

; set coordinate system up direction
(sde:set-process-up-direction "+z")

; Create material regions for Silicon and Gold
(sdegeo:create-rectangle (position -10 0 0) (position 35 6 0) "Silicon" "region_Psub")
(sdegeo:create-rectangle (position 2 0 0)  (position 3 -0.01 0) "Gold" "oxide_N+")
(sdegeo:create-rectangle (position 22.5 0 0)  (position 23.5 -0.01 0) "Gold" "oxide_P+")

; Define the contacts
(sdegeo:define-contact-set "Anode" 4 (color:rgb 1 0 0) "##")
(sdegeo:define-contact-set "Anode2" 4 (color:rgb 1 0 0) "##")
(sdegeo:define-contact-set "Cathode" 4 (color:rgb 0 1 0) "##")

; Set the contacts to the structure
(sdegeo:set-contact (list (car (find-edge-id (position 23 -0.01 0)))) "Anode")
(sdegeo:set-contact (list (car (find-edge-id (position 12.5 6 0)))) "Anode2")
(sdegeo:set-contact (list (car (find-edge-id (position 2.50 -0.01 0)))) "Cathode")

; Define the evaluation windows for doping and meshing
(sdedr:define-refeval-window "global_ref_eval" "Rectangle"  (position -10 -0.01 0) (position 35 6 0))
(sdedr:define-refeval-window "n+_ref_eval" "Line"  (position 0.0 0 0) (position 17 0 0))
(sdedr:define-refeval-window "p+_ref_eval" "Line"  (position 21.5 0 0) (position 24.5 0 0))
```

```
; Define the doping profiles
(sdedr:define-constant-profile "constant_Psub" "BoronActiveConcentration" 5e+11)
(sdedr:define-gaussian-profile "guassian_P+" "BoronActiveConcentration" "PeakPos" 0  "PeakVal" 5e+20
"ValueAtDepth" 5e+16 "Depth" 0.4 "Gauss"  "Factor" 0.8)
(sdedr:define-gaussian-profile "guassian_N+" "PhosphorusActiveConcentration" "PeakPos" 0  "PeakVal" 5e+20
"ValueAtDepth" 5e+16 "Depth" 0.4 "Gauss"  "Factor" 0.8)

; Place the doping profiles
(sdedr:define-constant-profile-placement "Psub_placement" "constant_Psub" "global_ref_eval")
(sdedr:define-analytical-profile-placement "n+_placement" "guassian_N+" "n+_ref_eval" "Both" "NoReplace"
"Eval")
(sdedr:define-analytical-profile-placement "p+_placement" "guassian_P+" "p+_ref_eval" "Both" "NoReplace"
"Eval")

; Define and place the mesh refinement
(sdedr:define-refinement-size "global_ref" 0.5 0.5 0 0.01 0.01 0)
(sdedr:define-refinement-placement "global_ref_placement" "global_ref" (list "window" "global_ref_eval" ) )
; Automatic adaptation of the grid with doping variation
(sdedr:define-refinement-function "global_ref" "DopingConcentration" "MaxTransDiff" 0.1)
; Automatic refinement of the mesh at the Si/Gold interface
(sdedr:define-refinement-function "global_ref" "MaxLenInt" "Silicon" "SiO2" 0.001 0.12 "DoubleSide")

; Save the structures and mesh creation
(sde:save-model "n@node@")
(sde:set-meshing-command "snmesh")
(sde:build-mesh "" "n@node@")
```

A2.3 PD3

```
; Reinitializing SDE
(sde:clear)

; set coordinate system up direction
(sde:set-process-up-direction "+z")

; Create material regions for Silicon and Oxide
(sdegeo:create-rectangle (position -10 0 0) (position 35 6 0) "Silicon" "region_Psub")
(sdegeo:create-rectangle (position 3 0 0)  (position 4 -0.01 0) "Gold" "oxide_N+")
(sdegeo:create-rectangle (position 22 0 0)  (position 23 -0.01 0) "Gold" "oxide_P+")

; Define the contacts
(sdegeo:define-contact-set "Anode" 4 (color:rgb 1 0 0) "##")
(sdegeo:define-contact-set "Anode2" 4 (color:rgb 0 0 1) "##")
(sdegeo:define-contact-set "Cathode" 4 (color:rgb 0 1 0) "##")

; Set the contacts to the structure
(sdegeo:set-contact (list (car (find-edge-id (position 22.50 -0.01 0)))) "Anode")
(sdegeo:set-contact (list (car (find-edge-id (position 12.50 6.00 0)))) "Anode2")
(sdegeo:set-contact (list (car (find-edge-id (position 3.50 -0.01 0)))) "Cathode")

; Define the evaluation windows for doping and meshing
(sdedr:define-refeval-window "global_ref_eval" "Rectangle"  (position -10 -0.01 0) (position 35 6 0))
(sdedr:define-refeval-window "n+_ref_eval" "Line"  (position 1.0 0 0) (position 16 0 0))
(sdedr:define-refeval-window "p+_ref_eval" "Line"  (position 22 0 0) (position 24.8 0 0))
(sdedr:define-refeval-window "nwell_ref_eval" "Line"  (position 0 0 0) (position 20 0 0))
```

```
; Define the doping profiles
(sdedr:define-constant-profile "constant_Psub" "BoronActiveConcentration" 5e+11)
(sdedr:define-gaussian-profile "guassian_P+" "BoronActiveConcentration" "PeakPos" 0  "PeakVal" 5e+20
"ValueAtDepth" 5e+16 "Depth" 0.4 "Gauss"  "Factor" 0.8)
(sdedr:define-gaussian-profile "guassian_N+" "PhosphorusActiveConcentration" "PeakPos" 0  "PeakVal" 5e+20
"ValueAtDepth" 5e+16 "Depth" 0.4 "Gauss"  "Factor" 0.8)
(sdedr:define-gaussian-profile "guassian_Nwell" "PhosphorusActiveConcentration" "PeakPos" 0  "PeakVal"
5e+17 "ValueAtDepth" 5e+14 "Depth" 1.3 "Gauss"  "Factor" 0.8)

; Place the doping profiles
(sdedr:define-constant-profile-placement "Psub_placement" "constant_Psub" "global_ref_eval")
(sdedr:define-analytical-profile-placement "nwell_placement" "guassian_Nwell" "nwell_ref_eval" "Both"
"NoReplace" "Eval")
(sdedr:define-analytical-profile-placement "n+_placement" "guassian_N+" "n+_ref_eval" "Both" "NoReplace"
"Eval")
(sdedr:define-analytical-profile-placement "p+_placement" "guassian_P+" "p+_ref_eval" "Both" "NoReplace"
"Eval")

; Define and place the mesh refinement
(sdedr:define-refinement-size "global_ref" 0.5 0.5 0 0.01 0.01 0)
(sdedr:define-refinement-placement "global_ref_placement" "global_ref" (list "window" "global_ref_eval" ) )
; Automatic adaptation of the grid with doping variation
(sdedr:define-refinement-function "global_ref" "DopingConcentration" "MaxTransDiff" 0.1)
; Automatic refinement of the mesh at the Si/Gold interface
(sdedr:define-refinement-function "global_ref" "MaxLenInt" "Silicon" "SiO2" 0.001 0.12 "DoubleSide")

; Save the structures and mesh creation
(sde:save-model "n@node@")
(sde:set-meshing-command "snmesh")
(sde:build-mesh "" "n@node@")
```

A2.4 PD4

```
; Reinitializing SDE
(sde:clear)

; set coordinate system up direction
(sde:set-process-up-direction "+z")

; Create material regions for Silicon and Oxide
(sdegeo:create-rectangle (position -10 0 0) (position 35 6 0) "Silicon" "region_Psub")
(sdegeo:create-rectangle (position 3 0 0)  (position 4 -0.01 0) "Gold" "oxide_N+")
(sdegeo:create-rectangle (position 12 0 0)  (position 13 -0.01 0) "Gold" "oxide_P+")

; Define the contacts
(sdegeo:define-contact-set "Anode" 4 (color:rgb 1 0 0) "##")
(sdegeo:define-contact-set "Anode2" 4 (color:rgb 1 0 0) "##")
(sdegeo:define-contact-set "Cathode" 4 (color:rgb 0 1 0) "##")

; Set the contacts to the structure
(sdegeo:set-contact (list (car (find-edge-id (position 12.50 -0.01 0)))) "Anode")
(sdegeo:set-contact (list (car (find-edge-id (position 12.50 6 0)))) "Anode2")
(sdegeo:set-contact (list (car (find-edge-id (position 3.50 -0.01 0)))) "Cathode")

; Define the evaluation windows for doping and meshing
(sdedr:define-refeval-window "global_ref_eval" "Rectangle"  (position -10 -0.01 0) (position 35 6 0))
```

```
(sdedr:define-refeval-window "n+_ref_eval" "Line"  (position 1.0 0 0) (position 5 0 0))
(sdedr:define-refeval-window "p+_ref_eval" "Line"  (position 7.0 0 0) (position 24 0 0))
(sdedr:define-refeval-window "nwell_ref_eval" "Line"  (position 0 0 0) (position 26 0 0))

; Define the doping profiles
(sdedr:define-constant-profile "constant_Psub" "BoronActiveConcentration" 5e+11)
(sdedr:define-gaussian-profile "guassian_P+" "BoronActiveConcentration" "PeakPos" 0  "PeakVal" 5e+20
"ValueAtDepth" 5e+16 "Depth" 0.4 "Gauss"  "Factor" 0.8)
(sdedr:define-gaussian-profile "guassian_N+" "PhosphorusActiveConcentration" "PeakPos" 0  "PeakVal" 5e+20
"ValueAtDepth" 5e+16 "Depth" 0.4 "Gauss"  "Factor" 0.8)
(sdedr:define-gaussian-profile "guassian_Nwell" "PhosphorusActiveConcentration" "PeakPos" 0  "PeakVal"
5e+17 "ValueAtDepth" 5e+14 "Depth" 1.3 "Gauss"  "Factor" 0.8)

; Place the doping profiles
(sdedr:define-constant-profile-placement "Psub_placement" "constant_Psub" "global_ref_eval")
(sdedr:define-analytical-profile-placement "nwell_placement" "guassian_Nwell" "nwell_ref_eval" "Both"
"NoReplace" "Eval")
(sdedr:define-analytical-profile-placement "n+_placement" "guassian_N+" "n+_ref_eval" "Both" "NoReplace"
"Eval")
(sdedr:define-analytical-profile-placement "p+_placement" "guassian_P+" "p+_ref_eval" "Both" "NoReplace"
"Eval")

; Define and place the mesh refinement
(sdedr:define-refinement-size "global_ref" 0.5 0.5 0 0.01 0.01 0)
(sdedr:define-refinement-placement "global_ref_placement" "global_ref" (list "window" "global_ref_eval" ) )
; Automatic adaptation of the grid with doping variation
(sdedr:define-refinement-function "global_ref" "DopingConcentration" "MaxTransDiff" 0.1)
; Automatic refinement of the mesh at the Si/Gold interface
(sdedr:define-refinement-function "global_ref" "MaxLenInt" "Silicon" "Gold" 0.001 0.12 "DoubleSide")

; Save the structures and mesh creation
(sde:save-model "n@node@")
(sde:set-meshing-command "snmesh")
(sde:build-mesh "" "n@node@")
```

A3 SDEVICE

A3.1 Parameter file

```
#define ParFileDir .

!(cd @pwd@)!


* <temp> is the simulation temperature,
* <wavelength> is  wavelength [micron],

!( set T @temp@ )!
!(
  source @pwd@/lib/helper_vis.tcl
  set kB $::BoltzmannConstant
  set h  $::PlanckConstant
  set pi $::Pi
  set m0 $::ElectronMass
  set q  $::ElementaryCharge
)!
Material="Gold" {
```

```
  #includeext "ParFileDir/Gold.par"
}
Material="Silicon" {
  #includeext "ParFileDir/Silicon.par"
}
Material="SiO2" {
  #includeext "ParFileDir/SiO2.par"
}
```

A3.2 Breakdownvoltage

```
#setdep @previous@

File{
  Grid      = "n@node|-1@_msh.tdr"
  Plot      = "@tdrdat@"
  Parameter = "@parameter@"
  Current   = "@plot@"
  Output    = "@log@"
}
*Grounding the contacts
Electrode{
  { Name="Anode"          Voltage=0.0 }
  { Name="Anode2"         Voltage=0.0 }
  { Name="Cathode"        Voltage=0.0 }
}


Physics{
        *AreaFactor = 1e4
        Temperature = 300
        EffectiveIntrinsicDensity(
                BandGapNarrowing(OldSlotboom)
        )
        Mobility(
                HighFieldsaturation
        )
        Recombination(
                SRH( DopingDep )
                Band2Band(E2)
                Avalanche( GradQuasiFermi )
        )
        Fermi
}



Math {
  Extrapolate            * (not needed for transient sweeps)
  Avalderivatives        * (only if Avalanche models are active)
  RelErrControl
  Digits=5               * (default)
  ErrRef(electron)=1.e10   * (default)
  ErrRef(hole)=1.e10       * (default)
  Iterations=20
  Notdamped=100
```

```
  * Selecting the model can be complex, read more in the manual
  *Method= Super     * Single device < 10k node/single processor
  Method= ParDiSo * Single device < 100k node/multi processor
  *Method= ILS     * > 8k node/multi processor

  * On Multi-core machines use these commands
  * to speed up the simulation, note that not all methods
  * have this option
  *Number_of_Threads= <int> # | maximum
  *Number_of_Assembly_Threads= <int>
  *Number_of_Solver_Threads= <int>
}


Solve {

NewCurrentPrefix= "tmp_"
        Poisson
        Plot (FilePrefix= "n@node@_eqbm")
        NewCurrentPrefix= ""
        Coupled (Iterations= 100){ Poisson Electron Hole }

        *ramp voltage at Cathode from 0V to 100 V
        Quasistationary (
                InitialStep= 1e-2 Increment= 1.4
                MinStep= 1e-6     MaxStep= 0.01
                Goal { Name="Cathode" Voltage= 100 }
        ){ Coupled { Poisson Electron Hole } }

        System("rm -f tmp*") *remove the plot we don't need anymore.
}*end Solve

Plot{
  *--Density and Currents, etc
  eDensity hDensity
  TotalCurrent/Vector eCurrent/Vector hCurrent/Vector
  eMobility/Element hMobility/Element
  eVelocity hVelocity
  eQuasiFermi hQuasiFermi

  *--Temperature
  eTemperature hTemperature Temperature

  *--Fields and charges
  ElectricField/Vector Potential SpaceCharge

  *--Doping Profiles
  Doping DonorConcentration AcceptorConcentration

  *--Generation/Recombination
  SRH Band2Band Auger
  AvalancheGeneration eAvalancheGeneration hAvalancheGeneration

  *--Driving forces
  eGradQuasiFermi/Vector hGradQuasiFermi/Vector
  eEparallel hEparallel eENormal hENormal
```

```
  *--Band structure/Composition
  BandGap
  BandGapNarrowing
  Affinity
  ConductionBand ValenceBand
  eQuantumPotential hQuantumPotential
}
```

A3.3 DepletionRegion

(same lines as “breakdownvoltage” but with a different type of Quasistationary)

```
Quasistationary(
     InitialStep=0.01 MinStep=1e-5 MaxStep=0.1
     Goal{ Name="Cathode" Voltage=3  }
     Plot{ Range = (0 1) Intervals=6 }
  ) { Coupled { Poisson Electron Hole } }
```

A3.4 Light simulation

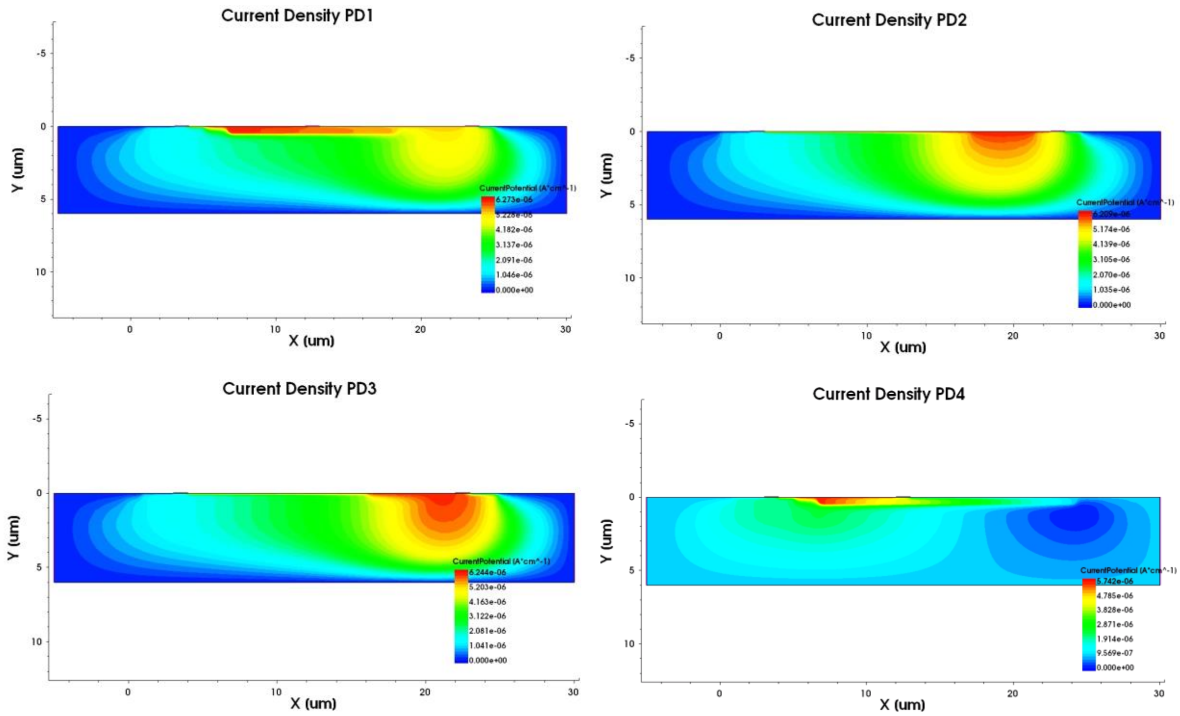
```
#setdep @node|sde@

File {
*-Input
            Grid=      "@tdr@"
            Parameter= "@parameter@"
*-Output
            Current=   "@plot@"
            Plot=      "@tdrdat@"
            Output=    "@log@"
}

Electrode {
            { Name= "Anode"  Voltage= 0 }
            { Name= "Anode2"  Voltage= 0 }
            { Name= "Cathode"  Voltage= 0 }
}

#if "@light@" == "on"
            RayTraceBC {
                        { Name= "Anode"
                                    Reflectivity= 1.0
                        }
                        { Name= "Anode2"
                                    Reflectivity= 1.0
                        }
                        { Name= "Cathode"
                                    Reflectivity= 1.0
                        }

                        { Name= "RTBCleftContact"
                                    Reflectivity= 1.0
                        }
                        { Name= "RTBCrightContact"
                                    Reflectivity= 1.0
                        }
```

```
	}
#endif

Physics {
	AreaFactor= 1.0
	Temperature= @temp@
	Thermionic
	HeteroInterfaces
	Mobility(HighFieldSaturation)
	EffectiveIntrinsicDensity(NoFermi)
	Recombination(
		SRH
		Auger
	)
	#if "@light@" == "on"
	Optics (
	ComplexRefractiveIndex (WavelengthDep(Real Imag))
		OpticalGeneration (
			QuantumYield (StepFunction (EffectiveBandgap)) * number of generated carriers per
photon, default: 1
			ComputeFromMonochromaticSource
		) * end OpticalGeneration
		Excitation (
			Wavelength= 0.5					* Incident light wavelength [um]
			Intensity= 0.00855				* Incident light intensity
[W/cm2]
			Polarization= 0.5				* Unpolarized light
			Theta= 0					* Normal incidence,		in y
direction
			Window(
				Origin= (0, -1) * Shift origin 1 um over the bottom photodiode surface
				Line(x1= -5 x2= 30) * Illumination window covers width of photodiode.
			)
		) * end Excitation
		OpticalSolver (
		RayTracing (
				RayDistribution(
					Mode= AutoPopulate
					NumberOfRays= 3500				* Number of
rays in the illumination window
				)
				CompactMemoryOption
				DepthLimit= 1000					* Stop tracing
a ray after passing through more than x material boundaries
				MinIntensity= 1e-5					* Stop tracing
a ray when its intensity becomes less than x times the original intensity
			) * end RayTracing
		)	* end OpticalSolver
	) * end Optics
	#endif
}

Plot {
*- Doping
	Doping DonorConcentration AcceptorConcentration
*- Band structure
	BandGap BandGapNarrowing ElectronAffinity
	ConductionBandEnergy ValenceBandEnergy
```

```
	eQuasiFermiEnergy hQuasiFermiEnergy
*- Carrier Densities:
	eDensity hDensity
	EffectiveIntrinsicDensity IntrinsicDensity
	eEquilibriumDensity hEquilibriumDensity
*- Fields, Potentials and Charge distributions
	ElectricField/Vector
	Potential
	SpaceCharge
*- Currents
	Current/Vector eCurrent/Vector  hCurrent/Vector
	CurrentPotential   * for visualizing current lines
	eMobility hMobility
	eVelocity hVelocity
*- Generation/Recombination
	SRHRecombination AugerRecombination TotalRecombination SurfaceRecombination Band2Band
RadiativeRecombination
	eLifeTime hLifeTime
#if "@light@" == "on"
*- Optical Generation
   ComplexRefractiveIndex QuantumYield
	OpticalIntensity AbsorbedPhotonDensity OpticalGeneration
* Visualizing raytracing. Can be time consuming to plot.
* RayTree cannot be  plotted if CompactMemoryOption is specified in Physics section.
*	RayTrees
#endif
}

Math {
	Extrapolate
	RelErrcontrol
	Digits= 5
	Notdamped= 20
	Iterations= 12
	ElementEdgeCurrent
	ErrRef(electron)= 1e3
	ErrRef(hole)= 1e3
}

Solve {
	NewCurrentPrefix= "tmp_"
	Poisson
	#if "@light@" == "off"
	Plot (FilePrefix= "n@node@_eqbm")
	#endif
	NewCurrentPrefix= ""
	Coupled (Iterations= 100){ Poisson Electron Hole }
	#if "@light@" == "on"
	Plot (FilePrefix= "n@node@_photo")
	#endif

	*ramp voltage at anode from 0V to 2 V
	Quasistationary (
		InitialStep= 1e-2 Increment= 1.4
		MinStep= 1e-6     MaxStep= 0.01
		Goal { Name="Cathode" Voltage= 2 }
	){ Coupled { Poisson Electron Hole } }
```

```
	System("rm -f tmp*") *remove the plot we don't need anymore.
}
```

A3.5 Current density



A4 SVISUAL

A4.1 Light and dark IV/Cathode applied voltage vs cathode total current

```
…
create_curve -name IV($N) -dataset PLT($N) \
	-axisX "Cathode OuterVoltage" -axisY "Cathode TotalCurrent"

#if "@light@" == "on"
set curveLabel "light I-V ($ID)"
#elif "@light@" == "off"
set curveLabel "dark I-V ($ID)"
#endif
set_curve_prop IV($N) -label "$curveLabel" \
	-color $color -line_style solid -line_width 3

set Vs [get_variable_data "Cathode OuterVoltage" -dataset PLT($N)]
set Is [get_variable_data "Cathode TotalCurrent" -dataset PLT($N)]
…
```

A4.2 Band diagram

```
…
echo "Plotting band diagram"
echo "creating cutline data"
load_file ${tdrfile} -name Structure($n)
create_plot -name Plot_Structure -dataset Structure($n)

set cut($n) [create_cutline -dataset Structure($n) -type $direction -at $position]
```

```
#--------------
echo "plotting band diagram"
if {[lsearch [list_plots] BandDgm_Plot] == -1} {
	create_plot -1d -name BandDgm_Plot
	link_plots [list_plots] -unlink
	set_legend_prop -location bottom_right -label_font_size 12 -label_font_att bold
	set_plot_prop -title "Energy Band Diagram" -title_font_size 20
	set_axis_prop -axis x -title {Y [<greek>m</greek>m]} \
		-title_font_size 16 -scale_font_size 14 \
		-min -5.0 -min_fixed -max 30.0 -max_fixed
	set_axis_prop -axis y -title {Energy [eV]} \
		-title_font_size 16 -scale_font_size 14 \
		-min -3.00 -min_fixed -max 3.0 -max_fixed
}
select_plots BandDgm_Plot

create_curve -name Ec($n)  -dataset $cut($n) -axisX "Y" -axisY "ConductionBandEnergy"
create_curve -name Efn($n) -dataset $cut($n) -axisX "Y" -axisY "eQuasiFermiEnergy"
create_curve -name Efp($n) -dataset $cut($n) -axisX "Y" -axisY "hQuasiFermiEnergy"
create_curve -name Ev($n)  -dataset $cut($n) -axisX "Y" -axisY "ValenceBandEnergy"

remove_plots Plot_Structure

#----------
echo "setting plot properties"
set_curve_prop Ec($n) -label "Conduction Band Energy ($ID)" -color black \
	-line_style solid -line_width 3 \
	-show_markers -markers_size 10 -markers_type $symbol
set_curve_prop Efn($n) -label "Electron Quasi Fermi Energy ($ID)" -color red \
	-line_style dash -line_width 3 \
	-show_markers -markers_size 10 -markers_type $symbol
set_curve_prop Efp($n) -label "Hole Quasi Fermi Energy ($ID)" -color blue \
	-line_style dash -line_width 3 \
	-show_markers -markers_size 10 -markers_type $symbol
set_curve_prop Ev($n) -label "Valence Band Energy ($ID)" -color grey \
	-line_style solid -line_width 3 \
	-show_markers -markers_size 10 -markers_type $symbol
```

A4.3 Current density

```
…
echo "Plotting current density vectors and current flow lines"
echo "###############################################################"

create_plot -name Plot_Current2D($N) -dataset Current2D($N)

set_field_prop CurrentPotential -show_bands
set_field_prop TotalCurrentDensity-V -show
set_plot_prop -title "Current Density and Current flow lines" -title_font_factor 1.4

set_axis_prop -axis x -title {X [um]}
set_axis_prop -axis y -title {Y [um]}

echo "###############################################################"
echo "computing carrier diffusion lengths"
echo "###############################################################"
```

```
create_field -name eDiffusionLength -dataset Current2D($N) -function
"$cmtoum*$cmtoum*sqrt($Vth*<eLifetime>*<eMobility>)"
create_field -name hDiffusionLength -dataset Current2D($N) -function
"$cmtoum*$cmtoum*sqrt($Vth*<hLifetime>*<hMobility>)"
```

A4.4 Reflectance

```
if {[lsearch [list_plots] Plot_RSpectra] == -1} {
	create_plot -1d -name Plot_RSpectra
	link_plots [list_plots] -unlink
	set_legend_prop -location top_left -label_font_size 12 -label_font_att bold

	set_plot_prop -title "Reflectance Spectra" -title_font_size 20
	set_axis_prop -axis x -title {Wavelength [um]} \
		-title_font_size 16 -scale_font_size 14 -type linear \
		-min @wstart@ -min_fixed -max @wend@ -max_fixed
	set_axis_prop -axis y -title {Factor} \
		-title_font_size 16 -scale_font_size 14 -type linear \
		-min 0.0 -min_fixed	-max 1.1 -max_fixed
}
select_plots Plot_RSpectra

#-----------------------------------------------------------
echo "creating wavelength curve"
#-----------------------------------------------------------
create_curve -name wl($N) -dataset PLT_OG($N) \
	-axisX $dsWavelength -axisY $dsWavelength

#-----------------------------------------------------------
echo "creating incident photon flux (Nin (s^-1)) curve"
#-----------------------------------------------------------
create_curve -name Nin($N) -dataset PLT_OG($N) \
	-axisX $dsWavelength -axisY "RaytracePhoton Input"

#-----------------------------------------------------------
echo "creating reflected (from top surface) photon flux (Nbot (s^-1)) curve"
#-----------------------------------------------------------
create_curve -name Nbot($N) -dataset PLT_OG($N) \
	-axisX $dsWavelength -axisY "RaytraceSensor reflection"

#-----------------------------------------------------------
echo "creating transmitted (from bottom surface) photon flux (Ntop (s^-1)) curve"
#-----------------------------------------------------------
create_curve -name Ntop($N) -dataset PLT_OG($N) \
	-axisX $dsWavelength -axisY "RaytraceSensor transmission"

#-----------------------------------------------------------
echo "creating absorbed photon flux (Nabs (s^-1)) curve"
#-----------------------------------------------------------
# Plot integrated optical generation rate Vs wavelength
create_curve -name intGabs($N) -dataset PLT_OG($N) \
	-axisX $dsWavelength -axisY $dsAbsorbedPhotonDensity
# Since unit of integration in Math section of S-Device command file is specified as cm,
# the unit of the integrated absorbed photon density  (double integral) is 1/(cm-s)
create_curve -name Nabs($N) -function "$Lz*$umtocm*<intGabs($N)>"
```

```
create_curve -name Nrta($N) -function "<Ntop($N)>+<Nbot($N)>+<Nabs($N)>"

create_curve -name R($N) -function "<Nbot($N)>/<Nin($N)>"
# Create Reflectance variable. Used for computing IQE
create_variable -name Reflectance -dataset ParticleFlux($N) \
	-values [get_curve_data R($N) -axisY]


create_curve -name T($N) -function "<Ntop($N)>/<Nin($N)>"

create_curve -name A($N) -function "<Nabs($N)>/<Nin($N)>"

create_curve -name RTA($N) -function "<R($N)>+<T($N)>+<A($N)>"

remove_curves "wl($N) intGabs($N) Nin($N) Nbot($N) Ntop($N) Nabs($N) Nrta($N)"

set_curve_prop R($N) -label "Reflectance ($ID)" -color green \
	-line_style solid -line_width 2 \
	-show_markers -markers_size 10 -markers_type $symbol
set_curve_prop T($N) -label "Transmittance ($ID)" -color blue \
	-line_style solid -line_width 2 \
	-show_markers -markers_size 10 -markers_type $symbol
set_curve_prop A($N) -label "Absorbance ($ID)" -color magenta \
	-line_style solid -line_width 2 \
	-show_markers -markers_size 10 -markers_type $symbol
set_curve_prop RTA($N) -label "R+T+A ($ID)" -color black \
	-line_style solid -line_width 2 \
	-show_markers -markers_size 10 -markers_type $symbol
```