Low-Noise Input Stage in Selected Modern Semiconductor Technologies

Cand. Scient. Thesis

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Preface

This thesis is the result of a study for the Cand. Scient. degree in Microelectronics at the Department of Informatics, University of Oslo. The thesis project was initiated in cooperation with my supervisor Joar Martin Østby, Senior Research Scientist at the SINTEF research center, and Associated Professor at University of Oslo.

The project has been a challenge for me in many ways, regarding both the theory and the design of an ASIC circuit. However, I have learned much in the course of the work and I believe that I have benefited from my work with this thesis. The thesis covers a wide range of issues, and I feel that I have gained much experience in several aspects of RF construction and noise reduction techniques in the analog ASIC design.

First and foremost I wish to thank my supervisor, Associated Professor Joar Martin Østby, for sacrificing many hours of his time guiding me through the various problems occurring throughout this thesis. With his experience and intimate knowledge of analog integrated circuit (IC) design, he has proved to be a valuable resource for me during my work.

I would also like to thank Senior Engineer Dag T. Wisland for his help regarding the use of the design tool Cadence.

Special thanks go to Øyvind Hagen and Omid Mirmotahari for our useful discussions and their valuable help on important issues of my work.

Next, I wish to thank Lisa Rypeng, Øystein Benjamin Lykkeslet and Marius Gaarde for their comments regarding the writing process of the thesis.

I also thank my fellow students and the employees at the Department of Informatics, for the pleasant atmosphere during my time at the department. Finally, I would like to thank my family for being supportive during my study.

   Oslo, May 2003

   Boris Savičić
Contents

1. INTRODUCTION ................................................................................................................. 5
  1.1. DATA ACQUISITION SYSTEMS .................................................................................. 6
  1.2. THE PURPOSE OF THE THESIS ............................................................................. 6
  1.3. THE CIRCUITS FUNCTION ...................................................................................... 7
    1.3.1. Noise figure ...................................................................................................... 8
  1.4. FUNDAMENTALS OF NOISE ................................................................................... 9
    1.4.1. Thermal noise .................................................................................................. 9
    1.4.2. Flicker noise .................................................................................................. 10
    1.4.3. Shot noise ...................................................................................................... 10
  1.5. DESIGN PROCEDURE .............................................................................................. 11

2. FIRST PART ......................................................................................................................... 13
  2.1. CMOS ARCHITECTURE ............................................................................................ 14
    2.1.1. LNA design ...................................................................................................... 14
      2.1.1.1. Description of the circuit ........................................................................... 15
      2.1.1.2. Varactor ................................................................................................... 17
      2.1.1.3. Basic resonant circuit ............................................................................. 19
      2.1.1.4. Improved resonant circuit ..................................................................... 20
    2.1.2. LNA simulations ............................................................................................... 22
      2.1.2.1. Gain simulation ......................................................................................... 22
      2.1.2.2. IMD and IP3 ............................................................................................ 23
      2.1.2.3. AC analysis and tuning range ................................................................... 23
    2.1.3. Component noise of the LNA ........................................................................... 26
      2.1.3.1. Direct or indirect affect ............................................................................ 26
      2.1.3.2. Noise model ............................................................................................. 27
      2.1.3.3. Miller effekt .............................................................................................. 28
      2.1.3.4. Total noise of the LNA ............................................................................ 32
      2.1.3.5. Noise simulations ..................................................................................... 37
      2.1.3.6. Calculative variation ............................................................................... 40
  2.2. MIXER ......................................................................................................................... 42
    2.2.1. Heterodyne and homodyne architectures ......................................................... 42
      2.2.1.1. Heterodyne receivers .............................................................................. 42
      2.2.1.2. Homodyne receivers .............................................................................. 45
    2.2.2. Down-conversion mixer ..................................................................................... 47
      2.2.2.1. Evaluation of the frequency domain ......................................................... 48
    2.2.3. Noise in mixers ................................................................................................. 49
      2.2.3.1. Noise calculation method .......................................................................... 49
      2.2.3.2. Flicker noise .............................................................................................. 51
      2.2.3.3. Thermal noise ............................................................................................ 51
  2.3. LAYOUT ......................................................................................................................... 53
    2.3.1. Pads .................................................................................................................... 53
      2.3.1.1. LO signal .................................................................................................. 53
      2.3.1.2. $V_{in}$ signal ............................................................................................... 53
2.3.1.3. The created pads ................................................................. 54
2.3.2. Layout noise and countermeasures ....................................... 54
  2.3.2.1. Placing of the components .............................................. 54
  2.3.2.2. Routing ........................................................................ 57
  2.3.2.3. Capacitive connections at the crossing points ............... 59
  2.3.2.4. Thermal noise in the gate poly ....................................... 61
  2.3.2.5. Digital and analog part of the circuit ............................. 62
2.3.3. Limitations .......................................................................... 63
  2.3.3.1. Realisation of the inductors ........................................... 63
  2.3.3.2. Output load .................................................................. 63
2.4. CONCLUSION – FIRST PART .................................................. 64

3. SECOND PART ........................................................................... 65
  3.1. INTRODUCTION - SECOND PART ........................................ 66
  3.2. LNA DESIGN AND FUNCTION OF THE CIRCUIT ............... 67
    3.2.1. Resonant circuit .............................................................. 69
    3.2.2. AC analysis and signal gain ........................................... 70
  3.3. COMPONENT NOISE OF THE LNA ........................................ 73
    3.3.1. Hybrid-\(\pi\) model ........................................................... 73
    3.3.2. Noise calculation in the LNA ........................................... 75
      3.3.2.1. First stage of the LNA ............................................... 75
      3.3.2.2. Second stage of the LNA ......................................... 80
      3.3.2.3. Third stage of the LNA ........................................... 84
      3.3.2.4. Fourth stage of the LNA ......................................... 87
    3.3.3. Noise in entire LNA ........................................................ 90
      3.3.3.1. Noise simulations .................................................. 91
  3.4. MIXER - BIPOLAR TECHNOLOGY ........................................ 94
  3.5. CONCLUSION SECOND PART ............................................. 96

4. CONCLUSION ............................................................................ 98
5. REFERENCES .............................................................................. 99

APPENDIX A
  Detailed calculation of the resonant frequency (CMOS technology) ....... ii

APPENDIX B
  Explanation: gain expressed in dB ................................................ iii

APPENDIX C
  Noise contributed by the transistors in the LNA. (CMOS technology) .... iv

APPENDIX D
  Detailed calculations of the voltage gain in the LNA (CMOS technology) .... vi

APPENDIX E
  Noise calculation of entire LNA (CMOS technology) ........................ viii
APPENDIX F
Noise in the mixer (CMOS technology) ................................................................. xii

APPENDIX G
Coupling noise at the crossing point (CMOS technology) ........................................ xiii

APPENDIX H
Noise calculation of the first stage (BiCMOS and SiGe technology) ....................... xiv

APPENDIX I
Noise calculation of the second stage (BiCMOS and SiGe technology) ............... xviii

APPENDIX J
Noise calculation of the third stage (BiCMOS and SiGe technology) .................. xx

APPENDIX K
Noise calculation of the fourth stage (BiCMOS and SiGe technology) ................. xxii

APPENDIX L
Noise calculation of entire LNA (BiCMOS and SiGe technology) .................. xxvi

APPENDIX M
Layout of the circuit (CMOS technology) ........................................................... xxvii
1. Introduction

Electronics equipment is becoming a part of our everyday lives. In cars, households, and everywhere around us, electronics take over more and more of the exercises previously done manually. Electric equipment turns on automatically and does tasks they are programmed for, so that the humans do not even have to think about it. In many cases human lives will be threatened if electronics do not work properly. We have heard stories about planes that had to make emergency landings due to electromagnetic interference; electronics devices, used by passengers, interfered with the electronics onboard and led to major malfunctions. Even hospital patients, whose lives are dependent on the function of sensitive electronics, are threatened by interference from external signals. This is the explanation why the use of cell phones is restricted in hospitals and on planes, since these can cause changing functionality of electronics equipment. In a worst-case scenario human lives could be lost. The widespread use of electronic circuits makes it necessary for circuits to operate in close proximity. Unfortunately, all too often these circuits affect each other adversely, and electric noise is very often responsible for this trend. Electric noise is defined as any unwanted disturbance obscuring or interfering with a desired signal. Electric noise is not only the problem between the different products. It can also be a problem internal in an electric product. All electrics products generate itself some noise, which can disturb its functionality. In general the electric noise can be divided into the coupling and the component noise. The coupling noise can occur between two components or between two products, while the component noise is generated in the component itself. Both the coupling and the component noise can cause reduced quality of measurements, lack of functions or execution of undesired functions. During the data transfer in wireless systems, electric noise can reduce data rate. For radio and TV this can mean low picture and sound quality. The signal range of the radio equipment can be reduced because of electric noise, and consequences can be serious if the radio signal is an emergency signal. As explained above, critical applications are also in larger degree controlled by electronics and therefore becoming more advanced every day. The designer’s goal is to optimize functionality, which means to take in use different methods, such as increasing a frequency and using newer technology. The new technology contains transistors with lower threshold voltage and smaller devices. Distance between the devices decrease also. The main advantage with this is that functionality and performance of the system will be better, however, a disadvantage is that a system will be more sensitive for small signal changes. In other words less noise will be required to alter the functionality of the products. Designers today have to keep in mind that circuits they design should not be affected by external noise sources and should not itself be a source of noise to the environment. System and circuit designers also have to think about countermeasures in advance, otherwise correcting errors will be much more expensive. If the tests show that a given circuit does not fully fit all noise demands required, designers have to reanalyze the circuit to find the dominant noise source, and then try to minimize this source. This time consuming process may lead to delays in the production, which again may lead to increased expenses. In many cases noise can not be predicted exactly, nor can it be totally eliminated, however its effect can be minimized.
1.1. Data acquisition systems

Modern data acquisition systems often consist of transducers and sensors coupled to electric circuits which transfer signals to a computer where we can read the results of the measurements. Sensors and transducers can be any device translating the characteristics of the physical world into electrical signals. These signals will be manipulated in different ways (amplified, filtered, converted analogue to digital) before they reach the computer in desired form. In modern systems it is often required that sensors must be very sensitive to be able to measure very small changes in a signal. The small noise contribution can be very critical here, because the small variation in a signal can affect the output signal in large degree. In worst case the system can be useless. All sensors have a basic limiting noise level and the challenge of system designers is to interface the sensor with an electronic circuit that contributes a minimum of additional noise. The key element for achieving optimum circuit performance is the noise in the first stage of the system. If there is too much noise in the first stage, no matter how good the rest of the circuit is, it will be impossible for designers to reduce this noise.

1.2. The purpose of the thesis

The construction of the preamplifier with low self-produced noise is essential in most sensor systems. This self-produced noise decides how exact a measure can be made. Considering for instance the particle detectors, how small values that can be detected is given by self-produced noise of the detector. Above also gives the possible range and/or rate of data transfers of a wireless system. The low noise is key factor in acquisition systems if it is desired to be able to make precise measurements. Different semiconductors have different properties concerning noise. Noise will therefore be one of the most important criteria when choosing technologies. Therefore the noise in this thesis will be considered as the function of the technology. In order to concrete this, some of the common RF architectures were chosen and it is focused on the component and internal coupling noise. Signal processing is not described in details, but some of trends that are part of the signal processing are mentioned and explained here. For instance in RF circuits where the desired signal is mixed with its harmonics or other signals, can lead to increased noise. Performing the frequency translation the noise will also be up/down converted in the same way as the desired signal. Those things can increase the noise, but to calculate the noise contribution caused by signal mixing will be out of the scope of this thesis.

This thesis will consider two different architectures of RF receivers - both in which the sensor is an antenna. The first architecture is a single-ended structure with MOS transistors, designed in 0.6 µm process. The idea was to design this circuit in the 0.18 µm process; however, this technology was not available at University of Oslo when this thesis was written. The second architecture is a differential structure designed with two different technologies, BiCMOS 0.8 µm and SiGe. In both architectures the input stage
consists of a low noise amplifier and a mixer. The noise contribution from dominant noise sources will be estimated, and calculation and simulation results will be compared.

<table>
<thead>
<tr>
<th>Technology</th>
<th>Process</th>
<th>Structure</th>
<th>Chapter</th>
</tr>
</thead>
<tbody>
<tr>
<td>CMOS</td>
<td>0.6 µm</td>
<td>Single-ended</td>
<td>2.0</td>
</tr>
<tr>
<td>CMOS</td>
<td>0.18 µm</td>
<td>Single-ended</td>
<td>Not available</td>
</tr>
<tr>
<td>BiCMOS</td>
<td>0.8 µm</td>
<td>Differential</td>
<td>3.0</td>
</tr>
<tr>
<td>BiCMOS SiGe</td>
<td>0.8 µm</td>
<td>Differential</td>
<td>3.0</td>
</tr>
</tbody>
</table>

### 1.3. The circuits function

The transmitted waveform in radio frequency (RF) communication is commonly a high frequency carrier modulated by the original signal. The desired signal is modulated in the transmitter. In other words up-converted to higher frequency carrier to could be easily transferred to the receiver. There are a few reasons for modulation, but the most important one is that the communication must occur in a certain part of the spectrum. The simple communication system consist of modulator, a channel and a demodulator, as illustrated in figure [1.3.1]

![Figure 1.3.1: Simple communication system](image)

The inverse of the modulation is demodulation, with the goal being to extract the original baseband signal with minimum noise and distortion. The circuits described in this thesis are the parts of the RF receivers where the demodulation is performed. The input signal is picked up by an antenna and has a frequency between 2.4 and 2.5 GHz. The antenna is connected to the Low Noise Amplifier (LNA) which amplifies the input signal and forwards it to the mixer. Mixers are usually used to multiply signals of different frequencies to achieve frequency translation. The reason for frequency translation is to simplify the filtering out a RF signal channel centered among many narrowly spaced neighboring channels. The downconversion of the RF carrier signal frequency makes this task much easier. The input signal is then mixed with a signal from the local oscillator LO, which has a frequency of 2.4 GHz. The figure [1.3.2] shows the circuit.
Both architectures presented in this thesis are RF receivers and consist of a LNA and a mixer. The difference is in the construction of those two components, but the frequency of the RF and LO signal is the same in both architectures. The details about the construction will be described later. Both architectures have a build in a band-pass filter at the output of the LNA which filter out the frequencies outside the passband. It will not be focused on construction of the low pass filter and other circuitry connected at the output of the mixer, because this will be out of the scope of this thesis. The goal is to minimize the noise and optimize the circuit so it can receive a signal of a magnitude as small as possible. The LNA is the first stage of a radio receiver and needs to provide sufficient gain and at the same time contribute with as little noise as possible.

1.3.1. Noise figure

An important measure of system noise performance is a parameter noise figure $NF$ or noise factor $F$. The noise factor of a system is defined to be the ratio of the signal-to-noise power ratio at the input to the signal-to-noise power ratio at the output measured at the standard temperature of 290°K, [(10), on page 44].

$$F = \frac{S_i / N_i}{S_o / N_o} \quad [1.3.1]$$

The noise factor can be expressed in decibels since it is a power ratio and than it will be referred to as the noise figure $NF$:

$$NF = 10 \log F \quad [1.3.2]$$

A perfectly noise-free amplifier would maintain the same signal-to-noise ratio at its input and output. A realistic amplifier, however, adds extra noise and degrades the signal-to-noise ratio. Therefore a low noise figure means that little noise is added by the network. The noise factor $F$ can also be defined as

$$F = \frac{Total - Equivalent - Input - Noise - Power}{Noise - Power - of - Source - Impedance} = \frac{E_{ni}^2}{E_i^2} \quad [1.3.3]$$

The equivalent input noise refers all noise sources to the signal source location. The $S/N$ can be easy evaluated because both the signal and equivalent input noise are presented at
the signal source location. The equivalent input noise can be expressed as the total output noise divided by the system gain.

\[ E_{ni}^2 = \frac{E_{no}^2}{K_i^2} \]  

[1.3.4]

The detailed calculation of those parameters is shown in subchapter [2.1.3]. In order to minimize the equivalent input noise, the system gain has to be highest possible at the desired frequency range. The gain in the first stage is necessary to be able to reduce the importance of the noise contribution after the input stage. When the system consists of \( n \) blocks the noise figure for the entire system is given by, [(10), on page 49]:

\[ F_n = 1 + \left( F_1 + 1 \right) + \frac{F_2 - 1}{A_1} + \ldots + \frac{F_n - 1}{A_1 \ldots A_{n-1}} \]  

[1.3.5]

where \( A \) is available power gain.

This is known as the Friis formula and typical results shows that the first stages in a cascade are the most critical in noise performance since the noise contributed by each stage decreases as the gain preceding the stage increases. Therefore, the noise figure of the LNA basically dominates the entire receiver sensitivity.

### 1.4. Fundamentals of noise

Noise can be defined as “everything” except from the desired signal. In an electronic system it is numerous noise sources disturbing the desired signal. Most of them are classified as the coupling noise, which can be reduced or eliminated by shielding. Other noise sources, which are irreducible by shielding due to the fact they are inherent in the system itself, is classified as component noise.

This thesis primarily focuses on component noise. However, countermeasures for coupling noise and shielding methods are also used and described. Three main types of component noise are considered in this thesis, thermal, flicker and shot noise. The importance of noise sources is to a great extent technology depended. Therefore the contribution of flicker noise is negligible in BiCMOS while the contribution of shot noise is negligible in CMOS technology.

#### 1.4.1. Thermal noise

The thermal noise is the most fundamental and important noise in electronic devices. This kind of noise is caused by the random thermally excited vibration of the charge carriers in a conductor. In every conductor or resistor at a temperature above zero, the electrons are in random motion and this vibration is dependent on temperature. Increased resistance, temperature or bandwidth, increases the thermal noise. This is given by formula for thermal noise: [(10), on page 10]
\[ E_t = \sqrt{4kTR\Delta f} \]  

where \( k \) is a Boltzmann’s constant, \( T \) is a temperature of the conductor in kelvins (K) and \( \Delta f \) is the noise bandwidth of the measuring system in hertz (Hz). Thermal noise ultimately limits the resolution of any measurement system. Even if an amplifier can be considered as the noise-free, the resistance of the signal source would still contribute noise.

### 1.4.2. Flicker noise

Flicker noise is known as 1/f noise since its spectral density is inversely proportional to the frequency. It increases without limit as frequency decrease. The major cause of flicker noise in semiconductor devices is because of the properties of the surface of the material. It is not only present in vacuum tubes, transistors, diodes, and resistors, but also in thermistors, carbon microphones, thin films, and light sources. The presents of this noise is common in channel of the MOS transistors. No electronic amplifier has been found to be free of flicker noise at the lowest frequencies. Improved surface treatment in manufacturing has decreased 1/f flicker noise. This kind of noise is technology and frequency depended.

### 1.4.3. Shot noise

The shot noise was first described by Schottky in 1918 as: 

\[ I_{sh}^2 = 2qI_{DC}\Delta f \]  

where \( I_{DC} \) is the DC current flowing across the device. It is white and occurs when quantized carriers cross barriers with random spacing as in Schottky diodes or p-n junctions. Two conditions are required for shot noise to occur: a flow of direct current and a potential barrier over which the carriers are extracted. Linear devices do not generate shot noise. Considering the MOSFETs, shot noise dominates the noise characteristics only when the device is in the subthreshold region owing to the carrier transport in this region, which is very similar to conditions in bipolar transistors. The shot noise is usual in bipolar transistors.
1.5. Design procedure

The procedure is almost the same for both architectures described in this thesis. The first step is to optimize the LNA, then the mixers in order to achieve the right functionality. The second step is to perform the noise calculation. During the optimization it was necessary to perform a few simulations that show the different properties of the circuits:

- Voltage gain
- IMD and IP3 simulations
- AC simulation
- Noise simulation
  - Equivalent input noise of the LNA
  - Output noise of the LNA
  - Noise figure of the LNA
- Transient analyses
  - Fourier transform

The LNA was optimized, making sure that it does not being saturated at a desired frequency. Undesired signals that are in the passband near a desired signal can be amplified, and if they are amplified too much, it can result that LNA goes over in saturation. The voltage gain simulation was performed with both minimum and maximum value of the input signal. Maximum signal value means the maximum value of the signal which LNA can process without being saturated. Performing intermodulation distortion (IMD) and 3rd Order Intercept Point (IP3) simulation will show how good the circuit is to suppress nearby interferers. IMD occurs when the non-linearity of a system with multiple input frequencies causes undesired outputs on other frequencies. In a communication system this means that a signal in one channel can cause interference with adjacent channels. AC analyze was performed on the output of the LNA, showing magnitude of the output signal. By using transient analysis and Fourier transform at the output of the mixer, it is possible to see magnitude of the intermediate frequency (IF). This is the desired signal at the output of the mixer.

After verifying the right function of the circuit, the next step will be to define the tuning range of the circuit. In other words, to optimize the circuit to be able to tune the frequency at the output of the LNA. Afterwards, the contribution of the component noise will be identified, and the challenge is to minimize this noise without reducing the gain of the desired signal. If the component noise is on an acceptable level, the layout of the circuit will be designed. In this part of the design phase, the goal is to minimize coupling noise as much as possible.
FIRST PART

CMOS Technology
2.1. CMOS architecture

The first part of this thesis describes the CMOS architecture, design, noise calculation and the layout. The figure [2.1.-1] shows the entire receiver. [(3), on page 2]

![CMOS receiver diagram]

**Figure 2.1-1: CMOS receiver**

2.1.1. LNA design

The first stage in this RF receiver architecture is a low noise amplifier (M1, M2, M3 and varactors). The LNA has to provide a sufficient gain and amplify the desired signal, so it then can overcome noise from the stages that follow. The other very important function of the LNA is to add itself a minimum noise. The special thing for this LNA design is that it has a great capability to suppress undesired signal in large degree. Not all amplifiers can suppress undesired signals, but this one has a built-in band-pass filter, which filters out the frequencies outside the passband. Therefore the signal characteristic at the output of the LNA has a band-pass filter characteristic. That means that both desired and undesired signals in the passband, i.e. signals that has frequency near the resonant frequency, will be amplified and forwarded to the mixer. Other signals that are not in the passband will fade. In the LNA design it is very important to consider how much the
signal can be amplified; it must be taken into consideration that other signals which end in the passband will be amplified. This can lead to disturbing of the desired signal in the next stage, or it can contribute to increasing noise around the down converted signal in the mixer. High frequency signals such as for instance LO signal from mixer can easy come trough the parasitic capacitance of the mixer’s input transistor and further on to the input of the LNA. That can cause distortion of the desired signal RF on the input of the LNA. This can be critical especially if the LO signal reach the antenna, because the circuit can work as a sender. In order to prevent this trend the total capacitance between input and output of the LNA must be reduced. This capacitance is reduced because of the transistor $M_2$, [Figure 2.1-2]. The transistor $M_2$ isolates the gain stage from the output and causes reduction of the Miller effect, which leads to higher bandwidth. The value of the Bias voltage of the transistor $M_2$ is not critical. This voltage should be high enough to guarantee that the transistor $M_1$ is in saturation and low enough to guarantee that transistor $M_2$ is in saturation, as well.

### 2.1.1.1. Description of the circuit

The input signal, $V_{in}$, is an AC signal, produced by the antenna. The capacitance $C_3$ stops the DC current from the antenna. Because of the high frequency, AC will come through the $C_3$. [Figure 2.1-2].
The AC signal will come into the gate of the transistor $M1$, which has a common source structure. Therefore the input voltage will be converted to the output current by the transistor $M1$. In other words the transistor $M1$ is a transconductor and is the first stage in the chain which amplifies the input signal. The transistor $M2$ has a common gate structure, which means that the signal path is from source to drain. The signal will not be amplified in this stage, only transferred to the output of the LNA. Since the signal input is at the gate of the $M1$ and the signal output is at the drain of the $M2$, the capacitance between the input and the output of the LNA is significantly lowered.

This is an important advantage because it minimizes the feedback from the output to the input of the LNA, which reduces the oscillation at high frequencies. The dominant capacitances at the output of the LNA are the $C_{gd}$ capacitance of the $M2$ and the $C_g$ capacitances of the mixer’s input transistors. Together with capacitance of the $C_2$ and inductance of the $L_2$, will this result in reactance at the output becomes equal to zero at 2.5 GHz frequency. The resonance frequency will occur and will cause a band-pass characteristic of the signal at the output of the LNA. The transistor $M3$ is in saturation all the time and works as a current source which delivers DC to the output of the LNA. The DC current on the gate of the $M1$ can be regulated by the current mirror at the input, [Figure 2.1-1]. The resistor $R$ is a bias resistor and it will be demonstrated that increased value of the resistance $R$ reduces the thermal noise at the input of the LNA. The inductor $L_1$ is used to make input impedance real and contribute to increased gain at the output of the LNA. $L_1$ also isolate transistor $M1$ from the substrate reducing the contribution of the EPI noise (substrate noise). In contradistinction to the inductor $L_2$, the inductor $L_1$ can not change frequency of the passband at the output.
2.1.1.2. Varactor

As explained above the total capacitance at the output of the LNA and inductance $L_2$ cancel each other at resonant frequency, which can be between 2.4 and 2.5 GHz. To be able to move the resonant frequency it is desired to adjust the capacitance or the inductance at the output of the LNA. The inductors can not be adjusted after producing the circuit. However, the capacitance at the output of the LNA could be changed by replacing the capacitor $C_2$ with a varactor. A varactor can be described as a voltage controlled capacitor or a variable reactor. The main reasons of using the varactor in this circuit are to:

- make the circuit less sensitive for process variations
- be able to tune the $RF$ frequency within demanded tunings range.

The typical application areas for varactors are LC resonant tank circuits where the frequency can vary by varying the capacitance. Voltage controlled capacitors can be made in different ways but there are a few things that should be considered in the design phase. Among these the four very important factors are:

1. Capacitance-voltage characteristic ($\Delta C$ as a function of $\Delta V_S$)
2. Q factor
3. Area on the chip
4. Applied only for small signals

These factors will be only mentioned here and will not be discussed in detail because that is not a part of this thesis. In this design the varactor was made of an NMOS transistor. Drain and source are coupled together and connected to the voltage source with a fixed potential. The signal is coupled to the gate of the transistor, [Figure 2.1-3]. The DC voltage of the signal will not vary much in this case. Figure [2.1-3] shows how the transistor is coupled. The total capacitance from the gate to the bulk is $C_{gb}$. This capacitance exhibit by two capacitors of value $C_{ox}$ and $C_c$, connected in series. The overlap capacitance to the source and drain is always there. The size of the $C_{ox}$ capacitance depends on the gate area and the thickness of the $t_{ox}$ layer. The total capacitance from the gate to the bulk when excluding the overlap capacitances are written as: [(12), on page 64]

$$\frac{1}{C'_{gb}} = \frac{1}{C'_{ox}} + \frac{1}{C'_{c}}$$  \[2.1.1\]

In accumulation region the $C_c$ is very large and from the expression [2.1.1] is it possible to see that the total capacitance between gate and bulk is approximately $C_{ox}$. In depletion
region the $C_c$ become smaller and then the total capacitance can be calculated from the expression [2.1.1.]. The thickness of the depletion layer will vary with voltage $V_{bg}$ and the $C_c$ capacitance will vary, too. The $C_c$ capacitance can be separated into two components $C_i$ and $C_b$, one owing to the depletion region charge and one owing to the inversion layer charge [(12), on page 66]. The details will not be discussed here. The expression [2.1.1] is expanded and can be written as:

$$\frac{1}{C_{gb}} = \frac{1}{C_{ox}} + \frac{1}{C'_b + C'_i} \quad [2.1.2]$$

In the weak inversion region the $C_i$ capacitance is negligible and the total capacitance $C_{gb}$ can be written as the series combination of $C_{ox}$ and $C_b$. As $V_{gb}$ increase the $C_b$ become smaller and the series combination of the $C_{ox}$ and $C_b$ decrease as well. Above the weak inversion the $C_i$ capacitance increases drastically. The last fraction of the expression [2.1.2] become very small and the $C_{gb}$ approaches $C_{ox}$. The figure [2.1-4] shows the plot of the total capacitance seen externally $C_{gb}$.

![Graph](image)

**Figure 2.1-4: MOS capacitance as a function of $V_{gs}$**

In our case the DC voltage on the gate, $V_g$ is about 3.3 V and this is higher than threshold voltage, $V_t$. The most interesting area will be the inversion area, because the small variation in the voltage on $V_d$ or $V_s$ will result in great changes of the capacitance. Figure [2.1-4] shows how the total capacitance for a MOS transistor varies when the transistor is in different areas. In moderate inversion when, $V_{ds}=V_g-V_t=0$, the variation of the capacitance is the largest. Therefore this area is the most interesting in this case. Variation in the $C_{gb}$ capacitance will result in the tuning of the frequency at the output of the LNA. The gain of the desired signal, at the output of the LNA, will vary with frequency, but this variation is not very large. The total capacitance, $(C_{gb} + C_{gs} + C_{gd})$ will vary between 1.32 pF and 5.5 pF and with this variation it will be possible to get a tunings range of the 100 MHz at the output of the LNA.
2.1.1.3. Basic resonant circuit

In order to tune the frequency at the output of the LNA, the inductor $L_2$ or the capacitance at the output has to be regulated. As explained in previous subchapter the capacitance is easiest to regulate and therefore the capacitor $C_2$ has been replaced with a varactor, [Figure 2.1-2]. By using the varactor it is possible to change frequency by regulating the voltage source connected to the varactor.

![The resonant circuit and its equivalent circuit](image)

Figure 2.1-5: The resonant circuit and its equivalent circuit

Figure [2.1-5a] shows the part of the amplifier that makes the resonant frequency at the output of the LNA. The circuit on the right in the figure above is equivalent circuit of this resonant circuit. If the $C_{\text{sum}} = C_{\text{gd}_2} + C_{\text{g}_m} + C_{\text{g}_m11}$ the reactance will be:

$$
\frac{1}{C_{\text{sum}}\omega_0} - \left( \frac{1}{\omega_0 C_{\text{var}_1}} + \omega_0 L_2 \right) = 0
$$

Therefore the resonant frequency can be written as:

$$
\omega_0 = \sqrt{\frac{C_{\text{var}_1} - C_{\text{sum}}}{L_2 C_{\text{var}_1} C_{\text{sum}}}}
$$

The demanded tunings range is 100 MHz. The biggest challenge is to take into consideration the process variation during the production. The inductors can not be realized precise and the parasitic capacitances must be taken into account. These things can contribute to the frequency moving from the desired range. By using the varactor it will be possible to make compensation for these aberrations. In this case it is possible to vary the $C_{\text{var}_1}$, compensating for variation in inductor $L_2$ without changing the frequency.
2.1.1.4. Improved resonant circuit

Examination of the figure [2.1-5], indicates that LNA contains a LC resonant circuit. The inductor $L_2$ and the varactor are parts of this circuit. Theoretically, there are only two options for how to keep the frequency of the desired signal in the demanded tunings range in the first place: to regulate the varactor capacitance and to regulate the inductance of the $L_2$. The first one is the correct solution in this case, because the inductance will be difficult to change after the production. The inductor can vary up to 4 nH without moving the frequency out of the tunings range which is between 2.4 GHz and 2.5 GHz. This solution could be used if the designing of the internal inductor was possible. The disadvantage of the internal inductors is that they use a lot of chip area, but in this case that was not a limitation. The problem is that the version of the design tool Cadence, which was used, had not implemented function for simulating and calculating inductance. To design an internal inductor without simulating first, will be risky because that can lead to a much greater aberration than expected in the first place. That is the only reason why the external inductors are used in this design. Use of external inductors implies difficulties to precisely predict the inductance. The variation of the 4 nH is not enough because the band leads contribute with inductance, too. Approximately the 1 mm of the band lead equals to about 1 nH inductance. Additionally things such as the parasitic capacitances and resistance in pins and pads must be considered. In this case these tings can involve the necessity of the inductor reduction. A large variation of the inductor involves that the total capacitance at the output of the LNA is too large so that the varactor can not compensate for it. Therefore the inductor has to be reduced to be able to keep the frequency in the demanded tunings range, 2.4 GHz – 2.5 GHz. By adding another varactor to the circuit it will be possible to tune up frequency without reducing the inductor $L_2$.

![Figure 2.1-6: Optimized resonant circuit and its equivalent circuit](image)

The total capacitance will be:

$$C_{\text{sum\_opt}} = C_{\text{var\_2}} + C_{\text{gd\_m2}} + C_{\text{g\_mb}} + C_{\text{g\_m11}}.$$

and the resonant frequency can be written as:
\[ \omega_0 = \frac{C_{\text{var}_1} - C_{\text{sum\_opt}}}{\sqrt{L_2 C_{\text{var}_1} C_{\text{sum\_opt}}}} \]  

[2.1.5]

The explanation of the expression [2.1.5] is shown in Appendix A. After the optimizing there was three degree of freedom making possible to regulate all three parts of the expression for resonant frequency. Therefore it is possible to compensate for the inductor in much higher degree. By adding the varactor2 to the circuit, the inductor variation increases up to 10 nH. That means that the inductor \( L_2 \) can vary up to 10 nH without moving the frequency from the desired tuning range. To be able to connect external inductor, two extra pads must be added. These pads, which were defined in the AMS library, had too much parasitic capacitance, approximately up to 5 pF. The inductor \( L_2 \) must therefore be reduced to 4 nH in order to compensate for the total capacitance at the output of the LNA. The inductance of the 4 nH will be difficult to achieve with the external inductors especially when the band leads can have an inductance larger then 4 nH. The consequence of this can be a reduced tunings range. In order to keep the demanded tunings range it will be necessary to reduce frequency of the desired signal. This is a trade off which will be discussed after the chip is produced.
2.1.2. LNA simulations

The LNA simulations described in this subchapter are primarily used to verify the correct function of the circuit.

2.1.2.1. Gain simulation

As explained before the most important function of the LNA is to amplify the desired signal. The signal gain can be expressed in voltage and in dB. The explanation is shown in Appendix B. In contradiction to AC, the voltage gain simulation shows the gain of both RF and its harmonics signals expressed in dB. This is the simulation where it is required that the designer apply the magnitude of the RF signal and number of its harmonics. The plotted result of the voltage gain simulation is illustrated in figure [2.1-7]. It shows the RF signal gain and its first harmonics at the output of the LNA.

![Voltage Gain](image)

**Figure 2.1-7: The gain of the RF signal and its first harmonic expressed in dB**

The plot also shows that the gain of the RF signal equals to 36 dB. Comparing the calculation and simulations results it illustrates that simulator use the following formula

\[ dB = 20 \log \frac{V_{out}}{V_{in}} \]  \[2.1.6\]

The formula [2.1.6] does not take into consideration the input and output impedance of the LNA. Only the voltage gain is calculated not the effect gain. The voltage gain can be great, but if there is too much load at the output, the circuit will not work properly because of the limit for how great load the outputs transistors will be able to drive. The formula for effect gain will give a more precise result, when it is a great load at the output of the LNA. The plot also shows that the gain of the RF signal is higher than the gain of its harmonics. The main reason for this is the bandpass filter characteristic at the output of the LNA.
2.1.2.2. IMD and IP3

The IMD stands for Intermodulation Distortion Measurement and occurs when the non-linearity of a device or system with multiple input frequencies causes undesired outputs at other frequencies. 3rd Order Intercept Point (IP3) measure LNA's capability to suppress the harmonics signals of the RF. Both IMD and IP3 show how the LNA suppresses signals that intrude the RF signal. Because of the non-linearity in the LNA, sums and differences of the input signals will be produced. To run the IMD simulation the designer has to apply two signals with the same AC magnitude (RF and distortion signal) at the input of the LNA. The plot of the IMD simulation shows RF, distortion signal, its sum and differences and the harmonics of all this signals. The greater difference between the RF and RF-DIST signals the better capability of the LNA to suppress the undesired signals. Since IP3 shows LNA's capability to suppress the harmonics signals of the RF, the IP3 measure is not important in this case. This is because the bandpass filter at the output of the LNA will filter out these harmonics signals.

2.1.2.3. AC analysis and tuning range

By performing AC analysis it is possible to see the resonant frequency at the output of the LNA, which is in this case between 2.4 and 2.5 GHz. The frequency of the 2.5 GHz was used as a test frequency, and the noise contribution is also calculated by this frequency. The top of the peak is at 2.5 GHz and the highest amplification is exactly at this point. This can be interpreted like the band pass filter characteristic, since signals which are out of the pass band will be faded by the LNA. This characteristic makes the LNA less sensitive for signals which are not near by resonant frequency. The signals which are near by the desired signal, 2.5 GHz, will be amplified and transferred to the mixer. To prevent this trend as much as possible, the goal will be to make smallest possible band around the RF signal. This leads to fading and filtering out more noise and undesired signals. AC analysis shows also the voltage magnitude of the desired signal at the output of the LNA:
After adding the varactor2, the inductor $L_2$ could vary between 20 and 30 nH, without moving the frequency of the desired signal out of the demanded tunings range (2.4 GHz-2.5 GHz). Two AC analysis, which shows tunings range when the value of the inductor $L_2$ is set to 20 and 30 nH were performed at the output of the LNA.
The table [2.1-1] shows the values of the inductor $L_2$ and DC voltage of the voltage sources $V_1$ and $V_2$ connected to the varactors. It shows also that the gain variation of the desired signal was small, even when the values of the $V_1$, $V_2$ and $L_2$ were changed. The circuit could be tuned to the upper limit of the tunings range when both $V_1$ and $V_2$ are on 5 V, contrary if $V_1$ and $V_2$ are on 0 V the frequency will reach the lower limit, 2.4 GHz. In case of reducing the inductor $L_2$ below 20 nH, the frequency will increase and the lower limit of the tunings rage will be 2.43 GHz. In other words it will be difficult to get a resonant frequency lower then 2.43 GHz. On the other hand increasing the inductor $L_2$ above 30 nH, the highest resonant frequency will not be able to reach 2.5 GHz. This means that the inductor $L_2$ must have a value between 20 and 30 nH to be able to keep the frequency in demanded tunings range.

<table>
<thead>
<tr>
<th>Resonant frequency</th>
<th>$V_1$</th>
<th>$V_2$</th>
<th>$L_2$</th>
<th>Signal value at resonant. frequency</th>
<th>Plot</th>
</tr>
</thead>
<tbody>
<tr>
<td>2.5 GHz</td>
<td>5 V</td>
<td>1.836 V</td>
<td>30 nH</td>
<td>78.77 mV</td>
<td>Figure 2.1-8</td>
</tr>
<tr>
<td>2.4 GHz</td>
<td>0 V</td>
<td>0 V</td>
<td>20 nH</td>
<td>83.70 mV</td>
<td>Figure 2.1-9</td>
</tr>
</tbody>
</table>

Table 2.1-1: Resonant frequency
2.1.3. Component noise of the LNA

Because the LNA is the first stage in the chain, the noise in LNA is decisive for a good circuit design. It is very important to identify all noise sources and consider different countermeasure to reduce the noise contribution from the LNA. In order to succeed in designing such an LNA, a few things have to be basically considered before starting the design phase. Many parameters, which are used in noise calculation, are technology depended. Therefore the choice of the technology is the key element in making a good design. Furthermore, the environment where the circuit will be used must also be carefully considered. The contribution of the component noise will to a great extent depend on the technology that was used during the circuit production. Shot noise contribution is negligible in the CMOS technology, but is essential in bipolar transistors. Additionally, bipolar transistors will also contribute flicker noise, but this noise will be a bigger problem in the mixer design than in the LNA, especially in the homodyne architecture. The reason is that the down converted signal in the mixer, \( IF \), has a low frequency and it can be difficult to filter out the flicker noise surrounding it without disturbing the \( IF \) signal.

2.1.3.1. Direct or indirect affect

The LNA contains different components like transistors, capacitors, inductors and resistors. All these components will increase or reduce the noise contribution directly or indirectly. The capacitors do not contribute the noise directly, but the noise current through these can affect the total noise contribution at the output. As explained above increased resistance will usually increase the thermal noise, but in some cases increased resistance can reduce the total noise at the output. That depends on the placing of the resistance with respect to the signal path. This is the one of the reasons why it is important to consider all components in the circuit when considering the noise countermeasure.
2.1.3.2. Noise model

In order to find the noise contribution of a MOS transistor, the small-signal equivalent circuit for high frequencies is used, [Figure 2.1-10]. Since the signal frequency is high, the most of the parasitic capacitors has to be included in the model. [Based on (10), on page 143]

![Small signal equivalent circuit for high frequencies](image)

Figure 2.1-10: Small signal equivalent circuit for high frequencies

The detailed noise calculation for transistors is shown in Appendix C, but procedure and decisions, which are supposed to simplify calculations, are described below. The formula for thermal noise in MOSFETs is given by: [(2), on page 20]

\[
I_{nd}^2 = 4kTΔf \gamma g_m
\]  \[2.1.7\]

where for long channel MOSFETs, the term \( \gamma \) satisfies the inequality \( \frac{2}{3} \leq \gamma \leq 1 \). The value of \( 2/3 \) holds when the transistor is in the channel pinch-off region and the value of \( 1 \) is valid when the drain bias is zero. Since the noise contribution is calculated when the noise bandwidth is 1 Hz, the formula for thermal noise used in these calculations, is:

\[
I_{nd}^2 = \frac{8KTg_m}{3}
\]  \[2.1.8\]

The \( g_m \) is the part of the expression above because this can be seen as the transconductance or inverse resistance in the channel. The temperature is in kelvins and is approximately 300 K at 17 degree of Celsius. Since the transistor is in saturation the following expression for \( I_D \) is used: [(10), on page 146]

\[
I_D = K_p \left( \frac{W}{L} \right) (V_{gs} - V_t)^2 (1 + \lambda V_{DS})
\]  \[2.1.9\]

Transconductance, \( g_m \), is the change of current, \( I_D \) caused by the change of the input voltage, \( V_{in} \), on the gate. See equation [2.1.10], [(10), on page 149]

\[
g_m = \frac{\partial I_D}{\partial V_{gs}} \Rightarrow g_m = 2K_p \left( \frac{W}{L} \right) (V_{gs} - V_t) (1 + \lambda V_{DS})
\]  \[2.1.10\]
From expression for the flicker noise [2.1.11], it is easy to see that flicker noise will be reduced at the high frequency since $f$ is inversely proportional to the square of the flicker noise $I_f^2$. Formula for flicker noise is given by, [(10), on page 150]:

$$I_f^2 = \frac{K_F I_D A_F}{f C_{ox} L_{ef}^2}$$  \[2.1.11\]

where $K_F$ is a flicker noise coefficient, $I_D$ is a source-drain current, $A_F$ is a constant, $f$ is a frequency of operation in hertz, $C_{ox}$ is gate oxide capacitance and $L_{ef}$ is the effective channel length. Most of the terms that are part of the formula [2.1.11] are technology depended. The flicker noise is caused by charge trapping in the gate oxide or at the boundary between the silicon and the silicon-dioxide interface. Larger MOSFETs exhibit less flicker noise since larger gate oxide capacitance smooth the fluctuations in channel charge. Flicker noise is larger in MOSFETs than in other types of devices since it is quite closely related to surface phenomena.

The total noise current for the transistor, when the noise caused by the Miller capacitance in not included, will be the sum of the flicker noise and the thermal noise. See equation below:

$$I_{no}^2 = I_{nd}^2 + I_f^2$$  \[2.1.12\]

### 2.1.3.3. Miller effekt

As explained before the total noise current, which occurs in the transistor, is written as $I_{no}^2$. This is not exactly the right answer, but it is a very good approximation especially if the signal path is from source to drain. If the transconductance transistors, where the signal path is from gate to drain as in transistor $M1$, [Figure 2.1-2], are taken into consideration then the Miller effect must be taken into consideration, as well. This is not important for low frequency signals since these do not pass through the capacitors. The Miller effect can be explained as the feedback through the parasitic capacitance between gate and drain, [Figure 2.1-11]. The resistance channel noise will also get back to the gate or in this case to the input of the circuit, through this feedback.

![Figure 2.1-11: The feedback coupling at the high frequency](image)
To be able to calculate the noise contribution caused by the feedback, the equivalent resistor between the gate and the source has to be added. The noise contribution will be the thermal noise of this resistor. The magnitude of the equivalent resistor is inversely proportional to the real part of the input admittance, \((10)\), on page 145. The imaginary part of the input admittance is the equivalent capacitance. This capacitance can be used to calculate the correlation factor between the noise at the input and the noise which returned to the input through the feedback capacitance. Obviously the noise source is the same, and that is the reason why the noise at the input is correlated with the noise caused by the feedback. Correlation factor will depend on the state of the noise currents, if it is in phase or anti phase, or maybe that they are partly correlated. This calculation will not be done in this thesis.

\[
R_{eq} = \frac{1}{\text{Re } Y_i} = \frac{1 + \omega^2 R^2_{L} C^2_{gd}}{\omega^2 g_m R^2_{L} C_{gd} C_L}
\]  \[2.1.13\]

\[
C_{eq} = \frac{C_{gd} (1 + g_m R_L) + R^2_{L} C^2_{gd} C_L}{1 + \omega^2 R^2_{L} C^2_{L}}
\]  \[2.1.14\]

The equivalent resistor can be seen as the noise source parallel with the input contributing the thermal noise current: \(\sqrt{\frac{4K T}{R_{eq}}}\)

### 2.1.3.4. \(R_{eq}\) and \(C_{eq}\) calculations

Source-drain load capacitance and the load resistance are parts of the expression for input admittance. The load capacitance \(C_L\) is the parallel coupling of the \(C_{ds}\) (drain-source capacitance of the transconductor \(M1\)) and the rest of the load capacitances in the LNA, \(C_D\).

\[
R_L = r_{ds} \| R_D
\]  \[2.1.15\]

\[
C_L = C_{ds} \| C_D
\]  \[2.1.16\]
To be able to simplify the calculation of the $C_L$ all the parasitic capacitances in the transistors has to be taken into consideration. In the expression for $C_L$, two varactors and a transistor $M2$, which is in saturation, are included. The equivalent circuit is shown in figure [2.1-13]

![Figure 2.1-13: LNA with load capacitance of the transistor $M1$ included](image)

![Figure 2.1-14: Load capacitance on the drain of the transistor $M1$](image)
In order to simplify the expression for $C_L$, it is necessary to compare the magnitudes of the $\frac{1}{\omega C_{DS}}$ and $r_{ds}$. One of these, which have the biggest resistance, will not be taken into calculation. $\frac{1}{\omega C_{DS}}$ and $r_{ds}$ are in parallel and the current will choose the path where the resistance is smallest, [Figure 2.1-15]. When the transistor is in saturation then $\frac{1}{\omega C_{DS}} >> r_{ds}$, in other words the $\frac{1}{\omega C_{DS}}$ will not be taken in calculation since this factor has a greatest resistance.

![Figure 2.1-15: Capacitance and resistance in the channel](image)

The expression for calculation of the $C_{M2}$ and $C_{M3}$ is as follow:

![Figure 2.1-16: Parasitic capacitances](image)

$$C_{M2}, C_{M3} = (C_{gs} \parallel C_{gd}) \parallel (C_{sb} \parallel C_{db})$$  \[2.1.17\]

Therefore the expression for $C_D$ is:

$$C_D = \left\{(C_{gs} \parallel C_{gd}) \parallel (C_{sb} \parallel C_{db})\right\}_{C_{M2}} + \left\{(C_{gs} \parallel C_{gd}) \parallel (C_{sb} \parallel C_{db})\right\}_{C_{M3}} + C_{vl} + C_{v2}$$ \[2.1.18\]

The figure [2.1-13] shows all capacitances that are included in formula [2.1.18]. The detailed calculations of the capacitances in the transistor are shown in Appendix E.
2.1.3.5.  **Total noise of the LNA**

The method for noise calculation explained above is used on all transistors. The total noise contribution of each transistor was calculated and these were summed up. The thermal and flicker noise were calculated for transistors, where the signal path is from source to drain. For transistor M1 where the signal path is from gate to drain, in addition to thermal and flicker noise the noise contribution caused by the Miller capacitance was included, too. The results show that the thermal noise is the dominant noise, and that is not surprising since the frequency of the RF signal is 2.5 GHz. The component noise contributed by the varactors, can be considered as negligible. The table [2.1-2] shows the noise contribution of some of the transistors in the LNA. The detailed calculation is shown in Appendix C.

<table>
<thead>
<tr>
<th>Transistor</th>
<th>Flicker noise current $I_f^2$</th>
<th>Thermal noise current $I_{nd}^2$</th>
<th>Total noise current $I_{M_1}^2$</th>
<th>Total noise voltage $E_{M_1}^2$</th>
</tr>
</thead>
<tbody>
<tr>
<td>M1</td>
<td>$4.15 \cdot 10^{-25} \frac{A^2}{Hz}$</td>
<td>$2.69 \cdot 10^{-23} \frac{A^2}{Hz}$</td>
<td>$2.73 \cdot 10^{-21} \frac{A^2}{Hz}$</td>
<td>$1.00 \cdot 10^{-17} \frac{V^2}{Hz}$</td>
</tr>
<tr>
<td>M2</td>
<td>$2.87 \cdot 10^{-25} \frac{A^2}{Hz}$</td>
<td>$2.21 \cdot 10^{-23} \frac{A^2}{Hz}$</td>
<td>$2.24 \cdot 10^{-21} \frac{A^2}{Hz}$</td>
<td>$1.23 \cdot 10^{-17} \frac{V^2}{Hz}$</td>
</tr>
<tr>
<td>M3</td>
<td>$3.53 \cdot 10^{-13} \frac{A}{\sqrt{Hz}}$</td>
<td>$1.70 \cdot 10^{-23} \frac{A^2}{Hz}$</td>
<td>$1.73 \cdot 10^{-21} \frac{A^2}{Hz}$</td>
<td>$1.58 \cdot 10^{-17} \frac{V^2}{Hz}$</td>
</tr>
</tbody>
</table>

Table 2.1-2: Noise in transistors

2.1.3.6.  **$E_n-I_n$ model**

The total noise contribution is calculated by using the $E_n-I_n$ model, [(10), on page 39]. The components at the input of the LNA are included in this model. The AC signal from the sensor was represented by the voltage source $V_{in}$, while the resistance $R_s$ represents the sensor’s internal resistance. This resistance is supposed to be 50 $\Omega$. The rest of the components are the same as in figure [2.1-17], where the input part of the LNA is shown.
In this case the total gain of the LNA is divided into two parts $K_{t1}$ and $K_{t2}$. The gain of the first stage can be expressed as:

$$K_{t1} = \frac{V_{\text{drain M1}}}{V_{\text{in}}} \approx \frac{R}{R_S + \frac{1}{\omega C_3} + R} \left( \frac{g_{ds\_M2} + g_{ds\_M3}}{g_{ds\_M3}} \right) \left( -\frac{g_{m\_M1}}{g_{m\_M2} + g_{mb\_M2}} \right)$$  \[2.1.19\]

This is the signal gain from output of the $M1$ to the input of the LNA. The gain of the second stage is written as:

$$K_{t2} = \frac{V_{\text{out}}}{V_{\text{drain M1}}} \approx \frac{g_{m\_M2}}{g_{ds\_M3}}$$  \[2.1.20\]

Therefore, the total gain from the input to the output of the LNA is expressed as:

$$K_{\text{tot}} = K_{t1} \cdot K_{t2} = \frac{V_{\text{out}}}{V_{\text{in}}} \approx \left( \frac{R}{R_S + \frac{1}{\omega C_3} + R} \right) \left( \frac{g_{ds\_M2} + g_{ds\_M3}}{g_{ds\_M3}} \right) \left( -\frac{g_{m\_M1}}{g_{m\_M2} + g_{mb\_M2}} \right) \left( \frac{g_{m\_M2}}{g_{ds\_M3}} \right)$$  \[2.1.21\]

Those gain calculations are based on the reference [(13), pages 287-292]. The detailed calculations are shown in Appendix D.

<table>
<thead>
<tr>
<th>Calculated gain</th>
</tr>
</thead>
<tbody>
<tr>
<td>$K_{t1}^2$</td>
</tr>
<tr>
<td>$K_{t2}^2$</td>
</tr>
<tr>
<td>$K_{\text{tot}}^2$</td>
</tr>
</tbody>
</table>

Table 2.1-3: Calculated gain
The noise which sensor contributes itself and the noise generated between the sensor and transconductance transistor $M1$ are amplified by the factor $Kt1$ and $Kt2$. The noise at the input of the $M1$, $E_i$ can be expressed as:

$$E_i^2 = E_n^2 + E_s^2 \left( \frac{R}{R_S + \frac{1}{\omega C_3} + R} \right) + \left( I_R^2 + I_n^2 \right) \left( R || \left( R_S + \frac{1}{\omega C_3} \right) \right)$$  \hspace{1cm} [2.1.22]

The noise at the gate of the $M1$ is noise generated by the transistor $M1$ and the rest of the components at the input stage. The component values that are the part of the $E_n$-$I_n$ model are calculated by formulas [2.1.22]-[2.1.26]. $E_S$ is the thermal noise produced by the sensor, and the sensor resistance is set to 50 $\Omega$. $E_n$ and $I_n$ represents the amplifier noise. In this case it represents the noise generated by transistor $M1$. $E_n$ is the thermal and flicker noise voltage generated by $M1$ and the $I_n$ present noise current caused by Miller effect. In order to calculate the $E_{ns}$, which represents the noise at the gate of the $M1$, the thermal end flicker noise voltage generated by $M1$, has to be divided by the gain of transistor $M1$. This is shown in expression below.

$$E_n^2 = \frac{E_{md}^2}{\left( g_{ds,M2} + g_{ds,M3} \right)^2} \left( -\frac{g_{m,M1}}{g_{m,M2} + g_{mbs,M2}} \right)^2 + \frac{E_f^2}{\left( g_{ds,M2} + g_{ds,M3} \right)^2} \left( -\frac{g_{m,M1}}{g_{m,M2} + g_{mbs,M2}} \right)^2$$  \hspace{1cm} [2.1.23]

The $E_n$ can also be measured by setting the $R_S$ equal to zero, form equation [2.1.22] it is easy to see that terms $R_S$ and $E_S$ drop out and the resulting noise generator is the $E_{ns}$, the noise of the amplifier. If the sensor resistance is set to infinity the noise from the sensor will overcome the noise generated by the $M1$, and expression [2.1.22] reduced to $E_i^2 = (I_R^2 + I_n^2)R_S^2$. $I_R$ is the thermal noise current of the bias resistor $R$ which is parallel with input signal $V_{in}$.

$$E_S = \sqrt{4KT R_S}$$  \hspace{1cm} [2.1.24]

$$I_n = \sqrt{\frac{4KT}{R_{eq}}}$$  \hspace{1cm} [2.1.25]

$$I_R = \sqrt{\frac{4KT}{R}}$$  \hspace{1cm} [2.1.26]

The total noise voltage at the output of the $M1$ is the result of the input noise multiplied by the gain of the transistor $M1$:

$$E_{no,M1}^2 = E_i^2 \left( \frac{g_{ds,M2} + g_{ds,M3}}{g_{ds,M3}} \right)^2 \left( -\frac{g_{m,M1}}{g_{m,M2} + g_{mbs,M2}} \right)^2$$  \hspace{1cm} [2.1.27]

$E_{no,M1}^2$ represents the total noise contribution at the output of the $M1$.  

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First part- 34

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Figure 2.1-19: Equivalent noise sources at the output of the LNA

The term $E_{M2}$ is the noise voltage generated by the transistor $M2$, and the $I_{M3}$ is the noise current generated by transistor $M3$. The total noise voltage at the output of the LNA is expressed as:

$$E_{\text{output}}^2 = (E_{\text{no, M1}}^2 + E_{M2}^2) \cdot K_{i2}^2 + I_{M3}^2 \cdot \frac{1}{1} \cdot \frac{1}{g_{ds.M3}} \cdot \left(1 \cdot g_{ds.M2} + g_{ds.M1} \right)$$

$$= \left(\frac{1}{1} \cdot \frac{1}{g_{ds.M3}} \cdot \left(1 \cdot g_{ds.M2} + g_{ds.M1} \right) \right)^2 \tag{2.1.28}$$

The noise voltage from the first stage $E_{\text{no, M1}}$ and the noise voltage generated by transistor $M2$ are amplified by the gain of the second stage. The noise current generated by the transistor $M3$ is multiplied by $r_{ds} || (r_{ds1} + r_{ds2})$. If exclude the term $E_{\text{no, M1}}$ from expression [2.1.28], it will results in expression for noise contributed by the second stage.

$$E_{\text{2, stage}}^2 = E_{M2}^2 \cdot K_{i2}^2 + I_{M3}^2 \cdot \frac{1}{1} \cdot \frac{1}{g_{ds.M3}} \cdot \left(1 \cdot g_{ds.M2} + g_{ds.M1} \right)$$

$$= \left(\frac{1}{1} \cdot \frac{1}{g_{ds.M3}} \cdot \left(1 \cdot g_{ds.M2} + g_{ds.M1} \right) \right)^2 \tag{2.1.29}$$

The expression for equivalent input noise voltage of the entire LNA can be written as:

$$E_{ni}^2 = \frac{E_{\text{no, M1}}^2}{K_{i1}^2} + \frac{E_{\text{2, stage}}^2}{K_{i2}^2} \tag{2.1.30}$$

The noise figure $NF$, [(10), on page 44], will be calculated to:

$$NF = 10\log \frac{E_{ni}^2}{E_S^2} \tag{2.1.31}$$
Results of noise calculations

<table>
<thead>
<tr>
<th></th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$E_S^2$</td>
<td>$8.28 \cdot 10^{-19} V^2$</td>
</tr>
<tr>
<td>$I_R^2$</td>
<td>$3.31 \cdot 10^{-24} A^2$</td>
</tr>
<tr>
<td>$I_n^2$</td>
<td>$2.16 \cdot 10^{-25} A^2$</td>
</tr>
<tr>
<td>$E_n^2$</td>
<td>$1.11 \cdot 10^{-18} V^2$</td>
</tr>
<tr>
<td>$E_i^2$</td>
<td>$1.90 \cdot 10^{-18} V^2$</td>
</tr>
<tr>
<td>$E_{noM1}^2$</td>
<td>$1.76 \cdot 10^{-17} V^2$</td>
</tr>
<tr>
<td>$E_{output}^2$</td>
<td>$1.86 \cdot 10^{-14} V^2$</td>
</tr>
<tr>
<td>$E_{2stage}^2$</td>
<td>$8.33 \cdot 10^{-15} V^2$</td>
</tr>
<tr>
<td>$E_{mi}^2$</td>
<td>$3.67 \cdot 10^{-18} V^2$</td>
</tr>
<tr>
<td>NF</td>
<td>6.48 dB</td>
</tr>
</tbody>
</table>

Table 2.1-4: Calculated noise values

The detailed calculations of the values shown in table below are shown in Appendix E.

### 2.1.3.7. Noise countermeasure

The calculated noise values shown in the table above are almost the same as the simulated values. The component noise can be reduced even more, but is a big challenge since the noise reduction can change the functionality of the circuit. For instance, the thermal noise generated by the transistors can be reduced, by reducing the $g_m$ of the transistor. This can affect the circuit’s functionality. Since the LNA is single-ended and the dominant noise sources are the transistors $M1$, $M2$ and $M3$ there are not many opportunities to reduce the component noise. It is possible to reduce the component noise even more, without changing the circuit’s functionality by:

- increasing the bias resistor $R$ ⇒ increase the voltage gain $K_{11}$ ⇒ reduce $E_{mi}$

The resistor $R$ can not be increased infinity, but can be increased to the point when the circuits gain start to decrease.
2.1.3.8. Noise simulations

As mentioned earlier it can be a big challenge to calculate very precisely the noise contribution from the components. The precise calculation requires that the correlations, parasites and undesired signals must be taken into consideration. Without simplifications and approximations it can be very difficult to calculate the noise contribution from different components. Neither does the Cadence simulator take into consideration all factors required to be able to get the precise results. The different noise simulations are done in order to find the variation between the simulation and calculation results. Simulation results show that the total noise is higher than the calculated total noise.

2.1.3.9. Noise at the output of the LNA

Analysis of the total noise contribution at the output of the LNA is shown in figure [2.1-20]. The highest noise contribution is at low frequencies and this is because of the flicker noise. Increasing the frequency leads to making the thermal noise more dominant, since the flicker noise decreases. The zoomed area of the figure [2.1-20] shows a noise contribution at the output of the LNA. The peak shows the amount of noise in the pass band, which will be forwarded to the mixer.

Figure 2.1-20: Simulated noise on the output of the LNA
2.1.3.10. **Noise at the input of the LNA**

Equivalent input noise is the output noise divided by the gain as shown in expression [2.1.30]. The lower limit of the equivalent input noise is the noise contributed by the sensor. Therefore it is very difficult to meet design requirements if the sensor contributes more noise than what is demanded for equivalent input noise. The equivalent input noise $E_{ni}$ represents all noise sources, referring all noise sources to the signal source location. This simplifies evaluation of S/N, because both signal and equivalent noise are then present at the same point in the system.

![Simulated equivalent input noise of the LNA](image)

**Figure 2.1-21: Simulated equivalent input noise of the LNA**

The figure [2.1-21] shows the equivalent input noise, and the noise is highest at low frequencies. As the graph shows, the noise around the RF frequency is lower compared with noise at other frequencies, because the gain is highest at this point.
2.1.3.11. Noise Figure

The noise figure is a measure of the signal-to-noise degradation attributed to the amplifier. The ideal amplifier adds no noise and that leads to the NF= 0 dB. In this case the simulator shows that NF around the RF frequency is 8.5 dB, [Figure 2.1-22]. The bandwidth during the simulation is set to 1 Hz.

![Noise figure graph](image)

**Figure 2.1-22: Noise figure**

According to the simulation the noise figure is lowest around frequency of 4 GHz. This is because both the gain and the equivalent input noise are lowest at this point. The calculation and simulation results are compared in the table below:

<table>
<thead>
<tr>
<th>Result of noise calculation and simulation at 2.5 GHz</th>
<th>Calculated results</th>
<th>Simulated results</th>
</tr>
</thead>
<tbody>
<tr>
<td>$K_{tot}$</td>
<td>71.15</td>
<td>78.77</td>
</tr>
<tr>
<td>$E_{output}^2$</td>
<td>$1.88 \cdot 10^{-14} V^2$</td>
<td>$4.02 \cdot 10^{-14} V^2$</td>
</tr>
<tr>
<td>$E_{ni}^2$</td>
<td>$3.67 \cdot 10^{-18} V^2$</td>
<td>$6.48 \cdot 10^{-18} V^2$</td>
</tr>
<tr>
<td>NF</td>
<td>6.48 dB</td>
<td>8.53 dB</td>
</tr>
</tbody>
</table>

**Table 2.1-5: Compared noise values**

As the table [2.1-5] shows there is a variation between the calculated and simulated values. The greatest variation is at the output of the LNA. It seems that the simulator includes some noise from the mixer at this point. This is the main reason for variation between simulation and calculation results.
2.1.3.12. Calculative variation

There is a variation between the calculation and simulation results. The small variation is expected and that is because of simplifying some of the expressions for noise calculation. For instance, not all parasitic were taken into consideration. Using a different formula caused the greatest variation. In documentation and manuals of the design tool, Cadence, it is explained which formulas that are used by the simulator.

<table>
<thead>
<tr>
<th></th>
<th>Formulas used by Cadence</th>
<th>Formulas used in calculations</th>
</tr>
</thead>
<tbody>
<tr>
<td>Output signal $V_{out}$</td>
<td>Not available</td>
<td>$V_{in} \left( \frac{R}{R_S + \frac{1}{\omega C_i} + R} \right) \left( \frac{g_{ds2} + g_{ds3}}{g_{ds3}} \right) \left( -\frac{g_{m1}}{g_{m2} + g_{mhr2}} \right) \left( \frac{g_{m2}}{g_{ds3}} \right)$</td>
</tr>
<tr>
<td>Thermal noise $I_{nd}^2$</td>
<td>$8kT (g_m + g_{mb} + g_{ds}) \Delta f \left[ \frac{3}{2} - \frac{V_D}{2V_{DSAT}} \right]$</td>
<td>$8kT g_m \Delta f$</td>
</tr>
<tr>
<td>Flicker noise $I_f^2$</td>
<td>$\frac{K_F I_{DS}^2 \Delta f}{C_{ox} W_{eff} L_{eff} f_{ef}^{AF}}$</td>
<td>$\frac{K_F I_D^2 \Delta f}{f C_{ox} L_{eff}^{2f}}$</td>
</tr>
</tbody>
</table>

Table 2.1-6: Formulas used by Cadence and in calculations

The formula for calculation of the output signal of the LNA, $V_{out}$, which is used in calculation, is given in table [2.1-6]. As the formula used by Cadence was not available, it is difficult to explain the difference. The difference is not great, but the formula for signal gain, where the term $V_{out}$ is part of, is affected by this difference. Since the noise calculation for entire LNA depends on the signal gain, this difference is also partly responsible for the calculative variations of the noise figure, equivalent input and output noise.

The formula for the calculation of thermal noise in an MOS transistor used by the simulator is more advanced than the formula used in calculation. In addition to transconductance $g_m$, this formula takes also into consideration channel conductance $g_{ds} = \frac{\partial I_{DS}}{\partial V_{DS}}$, body transconductance $g_{mb} = \frac{\partial I_{DS}}{\partial V_{SB}} g_{mb}$ and the term $\left[ \frac{3}{2} - \frac{V_D}{2V_{DSAT}} \right]$. The formula used by Cadence simulator gives the more precise result than the formula used in calculation, [Table 2.1-6]. Since the term transconductance $g_m$ is much greater than $g_{ds}$ and $g_{mb}$, excluding the terms $g_{ds}$ and $g_{mb}$ gives a very good approximation. Additionally the Cadence includes the thermal noise from the layout. It includes noise caused by resistance in the poly layer, which the gate of the transistor is made of. This difference also affects the calculative variation of the equivalent input and output noise of entire LNA, but not so much as the difference of the calculation and simulation of $V_{out}$. 
The formula for calculation of the flicker noise used by Cadence calculates the noise voltage on the gate. It divides the flicker noise by the $g_{m}$ of the transistor. Independent of the signal path, the flicker noise is calculated back to the gate of the transistor. This method is not the same as the method described in references of this thesis, [(10), on page 150]. If desired to calculate the flicker noise over a wider frequency range, the formula [2.1.32] will give the most correct result.

$$\int_{f_{c}}^{f} \frac{1}{f} \, dt$$

[2.1.32]

In formula for flicker noise, the Cadence uses this approximation: \(\int_{f}^{f} \frac{1}{f} \, dt \approx \frac{1}{f} \Delta f\). This will give only a small variation in calculation when $\Delta f$ is relative small.

The calculative variation of the final result as for instance the noise figure of the LNA can be affected by different factors. The conclusion is that it is a great challenge to get the simulation and calculation results to be exactly the same especially when the different formulas and simplifications are used.
2.2. Mixer

Mixer is usually used to perform the frequency translation to the frequency which is more suitable for further processing in the next stage. The operation in the next stage can consists of transmitting the signal through the antenna or signal processing in a receiver. If the IF frequency at the output of the mixer is higher than the RF frequency, the up-conversion mixer is used. Those mixers are usually part of the transmitter architectures. The architectures described in this thesis are receivers, which mean that the output frequency of the mixer is lower than RF frequency. The mixer used in receiver architectures is down-conversion mixer. The receiver architectures can be divided into heterodyne and homodyne receivers.

2.2.1. Heterodyne and homodyne architectures

2.2.1.1. Heterodyne receivers

The advantage of the heterodyne receivers is that the signal band is translated into much lower frequencies, and this again results in lower demand on Q of channel select filters. The signal is transformed by means of the mixer, where the multiplication is performed. In order to translate the frequency from $\omega_1$ to the lower frequency $\omega_2$, the signal first gets mixed with $A \cos \omega_0 t$ where $\omega_0 = \omega_1 - \omega_2$. The rest of the signals that occur in the spectrum can be removed by the LP filter. This operation is called downconversion mixing. [(1), on page 123]

![Figure 2.2-1: Simple heterodyne downconversion](image)

What makes demands to the LP filter is the size of the RF-LO signal and its distance from other unwanted signals. If the distance between the RF-LO signal and the rest of the unwanted signals is large, it means little demand from the filter. The distance between neighbour frequencies is very important when it comes to which order the filter is going to get, especially when the band-pass filters are considered. If the distance to the neighbour signal is too short, it can be taken into consideration to move the frequency of the LO signal closer to the RF frequency, so the down converted signal gets a lower
frequency. The filter order is equal to the frequency of the desired signal divided by the frequency bandwidth that will pass through the filter. Consequently, there will be less demand to the filter as long as the desired signal is a low frequent signal, or the distance of the neighbour is greater.

\[ n = \frac{\omega_{RF}}{\Delta\omega} \]  

After the filtration the RF-LO signal, known as intermediate frequency IF, will be taken out to further processing. A system that is able to multiply two signals and get multiple frequency components at the output will be based on either multiplication or nonlinearity.

### 2.2.1.2. Image frequency

A problem which may occur in suchlike architectures is the image frequency. By analog multiplication, the polarity of the difference between the two input frequencies does not make any difference. E.g. if two frequencies \( RF(t) \) and \( LO(t) \) that will be mixed, the filtered product of these two frequencies could be written as [9]:

\[
RF(t) = A_{RF} \cos \omega_{RF} t \quad \text{LO}(t) = A_{LO} \cos \omega_{LO} t \Rightarrow \\
RF(t) * \text{LO}(t) = \cos(\omega_{RF} - \omega_{LO}) t = \cos(\omega_{LO} - \omega_{RF}) t
\]

Frequencies placed symmetrical on each side of the LO frequency, are down-converted to the same centre frequency. [(9), on page 580]
The RF signal \( \omega_{RF} = \omega_{LO} + \omega_{IF} \) frequency is transformed in this way:

\[
\omega_{RF} - \omega_{LO} \Rightarrow \omega_{IF}
\]

while the image frequency \( \omega_{IM} = \omega_{LO} - \omega_{IF} \) is transformed in this way:

\[
\omega_{IM} - \omega_{LO} = (\omega_{LO} - \omega_{IF}) - \omega_{LO} \Rightarrow -\omega_{IF}
\]

![Figure 2.2-2: The generation of the image frequency](image-url)
By that very fact, that $\cos(-\omega_{IF}t) = \cos(\omega_{IF}t)$, this shows that both frequency spectra end up at the same place. This problem can be very serious, especially within wireless standards. Here it can be possible to control own signals, but keeping track of signals that come from other bands is much harder.

2.2.1.3. **Trade off in heterodyne architectures**

Trade off in heterodyne architectures means trade off between image rejection and channel selection. So saying it can be problematic to choose a reasonable $IF$ frequency. To do this several factors must be considered:
- The amount of image noise
- The distance between wanted band and the image frequency
- The availability and the filter’s physical size for different frequencies

Choosing a high frequency of the $IF$ signal leads to better image rejection, while at low frequencies of $IF$, it is easier to suppress neighbouring frequencies. With that, the choice of $IF$ implies trade off between sensitivity and selectivity, since the image can degrade the sensitivity of the receiver. This problem can be solved in several ways and one of them is to introduce e.g. dual $IF$ topology, i.e. making multiple down-conversions, where each one of them is followed by filtering and amplification. A disadvantage within heterodyne architectures can be that image reject filter is often carried out as a passive, external component. The result of this may be that LNA has to drive 50 $\Omega$ input impedance of the filter that leads to more trade off between amplification, NFS and stability.
2.2.1.4. Homodyne receivers

The distinctive feature of homodyne receivers is that the \( RF \) and \( LO \) frequency are equal. There are both advantages and disadvantages with this. The two most important advantages with this architecture are that there is no need for image filter, and that LNA doesn’t need to drive 50 \( \Omega \) as mentioned above. It needs only LP filter that can filter out unwanted frequencies. It must also allow for the fact that it is more difficult rejecting out the channel interferers by means of an active LP than a passive LP, [(1), on page 130].

\[
V_{\text{out}}(t) = I_{DS}R_D[a + bS(t)]
\]  

[2.2.3]

When the leakage signal of \( LO \) comes to the output of LNA, and gets mixed with \( LO \), this will produce a DC component, i.e. the term \( a \) will increase. The same can happen when the leakage signal of \( RF \) comes over \( LO \)’s section and gets mixed with itself. As opposed to homodyne receivers, this problem is much smaller for heterodyne since \( LO \) is different from \( RF \). Self-mixing may occur here as well, but DC is easily removed since \( IF \) signal is far away from 0 frequency area. So the disadvantage of homodyne receivers is that it needs DC offset cancellation.
2.2.1.6. Feedthrough

In reality, mixers have direct feedthrough from the RF input to the IF output, especially if it is high frequencies design. The causes of feedthrough are either parasitic capacitances or the actual switching of LO transistors. When they switch off and on, in a short period of time it happens that both transistors are on and then it is opened for the signals in the RF band to pass right through to the IF output. Due to the asymmetry, the mixers’ operation can be expressed like this:

\[ V_{RF}(t)(a + A \cos \omega_{LO}t) \] where \( a \) is a constant. With that, \( V_{RF}(t) \) can occur at the output without frequency transformation

If \( X_{IN}(t) = (A + \epsilon \cos \omega_n(t))(a \cos \omega_c(t) + b \sin \omega_c(t)) \) where \( \epsilon \cos \omega_n(t) \) is low frequencies amplitude with signal. Second-order term can then be written as \((a^2 + b^2)A \epsilon \cos \omega_n(t)\).

This term is a modulated signal transformed to the IF band that passes through the mixer and interfere the IF signal.

2.2.1.7. Flicker noise

Because of the fact that the down-converted signal lies at 0 frequency, it can be very hard to pick it up for further processing because of a big part of the flicker noise. This type of noise is, as explained before, a low frequency noise. Avoiding this depends on high amplification in the RF area. Therefore it is common to use active mixers in design, since these mixers amplify the RF signal. It is also possible to increase the size of the transistors in the following stage. From the formula for flicker noise, it is easy to see that the increased size of the transistors reduces that kind of noise.
2.2.2. **Down-conversion mixer**

After the RF signal is picked up and amplified by the LNA, it is forwarded to the mixer. The figure [2.2-4] shows the mixer used in the CMOS architecture described in this thesis.

![Figure 2.2-4: CMOS mixer](image)

The advantage of this mixer is that the RF and LO signals are isolated from each other, [Figure. 2.2-4], and this reduces LO leakage to the antenna. This mixer converts RF signals to current by means of the input transistor, M8, of the mixer and thereafter a multiplication with a square wave of the LO frequency is performed. The current at the output is then:

$$I_{out}(t) = \left[ A_{LO} g_{m\_LO} \frac{2}{\pi} \cos \omega_{LO} t \right] I_{BIAS} + A_{RF} g_{m\_RF} \frac{2}{\pi} \cos \omega_{RF} t$$

[2.2.4]

The LO signal is a typical square pulse which can be written as \( \frac{4}{\pi} \cos \) of the fundamental frequency, but in this case it was written as \( \frac{2}{\pi} \) since the amplitude is \( \frac{A_{LO}}{2} \).

This mixer is differential and it implies that it has odd symmetry. This means that the square wave consists of odd harmonic and therefore the current is multiplied with odd integers. The frequency spectrum at the output consists, as mentioned before, of the sum and the difference of RF and LO. In addition, the odd harmonic of the LO signal will come directly to the output because of the multiplication of the LO signal with DC bias current. This type of mixer is known as a single balanced mixer, because the LO signal is presented with the frequency spectrum at the output. The current at the output of the mixer can be defined as the sum of all odd harmonics. The higher harmonics are not so
important since they are not amplified so much and therefore do not contribute with much interference. The current at the output can be defined like this:

\[ I_{\text{out}} = \sum_{n=1,3,5,\ldots}^{\infty} \alpha_n A^n \cos^n \omega_{LO} \left[ I_{\text{BIAS}} + B \cos \omega_{RF} \right] \]  

where \( n = \text{odd number} \)

\[ A = A_{LO} g_{m6} \frac{2}{\pi} \quad \text{(2.2.6)} \]

\[ B = A_{RF} g_{m8} \frac{2}{\pi} \quad \text{(2.2.7)} \]

where \( g_m \) is the transconductance of \( LO \) and \( RF \) transistor of the mixer. Both \( RF \) and \( LO \) are transformed from voltage to current by means of these transistors and AC must be multiplied with the transconductance. If it is desired to avoid the presence of the \( LO \) signal at the output, more advanced mixers like for instance, double balanced mixers can be used, but they are not described in this thesis.

### 2.2.2.1. Evaluation of the frequency domain

When one carries out Direct Fourier transform, \( DFT \), analysis at the output of the mixer, different signals occur. Some of these are predictable, while some others can be noise contribution from different components in the circuit.

![Fourier transform on V_{IF}](image)

The DFT analysis performed at the output of the mixer in CMOS architecture shows clearly the \( IF \) signal which is at 100 MHz frequency. \( LO \) and \( RF \) signals come trough because this is a single balanced mixer. The odd harmonics of the \( LO \) are also clearly shown in the figure [2.2-5]. Since all those signals are not close to the \( IF \) signal it will be easy to pick up the \( IF \) signal and filter those other signals out.
2.2.3. Noise in mixers

Beside the noise which is generated by the components that the mixer and LNA consist of, other signals that come into the desired spectre have to be taken into account. These can also contribute in interfering with the IF signal. Both the image frequency and the harmonic of the LO contribute to increased noise in the down-conversion band. To simplify the calculation, the higher harmonic can be disregarded, since it has lower amplitude and hence contribute with less noise. Besides, LNA have band pass filter characteristic at the output that leads to limited bandwidth of the RF signal. This again leads to reduction of the conversion gain at high frequencies. Even though this concerns high frequencies of the RF and LO inputs, the flicker noise is nevertheless important, especially if the receiver is homodyne.

2.2.3.1. Noise calculation method

In order to simplify the calculations, the circuit was divided into three sections [(1), on page 199], [(5), on page 5]:

![Mixer sections diagram]

1. IF section
2. Time – Variant section
3. RF section

Thereafter the noise sources in these different sections have to be identified.
2.2.3.2. IF section

The IF section consists of two resistors, $R_D$, and the contribution is thermal noise. Other components could be used to make resistors as well, but it is preferably with components that contribute with as little flicker noise as possible, especially concerning down-conversion mixers.

2.2.3.3. RF section

The noise contribution of the RF section consists of the noise that comes from the LNA, and the noise that the transistor $M_8$ itself contributes with. At lower frequencies, flicker noise from the input transistor, $M_8$, and from the LNA can place itself upon the RF signal. In the same way as the RF signal, it will be transformed in frequencies. At high frequencies, the thermal noise is dominating. Still, some of the flicker noise may pass through, because the LNA does not have a perfect band-pass filter characteristic at the output.

2.2.3.4. Time variant section

The time variant section consists of switch transistors that produce thermal and flicker noise. These transistors make the noise contribution from the time variant section to be both direct and indirect.

**Direct influence:**
Flicker noise that occurs at the gate of the LO transistors is directly pursued to the output without frequency transformation, and this can interfere with the signal down-converted to IF. The thermal noise placed on the LO signal will most likely place itself at DC value.

**Indirect influence:**
The noise at the output of the mixer is highly dependent on the bias current through the transistors. Since the LO transistors switch in anti-phase, this will lead to charging and discharging of the gate-drain capacitance of the $M_6$ and $M_7$, as the transistors switch. If the LO signal is digital, this influence can result in spikes placing themselves at the edge of the square-shaped pulse, i.e. when the signal is going up or down.
2.2.3.5. Flicker noise

The maximum contribution of the flicker noise can be achieved from the LO transistors, while the contribution from the RF input is less, since this transistor is not directly connected to the output. SNR of a single balanced mixer is expressed as [(2), on page 17]:

\[
\text{SNR} = \frac{4\pi A}{2\pi (V_{GS} - V_t) V_n} \frac{V_{in}}{V_{V}} = \frac{2A}{(V_{GS} - V_t) V_n} \quad [2.2.8]
\]

Where \( A \) is the amplitude of the LO signal, considering that the LO signal is a sinus signal. \( V_{in} \) is an input signal, in other words the RF signal at the gate of the transistor M8. \( V_n \) is flicker noise on the gate of the LO transistors. In order to reduce the flicker noise, there are three options:

- From the formula for flicker noise, it is easy to see that noise can be reduced by increasing the size of the LO transistors.
- The formula for SNR also shows that reduction of \((V_{GS} - V_t)\), improves SNR.
- Lower amplitude of the LO signal leads to less noise at the output.

In this case, the reduction of the flicker noise can lead to change of the bandwidth.

2.2.3.6. Thermal noise

Thermal noise is independent on the frequency and will be produced by both the \( R_D \) resistances and transistors that are a part of the mixer architecture. The LO transistors contribute with noise at the output when both are turned on. If one of the transistors is off, it does not contribute with thermal noise, neither does the one that is on, since it works like a cascade transistor, whose tail current is fixed to \( I \) by the RF input transconductance stage [(2), on page 20]. The power spectral density of the output current is expressed as follows:

\[
i_{o,n}^2 = 4kT\gamma \frac{I}{\pi A} \quad [2.2.9]
\]

This means that the thermal noise at the output of the LO transistors depends only on the LO amplitude and bias current, and not of the size of the transistor. If the size of the transistors increases, they use shorter time to turn themselves on and the bandwidth increases too. Nevertheless, since the transistor size increases, the input referred noise density will be reduced. The input noise is expressed by [(2), on page 20]:

\[
V_n^2 = \frac{4kT\gamma}{G_m} \quad [2.2.10]
\]

where \( G_m \) is transconductance at zero crossing and is given as:

\[
G_m = \frac{2I}{\Delta V} \quad [2.2.11]
\]
If the width is increased, the current through the transistor and $G_m$ increases. Increased $G_m$ leads to reduction of the input noise. Consequently, the integrated $rms$ noise at the output stays constant. As explained previously, the LO frequency and its odd harmonic will down-convert the noise of the IF band. Including the mixer conversion gain, that is $\frac{2}{\pi}$, the noise in the IF band can be written as follows [(2), on page 21]:

$$V_{o,n}^2 = n \times \frac{4kT\gamma}{g_m} \left( \frac{2}{\pi} g_m R_D \right)^2$$  \hspace{1cm} [2.2.12]

$n$ is given as:

$$n = 2 \left( 1 + \frac{1}{3^2} + \frac{1}{5^2} + \ldots \right) = \frac{\pi^2}{4}$$ \hspace{1cm} [2.2.13]

The term 1, first part of the expression [2.2.13] is noise $\omega_{LO} \pm \omega_{IF}$, down-converted by $LO$, the second part, $\frac{1}{3^2}$, is noise $3\omega_{LO} \pm \omega_{IF}$ down-converted by the third harmonic of $LO$, etc. Including the noise from resistances and switches, the total noise can be written as [2]:

$$V_{o,n}^2 = 8kTR_D + 8kT\gamma \frac{R_D^2 I}{\pi A} + n \times \frac{4kT\gamma}{g_m} \left( \frac{2}{\pi} g_m R_D \right)^2$$  \hspace{1cm} [2.2.14]

since $n = \frac{\pi^2}{4}$ the entire expression is simplified to this:

$$V_{o,n}^2 = 8kTR_D \left( 1 + \gamma \frac{R_D I}{\pi A} + \gamma \frac{g_m R_D}{2} \right)$$ \hspace{1cm} [2.2.15]

The first part is noise contribution from two resistances $R_D$, the second part is the output noise that is caused by the LO transistors, and the third part shows the noise pursued from the RF transistor $M8$ to the output of the mixer. This shows that the noise at the output of the mixer varies with the bias current and the amplitude of the LO signal. The table [2.2-1] shows the noise contribution from different parts of the mixer [Figure 2.2-6]. The calculation is shown in Appendix F.

<table>
<thead>
<tr>
<th>Mixer sections</th>
<th>Noise values</th>
</tr>
</thead>
<tbody>
<tr>
<td>IF section</td>
<td>$3.311 \cdot 10^{-16} V^2/Hz$</td>
</tr>
<tr>
<td>RF section</td>
<td>$5.82 \cdot 10^{-16} V^2/Hz$</td>
</tr>
<tr>
<td>Time Variant section</td>
<td>$2.17 \cdot 10^{-16} V^2/Hz$</td>
</tr>
<tr>
<td>Total noise in the mixer</td>
<td>$1.13 \cdot 10^{-15} V^2/Hz$</td>
</tr>
</tbody>
</table>

Table 2.2-1: Calculated noise values in the mixer
2.3. Layout

Even when the component noise is on an acceptable level, it is very important that the layout of the circuit is taken into consideration. There is a good chance that the results will not be as expected, and the reason for this is parasitics that occur in the layout. The parasitics contribute to the increased coupling noise in the circuit. The higher the frequency, the more noise is transferred through those parasitics components. Other factors like a choice of pads, signals properties and layout techniques are playing a key role considering the coupling noise in the circuit. The layout is shown in Appendix M.

2.3.1. Pads

There are different types of pads for different purposes. This is dependent on different factors, like the resistance in the pad, parasitic capacitances and the requirement for protection of the circuit (ESD). Basically, it was supposed to use RF pads that are 8-edged and have less capacitance than the pads which were used. The AMS library didn’t contain RF pads, and designing the actual pad was not a part of this thesis, so pads from the library were used. The pads which were used had much greater capacitance than expected in the first place when the circuit was optimized in the schematic.

2.3.1.1. LO signal

The clock signal from the local oscillator is digital and therefore it wasn’t critical to use pads with 200 Ω resistance. The LO signal is applied onto the gate of the transistors, and it is therefore important with ESD protection. These pads had better ESD protection than the pads with lower resistance [7].

2.3.1.2. $V_{in}$ signal

The $V_{in}$ signal is very small and the use of 200 Ω pads were not preferred here. The reason for this is that the noise of the input stage should be reduced to minimum, and a resistance in the signal path will increase the noise. Therefore, minimum resistance in the pad is desired, but the pads without resistance have a low ESD protection. This trade off was taken into consideration, and therefore the pad of 50 Ω was used here instead of the pad of 200 Ω. This implies that we have to figure on an extra resistance (that is serial with the resistance of the sensor) in the $E_n-I_n$ model.


2.3.1.3. The created pads

The pads where the inductors and the output signals are supposed to connect to are completely without protection. The reason for this is reducing the capacitance and the load on these places so that it doesn’t go at the sacrifice of the circuit’s functionality. In order to reduce the capacitance the signals had to be routed in metal 2 and the resistances in the pads were removed completely, since they contribute to increased load. This means that there is very little ESD protection on these places. The drain of the transistors in LNA will protect the circuit to a certain level. The reducing of the ESD protection is not critical at the output of the mixer either, since the outputs are connected to the drain of the LO transistors.

2.3.2. Layout noise and countermeasures

Especially in the high-frequency constructions, it is very important to think of noise countermeasures in the layout. This means:

- Placing of the components (not always important)
- Routing and shielding (very important)
- Analog and digital circuit. (important)

2.3.2.1. Placing of the components

Placing of the components in relation to each other can be a very important factor in noise reduction. The components that interfere too much should be placed farther away from the input stage and the parts of the circuit that are most sensitive to noise. The distance between the resistors and the LNA was increased, because the resistors are able to produce more heat than other components. It can increase the thermal noise since the temperature T is increased, but this is not critical in this design.
The input stage was placed to the left in the figure [2.3-1]. Greater distance was made between the input signal and the digital part of the circuit. The $V_{in}$ signal should have a shorter path from the pad to the ASIC. This was difficult to make because the shortest possible path should be at the place where the inductors were supposed to connect. Therefore more thermal noise at the input signal has to be taken in account. The resistance of the path will increase when the length increases, but not when the width increases. The total resistance in the path was calculated to 12 $\Omega$. $E_{n-I_n}$ model, [(10), on page 39], can be extended with the resistor in the pad, $R_{pad}$ and the resistor in the path, $R_{path}$. Since the $R_{pad}$ and the $R_{path}$ are serial with $R_S$, the noise from these resistors can be represented by means of an equivalent noise source, $E_{input}$.
Equivalent input noise can be found using this formula:

\[
E_i^2 = E_{i}^2 + E_{input}^2 \left( \frac{R}{R_S + R_{pad} + R_{path} + \frac{1}{\omega C_3} + R} \right)^2 + \\
\left( I_n^2 + I_n^2 \right) R \left( R_S + R_{pad} + R_{path} + \frac{1}{\omega C_3} + R \right)^2
\]

[2.3.1]

The results of the noise calculations, with and without the resistance in the pad and in the signal path, are compared in the table [2.3-1].

<table>
<thead>
<tr>
<th>Result of noise calculation</th>
<th>Noise excluding pad and path resistance</th>
<th>Noise including pad and path resistance</th>
</tr>
</thead>
<tbody>
<tr>
<td>(E_i^2)</td>
<td>1.90 (\cdot10^{-18} V^2)</td>
<td>2.94 (\cdot10^{-18} V^2)</td>
</tr>
<tr>
<td>(E_{no}^2)</td>
<td>1.76 (\cdot10^{-17} V^2)</td>
<td>2.66 (\cdot10^{-17} V^2)</td>
</tr>
<tr>
<td>(E_{output}^2)</td>
<td>1.86 (\cdot10^{-14} V^2)</td>
<td>2.39 (\cdot10^{-14} V^2)</td>
</tr>
<tr>
<td>(E_{2stage}^2)</td>
<td>8.33 (\cdot10^{-15} V^2)</td>
<td>8.33 (\cdot10^{-15} V^2)</td>
</tr>
<tr>
<td>(E_{ni}^2)</td>
<td>3.67 (\cdot10^{-18} V^2)</td>
<td>4.83 (\cdot10^{-18} V^2)</td>
</tr>
<tr>
<td>NF</td>
<td>6.48 dB</td>
<td>7.67 dB</td>
</tr>
</tbody>
</table>

Table 2.3-1: Result of noise calculation

Because of the thermal noise caused by the resistance in the path and from the resistance in the pad, the noise figure of the entire LNA has increased from 6.48 dB to 7.67 dB. The placing of the components in relation to each other is very important in the PCB design, as well. The band threads can bring noise from outside, through parasitic capacitances. The band threads should therefore be as short as possible, and this is dependent on the form of the package. The signals that are most sensitive to noise, i.e. the input signals, should be placed as close to the pin as possible. This was not done in this circuit, because shortest possible band threads had to have to pins where the inductors were supposed to be connected. Because of this, the circuit was displaced to the side of the package [Figure 2.3-3].
The consequence of this placing is that the input signal now has longer way from the pin to the circuit.

### 2.3.2.2. Routing

Routing of the layout means consideration of several things to be able to reduce the coupling noise. A broad path leads an increase of capacitance between the path and the substrate, while the resistance in the path is reduced. The most signals are routed in metal 2 since it has lowest capacitance to the substrate. At some places, where the signals are most sensitive to noise, the signals were shielded. The input signal was routed in metal 2 and under it a layer with metal 1, which is broader than the metal 2 layer, was placed. This leads to further reduction of the capacitance and the fringing fields between metal 2 and the substrate. The metal 1 protection layer was connected to the guarding of the input capacitor and consequently the input signal was separated from the substrate. Figure [2.3-4] shows the fringing fields and if the wider plate presents shielding, it is possible to see that the shield will stop these fields. If such a shield is placed between the “noisy signal” and the receptor, the receptor will not be affected by the noise from the “noisy signal”.

![Figure 2.3-3: The band diagram](image)

![Figure 2.3-4: Fringing capacitances](image)
The output of the pre-amplifier was protected in the same way, except that the shield here was connected to the capacitor in the mixer. In the layout it was hard to avoid the high-frequency signals crossing each other and in order to avoid the interference on the crossings the capacitance had to be reduced on these crossing points. The formula for the capacitance is given below, where \( W \) is the width and \( L \) is the length of the path, while \( D \) is the distance between the paths:

\[
C \approx \varepsilon \frac{WL}{D}
\]  

[2.3.2]

From the formula, it is easy to see that the capacitance is reduced by:

1. Reducing the surfaces of the paths
2. The increase of the distance between the signals
3. Shielding/protection

On the crossing itself, the signal path was narrowed, so that the area was reduced. A two layer process was used and this process does not allow any poly 1, poly 2, metal 1 and metal 2 on top of each other. The best solution would be to route one signal in poly 2 and the other one in metal 2, and connect poly 1 and metal 1 to the ground. Both signals will then be shielded from the substrate and from each other [Figure 2.3-5]:

![Figure 2.3-5: The shielding of the signals at the crossing points](image)

Because of the two layer process [8], the digital signal, \( LO \), had to be routed in poly 1 and \( CO \) signal, which is the analog signal, in metal 2. Between these signals, metal 1 layer was putted and connected to the ground potential. \( LO \) and \( CO \) signals were then shielded from each other, while \( LO \) was not shielded from the substrate. The shield was broadened as explained above, and it could now catch the noise contribution from the \( LO \) and \( CO \) signal together with fringing fields from these. The consequence of reducing the area of the signal path at the crossing points is increased resistance, but in this case this was not a big problem. The routing of signals in poly layer results in more resistance in the signal path and larger capacitance to the substrate. Since the \( LO \) signal is digital and a stronger signal then \( CO \), it was routed in poly.
2.3.2.3. Capacitive connections at the crossing points

At the crossing point between two high frequency signals, the coupling capacitance $C_{12}$ between these might cause a distortion of the signals, [(11), on page 34].

Figure 2.3-6: Capacitive coupling on the crossing point

In the layout, it was hard to avoid the LO signal crossing the RF signal [Figure 2.3-7]

Figure 2.3-7: Crossing point

In this case, the digital signal might interfere with the analog signal. The noise voltage $V_n$ between the analog signal path and ground might be calculated by means of the expression below [(11), on page 30]:

$$V_N = \frac{j\omega}{1 + \frac{j\omega}{R(C_{12} + C_{2G})}} V_1$$  \[2.3.3\]
The values of the terms are estimated by the Cadence in the layout editor.

<table>
<thead>
<tr>
<th>Term</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$C_{12}$</td>
<td>$0.027 \cdot 10^{-15} \text{ F}$</td>
</tr>
<tr>
<td>$C_{2G}$</td>
<td>$0.020 \cdot 10^{-15} \text{ F}$</td>
</tr>
<tr>
<td>$R$</td>
<td>$1157379.77 \Omega$</td>
</tr>
<tr>
<td>$V_1$</td>
<td>$300 \cdot 10^{-3} \text{ V}$</td>
</tr>
<tr>
<td>$\omega$</td>
<td>$1.508 \cdot 10^{-8}$</td>
</tr>
</tbody>
</table>

The noise voltage produced between the receptor, $CO$, and ground is calculated to:

$$V_N = 1.41 \cdot 10^{-16} \text{ V}$$

This is shown in Appendix G. The $LO$ signal is a digital signal from the local oscillator and is the one that is least sensitive to noise. It is possible to see the capacitances on the figure [2.3-6]. The resistance $R$ is impedance from the receptor layer to the ground. If there is a shield provided, that is connected to the ground, the voltage between these layers will be:

$$V_N = V_S = 0$$  \[2.3.4\]

This is illustrated in figure [2.3-8]. Through the capacitors $C_{2S}$ and $C_{1S}$ the noise from both $LO$ and the receptor layers will be transferred to the shield and pursued directly to the ground, since the shield is connected to the ground, [(11), on page 30].

![Diagram ofshielded crossing point](image)

**Figure 2.3-8: Shielded crossing point**

In our case, the shield covers the entire crossing point between $LO$ and the receptor. This is the ideal solution, because noise influence is then eliminated.
2.3.2.4. 45 degrees routing angle

In high-frequency constructions the reflections are much more considered than in low-frequency constructions. It is a great danger that the desired signal gets interfered with by reflections both at ASIC and at PCB. Therefore the sharp curves, 90 degrees routing, should be avoided. Besides, the radiation is reduced because if the signal comes across a 90 degrees or sharper curve, it may cause the signal to radiate more than normal on the actual curve. Therefore all signal paths were routed in a 45 degrees angle.

2.3.2.5. Thermal noise in the gate poly

The gate of the transistors is made of polysilicon, and since it has high resistance, the thermal noise will often be able to overcome the channel noise. Equivalent resistance from the gate can be calculated using following formula, [(4), page 22-24]:

\[ R_g \approx \frac{K R_o W}{n^2 L} \]  \[2.3.5\]

\( R_o \) = sheet resistance
\( W \) = the complete transistor width
\( L \) = the length of the gate
\( n \) = number of poly stripes (gate fingers)

\( K = 1/3 \) since gate fingers are connected to only one side; otherwise it is 1/12 when gate fingers are connected on both sides.

With these assumptions the thermal noise on the gate is then calculated out from this formula:

\[ E_{t\_gate} = \sqrt{4kT R_g} \]  \[2.3.6\]

The noise on the gate was calculated for the following transistors:
The $LO$ signals are digital while the rest of the circuit is analog. The digital signals can contribute with noise because of the fact that some high spikes can occur where the signals switch. In some cases, a coupling capacitor can be used to filter out spikes [7]. This was not necessary in this case since the circuit was divided into two parts, analog and digital. The pad ring was broken at two places and every part had its own $V_{DD}$ and $V_{SS}$ pads. The digital part consists of 4 $LO$ signals and 4 different ground pads. Each of the $LO$ signals had its own shield that was connected to the ground, and these ground points were, as mentioned above, separated from each other. So saying the $LO$ signal was then shielded all the way from the substrate, except for at the intersection between $LO$ and $CO$, which is the analog signal between the drain of the transistor $M8$ and the sources of the transistors $M6$ and $M7$.

<table>
<thead>
<tr>
<th>Transistor</th>
<th>$E_{i_{gate}}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>M1</td>
<td>$9.08 \cdot 10^{-10}$ $V$ $/ \sqrt{Hz}$</td>
</tr>
<tr>
<td>M2</td>
<td>$7.83 \cdot 10^{-10}$ $V$ $/ \sqrt{Hz}$</td>
</tr>
<tr>
<td>M3</td>
<td>$6.36 \cdot 10^{-10}$ $V$ $/ \sqrt{Hz}$</td>
</tr>
<tr>
<td>M8</td>
<td>$4.85 \cdot 10^{-10}$ $V$ $/ \sqrt{Hz}$</td>
</tr>
<tr>
<td>M9</td>
<td>$4.98 \cdot 10^{-10}$ $V$ $/ \sqrt{Hz}$</td>
</tr>
<tr>
<td>M6/M7</td>
<td>$1.29 \cdot 10^{-9}$ $V$ $/ \sqrt{Hz}$</td>
</tr>
</tbody>
</table>

Table 2.3-2: Gate noise values
2.3.3. Limitations

2.3.3.1. Realisation of the inductors

The biggest problem in the design was realisation of the inductors. The version of Cadence that was used was not very suitable for RF design and could not estimate the inductance on the inductors placed on the chip. Without simulation it would be hard to find the exact value of these, and this could have resulted in a bigger variance under the production than that was estimated. It was necessary to know exactly the inductance value at the output of the LNA, to be able to decide the wanted resonance frequency. With this we agreed to use external inductors. The fact that the pads have very much capacitance to the substrate led to the conclusion that the inductor must have an inductance of 4 nH. This is hard to achieve because the band-leads amount to more than that. Approximated value of inductance is: 1 mm of the band-leads has about 1 nH inductance. Band-leads to the pad where the inductor is connected have to be made as short as possible In order to reduce the length of the band-leads, the process house placed the circuit in the package as shown in figure [2.3-3]. If the inductor cannot compensate for all that capacitance, then the resonant frequency must be reduced.

2.3.3.2. Output load

The only reason why the circuit is placed as it is, is because of the inductors. The signal paths that lead the signal to the output got much longer than planned because of the placing. This caused increased capacitance to the substrate together with the increased load at the output. The most important reason to increased load at the output is the pads. The load caused reduction of DC current that could lead the signal to the output. This problem was partly solved, by making new pads that made the capacitance almost half of what it was before. The resistance in the pad was also removed and this again sacrificed the ESD protection of the pads at the output. In addition, the mixer was modified so that it was possible to get more DC at the output. The modification aimed at reducing the resistors \( R_D \). The signal was not completely perfect, but this improved the results considerably. Another suggestion came up: to make voltage followers but the amplifiers which were found in the library were too slow and not suitable for signals greater than 7 MHz. Because the desired signals had a higher frequency than this, these amplifiers would only fade the outputs signal. The time was a limiting factor for making the amplifiers myself and this could affect my thesis work. At the end, the input signal \( V_{in} \) had to be increased to 5 – 10 mV instead of 1 mV, in order to get a result which is possible to measure. Factors which could have improved results:

- RF pads
- Inductors on the chip
- RF package
- Voltage follower
2.4. Conclusion – First part

In the first part a single-ended LNA and a single balanced mixer implemented in a 0.6 μm CMOS technology were analyzed. The noise contribution was calculated manually and by using the noise models included in the design tool Cadence. The layout of the circuit was made and the chip was produced. The layout is shown in Appendix M. Component noise was calculated for both LNA and mixer, and calculations show that the noise of the first stage of the LNA is dominant. The noise generated by the mixer does not affect the equivalent input noise of the LNA in great extent. The dominant component noise source is the thermal noise produced by the sensor which in this case is an antenna. Another dominant noise source is the thermal noise generated by the input transistor. The most important noise sources of coupling noise were taken into consideration, and some of the noise reduction techniques were used. For instance, the shielding was used in different ways, and the digital and analog signals were separated by dividing the pad ring into two parts. Applying these techniques result in great reduction of the coupling noise. Use of pads was also carefully considered, concerning the noise generated in different pad types. Pads used from the AMS library have different logics that provide the ESD protection. The components that provides the ESD protection also generates noise that has to be taken into consideration. Considering both the component and the coupling noise, the dominant noise sources are:

1. thermal noise contributed by the sensor resistance, which in this case is an antenna
2. thermal noise generated in the input pad. This is caused by the resistor that lies in the signal path. The resistor is the part of the pads ESD protection.
3. noise generated by the input transistor
4. thermal noise generated by the parasitic resistor of the metal layer between the pad and the inputs transistor M1.

Including the coupling noise sources mentioned above, the noise figure, NF, of the LNA increased from 6.48 to 7.67 dB. There is a variation between the simulated and calculated results. However, the variation is not great. Since the documentation of the design tool Cadence is not available, it is difficult to explain exactly the difference between the simulation and calculation. Comparing the component noise results with the results of the similar architecture shows that the NF is almost the same.

<table>
<thead>
<tr>
<th>Noise figure</th>
<th>Calculated:</th>
<th>Simulated:</th>
<th>Reference [16]:</th>
</tr>
</thead>
<tbody>
<tr>
<td>NF</td>
<td>6.48 dB</td>
<td>8.53 dB</td>
<td>5 dB</td>
</tr>
</tbody>
</table>

It is possible to reduce it even more according to the noise countermeasures shown in subchapter [2.1.3.4.2]. The final results of this part are useful guidance when the noise contribution of similar architectures is considered. The method and procedure used in this part can be applied to other CMOS technologies as well. Since the chip is produced the measurements can be done in further work and results can be compared with the calculated results.
SECOND PART

BiCMOS and SiGe Technology
3.1. Introduction –Second part

The second part of the thesis describes the receiver architecture designed in two different technologies, BiCMOS and SiGe. Like the architecture described in part one, this one also consists of the LNA and the mixer. The difference is that in this architecture the differential LNA was used instead of the single ended. The mixer architecture is also different from the mixer designed in part one.

The main purposes are to:

• calculate and simulate the noise contribution of the LNA in both the BiCMOS and the SiGe technology and compare the results
• find out how the noise generated by the LNA can be minimized
• conclude which circuit is best suited for use

Since the receiver architecture is similar for both BiCMOS and SiGe, it is interesting to see which technology has the higher noise contribution and how much noise can be reduced by choosing the most expensive technology. It is expected that using the SiGe technology in this architecture will result in less noise contribution than using the BiCMOS. The calculation results will show that in addition to choice of technology, other factors will also play a key role in achieving a noise reduction. Even when the most expensive technology is chosen, there is not guarantee that the total noise contribution will be less. The receiver architectures for both BiCMOS and SiGe are similar, as explained above, but the size of some of the components is different. The frequency and amplitude of the RF and LO signals are also the same. Those similarities simplify the calculations since the same formulas were used for both technologies. The procedure in the design phase was almost the same as in part one. The same simulations were performed and the calculation results are compared with the simulation results. A value of operations points of transistors was calculated by the design tool Cadence, and was used in the calculations. The main difference is that this circuit is not produced and therefore the reduction and calculation of layout noise was not taken in consideration as in part one. Only the calculation of component noise was taken into account. Reduction of the layout noise depends to a large degree on layout technique and almost the same contra measures as described in part one will be used. The $E_{n}J_{n}$ model was used in both the CMOS and the BiCMOS design, and the main advantage of this model is exactly that it can be used to present any type of amplifier, independent of choice of technology. The noise transistor model was not the same. The hybrid-$\pi$ model was used in bipolar technology. LNA, described in the second part, has four stages. Providing the sufficient gain in each stage, the noise contribution from the mixer will not be critical for equivalent input noise of the LNA. The major difference considering noise contribution in bipolar and CMOS technology is that the CMOS transistors contribute more flicker noise while the bipolar transistors contribute more shot noise. The contribution of the shot noise is negligible in CMOS technology, while flicker noise is negligible in the bipolar technology. Generating as little flicker noise as possible is a great advantage in mixer design, because it is easier to filter out the desired signal at the output of the mixer, especially if the desired signal is low frequent. This receiver architecture also has a resonant circuit which can be used to tune the frequency at the output of the LNA.
Therefore, this receiver can be both homodyne and heterodyne, as explained in Chapter 2.2. The importance of flicker noise contribution at the output of the mixer becomes even more important if the receiver is homodyne.

### 3.2. LNA design and function of the circuit

The LNA is the differential amplifier and an emitter-coupled pair shown in figure [3.2-1]. This LNA has two input signals, $V_1$ and $V_2$, and has the ability to amplify the differential signals. The objective of the differential amplifier is to amplify only the difference signal and to reject the common signal. Another advantage of the differential amplifier is to provide a high gain with a good DC stability. Input signals $V_1$ and $V_2$ can be separated into a differential mode signal $V_{DM}$ and common-mode signal $V_{CM}$.

![Figure 3.2-1: Low noise amplifier](image)

Each signal has half of the difference signal and the entire common signal. A situation where equal signals are applied at the input is called common mode. In this case the situation is referred to as the differential mode because the inputs signals $V_1$ and $V_2$ are equal, but in anti-phase, which leads to a situation where $V_{DM}$ exists. Differential mode $V_{DM}$ and common mode $V_{CM}$ can be described as:

$$V_{DM} = V_1 - V_2$$
$$V_{CM} = \frac{V_1 + V_2}{2}$$

Since the two sides of the circuit are identical, only one side has to be analyzed. This half-circuit concept is used to analyze the differential amplifier and its noise contribution.
This can simplify noise calculation since the two sides of the amplifier are mirror images and the noise generators of both sides are equal. Values of the input signal $V_1$ and $V_2$ are shown in the table below:

<table>
<thead>
<tr>
<th>Values</th>
<th>$V_1$</th>
<th>$V_2$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Amplitude</td>
<td>1 mV</td>
<td>1 mV</td>
</tr>
<tr>
<td>Phase</td>
<td>0</td>
<td>180</td>
</tr>
<tr>
<td>Frequency</td>
<td>2.5GHz</td>
<td>2.5GHz</td>
</tr>
</tbody>
</table>

Table 3.2-1: Properties of the input signals

The differential amplifier used in this architecture has four stages, [Figure 3.2-1]. The input stage is the common emitter stage, while the second stage is the common base. Since the signal gain in the first stage has a major importance in reduction of equivalent input noise, the common emitter structure was used here. This configuration provides the greatest effect gain. Common base configuration is used in places where the low input impedance and high output impedance are desired. The combination of these stages to a CE-CB structure, [Figure 3.2-2], will minimize the high frequency feedback capacitance, [(13), on page 495-498].

To be able to increase the gain it is desired to reduce the base impedance or increase the load at the output of the common base stage. This is the reason why the next stage has a common collector configuration, [Figure 3.2-3]. Common collector structure is used where the high input impedance and the low output impedance are desired. High input impedance in the common collector configuration increases the gain of the second stage, since it increase the load of the second stage. The output stage of the LNA has a common emitter configuration, and the load of this stage is the input impedance of the next block which is the mixer.
3.2.1. **Resonant circuit**

As mentioned before a part of the LNA consists of a resonant circuit. The inductor and the variable capacitor are placed between the second (CB) and the third stage (CC). The inductance and the capacitance cancel each other at resonant frequency. Either the inductor or the capacitor is considered in the noise calculation because the noise contribution is interesting at the resonant frequency. Since the variable capacitor is made of a bipolar transistor, the amount of shot noise and the thermal noise of the base resistance could be included in the total noise contribution. Those noise sources are between the second and third stage and is almost negligible. Therefore it was not taken into the calculations.

To be able to tune the desired frequency at the output of the LNA, the varactor has to be used, as explained in part one. Since this is not a CMOS technology, the varactor was designed in a different way. The varactor was made by coupling the collector and the emitter together while the base was connected to the voltage source. Figure [3.2-4] shows the varactor. The capacitance between the base and the emitter/collector will vary as a function of the voltage source connected to the base. The principle is the same as explained in part one, but since this is a bipolar transistor there are a lot of different details, compared with CMOS, which will not be explained in this thesis.
3.2.2. **AC analysis and signal gain**

An AC analysis at the output of the LNA was performed and the purpose with this analysis is the same as described in the part one, [subchapter 2.1.2.3]. Changing the voltage of the voltage source connected to the varactor, results in a movement of the resonant frequency at the output of the LNA. After performing AC simulations, it is shown that the tunings range of the circuit designed in SiGe technology is greater than the tunings range of the circuit designed in BiCMOS. Tunings range of the LNA designed in SiGe technology is from 2.254 GHz to 2.509 GHz and from 2.239 GHz to 2.562 GHz for the circuit designed in BiCMOS technology. These results show that the tunings range of both circuits is much greater than the demanded range, which is between 2.5 GHz and 2.4 GHz. This indicates that the circuit will be able to compensate for inductor variation even when external inductors are used. In the layout design the parasitic capacitance of pads, where the inductors are connected to, will not affect the function of the circuit to a great extent. The table below and figure 3.2-5 shows the AC magnitude of the desired signal at the upper and lower limit of the demanded tunings range.

<table>
<thead>
<tr>
<th>Technology</th>
<th>Resonant frequency</th>
<th>V_varactor</th>
<th>L</th>
<th>Signal magnitude</th>
<th>Figure</th>
</tr>
</thead>
<tbody>
<tr>
<td>BiCMOS 0.8µm</td>
<td>2.5 GHz</td>
<td>2.1 V</td>
<td>15 nH</td>
<td>239 mV</td>
<td>3.2-5 b</td>
</tr>
<tr>
<td>BiCMOS 0.8µm</td>
<td>2.4 GHz</td>
<td>3.9 V</td>
<td>15 nH</td>
<td>1.02 V</td>
<td>3.2-5 a</td>
</tr>
<tr>
<td>SiGe</td>
<td>2.5 GHz</td>
<td>400 mV</td>
<td>20 nH</td>
<td>1.18 V</td>
<td>3.2-5 d</td>
</tr>
<tr>
<td>SiGe</td>
<td>2.4 GHz</td>
<td>2.99 V</td>
<td>20 nH</td>
<td>99.58 mV</td>
<td>3.2-5 c</td>
</tr>
</tbody>
</table>

*Table 3.2-2: Resonant frequency*
The LNA consists of four stages, and the desired signal is amplified in each stage. The gains provided by those stages are depended on stage configuration. As explained before, the common base transistor structure provides high voltage gain and the calculation results confirm this theory. The gain varies between those two technologies even when the configuration is the same. This is because of the technology parameters and different size of the components. The results shown in the table below are calculated when the circuit is tuned to 2.5 GHz at the output of the LNA. The table [3.2-3] shows gain, $K_t$, provided by each stage: The detailed calculations are shown in Appendix H-K.

<table>
<thead>
<tr>
<th>Stage</th>
<th>Configuration</th>
<th>BiCMOS 0.8µm $K_t$</th>
<th>SiGe $K_t$</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>CE</td>
<td>$1.76 \cdot 10^2$</td>
<td>$2.79 \cdot 10^2$</td>
</tr>
<tr>
<td>2</td>
<td>CB</td>
<td>10.60</td>
<td>19.00</td>
</tr>
<tr>
<td>3</td>
<td>CC</td>
<td>0.69</td>
<td>0.95</td>
</tr>
<tr>
<td>4</td>
<td>CE</td>
<td>48.6</td>
<td>1.75</td>
</tr>
</tbody>
</table>

Table 3.2-3: Gain of each stage

The voltage gain can be expressed as:

$$K_t = \frac{V_{out}}{V_{in}}$$  \[3.2.1\]
where $V_{out}$ is the voltage at the output and $V_{in}$ is the voltage at the input of a stage. In each transistor there are three possible voltage gains: common emitter, common base and common collector. For instance, the voltage gain of a common emitter stage of transistor $T_2$ is defined as $K_{1,CE,T_2}$. The term CE stands for common emitter, and the $T_2$ shows which transistor it yields. This method was used during the noise calculation. The table [3.2-3] shows the voltage gain of each stage. The gain calculation will be discussed in detail in the next chapter.
3.3. Component noise of the LNA

3.3.1. Hybrid-π model

The hybrid-π model is an equivalent circuit for a bipolar transistor, where it is possible to include noise sources which present the noise generated in a transistor. The model is used in this thesis for gain calculation and noise contribution of transistors. Advantages of this model are that it can be used over a wide frequency range and can present all three structures of a bipolar transistor: CB, CC and CE. The basic hybrid-π model consists of seven components and can be applied to both NPN and PNP type bipolar transistors, [(10), on page 110-113].

\[
E_{X}^{2} = 4kT r_{x}
\]  

[3.3.1]
On the other hand, resistors $r_o$ and $r_π$ are dynamical resistors and non-ohmic resistors, which mean that they do not generate noise. Both base and collector current generate shot noise. Shot noise increases when the base or collector current increases, [(10), on page 13].

$$I_{nbl}^2 = 2qI_B$$  \[3.3.2\]

$$I_{ncl}^2 = 2qI_C$$  \[3.3.3\]

The flicker noise is generated by a current flow

$$I_f^2 = \frac{2qf_l I_B^2}{f}$$  \[3.3.4\]

The amount of flicker noise will be small, especially when the high frequency design is considered in addition to bipolar technology. Another element which separates the high from the low frequency design is a calculation of the input impedance of the transistor. The capacitance between the base and the collector, $C_\mu$, is the high frequency feedback capacitance which should be taken into consideration. This is also called the Miller capacitance which can be included into the hybrid-\(\pi\) model as shown in figure [3.3-3].

![Figure 3.3-3: Hybrid-\(\pi\) model with the Miller capacitance](image)

The Miller capacitance can be expressed as the $C_\mu$ capacitance multiplied by the voltage gain, $g_m$, and the load of the transistor, $R_L$. Since the Miller capacitance as shown in figure [3.3-3] is parallel with the $C_π$ capacitance, the sum of those capacitances can be expressed as, [(13), on page 473]:

$$C_M = C_π + (1 + g_m R_L) C_\mu$$  \[3.3.5\]

The formula [3.3.5] shows that a reduction of the load at the output of the transistor leads to a reduction of the Miller effect. The impedance $Z_π$ is used instead of the resistance $r_π$ in expression for the input impedance. The impedance $Z_π$ consists of the parallel coupling of the capacitor $C_M$ and the resistor $r_π$ shown in the hybrid-\(\pi\) model.

$$Z_π = \frac{r_π}{(ωC_M r_π + 1)}$$  \[3.3.6\]
3.3.2. Noise calculation in the LNA

The LNA consists of different stages and to be able to calculate the equivalent input noise it is necessary to consider each stage separately. Afterwards, the entire LNA has to be considered as a system. The transistor parameters are calculated by Cadence and these results were used in noise calculations described in the following subchapters.

3.3.2.1. First stage of the LNA

The first stage in the LNA is a common emitter structure, and this structure has the capability to provide the high effect gain. The input signal, $V_{in}$, is applied on the base of the transistor $T2$ and the output, $V_o$, is on the collector. The model below includes both sensor resistance $R_s$ and bias resistor $R_7$.

![CE stage and its equivalent circuit](image)

The load of the first stage is defined as the output resistance of the $T2$ and the input resistance of $T3$, coupled in parallel. The voltage gain of the first stage can be divided into two parts, the gain in the transistor itself and the gain in front of the base. Since this is the differential amplifier, the AC magnitude at the output of the first stage can be calculated by the following formula, [(15), on page 232]:

\[
\text{Gain} = \frac{V_o}{V_{in}} = \frac{V_o}{V_{in}}
\]
The signal voltage at the output of the \( T_1 \) is found by the expression [3.3.7]. The \( V_e \) is not constant, but the \textit{rms} value is used in the expression above.

The gain of the first stage can be expressed as:

\[
K_{l\_CE\_T2} = \frac{V_o}{V_{in}} \tag{3.3.8}
\]

This is the gain from the base to the collector of the transistor \( T_2 \), and the calculated and simulated results are almost the same. The transistor \( T_2 \) will also amplify the shot noise generated on the collector of the transistor \( T_1 \). This gain can be considered as the voltage gain from the emitter to the collector of the \( T_2 \). Therefore it can be expressed as, [(13), on page 420]:

\[
K_{l\_CB\_T2} = -\frac{R_{L\_T2}}{R_{l\_CB\_T2}} \frac{\beta_{T2}}{1 + \left( \frac{\beta_{T2} R_{L\_T2}}{R_{C\_T2}} \right)} \tag{3.3.9}
\]

Where the input resistance for CB configuration of the \( T_2 \) is:

\[
R_{l\_CB\_T2} = \frac{r_{s\_T2} + Z_{\pi\_T2}}{\left( \beta_{T2} \frac{R_{L\_T2}}{R_{C\_T2}} \right) + 1} \tag{3.3.10}
\]

Since the output noise is considered as the noise voltage, the shot noise current generated by the collector is converted to the shot noise voltage by the formula given below, [(10), on page 116]:

\[
E_{nc}^2 = \frac{2qI_C}{g_m} \tag{3.3.11}
\]

In order to calculate the \( E_{n\_{T2}}^2 \), the sensor resistance has to be equal to zero. This means that the sensor does not contribute noise, and the noise at the output will be a result of noise contributed by components of the first stage. If the sensor resistance in the expression [3.3.14] approaches infinity the result will be term \( I_{n\_{T2}}^2 \), which is part of the \( E_n-I_n \) model. Both \( E_{n\_{T2}}^2 \) and \( I_{n\_{T2}}^2 \) terms are used in noise calculation for the entire system. Therefore the expressions for \( E_{n\_{T2}}^2 \) and \( I_{n\_{T2}}^2 \) can be written as:
\[ E_{no,T2}^2 = E_{nc,T2}^2 + \left( E_{X,T2}^2 + \left( I_{nb,T2}^2 + I_{f,T2}^2 \right) f_{X,T2}^2 \right) K_{i,CE,T2}^2 + E_{nc,T1}^2 K_{i,CB,T2}^2 \]  

\[ I_{n,T2}^2 = \frac{I_{nc,T2}^2}{K_{i,CE,T2}^2} + I_{nb,T2}^2 + I_{f,T2}^2 \]

Figure 3.3-5: Transistor noise model of the input stage

The noise generated at the base of the \( T2 \) is amplified by the base-collector voltage gain, while the noise generated by the transistor \( T1 \) is amplified by the emitter-collector voltage gain of the \( T2 \). Total noise voltage at the base of the \( T2 \), including the thermal noise contributed by the sensor resistance and the bias resistor \( R_7 \), is written as:

\[ E_{i,T2}^2 = \frac{E_{no,T2}^2}{K_{i,CE,T2}^2} + E_{S}^2 \left( \frac{R_7}{R_5 + R_7} \right)^2 + \left( I_{R7}^2 + I_{i,T2}^2 \right) \left( R_7 \parallel R_5 \right)^2 \]  

\[ [3.3.14] \]

Therefore the total noise voltage at the output of the first stage is given by:

\[ E_{no,T2}^2 = E_{i,T2}^2 K_{i,CE,T2}^2 \]  

\[ [3.3.15] \]

Minimizing the load \( R_{LT2} \) will reduce the feedback capacitance \( C_M \). This trend reduces the noise feedback to the base of \( T2 \). On the other hand, the reduction of the \( R_{LT2} \) reduces the gain of the first stage, which leads to increased equivalent input noise. In this case the equivalent input noise will be more reduced by increasing the gain then by reducing the Miller capacitance.
Detailed calculations are shown in Appendix H. Calculated noise values of the first stage are shown in the table below:

<table>
<thead>
<tr>
<th>Calculated noise values of first stage</th>
<th>BiCMOS 0.8 µm</th>
<th>SiGe</th>
</tr>
</thead>
<tbody>
<tr>
<td>( E_{no}^2 )</td>
<td>( 8.94 \cdot 10^{-14} )</td>
<td>( 1.01 \cdot 10^{-13} )</td>
</tr>
<tr>
<td>( I_n^2 )</td>
<td>( 3.77 \cdot 10^{-24} )</td>
<td>( 1.21 \cdot 10^{-24} )</td>
</tr>
<tr>
<td>( E_{ni}^2 )</td>
<td>( 3.63 \cdot 10^{-18} )</td>
<td>( 2.11 \cdot 10^{-18} )</td>
</tr>
<tr>
<td>( E_{no}^2 )</td>
<td>( 1.12 \cdot 10^{-13} )</td>
<td>( 1.64 \cdot 10^{-13} )</td>
</tr>
</tbody>
</table>

Table 3.3-1: Calculated noise values

### 3.3.2.1.1. Noise countermeasure

In most cases, when the component noise is considered, it is a trade off between the noise reduction and the circuit’s functionality. In this chapter the functionality is not considered when the noise reduction is discussed. It is suggested which of the components has to be increased/decreased in order to reduce the noise. The limiting noise of the first stage is the thermal noise voltage of the base resistance \( r_x \). This is the most dominant noise source. Other sources which are also important to minimize is the sensors thermal noise and the shot noise caused by the collector current. In order to reduce the noise in the first stage the following things has to be done:

1. **Reduce \( r_x \)**
   Increasing the transistor size (device area) leads to reduced base resistance. This reduction will:
   - reduce the thermal noise generated by the base resistance \( r_x \)
   - reduce the input impedance \( R_{i,CE,T2} \) ⇒ increased signal gain \( K_{t,CE,T2} \) ⇒ reduced equivalent input noise
   - reduce the gain \( K_{t,CE,T2} \) ⇒ lower amplification of the shot noise generated by the \( T1 \)

2. **Increase \( R_c \) of \( T2 \)**
   This is the input resistance of the next stage, and increasing it can affect the noise contribution in the next stage. Increased \( R_c \) will:
   - Increase the gain \( K_{t,CE,T2} \) ⇒ reduced equivalent input noise

3. **Increase \( g_m \)**
   It leads to:
   - Increased gain \( K_{t,CE,T2} \) ⇒ decreased equivalent input noise
This contributes to the increased shot noise of the collector of $T2$. The shot noise can be reduced by minimizing the $Ic$ current. The term $g_m$ can be expressed as:

$$g_m = \frac{qI_c}{kT}$$

In order to increase the $g_m$, the $Ic$ has to be increased as well, which leads to increased shot noise of the collector of the $T1$. The increased $g_m$ increase the common base voltage gain, which amplify the shot noise generated on the collector of the $T1$. Those trade offs has to be taken into consideration.

The calculated noise values are shown in the table above. Those values do not vary from the simulated values. The signal gain of the first stage is almost the same as simulated results shows. Calculation results show that the dominant noise source is the noise generated by the base resistance of $T1$. It is obvious, since the desired signal goes thought this resistance. The simulation and calculation results of the first stage are almost the same.
3.3.2.2. Second stage of the LNA

The second stage consists of the transistor with a common base structure. The typical characteristic for this kind of transistor structure is low input and high output impedance. The signal path is from emitter to collector and this CB structure also provides a high voltage gain. The figure [3.3-6] shows the second stage and its equivalent circuit.

![CB stage and its equivalent circuit](image)

The resistor \( R_6 \) is a bias resistor and generates thermal noise, which is serial, coupled with a noise generated by base resistor, \( r_x \). The output load of this stage is a parallel coupling of the non-ohmic resistor, \( r_o \), and the input resistance of the next stage, \( R_{in,T4} \). The resistance \( r_o \) can also be expressed as the term \( R_c \) which is used in the formulas below. The resonant part of the circuit consists of an inductor and a varactor. This circuit is between the second and third stage, and therefore it should be included as the outputs load of the second stage. Component values and the noise contribution are calculated at the resonant frequency. Since inductance of \( L \) and capacitance of the varactor cancel each other at the desired frequency, it is not necessary to take them into consideration. The rest of the components in the equivalent circuit of the CB stage are the same as explained in the previous subchapter. The noise contribution at the base of the \( T3 \) is amplified by the base-collector voltage gain. The output noise voltage of the previous stage is amplified by the emitter-collector voltage gain of the \( T3 \). To be able to calculate this gain, both the common base and the common emitter input resistance of the \( T3 \) has to be taken into consideration. An input resistance of the \( T3 \) is given by the following expressions [(13), on page 420]:

\[
R_{i,\text{CB}_T3} = \frac{R_6 + r_{s,T3} + Z_{\pi,T3}}{\left(\frac{R_k_{T3}}{\beta_{T3}}\right) + 1 + \frac{1}{R_{C,T3}}} \tag{3.3.16}
\]

\[
R_{i,\text{CE}_T3} = R_6 + r_{s,T3} + Z_{\pi,T3} \tag{3.3.17}
\]

The voltage gain of the CB and CE configurations of the transistor \( T3 \) is expressed as:
\[ K_{t_{-CB_{-T3}}} = \frac{-R_{L_{-T3}}}{R_{i_{-CB_{-T3}}}} \frac{\beta_{T3}}{1 + \left( \frac{\beta_{T3} R_{L_{-T3}}}{R_{C_{-T3}}} \right)} \]  
[3.3.18]

\[ K_{t_{-CE_{-T3}}} = \frac{-\beta_{T3} R_{L_{-T3}}}{R_{6} + r_{x_{-T3}} + Z_{x_{-T3}}} \]  
[3.3.19]

Since this is a second stage in a LNA, there is no sensor resistance at this stage. This may be confusing if it is desired to calculate \( E_{n} \) and \( I_{n} \). The equivalent input noise of the CB stage is equal to the noise generated by the second stage itself, in addition to the output noise of the first stage. When the sensor resistance is zero, the thermal noise of the sensor resistance \( E_{s} \) is zero and the noise current term \( I_{n}R_{s} \) is also zero. This is because it was chosen to calculate the output noise voltage and not an output noise current. The shot noise at the output is expressed as the voltage. Therefore, the total equivalent input noise is the noise voltage \( E_{n} \). Usually \( E_{n} \) can be calculated by the formula [3.3.20] when the \( R_{s} \) is included in the expression for \( E_{no} \).

\[ E_{n}^{2} = \lim_{R_{s} \to 0} \frac{E_{no}^{2}}{K_{t}^{2}} \]  
[3.3.20]

In this case, there is no \( R_{s} \) in expression for \( E_{no} \) and therefore the \( E_{n} \) is equal to \( E_{ni} \). The noise voltage contributed by the transistor \( T3 \) where the thermal noise generated by the bias resistor \( R_{6} \) is included is written as:

\[ E_{no_{-T3}}^{2} = E_{nc_{-T3}}^{2} + \left( E_{X_{-T3}}^{2} + E_{R6}^{2} + \left( I_{na_{-T3}}^{2} + I_{i_{-T3}}^{2} \right) \left( r_{X} + R_{6} \right)^{2} \right) K_{t_{-CE_{-T3}}}^{2} \]  
[3.3.21]

To calculate the noise current \( I_{n} \), \( E_{ni} \) has to be recalculated with a very large sensor resistance \( R_{s} \). This is expressed in formula [3.3.22]

\[ I_{n}^{2} = \lim_{R_{s} \to \infty} \frac{E_{no}^{2}}{K_{t}^{2}} \]  
[3.3.22]

According to the \( E_{n} \)-\( I_{n} \) model the expression for equivalent input noise is: \( E_{ni}^{2} = E_{S}^{2} + E_{n}^{2} + I_{n}^{2} R_{S}^{2} \). Referring to the formula [3.3.22] and for instance assuming that the \( R_{s} \) is not zero, the term \( I_{n}R_{s} \) will be dominant in an expression for equivalent input noise. This means that the expression \( E_{ni}^{2} = E_{S}^{2} + E_{n}^{2} + I_{n}^{2} R_{S}^{2} \) can be simplified to \( E_{ni}^{2} = I_{n}^{2} R_{S}^{2} \). In other words \( I_{n} \) can be expressed as equivalent input noise divided by sensor resistance:

\[ I_{n}^{2} = \frac{E_{ni}^{2}}{R_{S}^{2}} \]  
[3.3.23]
If $R_s$ is large enough, the $I_n R_s$ term dominates the $E_n$ term, and it also dominates the thermal noise voltage generated by the sensor $E_s$. This is because the thermal noise voltage $E_s$ increases as the square root of the resistance, whereas the $I_n R_s$ term increases linearly with resistance. Since the $I_n$ is expressed as equivalent input noise divided by sensor resistance, and in this case the sensor resistance is zero since there is no sensor, the $I_n$ is also equal to zero. Therefore, in this case the $I_n$ term is only calculated in the first stage and not in the following stages of the LNA.

In addition to the noise contributed by the $T3$ the noise from the previous stage has to be included when calculating the total noise contribution at the output of the second stage. The expression for this is given below:

$$E_{no,T2}^2 = E_{no,T3}^2 + E_{o,T2}^2 K_{T3}^2$$  \[3.3.24\]

The noise contribution of the second stage, $E_{n,T3}^2$, has to be divided by the emitter-collector gain (CB-gain) when the equivalent input noise of the entire LNA is considered. This is shown in subchapter 3.3.3. Detailed calculations are shown in Appendix I. Calculated noise values of the second stage are shown in the table below.

<table>
<thead>
<tr>
<th>Calculated noise values of second stage</th>
<th>BiCMOS 0.8 µm</th>
<th>SiGe</th>
</tr>
</thead>
<tbody>
<tr>
<td>$E_{no,T3}^2$</td>
<td>$3.20 \cdot 10^{-14}$</td>
<td>$3.18 \cdot 10^{-13}$</td>
</tr>
<tr>
<td>$E_{no,T2}^2$</td>
<td>$1.26 \cdot 10^{-11}$</td>
<td>$5.94 \cdot 10^{-11}$</td>
</tr>
</tbody>
</table>
3.3.2.2.1. Noise countermeasure

The following noise contra measure can be done in this stage:

1. Decreased R₆
   
   This will:
   
   • reduce the thermal noise generated by the $R₆$ ⇒ reduce the noise $E_n'$ of the $T₂$
   • increase the $R_{l_{CE}T₂}$ ⇒ decrease the $K_{l_{CE}T₂}$ ⇒ minimize the amplification of the noise generated on the base of $T₂$
   • reduced $R_{l_{CB}T₃}$ ⇒ increased $K_{l_{CB}T₃}$ ⇒ reduce $E_n$ of the $T₂$ ⇒ minimized NF of the entire LNA

   Since $R₆$ is serial coupled with base resistance, $rₓ$, reducing the $rₓ$ will affect the noise reduction in the same way as when reducing the $R₆$. Reducing the $R₆$ will affect the circuit’s functionality as well.

2. Reduced the Ic
   
   This will:
   
   • reduce the shot noise of the $T₂$
   • reduce the $g_m$ ⇒ reduce the gain.

   The consequences of reducing the $Ic$ has also to be considered since this also reduce the signal gain of this stage.

   The variation between the noise simulation and the calculation results of entire LNA is great, and this is because of the gain in the second stage. The variation of calculated and simulated noise results of the entire LNA are affected to a great extent of the gain difference in the second stage. Since the documentation of the simulator was not available it was difficult to explain this great variation. The noise contribution of the second stage is as expected.
3.3.2.3. Third stage of the LNA

The third stage of the LNA contains a transistor which has a common collector structure. The signal path is from the base to the emitter. Common collector structure is used where the high input impedance and the low output impedance are desired. In this case high input impedance increases the load at the output of the previous stage, which again increases the gain of the previous stage. The input of the third stage is a resonant part of the LNA, which consists of an inductor and a varactor, [Figure 3.3-8].

At resonant frequency the inductance $L$ and capacitance $C_{var}$ can be excluded in the calculation of output load of the second stage, since $\omega^2 C_{var} L = 1$. This means that inductance $L$ and capacitance $C_{var}$ cancel each other. The noise source, which could be included at the input of the third stage, is the thermal noise generated by the base resistance of the varactor. This noise can be transferred through the base collector/emitter capacitance to the signal path. Since this noise source will affect the equivalent input noise at the input of the LNA to a very small degree, it is not taken into consideration.

The input resistance of this stage can be expressed as [(13), on page 420]:

$$R_{i_{CC-T4}} = r_x + Z_{\pi-T4} + R_{L-T4} \left( 1 + \beta_T \right)$$

[3.3.25]

The voltage gain of this stage $K_{t-CC-T4}$ is given by:
The output load of this stage consists of input resistance of the next stage \( R_{l,T5} \), parallel coupled with resistor \( R_{12} \) shown in figure [3.3-10]

\[
R_{l,T4} = r_{o,T4} \parallel R_{E,T4} \Rightarrow r_{o,T4} \parallel R_{12} \parallel R_{l,T5}
\]  

[3.3.27]

The bias resistor \( R_{12} \) at the output of the third stage generates a noise current equal to \( \sqrt{\frac{4kT}{R_{12}}} \). Since this noise source is at the output of the CC stage, it is not multiplied by the gain of this stage.

\[
E_{no,T4}^2 = I_{R12}^2 \left( r_{o,T4} \parallel R_{12} \right) + E_{nc,T4}^2 + \left( E_{X,T4}^2 + \left( I_{nb,T4}^2 + I_{f,T4}^2 \right) r_{o,T4}^2 \right) K_{l,CC,T4}^2
\]  

[3.3.28]

The \( I_n \) term does not exist here either, and the reason is augmented in the pervious subchapter. The total noise contribution at the output of this stage is expressed as:

\[
E_{no,T4}^2 = E_{no,T4}^2 + E_{no,T3}^2 K_{l,CC,T4}^2
\]  

[3.3.29]

The terms used in this formula are shown in figure [3.3-10]
Calculated noise values of the third stage are shown in the table below. Detailed calculations are shown in Appendix J.

<table>
<thead>
<tr>
<th>Calculated noise values of third stage</th>
<th>BiCMOS 0.8 µm</th>
<th>SiGe</th>
</tr>
</thead>
<tbody>
<tr>
<td>$E_{no}^2$</td>
<td>$9.77 \cdot 10^{-17}$</td>
<td>$1.49 \cdot 10^{-17}$</td>
</tr>
<tr>
<td>$E_{no}^2$</td>
<td>$5.99 \cdot 10^{-12}$</td>
<td>$5.36 \cdot 10^{-11}$</td>
</tr>
</tbody>
</table>

Table 3.3-3: Calculated noise values

### 3.3.2.3.1. Noise countermeasure

Noise reduction in this stage can be done by:

1. **Reducing $r_x$**
   
   This will
   
   - reduce the thermal noise generated by the base resistance ⇒ reduce $E_n$ of the third stage

2. **Increasing $R_{12}$**
   
   - reduce $E_n$ of the third stage ⇒ reduce NF of entire LNA

3. **Reducing $I_C$**
   
   - reduce the shot noise ⇒ reduce the $E_n$ of the third stage

The gain of the CC stage is typical around 1, and changing the values mentioned above ($r_x$, $R_{12}$) will not affect gain in this stage in a large degree.

The calculated noise values are as expected in this stage, too. There is a small variation between the gain calculation and simulation.
3.3.2.4. Fourth stage of the LNA

The fourth stage of the LNA is, like the first stage, a common emitter configuration. The advantage of CE configuration is the capability of providing a high effect gain. In this case, the feeding of the desired signal in this stage, gives the higher amplitude of the IF signal at the output of the mixer. Therefore the voltage gain of this stage is lower than 1.

The figure [3.3-11] shows the fourth stage of the LNA, and the part of the mixer, which is connected to the output of the LNA. The part of the mixer architecture is considered in this subchapter because the mixer is the output load of the LNA. The LNA has two outputs which in figure [3.3-11] are called $V_{out_1}$ and $V_{out_2}$. LNA is a differential and input signals have almost the same properties except that they are in anti phase. Anyway, the noise is equal for both signals because of the symmetry of the LNA. After the output signals of the LNA are mixed with $LO$ signals of the mixer, the output signals of the mixer are called $V_{out_3}$ and $V_{out_4}$.

The desired signal and the noise at the base of the $T5$ are amplified by the CE gain, and the noise at the emitter of the $T5$ is amplified by the CB gain of the $T5$. Therefore both
the CE and the CB input resistance has to be considered. They are expressed as [(13), on page 420]:

\[
R_{i,CE,T5} = r_x + Z_\pi + \frac{R_{E,T5}(r_0 + R_C)}{r_0 + R_C + R_E} \tag{3.3.30}
\]

\[
R_{i,CB,T5} = \frac{r_x + Z_\pi + \frac{R_L}{R_C}}{(\beta T5 R_L R_C)} + 1 \tag{3.3.31}
\]

The emitter resistance, \(R_E\), of the transistor \(T5\), is the dynamic resistor of the transistor \(T6\). This resistor is non-ohmic and does not generate noise. The shot noise voltage at the collector of the \(T6\) is marked as the noise source in the figure [3.3-12]. This noise is amplified by the CB-gain of the \(T5\).

The collector resistance, \(R_C\), of the transistor \(T5\) is the resistor \(R_4\) parallel coupled with an input resistance of the mixer, \(R_{in \_ mix}\). Since the output signal, \(V_{out \_ 1}\), enters the base of the transistors \(T7\) and \(T8\), the input resistance of the mixer is a parallel combination of the base resistances of \(T7\) and \(T8\). \(R_c\) and \(R_E\) can therefore be written as:

\[
R_C = R_4 || R_{i,T7} || R_{i,T8} \tag{3.3.32}
\]

\[
R_E = r_o + R_{T6} \tag{3.3.33}
\]

The voltage gain seen both from the base (CE-gain) and emitter (CB-gain) of the \(T5\) is expressed as [(13), on page 420]:

\[
K_{i,CE,T5} = \frac{\beta T5 R_L}{r_x + Z_\pi} \tag{3.3.34}
\]

\[
K_{i,CB,T5} = \frac{-R_L}{R_{i,CB,T5}} + \frac{\beta T5}{\left(\frac{\beta T5 R_L R_C}{R_C} \right)} \tag{3.3.35}
\]

The output load of this stage is:

\[
R_{L,T5} = r_o || R_4 || R_{i,CE,T7} || R_{i,CE,T8} \tag{3.3.36}
\]

The simplified input impedance of both transistors \(T7\) and \(T8\) can be written as:

\[
R_{i,T7/T8} = Z_\pi + r_x \tag{3.3.37}
\]

The fourth stage noise contribution is given by:
\[ E_{no,T5}^2 = I_{R4}^2 \left( R_4 \parallel r_{o,T5} \right) + E_{nc,T5}^2 + \left( E_{X,T5}^2 + \left( I_{nb,T5}^2 + I_{f,T5}^2 \right) r_{X,T5}^2 \right) K_{i,CE,T5}^2 + E_{nc,T6}^2 K_{i,CB,T5}^2 \]

The output noise current of the fourth stage is:

\[ E_{no,T5}^2 = E_{no,T5}^2 + E_{no,T4}^2 K_{i,CE,T5}^2 \]  

[3.3.38]

[3.3.39]

Calculated noise values of the fourth stage are shown in the table below and the detailed calculations are shown in Appendix K.

<table>
<thead>
<tr>
<th>Calculated noise values of fourth stage</th>
<th>BiCMOS 0.8 μm</th>
<th>SiGe</th>
</tr>
</thead>
<tbody>
<tr>
<td>( E_{no}^2 )</td>
<td>1.32 \cdot 10^{-13}</td>
<td>3.76 \cdot 10^{-18}</td>
</tr>
<tr>
<td>( E_{no}^2 )</td>
<td>1.41 \cdot 10^{-8}</td>
<td>1.63 \cdot 10^{-10}</td>
</tr>
</tbody>
</table>

Table 3.3-4: Calculated noise values

### 3.3.2.4.1. Noise countermeasure

This stage has a CE configuration, the same configuration as the first stage. Therefore almost the same arguments for noise reduction can be used

1. **Reducing \( r_x \)**
   This will:
   - reduce thermal noise generated by the base resistance
   - reduce input impedance \( \Rightarrow \) increase gain \( K_{i,CE,T5} \) \( \Rightarrow \) reduce \( E_n \) of the \( T5 \)
   - reduce gain \( K_{i,CB,T5} \) \( \Rightarrow \) reduce shot noise contribution of the transistor \( T6 \)

2. **Increasing \( R_c \)**
   This will:
   - increase gain \( K_{i,CE,T5} \) \( \Rightarrow \) reduce \( E_n \) of the \( T5 \)

3. **Increasing \( R_{12} \)**
   This will:
   - increase gain \( K_{i,CE,T5} \) \( \Rightarrow \) reduce \( E_n \) of the \( T5 \)

The variation between the gain simulation and calculation is present in this stage, as well. This variation is not great, and will almost not affect the equivalent input noise of the LNA. At the output of this stage it is possible that the simulator adds some noise from the mixer, but since this is a fourth stage of the LNA, the noise from the mixer will affect the equivalent input noise in a small degree.
3.3.3. Noise in entire LNA

Since the noise contribution is calculated for each stage, the noise of the entire LNA is simply calculated by \( E_n \) and \( I_n \) of the first stage and \( E'_n \) of the following stages, as shown in figure [3.3-13]. The sensor resistance is not shown in this model since this is included in the noise contribution of the first stage.

![Figure 3.3-13: \( E_n-I_n \) model for entire LNA](image)

From the expression of equivalent input noise for the entire LNA [3.3.40], it is clearly shown that the noise in the first stage is dominant. The noise of the following stages is divided by the gain of the first stage, and this explains the importance of increased gain, especially in the first stage, [based on (10), page 231].

\[
E_{ni}^2 = \frac{E_{no-T2}^2}{K_{t-T2}^2} + \frac{E_{no-T3}^2}{K_{t-T2}^2 K_{t-T3}^2} + \frac{E_{no-T4}^2}{K_{t-T2}^2 K_{t-T3}^2 K_{t-T4}^2} + \frac{E_{no-T5}^2}{K_{t-T2}^2 K_{t-T3}^2 K_{t-T4}^2 K_{t-T5}^2} \quad [3.3.40]
\]

The noise figure is calculated by the following formula:

\[
NF = 10 \log \frac{E_{ni}^2}{E_S^2} \quad [3.3.41]
\]

Detailed calculations of the values given in table below are shown in Appendix L.

<table>
<thead>
<tr>
<th>Calculated values of ( E_{ni} ) and ( NF )</th>
</tr>
</thead>
<tbody>
<tr>
<td>BiCMOS 0.8 µm</td>
</tr>
<tr>
<td>----------------</td>
</tr>
<tr>
<td>( E_{ni}^2 )</td>
</tr>
<tr>
<td>( V^2 )</td>
</tr>
<tr>
<td>NF</td>
</tr>
<tr>
<td>dB</td>
</tr>
</tbody>
</table>

Table 3.3-5: Calculated values of \( E_{ni} \) and \( NF \)

As the results show, the noise contributed by the first stage is dominant. In order to minimize the NF of the entire system, it is important to minimize the noise contribution of the first stage.
3.3.3.1. Noise simulations

The noise simulations were performed for the entire LNA. Noise at the output of the LNA, and the NF of entire LNA are shown in the figures below.

![Figure 3.3-14: Noise at the output of the LNA](image)

Figure 3.3-14: Noise at the output of the LNA
Figure 3.3-15: The noise figure

a) BiCMOS:

b) SiGe
As explained before there are variation between calculated and plotted noise results. The main reason is the great difference between the calculated and simulated results of the gain in the second stage. This variation causes the great difference between the calculated and simulated NF results. The table below shows the calculated and simulated results:

<table>
<thead>
<tr>
<th></th>
<th>Calculated values</th>
<th>Simulated values</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>BiCMOS 0.8 µm</td>
<td>SiGe</td>
</tr>
<tr>
<td>$E_{no}^2$</td>
<td>$1.41 \cdot 10^{-8}$</td>
<td>$1.63 \cdot 10^{-10}$</td>
</tr>
<tr>
<td>$E_{mi}^2$</td>
<td>$3.64 \cdot 10^{-18}$</td>
<td>$2.12 \cdot 10^{-18}$</td>
</tr>
<tr>
<td>NF</td>
<td>6.43</td>
<td>4.08</td>
</tr>
</tbody>
</table>

Table 3.3-6: Calculated and simulated noise values of entire LNA
3.4. Mixer - bipolar technology

The mixer architecture is also the same for both technologies. This mixer is a differential mixer with two inputs and two outputs. The principle of the mixer is almost the same as described in Chapter 2.2. Fourier transform performed at the output shows the magnitude of the IF, RF and LO signals. This analysis compared with the analysis in part one; it shows that bipolar technologies contribute much less flicker noise than CMOS.

Some of the noise contributed by the mixer is taken into the consideration of the equivalent input noise of the LNA. That is thermal noise generated by the base resistors of $T7$ and $T8$ in parallel with the bias resistor, $R_{14}$. These components are part of the output load of the LNA. Since noise contributed by the mixer is divided by the gain product of all four stages, it will affect the equivalent input noise of the LNA to a very small degree. The noise contributed by the mixer is important for the output signal. The contribution of the flicker noise is very small in both technologies, and therefore this type of noise is not considered here. This is an important advantage, when the filtering of the IF signals is performed.
The Fourier transform at the output of the mixer is performed in both circuits. It shows that the circuit designed in BiCMOS contribute more noise around the IF signal than the circuit designed in SiGe technology. The magnitude of the desired signal, IF, is higher in the SiGe technology. There are also much less undesired signals around the IF signal, which simplified the signal processing in the next stage. Analyzing the AC simulation of these two technologies when the circuits are tuned to 2.5 GHz, shows that the gain at the output of the LNA is much higher in the SiGe technology. The band-pass filter characteristic at the output of the LNA is better in the circuit made of SiGe technology. It means that suppression of noise and other undesired signals around the RF is better. As small as possible amount of noise and undesired signals at the input of the mixer, results
in better down conversions. This again leads to a lower demand of the filter which is part of the next stage.

### 3.5. Conclusion-second part

In the second part of this thesis a differential LNA and mixer were analyzed. In the second part also all transistors are bipolar. The circuit was designed in two different technologies, SiGe and BiCMOS. Similarly with the part one the noise was calculated manually and by use of the noise models included in the design tool Cadence. The difference is that in this part only the component noise was considered. The results were compared and this can be a useful factor when considering the noise as the function of the technology.

Excluding the noise generated by the sensor, the noise contributed by the input transistor is dominant. This is the thermal noise of the base resistance and the shot noise at the collector of the input transistor. According to the calculation results the circuit designed in SiGe technology has a lower noise figure, NF, than the circuit designed in BiCMOS. The circuit designed in the SiGe has also a lower noise contribution in each stage compared with the circuit designed in BiCMOS. In order to reduce the noise even more, the calculation results show that the base resistance and the collector current has to be minimized. The trade off is that the current trough the transistor will be affected. This can change the functionality of the circuit. Thermal noise of the base and the shot noise generated on the collector of each transistor dominates the noise contribution by each stage. Another option is to increase the gain of the each stage if possible. Anyway, the circuit designed in SiGe has a better noise performance.

The magnitude of the desired signal, \( IF \), is higher in SiGe than in BiCMOS technology and there are much less undesired signals around the \( IF \) signal, [Figure 3.4-2]. This simplifies the signal processing in the next stage. When comparing the given results with a single ended bipolar amplifier, the variation of the calculated noise figure is not great.

<table>
<thead>
<tr>
<th>Noise figure</th>
<th>Calculated: 6.48 dB</th>
<th>Simulated: 8.53 dB</th>
<th>Reference [16]: 5 dB</th>
</tr>
</thead>
</table>

There is a variation between the simulation and calculation results. This is difficult to explain, especially when the documentation of the simulator is not available. The accuracy of the simulator may be lowered, if the circuit consists of many components. This is because the simulator does not take into consideration all noise caused by the correlation. This is also one of the reasons why there is a variation between the simulated and calculated results. However, the procedure and method of noise calculation used in part two can be applied on most of the circuits designed in BiCMOS and SiGe technologies.
Conclusion & References
4. Conclusion

As mentioned before, the noise added by a circuit in some cases depends more on the circuit’s architecture and functionality than on the technology. When comparing the results of the single ended and differential LNA, one finds that the differential LNA has a lower equivalent input noise. This is because the differential LNA in this case provides much higher gain than the single ended LNA. Considering the situation where these two architectures provide the same gain, the singe-ended architecture will have a lower equivalent input noise. This is because the noise generated by the input transistor of the opposite input signal will increase the total noise of the first stage.

At low frequencies the amount of flicker noise will increase. The thermal and shot noise will not be directly affected by lowering the signal frequencies. Indirectly the amount of thermal and shot noise will be reduced since the noise contribution caused by the correlation will decrease. This applies only when the correlated noise is not in anti-phase. At low frequencies the layout noise contribution will be reduced in a much higher degree than the component noise. Considering the noise as a function of the technologies used in this thesis, the SiGe technology will be preferred. Noise is perhaps one of the major advantages of SiGe over CMOS for RF design. The flicker noise due to carrier trapping-detrapping at interface states and thermal noise due to gate and channel resistances are both significantly higher in CMOS than in SiGe. Considering the noise generated by the CMOS and BiCMOS technology the CMOS will be preferred. The shot noise at the collector and the thermal noise of the base resistance generated by a BiCMOS transistor are higher than the noise generated by a CMOS transistor.

According to the noise calculation results, the noise can be reduced even more by choosing the more expensive technology. As explained before, the SiGe contributes less noise than the BiCMOS technology. Reducing the channel length of a CMOS transistor will result in reduced channel resistance. This will lead to minimized thermal noise generated in the channel. Reduced channel length increases the flicker noise contribution at low frequencies. This trade off can be taken into consideration at low frequencies.

The final results of this thesis will be a useful guidance when considering the noise countermeasure of similar architectures. Studying the details concerning noise, calculations clearly shows which noise sources dominate in affecting the noise figure of the entire system. Increased signal gain of the input stage is the most important factor when reducing the equivalent input noise. It applies to all systems independent of the choice of technology. The methods and the procedures shown in this thesis will also be a useful guidance when considering the noise contribution of any circuit designed in the given technologies. However, noise reductions techniques require that the various factors and many trade offs have to be carefully considered.
5. References


[5] Li Li, Jianhua Guo and Hannu Tenhunen, "State Equation Approach For Analysis of Noise in CMOS Downconversion Balanced Mixer" Royal Institute of Technology, Sweden


[8] Austria Mikro Systeme International AG "LV ESD Design Rules" Revision A


RF-amplifier AD8353
APPENDIX
Appendix A

Detailed calculation of the resonant frequency (CMOS technology)

The final formula is shown in subchapter 2.1.1.3. The method is shown below:

\[
\frac{1}{C_{sum}\omega_0} = \frac{1}{C_{var,1}\omega_0} + L_2\omega_0 \\
\frac{1}{C_{sum}\omega_0} - \frac{1}{C_{var,1}\omega_0} = L_2\omega_0 = 0
\]

\[
1 = \frac{C_{sum}}{C_{var,1}} + L_2\omega_0^2C_{sum}
\]

\[
L_2\omega_0^2C_{sum}C_{var,1} = -C_{sum} + C_{var,1}
\]

\[
\omega_0^2 = \frac{C_{var,1} - C_{sum}}{L_2C_{sum}C_{var,1}}
\]

\[
\omega_0 = \sqrt{\frac{C_{var,1} - C_{sum}}{L_2C_{sum}C_{var,1}}}
\]
Appendix B

Explanation: gain expressed in dB

The gain of the LNA expressed in dB when the input and output impedance are taken into consideration.

Detailed explanation:

\[
Bell = \log \frac{P}{P_r} \Rightarrow dB = 10 \log \frac{P}{P_r}
\]

\[
P = \frac{V^2}{R}
\]

\[
dB = 10 \log \frac{R}{V_r^2} = 10 \log \left( \frac{V^2}{R} \right) = 10 \log \left( \frac{V}{V_r} \right)^2 + 10 \log \frac{R}{V_r} = 20 \log \frac{V}{V_r} + 10 \log \frac{R}{R_r}
\]

In this case:

\(R_r\) = input impedance of the LNA
\(R\) = output impedance of the LNA
\(V\) = voltage of the output signal
\(V_r\) = voltage of the input signal
Appendix C

Noise contributed by the transistors in the LNA (CMOS technology)

Simulated values:

<table>
<thead>
<tr>
<th></th>
<th>M1</th>
<th>M2</th>
<th>M3</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>W</td>
<td>24.45</td>
<td>18.20</td>
<td>12.5</td>
<td>µm</td>
</tr>
<tr>
<td>L</td>
<td>0.60</td>
<td>0.60</td>
<td>0.60</td>
<td>µm</td>
</tr>
<tr>
<td>Vgs</td>
<td>1.29</td>
<td>1.67</td>
<td>1.84</td>
<td>V</td>
</tr>
<tr>
<td>Vds</td>
<td>2.02</td>
<td>1.13</td>
<td>1.84</td>
<td>V</td>
</tr>
<tr>
<td>gm</td>
<td>310.44 × 10^{-3}</td>
<td>2.00 × 10^{-3}</td>
<td>1.63 × 10^{-3}</td>
<td>A/V</td>
</tr>
<tr>
<td>gds</td>
<td>510.95 × 10^{-5}</td>
<td>1.25 × 10^{-4}</td>
<td>8.26 × 10^{-5}</td>
<td>A/V</td>
</tr>
<tr>
<td>g_mbs</td>
<td>4.11 × 10^{-5}</td>
<td></td>
<td></td>
<td>A/V</td>
</tr>
</tbody>
</table>

In this appendix the noise calculation of a transistor is shown and the same method is applied on the other transistors, too. The thermal noise and the flicker noise current of each transistor are calculated by the following formulas:

\[
I_{\text{nd-M1}}^2 = \frac{8kTg_{m\_M1}}{3} = 8 \cdot 1.38 \cdot 10^{-23} \cdot 300 \cdot 2.44 \cdot 10^{-3} = 2.69 \cdot 10^{-23} \frac{A^2}{Hz}
\]

\[
I_{\text{f-M1}}^2 = \frac{K_F I_D^{AF}}{fC_{\alpha L_{eff}}^2} = \frac{6.90 \cdot 10^{-27} \cdot (9.34 \cdot 10^{-4})^{1.34}}{2.5 \cdot 10^9 \cdot 2.72 \cdot 10^{-7} \cdot (4.56 \cdot 10^{-5})^2} = \frac{5.89 \cdot 10^{-31}}{1.42 \cdot 10^{-6}} = 4.15 \cdot 10^{-25} \frac{A^2}{Hz}
\]

The calculation of the noise contribution of the M1 is shown above.

\[
I_{M1}^2 = I_{\text{nd-M1}}^2 + I_{\text{f-M1}}^2 = 2.69 \cdot 10^{-23} + 4.15 \cdot 10^{-25} = 2.73 \cdot 10^{-23} \frac{A^2}{Hz}
\]

In order to write this noise current as a noise voltage, the equivalent resistance has to be found.

\[
R_{eq\_M1} = \frac{4kT}{I_{M1}^2} = 6.06 \cdot 10^2 \Omega
\]

\[
E_{M1}^2 = 4kTR_{eq\_M1} = 4 \cdot 1.38 \cdot 10^{-23} \cdot 300 \cdot 6.06 \cdot 10^2 = 1.00 \cdot 10^{-17} \frac{V^2}{Hz}
\]
<table>
<thead>
<tr>
<th>Transistor</th>
<th>Flicker noise current $I_f^2$</th>
<th>Thermal noise current $I_{nd}^2$</th>
<th>Total noise current $I_{Mx}^2$</th>
<th>Total noise voltage $E_{Mx}^2$</th>
</tr>
</thead>
<tbody>
<tr>
<td>M1</td>
<td>$4.15 \cdot 10^{-25} \frac{A^2}{Hz}$</td>
<td>$2.69 \cdot 10^{-23} \frac{A^2}{Hz}$</td>
<td>$2.73 \cdot 10^{-23} \frac{A^2}{Hz}$</td>
<td>$1.00 \cdot 10^{-17} \frac{V^2}{Hz}$</td>
</tr>
<tr>
<td>M2</td>
<td>$2.87 \cdot 10^{-25} \frac{A^2}{Hz}$</td>
<td>$2.21 \cdot 10^{-23} \frac{A^2}{Hz}$</td>
<td>$2.24 \cdot 10^{-23} \frac{A^2}{Hz}$</td>
<td>$1.23 \cdot 10^{-17} \frac{V^2}{Hz}$</td>
</tr>
<tr>
<td>M3</td>
<td>$8.62 \cdot 10^{-13} \frac{A}{\sqrt{Hz}}$</td>
<td>$1.70 \cdot 10^{-23} \frac{A^2}{Hz}$</td>
<td>$1.73 \cdot 10^{-23} \frac{A^2}{Hz}$</td>
<td>$1.58 \cdot 10^{-17} \frac{V^2}{Hz}$</td>
</tr>
</tbody>
</table>
Detailed calculations of the voltage gain in the LNA (CMOS technology)

Simulated values:

<table>
<thead>
<tr>
<th></th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>R</td>
<td>5.00 \cdot 10^3</td>
<td>Ω</td>
</tr>
<tr>
<td>Rs</td>
<td>50</td>
<td>Ω</td>
</tr>
<tr>
<td>C3</td>
<td>1.00 \cdot 10^{-12}</td>
<td>F</td>
</tr>
</tbody>
</table>

The gain of the first stage can be expressed as:

\[
K_{t1} = \frac{V_{\text{drainM1}}}{V_{\text{in}}} \approx \left( \frac{R}{R_s + \frac{1}{\omega C_3} + R} \right) \left( g_{ds\_M2} + g_{ds\_M3} \right) \left( -g_{m\_M1} \right) \left( g_{m\_M2} + g_{mb\_M2} \right)
\]

\[
= \left( \frac{5.00 \cdot 10^3}{50 + 63.69 + 5.00 \cdot 10^3} \right) \left( 1.25 \cdot 10^{-4} + 8.26 \cdot 10^{-5} \right) \left( 2.44 \cdot 10^{-3} \right)
\]

\[
= 0.98 \cdot 2.51 \cdot 1.20 = 2.94
\]

This is the signal gain from output of the M1 to the input of the LNA. The gain of the second stage is written as:

\[
K_{t2} = \frac{V_{\text{out}}}{V_{\text{drainM1}}} \approx \frac{g_{m\_M2}}{g_{ds\_M3}} = \frac{2.00 \cdot 10^{-3}}{8.26 \cdot 10^{-5}} = 24.21
\]

Therefore, the total gain from the input to the output of the LNA is expressed as:

\[
K_{tot} = K_{t1} \cdot K_{t2} = \frac{V_{\text{out}}}{V_{\text{in}}} \approx \left( \frac{R}{R_s + \frac{1}{\omega C_3} + R} \right) \left( g_{ds\_M2} + g_{ds\_M3} \right) \left( -g_{m\_M1} \right) \left( g_{m\_M2} + g_{mb\_M2} \right) \left( g_{ds\_M3} \right)
\]

\[
= 2.94 \cdot 24.21 = 71.18
\]
These gain calculations are based on the reference [(13), pages 287-292].

<table>
<thead>
<tr>
<th>Calculated gain</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>$K_{r1}^2$</td>
<td>8.64</td>
</tr>
<tr>
<td>$K_{r2}^2$</td>
<td>585.70</td>
</tr>
<tr>
<td>$K_{tot}^2$</td>
<td>5062.21</td>
</tr>
</tbody>
</table>

Table 2.3-2: Calculated gain
Appendix E

Noise calculation of entire LNA (CMOS technology)

Simulated capacitances:

<table>
<thead>
<tr>
<th></th>
<th>M1</th>
<th>M2</th>
<th>M3</th>
<th>C_{var1}</th>
<th>C_{var2}</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$C_{gs}$</td>
<td>16.64 \times 10^{-15}</td>
<td>11.54 \times 10^{-15}</td>
<td>8.75 \times 10^{-15}</td>
<td></td>
<td></td>
<td>F</td>
</tr>
<tr>
<td>$C_{gd}$</td>
<td>8.24 \times 10^{-15}</td>
<td>5.94 \times 10^{-15}</td>
<td>4.07 \times 10^{-15}</td>
<td></td>
<td></td>
<td>F</td>
</tr>
<tr>
<td>$C_{db}$</td>
<td>473.1 \times 10^{-21}</td>
<td>3.75 \times 10^{-21}</td>
<td>623.2 \times 10^{-21}</td>
<td></td>
<td></td>
<td>F</td>
</tr>
<tr>
<td>$C_{sb}$</td>
<td>3.44 \times 10^{-15}</td>
<td>87.80 \times 10^{-18}</td>
<td>14.80 \times 10^{-18}</td>
<td></td>
<td></td>
<td>F</td>
</tr>
<tr>
<td>$C_{gb}$</td>
<td></td>
<td></td>
<td></td>
<td>1.50 \times 10^{-12}</td>
<td>14.77 \times 10^{-15}</td>
<td>F</td>
</tr>
</tbody>
</table>

The following formula is used when the drain-source capacitance is calculated.

$$C_{MX} = (C_{gs} \parallel C_{gd}) \parallel (C_{sb} \parallel C_{db})$$

$$C_{M1} = (16.64 \times 10^{-15} + 8.24 \times 10^{-15}) + (3.44 \times 10^{-15} + 473.1 \times 10^{-21}) = 2.83 \times 10^{-14} \text{ F}$$

Calculated capacitances:

<table>
<thead>
<tr>
<th></th>
<th>M1</th>
<th>M2</th>
<th>M3</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$C_{MX}$</td>
<td>2.83 \times 10^{-14}</td>
<td>1.76 \times 10^{-14}</td>
<td>1.28 \times 10^{-14}</td>
<td>F</td>
</tr>
</tbody>
</table>

$$C_{D} = \left\{(C_{gs} \parallel C_{gd}) \parallel (C_{sb} \parallel C_{db})\right\}_{C_{M1}} + \left\{(C_{gs} \parallel C_{gd}) \parallel (C_{sb} \parallel C_{db})\right\}_{C_{M2}} + C_{v1} + C_{v2} = 1.76 \times 10^{-14} + 1.28 \times 10^{-14} + 1.50 \times 10^{-12} + 14.77 \times 10^{-15} = 1.54 \times 10^{-12} \text{ F}$$

$$R_{D} = \frac{1}{g_{ds\_M2}} \parallel \frac{1}{g_{ds\_M3}} = \frac{1}{g_{ds\_M2}} + \frac{1}{g_{ds\_M3}} = \frac{1}{1.25 \times 10^{-4}} + \frac{1}{8.26 \times 10^{-5}} = 4816.95 \Omega$$

The total capacitive and resistive load of the $M1$ can be written as:

$$C_{L} = C_{ds\_M1} \parallel C_{D} = 1.99 \times 10^{-18} + 1.54 \times 10^{-12} = 1.54 \times 10^{-12} \text{ F}$$

$$R_{L} = r_{ds\_M1} \parallel R_{D} = \frac{1}{\frac{5.95 \times 10^{-5}}{4816.95}} = 3743.91 \Omega$$
The admittance is therefore written as:

\[
Y_1 = \frac{-\omega^2 R_L C_{gd} + \omega^2 C_{gd} (1 + g_m R_L) R_L C_L + \omega C_{gd} \left[1 + g_m R_L + \omega^2 R_L^2 C_L^2 \right]}{1 + \omega^2 R_L^2 C_L^2}
\]

\[
\text{Re}Y_1 = \frac{\omega^2 g_m R_L^2 C_{gd} C_L}{1 + \omega^2 R_L^2 C_L^2} = \frac{1 + \left(1.57 \cdot 10^{10}\right)^2 \cdot 3743.91^2 \cdot (1.54 \cdot 10^{-12})^2}{(1.57 \cdot 10^{10})^2 \cdot 2.44 \cdot 10^{-3} \cdot 3743.91^2 \cdot 8.24 \cdot 10^{-15} \cdot 1.54 \cdot 10^{-12}}
\]

\[
= \frac{8.19 \cdot 10^3}{1.07 \cdot 10^{-3}} = 7.66 \cdot 10^4 \Omega
\]

\[
\text{Im}Y_1 = \frac{j \omega \left[C_{gd} (1 + g_m R_L) + C_{gd} \omega^2 R_L^2 R_L^2 C_L^2 \right]}{1 + \omega^2 R_L^2 C_L^2}
\]

\[
C_{eq} = \frac{C_{gd} (1 + g_m R_L) + C_{gd} \omega^2 R_L^2 C_L^2}{1 + \omega^2 R_L^2 C_L^2}
\]

\[
I_n^2 = \frac{4kT}{R_{eq}} = \frac{4 \cdot 1.38 \cdot 10^{-23} \cdot 300}{7.66 \cdot 10^4} = 2.16 \cdot 10^{-25} A^2
\]

\[
E_n = \frac{E_{nd}^2}{\left(\frac{g_{ds,M2} + g_{ds,M3}}{g_{ds,M3}}\right)^2 \left(\frac{-g_{m,M3}}{g_{m,M2} + g_{mb,M2}}\right)^2 + \left(\frac{g_{ds,M2} + g_{ds,M3}}{g_{ds,M3}}\right)^2 \left(\frac{-g_{m,M1}}{g_{m,M2} + g_{mb,M2}}\right)^2 + \left(\frac{g_{ds,M2} + g_{ds,M3}}{g_{ds,M3}}\right)^2 \left(\frac{-g_{m,M1}}{g_{m,M2} + g_{mb,M2}}\right)^2}
\]

\[
= \frac{1.25 \cdot 10^{-4} + 8.26 \cdot 10^{-5}}{8.26 \cdot 10^{-5}} \left(\frac{2.00 \cdot 10^{-3} + 4.11 \cdot 10^{-5}}{1.00 \cdot 10^{-17}}\right)^2
\]

\[
= 1.11 \cdot 10^{-18} V^2
\]
The thermal noise contributed by the sensor is written as:

\[ E_S^2 = 4kT R_s = 4 \cdot 1.38 \cdot 10^{-23} \cdot 300 \cdot 50 = 8.28 \cdot 10^{-19} V^2 \]

The noise current generated by the bias resistor \( R \) is:

\[ I_R^2 = \frac{4kT}{R} = \frac{4 \cdot 1.38 \cdot 10^{-23}}{5.00 \cdot 10^3} = 3.31 \cdot 10^{-24} A^2 \]

The noise at the input of the \( M1 \) is written as:

\[
E_i^2 = E_n^2 + E_s^2 \left( \frac{R}{R_s + \frac{1}{\omega C_3} + R} \right)^2 + \left( I_R^2 + I_n^2 \right) \left( R \parallel (R_s + \frac{1}{\omega C_3}) \right)^2 = \\
1.11 \cdot 10^{-18} + 8.28 \cdot 10^{-19} \left( \frac{5.00 \cdot 10^3}{50 + 63.69 + 5.00 \cdot 10^3} \right)^2 + \\
(3.31 \cdot 10^{-24} + 2.16 \cdot 10^{-25}) \left( \frac{5.00 \cdot 10^3 (50 + 63.69)}{5.00 \cdot 10^3 + (50 + 63.69)} \right)^2 = \\
1.92 \cdot 10^{-18} + 4.36 \cdot 10^{-20} = 1.95 \cdot 10^{-18} V^2
\]

The noise at the output of the \( M1 \):

\[
E_{\text{no-M1}}^2 = E_i^2 \left( \frac{g_{ds,M2} + g_{ds,M3}}{g_{ds,M3}} \right)^2 \left( \frac{-g_{m,M1}}{g_{m,M2} + g_{mb,M2}} \right)^2 = \\
1.95 \cdot 10^{-18} \left( \frac{1.25 \cdot 10^{-4} + 8.26 \cdot 10^{-5}}{8.26 \cdot 10^{-5}} \right)^2 \left( \frac{-2.44 \cdot 10^{-3}}{2.00 \cdot 10^{-3} + 4.11 \cdot 10^{-5}} \right)^2 = \\
1.95 \cdot 10^{-18} \cdot 6.33 \cdot 1.43 = 1.76 \cdot 10^{-17} V^2
\]
The total noise voltage at the output of the LNA:

\[ E_{\text{output}}^2 = \left( E_{\text{noise,M}_1}^2 + E_{M_2}^2 \right) K_{t_2}^2 + I_{M_3}^2 \cdot \left( \frac{1}{g_{ds,M_3}} \left( \frac{1}{g_{ds,M_2}} + \frac{1}{g_{ds,M_1}} \right) \right)^2 = \left( 1.76 \times 10^{-17} + 1.23 \times 10^{-17} \right) \cdot 585.70 + 1.73 \times 10^{-23} \cdot 8130.61^2 = 1.76 \times 10^{-14} + 1.15 \times 10^{-15} = 1.86 \times 10^{-14} V^2 \]

Noise contributed by the second stage:

\[ E_{2,\text{stage}}^2 = E_{M_2}^2 \cdot K_{t_2}^2 + I_{M_3}^2 \cdot \left( \frac{1}{g_{ds,M_3}} \left( \frac{1}{g_{ds,M_2}} + \frac{1}{g_{ds,M_1}} \right) \right)^2 = 7.18 \times 10^{-15} + 1.15 \times 10^{-15} = 8.33 \times 10^{-15} V^2 \]

The expression of equivalent input noise voltage of the entire LNA can be written as:

\[ E_{ni}^2 = \frac{E_{\text{noise,M}_1}^2}{K_{t_1}^2} + \frac{E_{2,\text{stage}}^2}{K_{t_1}^2 K_{t_2}^2} = \frac{1.76 \times 10^{-17}}{8.64} + \frac{8.33 \times 10^{-15}}{5062.21} = 2.03 \times 10^{-18} + 1.64 \times 10^{-18} = 3.67 \times 10^{-18} V^2 \]

Noise figure, \( NF \), is calculated to:

\[ NF = 10 \log \frac{E_{ni}^2}{E_S^2} = 10 \log \left( \frac{3.67 \times 10^{-18}}{8.28 \times 10^{-19}} \right) = 10 \log (4.44) \approx 6.48 dB \]
Appendix F

Noise in the mixer (CMOS technology)

Simulated values:

<table>
<thead>
<tr>
<th></th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_D$</td>
<td>$10.00 \cdot 10^3$</td>
<td>$\Omega$</td>
</tr>
<tr>
<td>$I_{bias}$</td>
<td>$9.25 \cdot 10^{-5}$</td>
<td>$A$</td>
</tr>
<tr>
<td>$\gamma$</td>
<td>$\frac{2}{3}$</td>
<td></td>
</tr>
<tr>
<td>$A_{LO}$</td>
<td>$0.3$</td>
<td>$V$</td>
</tr>
<tr>
<td>$g_{m,M8}$</td>
<td>$5.27 \cdot 10^{-4}$</td>
<td>$A/V$</td>
</tr>
</tbody>
</table>

\[
V_{o,n}^2 = 8kT R_D \left( 1 + \gamma \frac{R_D I}{\pi A} + \gamma \frac{g_m R_D}{2} \right) = \\
8 \cdot 1.38 \cdot 10^{-23} \cdot 300 \cdot 10.0 \cdot 10^3 \left( 1 + \frac{2 \cdot 10.0 \cdot 10^3 \cdot 9.25 \cdot 10^{-5}}{3 \pi 0.3} + \frac{2 \cdot 10.0 \cdot 10^3 \cdot 5.27 \cdot 10^{-4}}{3 \cdot 2} \right) = \\
3.31 \cdot 10^{-16} + 2.17 \cdot 10^{-16} + 5.82 \cdot 10^{-16} = 1.13 \cdot 10^{-15} \frac{V^2}{Hz}
\]
Appendix G

Coupling noise at the crossing point between two signals (CMOS technology)

The noise voltage calculated below is the noise at the crossing point between the CO and ground signals, shown in subchapter [2.3.2.3].

The values of the terms are estimated by the Cadence in the layout editor.

<table>
<thead>
<tr>
<th></th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$C_{12}$</td>
<td>$0.027 \cdot 10^{-15}$</td>
<td>F</td>
</tr>
<tr>
<td>$C_{2G}$</td>
<td>$0.020 \cdot 10^{-15}$</td>
<td>F</td>
</tr>
<tr>
<td>$R$</td>
<td>1157379.77</td>
<td>Ω</td>
</tr>
<tr>
<td>$V_1$</td>
<td>$300 \cdot 10^{-3}$</td>
<td>V</td>
</tr>
<tr>
<td>$\omega$</td>
<td>$1.508 \cdot 10^{-8}$</td>
<td></td>
</tr>
</tbody>
</table>

\[
V_N = j \omega \left( \frac{C_{12}}{C_{12} + C_{2G}} \right) \quad \text{and} \quad V_1 = \frac{1.508 \cdot 10^{-8}}{1 + \frac{0.027 \cdot 10^{-15}}{1157379.77 \cdot (0.027 \cdot 10^{-15} + 0.020 \cdot 10^{-15})}} \cdot 300 \cdot 10^{-3} \quad \frac{2598 \cdot 10^{-9}}{18383417695.9} = 1.41 \cdot 10^{-16} V^2
\]
Appendix H

Noise calculation of the first stage (BiCMOS and SiGe technology)

The same formulas were used for both BiCMOS and SiGe technologies. Therefore it was not necessary to show calculation of both technologies. The detailed calculation is shown only for SiGe technologies, but the simulated and calculated values of the BiCMOS are given in tables below. The noise calculation is based on the simulated values of the terms used in formulas.

<table>
<thead>
<tr>
<th>Simulated values of transistor T2</th>
<th>BiCMOS 0.8 µm</th>
<th>SiGe</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_s$</td>
<td>50</td>
<td>50</td>
</tr>
<tr>
<td>$R_T$</td>
<td>$4.00 \cdot 10^2$</td>
<td>$2.20 \cdot 10^3$</td>
</tr>
<tr>
<td>$g_m$</td>
<td>$3.83 \cdot 10^{-2}$</td>
<td>$1.32 \cdot 10^{-2}$</td>
</tr>
<tr>
<td>$\beta_0$</td>
<td>$8.43 \cdot 10^1$</td>
<td>$9.06 \cdot 10^1$</td>
</tr>
<tr>
<td>$r_x$</td>
<td>$1.68 \cdot 10^2$</td>
<td>$7.77 \cdot 10^1$</td>
</tr>
<tr>
<td>$r_T$</td>
<td>$2.20 \cdot 10^3$</td>
<td>$6.88 \cdot 10^3$</td>
</tr>
<tr>
<td>$C_{x_T}$</td>
<td>$4.52 \cdot 10^{-13}$</td>
<td>$3.87 \cdot 10^{-13}$</td>
</tr>
<tr>
<td>$C_{\mu}$</td>
<td>$6.31 \cdot 10^{-30}$</td>
<td>$1.63 \cdot 10^{-14}$</td>
</tr>
<tr>
<td>$r_o$</td>
<td>$2.63 \cdot 10^4$</td>
<td>$2.70 \cdot 10^5$</td>
</tr>
<tr>
<td>$I_b$</td>
<td>$1.18 \cdot 10^{-5}$</td>
<td>$3.76 \cdot 10^{-6}$</td>
</tr>
<tr>
<td>$I_c$</td>
<td>$1.04 \cdot 10^{-3}$</td>
<td>$3.49 \cdot 10^{-4}$</td>
</tr>
<tr>
<td>$V_T$</td>
<td>$181.8 \cdot 10^{-3}$</td>
<td>$972 \cdot 10^{-3}$</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Simulated values of transistor T1</th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>$g_m$</td>
<td>$8.04 \cdot 10^{-2}$</td>
<td>$8.64 \cdot 10^{-2}$</td>
</tr>
<tr>
<td>$I_c$</td>
<td>$2.05 \cdot 10^{-3}$</td>
<td>$7.20 \cdot 10^{-4}$</td>
</tr>
<tr>
<td>$r_o$</td>
<td>$2.09 \cdot 10^{-2}$</td>
<td>$1.22 \cdot 10^5$</td>
</tr>
</tbody>
</table>

Calculations performed on all transistors independent of the transistors structure

Detailed calculation of thermal and shot noise generated by a bipolar transistor is shown below. It is shown only the detailed calculation of the transistor $T2$ (SiGe technology), but this is equal for all transistors:

The shot noise voltage at the collector of $T2$:

$$E_{nc}^2 = \frac{2qI_c}{g_m^2} \cdot \frac{2 \cdot 1.60 \cdot 10^{-19} \cdot 3.49 \cdot 10^{-4}}{(1.32 \cdot 10^{-2})^2} = 6.45 \cdot 10^{-19} V^2$$
The shot noise current at the base of the \( T2 \):
\[
I_{mb}^2 = 2qI_b = 2 \cdot 1.60 \cdot 10^{-19} \cdot 3.76 \cdot 10^{-6} = 1.20 \cdot 10^{-24} \, A^2
\]

The flicker noise at the base of \( T2 \):
\[
I_f^2 = \frac{2qf_i I_b^\nu}{f} = \frac{7.80 \cdot 10^{-12} \cdot \left(3.76 \cdot 10^{-6}\right)^{1.10}}{2.5 \cdot 10^9} = 3.36 \cdot 10^{-27} \, A^2
\]

The thermal noise generated by the base resistor:
\[
E_X^2 = 4kT_R = 4 \cdot 1.38 \cdot 10^{-23} \cdot 300 \cdot 77.7 = 1.29 \cdot 10^{-18} \, V^2
\]

The noise current generated by the bias resistor \( R_7 \):
\[
I_{R7}^2 = \frac{4kT}{R_7} = \frac{4 \cdot 1.38 \cdot 10^{-23} \cdot 300}{2.20 \cdot 10^3} = 7.53 \cdot 10^{-24} \, A^2
\]

Detailed calculation of the Miller capacitance and the term \( Z_\pi \) is also the same for all transistors. Below it is shown detailed calculations of those values for \( T2 \) (SiGe technology). The Miller capacitance:
\[
C_M = C_\pi + (1 + g_m R_L)C_\mu = 3.87 \cdot 10^{-13} + \left(1 + 1.32 \cdot 10^{-2} \cdot 21.7\right) \cdot 1.63 \cdot 10^{-14} = 4.08 \cdot 10^{-13} \, F
\]

The Miller capacitance parallel coupled with the \( r_\pi \) resistor:
\[
Z_\pi = \frac{r_\pi}{(\omega C_M r_\pi + 1)} = \frac{6.88 \cdot 10^3}{(1.59 \cdot 10^{10} \cdot 4.08 \cdot 10^{-13} \cdot 6.88 \cdot 10^3 + 1)} = \frac{6.88 \cdot 10^3}{45.63} \approx 1.53 \cdot 10^2 \, \Omega
\]

<table>
<thead>
<tr>
<th>Calculated values of T2</th>
<th>BiCMOS 0.8 µm</th>
<th>SiGe</th>
</tr>
</thead>
<tbody>
<tr>
<td>( E_{nc}^2 )</td>
<td>2.26 \cdot 10^{-19}</td>
<td>6.45 \cdot 10^{-19}</td>
</tr>
<tr>
<td>( I_{mb}^2 )</td>
<td>3.76 \cdot 10^{-24}</td>
<td>1.20 \cdot 10^{-24}</td>
</tr>
<tr>
<td>( I_f^2 )</td>
<td>5.18 \cdot 10^{-30}</td>
<td>3.36 \cdot 10^{-27}</td>
</tr>
<tr>
<td>( E_x^2 )</td>
<td>2.78 \cdot 10^{-18}</td>
<td>1.29 \cdot 10^{-18}</td>
</tr>
<tr>
<td>( I_{R7}^2 )</td>
<td>4.14 \cdot 10^{-23}</td>
<td>7.53 \cdot 10^{-24}</td>
</tr>
<tr>
<td>( C_M )</td>
<td>4.52 \cdot 10^{-13}</td>
<td>4.08 \cdot 10^{-13}</td>
</tr>
<tr>
<td>( Z_\pi )</td>
<td>1.31 \cdot 10^2</td>
<td>1.53 \cdot 10^2</td>
</tr>
</tbody>
</table>
**Gain calculation of T2**

The desired signal at the output of the T2 is expressed as:

\[ V_0 = -g_{m\_T2}R_{C\_T2}(V_{in} - V_e) = -1.32 \times 10^{-2} \cdot 21.77(1 \times 10^{-3} - 972 \times 10^{-3}) \approx 279 \times 10^{-3} V \]

The collector resistance is the input stage resistance of the next stage:

\[ R_C = R_{l\_CE\_T3} = 21.77 \Omega \]

The common emitter voltage gain of the T2 can be calculated by the following expression:

\[ K_{t\_CE\_T2} = \frac{V_o}{V_{in}} = \frac{279 \times 10^{-3}}{1 \times 10^{-3}} \approx 279 \]

The load of T2 is given by:

\[ R_L = R_{l\_CE\_T3} || r_{o\_T2} \Rightarrow \frac{R_{l\_CE\_T3} \cdot r_{o\_T2}}{R_{l\_CE\_T3} + r_{o\_T2}} = \frac{21.77 \cdot 2.7 \times 10^5}{21.77 + 2.7 \times 10^5} \approx 21.7 \Omega \]

The common base voltage gain of T2 is:

\[ K_{t\_CB\_T2} = \frac{-R_{L\_T2}}{R_{l\_CB\_T2}} \frac{\beta_{T2}}{1 + \left( \frac{\beta_{T2} \cdot R_{L\_T2}}{R_{C\_T2}} \right)} \approx -21.7 \cdot 2.4 \left( \frac{90.6}{21.7} \right) \approx -8.59 \]

The common base input impedance of T2:

\[ R_{l\_CB\_T2} = \frac{r_{\pi\_T2} + Z_{\pi\_T2}}{\beta_{T2}} \frac{R_{L\_T2}}{R_{C\_T2}} + 1 \approx \frac{77.7 + 153}{90.6} = 2.43 \Omega \]

<table>
<thead>
<tr>
<th>Calculated values of T2</th>
<th>BiCMOS 0.8 µm</th>
<th>SiGe</th>
<th>V</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_o )</td>
<td>176 \times 10^{-3}</td>
<td>279 \times 10^{-3}</td>
<td>( V )</td>
</tr>
<tr>
<td>( K_{t_CE} )</td>
<td>176</td>
<td>279</td>
<td></td>
</tr>
<tr>
<td>( R_L )</td>
<td>25.4</td>
<td>21.7</td>
<td>( \Omega )</td>
</tr>
<tr>
<td>( K_{t_CB} )</td>
<td>-7.15</td>
<td>-8.59</td>
<td></td>
</tr>
<tr>
<td>( R_{l_CB} )</td>
<td>3.51</td>
<td>2.43</td>
<td>( \Omega )</td>
</tr>
</tbody>
</table>
Noise calculations of the first stage

The noise contributed by $T_2$:

$$ E_{no\_T2}^2 = E_{nc\_T2}^2 + \left( E_{X\_T2}^2 + (I_{nb\_T2}^2 + I_{f\_T2}^2) r_{X\_T2}^2 \right) K_{t\_CE\_T2}^2 + E_{nc\_T1}^2 K_{t\_CB\_T2}^2 = $$

$$ 6.45 \cdot 10^{-19} + \left( 1.29 \cdot 10^{-18} + \left( 1.20 \cdot 10^{-24} + 3.36 \cdot 10^{-27} \right) 77.7^2 \right) 279^2 + 3.08 \cdot 10^{-20} \cdot 8.81^2 \approx $$

$$ 6.45 \cdot 10^{-19} + 1.30 \cdot 10^{-18} \cdot 279^2 + 2.37 \cdot 10^{-18} \approx 1.01 \cdot 10^{-13} V^2 $$

$$ I_{n\_T2}^2 = \frac{I_{nc\_T2}^2}{K_{t\_CE\_T2}^2} + I_{nb\_T2}^2 + I_{f\_T2}^2 = \frac{1.12 \cdot 10^{-22}}{279^2} + 1.20 \cdot 10^{-24} + 3.36 \cdot 10^{-27} = 1.21 \cdot 10^{-24} A^2 $$

$$ E_{i\_T2}^2 = \frac{E_{no\_T2}^2}{K_{t\_CE\_T2}^2} + E_s \left( \frac{R_7}{R_s + R_7} \right)^2 + (I_{R7}^2 + I_n^2) (R_7 || R_s)^2 = $$

$$ \frac{9.93 \cdot 10^{-14}}{279^2} + 8.28 \cdot 10^{-19} \left( \frac{2.20 \cdot 10^3}{2.20 \cdot 10^3 + 50} \right)^2 + (7.53 \cdot 10^{-24} + 1.21 \cdot 10^{-24} \left( \frac{2.20 \cdot 10^3 \cdot 50}{2.20 \cdot 10^3 + 50} \right)^2 \approx $$

$$ \frac{9.93 \cdot 10^{-14}}{279^2} + 7.92 \cdot 10^{-19} + 2.08 \cdot 10^{-20} \approx 2.11 \cdot 10^{-18} V^2 $$

The total noise at the output of $T_2$:

$$ E_{no\_T2}^2 = E_{i\_T2}^2 K_{t\_CE\_T2}^2 = 2.11 \cdot 10^{-18} \cdot 279^2 = 1.64 \cdot 10^{-13} V^2 $$

Calculated noise values of the first stage are shown in table below:

<table>
<thead>
<tr>
<th>Calculated noise values of first stage</th>
<th>BiCMOS 0.8 µm</th>
<th>SiGe</th>
</tr>
</thead>
<tbody>
<tr>
<td>$E_{no}^2$</td>
<td>8.94 $\cdot$ 10^{-14}</td>
<td>1.01 $\cdot$ 10^{-13}</td>
</tr>
<tr>
<td>$I_n^2$</td>
<td>3.77 $\cdot$ 10^{-24}</td>
<td>1.21 $\cdot$ 10^{-24}</td>
</tr>
<tr>
<td>$E_{ni}^2$</td>
<td>3.63 $\cdot$ 10^{-18}</td>
<td>2.11 $\cdot$ 10^{-18}</td>
</tr>
<tr>
<td>$E_{no}^2$</td>
<td>1.12 $\cdot$ 10^{-13}</td>
<td>1.64 $\cdot$ 10^{-13}</td>
</tr>
</tbody>
</table>
Appendix I

Noise calculation of the second stage (BiCMOS and SiGe technology)

Simulated results:

<table>
<thead>
<tr>
<th>Simulated values of transistor T3</th>
<th>BiCMOS 0.8 µm</th>
<th>SiGe</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_6$</td>
<td>$1.0 \cdot 10^3$</td>
<td>$1.7 \cdot 10^3$</td>
</tr>
<tr>
<td>gm</td>
<td>$3.38 \cdot 10^{-2}$</td>
<td>$1.25 \cdot 10^{-2}$</td>
</tr>
<tr>
<td>$\beta_0$</td>
<td>$6.66 \cdot 10^{-1}$</td>
<td>$9.55 \cdot 10^{1}$</td>
</tr>
<tr>
<td>$r_x$</td>
<td>$5.26 \cdot 10^2$</td>
<td>$1.51 \cdot 10^2$</td>
</tr>
<tr>
<td>$r_p$</td>
<td>$1.97 \cdot 10^3$</td>
<td>$7.65 \cdot 10^3$</td>
</tr>
<tr>
<td>$C_\pi$</td>
<td>$4.14 \cdot 10^{-13}$</td>
<td>$1.83 \cdot 10^{-13}$</td>
</tr>
<tr>
<td>$C_\mu$</td>
<td>$3.15 \cdot 10^{-30}$</td>
<td>$1.31 \cdot 10^{-14}$</td>
</tr>
<tr>
<td>$r_o$</td>
<td>$2.53 \cdot 10^4$</td>
<td>$4.46 \cdot 10^5$</td>
</tr>
<tr>
<td>$I_b$</td>
<td>$1.31 \cdot 10^{-5}$</td>
<td>$3.38 \cdot 10^{-6}$</td>
</tr>
<tr>
<td>$I_c$</td>
<td>$9.92 \cdot 10^{-4}$</td>
<td>$3.32 \cdot 10^{-4}$</td>
</tr>
</tbody>
</table>

Gain calculations

Two different impedances are calculated for this stage:

1. The common base impedance:

$$R_{i\_CB\_T3} = \frac{R_6 + r_x\_T3 + Z_{\pi\_T3}}{\beta_{T3} \frac{R_L\_T3}{R_C\_T3} + 1} = \frac{1.7 \cdot 10^3 + 1.51 \cdot 10^2 + 2.32 \cdot 10^2}{95.5 \frac{2.29 \cdot 10^3}{2.31 \cdot 10^3} + 1} = \frac{2083}{95.5 \frac{3.26 \cdot 10^3}{3.29 \cdot 10^3} + 1} \approx 21.77 \Omega$$

2. The common emitter impedance:

$$R_{i\_CE\_T3} = R_6 + r_x\_T3 + Z_{\pi\_T3} = 1.7 \cdot 10^3 + 1.51 \cdot 10^2 + 2.32 \cdot 10^2 = 2.08 \cdot 10^3 \Omega$$

Load at the output of the T3:

$$R_{C\_T3} = R_{i\_CC\_T4} = 2.31 \cdot 10^3 \Omega$$

$$R_L\_T3 = R_C\_T3 \parallel r_o\_T3 \Rightarrow \frac{R_{C\_T3} \cdot r_o\_T3}{R_{C\_T3} + r_o\_T3} = \frac{2.31 \cdot 10^3 \cdot 4.46 \cdot 10^5}{2.31 \cdot 10^3 + 4.46 \cdot 10^5} \approx 2.29 \cdot 10^3 \Omega$$
The common base and the common emitter voltage gain:

\[
K_{t_{-} CB_{-} T3} = \frac{-R_{L_{-} T3}}{R_{i_{-} CB_{-} T3}} \cdot \frac{\beta_{T3}}{1 + \left( \frac{\beta_{T3} R_{L_{-} T3}}{R_{C_{-} T3}} \right)} = \frac{-2.29 \cdot 10^3}{21.70} \cdot \frac{95.5}{1 + \left( \frac{95.5 \cdot 2.29 \cdot 10^3}{2.31 \cdot 10^3} \right)} \approx -19.0
\]

\[
K_{t_{-} CE_{-} T3} = \frac{-\beta_{T3} R_{L_{-} T3}}{R_6 + r_s_{-} T3 + Z_{\pi_{-} T3}} = \frac{-95.5 \cdot 2.29 \cdot 10^3}{1.7 \cdot 10^3 + 1.51 \cdot 10^2 + 2.32 \cdot 10^2} = \frac{218695}{2083} \approx 105
\]

<table>
<thead>
<tr>
<th>Calculated values of T3</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
</tr>
<tr>
<td>( R_{i_{-} CB} )</td>
</tr>
<tr>
<td>( R_{i_{-} CE} )</td>
</tr>
<tr>
<td>( R_L )</td>
</tr>
<tr>
<td>( K_{t_{-} CB} )</td>
</tr>
<tr>
<td>( K_{t_{-} CE} )</td>
</tr>
</tbody>
</table>

Noise calculations of the second stage

The noise generated by the second stage at the output of the second stage:

\[
E_{no_{-} T3}^2 = E_{nc_{-} T3}^2 + \left( E_{X_{-} T3}^2 + E_{R6}^2 + \left( I_{b_{-} T3}^2 + I_{f_{-} T3}^2 \right) \left( r_X + R_6 \right) \right) K_{t_{-} CE_{-} T3}^2 = 6.83 \cdot 10^{-19} + \left( 2.50 \cdot 10^{-18} + 2.82 \cdot 10^{-17} + \left( 1.08 \cdot 10^{-24} + 2.99 \cdot 10^{-27} \right) \cdot (151 + 1700)^2 \right) \cdot 105^2 = 6.83 \cdot 10^{-19} + \left( 3.07 \cdot 10^{-17} + 3.71 \cdot 10^{-18} \right) \cdot 105^2 \approx 3.80 \cdot 10^{-13} V^2
\]

The total noise at the output of the T3:

\[
E_{no_{-} T3}^2 = E_{no_{-} T3}^2 + E_{no_{-} T2}^2 K_{t_{-} CB_{-} T3}^2 = 3.80 \cdot 10^{-13} + 1.64 \cdot 10^{-13} \cdot (-19.0)^2 \approx 5.94 \cdot 10^{-11} V^2
\]

<table>
<thead>
<tr>
<th>Calculated noise values of second stage</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
</tr>
<tr>
<td>( E_{no}^2 )</td>
</tr>
<tr>
<td>( E_{no}^2 )</td>
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</tbody>
</table>
Appendix J

Noise calculation of the third stage (BiCMOS and SiGe technology)

Simulated results:

<table>
<thead>
<tr>
<th>Simulated values of transistor T4</th>
<th>BiCMOS 0.8 µm</th>
<th>SiGe</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_{12}$</td>
<td>$1.70 \cdot 10^4$</td>
<td>$9.30 \cdot 10^2$</td>
</tr>
<tr>
<td>$g_m$</td>
<td>$1.76 \cdot 10^{-2}$</td>
<td>$1.95 \cdot 10^{-1}$</td>
</tr>
<tr>
<td>$\beta_0$</td>
<td>$8.10 \cdot 10^1$</td>
<td>$7.55 \cdot 10^1$</td>
</tr>
<tr>
<td>$r_x$</td>
<td>$8.38 \cdot 10^1$</td>
<td>$6.71 \cdot 10^1$</td>
</tr>
<tr>
<td>$r_o$</td>
<td>$4.59 \cdot 10^3$</td>
<td>$3.88 \cdot 10^2$</td>
</tr>
<tr>
<td>$C_\pi$</td>
<td>$3.83 \cdot 10^{-13}$</td>
<td>$8.56 \cdot 10^{-13}$</td>
</tr>
<tr>
<td>$C_\mu$</td>
<td>$2.00 \cdot 10^{-28}$</td>
<td>$4.33 \cdot 10^{-14}$</td>
</tr>
<tr>
<td>$r_o$</td>
<td>$2.40 \cdot 10^4$</td>
<td>$1.58 \cdot 10^4$</td>
</tr>
<tr>
<td>$I_b$</td>
<td>$5.62 \cdot 10^{-6}$</td>
<td>$6.67 \cdot 10^{-5}$</td>
</tr>
<tr>
<td>$I_c$</td>
<td>$4.65 \cdot 10^{-4}$</td>
<td>$5.34 \cdot 10^{-3}$</td>
</tr>
</tbody>
</table>

Gain calculations:

The input impedance of the fourth stage is found by this:

$$R_{i_{-CC-T4}} = r_{N_{-T4}} + Z_{x_{-T4}} + R_{L_{-T4}} (1 + \beta_{T4}) = 67.1 + 48.4 + 28.6 \cdot (1 + 75.5) \approx 2.31 \cdot 10^3 \Omega$$

The voltage gain of the third stage:

$$K_{t_{-CC-T4}} = \frac{(1 + \beta_{T4})R_{L_{-T4}}}{R_{i_{-CC-T4}}} = \frac{(1 + 75.5) \cdot 28.6}{1.31 \cdot 10^3} \approx 0.95$$

The load of the third stage where the resistor $R_{12}$ is included:

$$R_{L_{-T4}} = r_{o_{-T4}} || R_{E_{-T4}} \Rightarrow r_{o_{-T4}} || R_{12} || R_{i_{-T5}} \Rightarrow \frac{r_{o_{-T4}} \cdot R_{12} \cdot R_{i_{-T5}}}{r_{o_{-T4}} \cdot R_{i_{-T5}} + R_{12} \cdot r_{o_{-T4}} + R_{i_{-T5}} \cdot R_{12}} = \frac{1.58 \cdot 10^4 \cdot 9.30 \cdot 10^2 \cdot 29.6}{1.58 \cdot 10^4 \cdot 29.6 + 9.30 \cdot 10^2 \cdot 1.58 \cdot 10^4 + 29.6 \cdot 9.30 \cdot 10^2} = 28.6 \Omega$$
Calculated values of T4

<table>
<thead>
<tr>
<th>BiCMOS 0.8 µm</th>
<th>SiGe</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_{t,CC}$</td>
<td>$7.72 \times 10^2$</td>
</tr>
<tr>
<td>$K_{t,CC}$</td>
<td>0.69</td>
</tr>
<tr>
<td>$R_L$</td>
<td>6.54</td>
</tr>
</tbody>
</table>

Noise calculations of the third stage

The noise generated by the third stage at the output of the third stage:

$$
E_{no,T4}^2 = I_{R12}^2 r_{no,T4}^2 + E_{no,T4}^2 + \left( E_{X,T4}^2 + \left( I_{nb,T4}^2 + I_{f,T4}^2 \right) r_{X,T4}^2 \right) K_{t,CC,T4}^2 = 
1.78 \times 10^{-23} \left( \frac{1.58 \times 10^4 \cdot 9.30 \times 10^2}{1.58 \times 10^4 + 9.30 \times 10^2} \right)^2 + 4.51 \times 10^{-20} + 
(1.11 \cdot 10^{-18} + (2.13 \cdot 10^{-23} + 7.95 \cdot 10^{-26}) \cdot 67.1^2) \cdot 0.95^2 = 
1.38 \cdot 10^{-17} + 1.20 \cdot 10^{-18} \cdot 0.95^2 = 1.49 \cdot 10^{-17} V^2
$$

The total noise at the output of the third stage:

$$
E_{no,T4}^2 = E_{no,T4}^2 + E_{no,T3}^2 K_{t,CC,T4}^2 = 1.49 \cdot 10^{-17} + 5.94 \cdot 10^{-11} \cdot 0.95^2 \approx 5.36 \cdot 10^{-11} V^2
$$

Calculated noise values of third stage

<table>
<thead>
<tr>
<th>BiCMOS 0.8 µm</th>
<th>SiGe</th>
</tr>
</thead>
<tbody>
<tr>
<td>$E_{no}^2$</td>
<td>$9.77 \cdot 10^{-17}$</td>
</tr>
<tr>
<td>$E_{no}^2$</td>
<td>$5.99 \cdot 10^{-12}$</td>
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</tbody>
</table>
Appendix K

Noise calculation of the fourth stage (BiCMOS and SiGe technology)

Simulated results:

<table>
<thead>
<tr>
<th>Simulated values of transistor T5</th>
<th>BiCMOS 0.8 µm</th>
<th>SiGe</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_4$</td>
<td>$1.20 \cdot 10^4$</td>
<td>$1.0 \cdot 10^4$</td>
</tr>
<tr>
<td>$g_m$</td>
<td>$6.51 \cdot 10^{-8}$</td>
<td>$1.68 \cdot 10^{-1}$</td>
</tr>
<tr>
<td>$\beta_0$</td>
<td>$9.09 \cdot 10^1$</td>
<td>$1.32 \cdot 10^1$</td>
</tr>
<tr>
<td>$r_x$</td>
<td>$9.75 \cdot 10^1$</td>
<td>$4.39 \cdot 10^1$</td>
</tr>
<tr>
<td>$r_\pi$</td>
<td>$1.39 \cdot 10^9$</td>
<td>$7.85 \cdot 10^1$</td>
</tr>
<tr>
<td>$C_\pi$</td>
<td>$1.26 \cdot 10^{-13}$</td>
<td>$1.48 \cdot 10^{-12}$</td>
</tr>
<tr>
<td>$C_\mu$</td>
<td>$1.89 \cdot 10^{-29}$</td>
<td>$1.67 \cdot 10^{-11}$</td>
</tr>
<tr>
<td>$I_b$</td>
<td>$4.15 \cdot 10^4$</td>
<td>$0.63 \cdot 10^1$</td>
</tr>
<tr>
<td>$I_c$</td>
<td>$1.93 \cdot 10^{-11}$</td>
<td>$5.45 \cdot 10^{-4}$</td>
</tr>
<tr>
<td>$I_{ce}$</td>
<td>$1.69 \cdot 10^{-9}$</td>
<td>$3.03 \cdot 10^{-4}$</td>
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</tbody>
</table>

<table>
<thead>
<tr>
<th>Simulated values of transistor T6</th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>$g_m$</td>
<td>$5.43 \cdot 10^{-2}$</td>
<td>$5.43 \cdot 10^{-2}$</td>
</tr>
<tr>
<td>$I_c$</td>
<td>$7.11 \cdot 10^{-5}$</td>
<td>$1.56 \cdot 10^{-3}$</td>
</tr>
<tr>
<td>$r_o$</td>
<td>$3.95 \cdot 10^5$</td>
<td>$6.81 \cdot 10^4$</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Simulated values of transistor T7</th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>$g_m$</td>
<td>$1.00 \cdot 10^{-2}$</td>
<td>$3.58 \cdot 10^{-3}$</td>
</tr>
<tr>
<td>$r_x$</td>
<td>$5.64 \cdot 10^2$</td>
<td>$1.13 \cdot 10^2$</td>
</tr>
<tr>
<td>$r_\pi$</td>
<td>$8.12 \cdot 10^3$</td>
<td>$2.67 \cdot 10^4$</td>
</tr>
<tr>
<td>$C_\pi$</td>
<td>$1.25 \cdot 10^{-13}$</td>
<td>$2.27 \cdot 10^{-13}$</td>
</tr>
<tr>
<td>$C_\mu$</td>
<td>$9.70 \cdot 10^{-30}$</td>
<td>$3.20 \cdot 10^{-14}$</td>
</tr>
<tr>
<td>$r_o$</td>
<td>$6.98 \cdot 10^4$</td>
<td>$7.71 \cdot 10^5$</td>
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<table>
<thead>
<tr>
<th>Simulated values of transistor T8</th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>$g_m$</td>
<td>$5.55 \cdot 10^{-2}$</td>
<td>$6.15 \cdot 10^{-2}$</td>
</tr>
<tr>
<td>$r_x$</td>
<td>$4.09 \cdot 10^2$</td>
<td>$1.29 \cdot 10^2$</td>
</tr>
<tr>
<td>$r_\pi$</td>
<td>$1.09 \cdot 10^3$</td>
<td>$1.41 \cdot 10^3$</td>
</tr>
<tr>
<td>$C_\pi$</td>
<td>$7.85 \cdot 10^{-13}$</td>
<td>$3.23 \cdot 10^{-13}$</td>
</tr>
<tr>
<td>$C_\mu$</td>
<td>$3.15 \cdot 10^{-30}$</td>
<td>$2.83 \cdot 10^{-14}$</td>
</tr>
<tr>
<td>$r_o$</td>
<td>$1.43 \cdot 10^4$</td>
<td>$5.48 \cdot 10^4$</td>
</tr>
</tbody>
</table>
Calculation of common emitter and common base impedance of $T5$:

$$R_{i,CE,T5} = r_{x,T5} + Z_\pi T5 + R_E T5 \left( r_0 T5 (1 + \beta T5) + R_C T5 \right)$$

$$43.9 + 1.76 + \frac{6.81 \times 10^4 \left( 6.26 \left( 1 + 13.2 \right) + 147 \right)}{6.26 + 147 + 6.81 \times 10^4} = 2.81 \times 10^2 \Omega$$

$$R_{i,CB,T5} = \frac{r_{x,T5} + Z_\pi T5}{\beta T5 R_L T5 + R_C T5} + 1 \left( \frac{13.2}{6.04} + 1 \right) = 29.60 \Omega$$

Collector and emitter resistance can be written as:

$$R_C = R_4 \parallel R_{i,T7} \parallel R_{i,T8} \Rightarrow \frac{R_4 \cdot R_{i,T7} \cdot R_{i,T8}}{R_{i,T7} \cdot R_{i,T8} + R_4 \cdot R_{i,T8} + R_4 \cdot R_{i,T7}} = \frac{1.0 \times 10^4 \cdot 349 \cdot 261}{349 \cdot 261 + 1.0 \times 10^4 \cdot 261 + 1.0 \times 10^4 \cdot 349} = 147.13 \Omega$$

$$R_E = r_o T6 = 6.81 \times 10^4 \Omega$$

Common emitter and common base voltage gain of $T5$:

$$K_{l,CE,T5} = \frac{\beta T5 R_L T5}{r_{x,T5} + Z_\pi T5} = \frac{13.2 \cdot 6.04}{43.9 + 1.76} = -1.75$$

$$K_{l,CB,T5} = \frac{-R_L T5}{R_{i,CB,T5}} \left( \frac{\beta T5}{1 + \left( \frac{\beta T5 R_L T5}{R_C T5} \right) \left( \frac{13.2}{147.13} \right)} \right) = -6.04 \cdot 29.60 + \frac{13.2}{147.13} \approx -1.75$$
The load of $T5$:

$$R_{L,T5} = r_{o,T5} \parallel R_4 \parallel R_{i,CE,T7} \parallel R_{i,CE,T8} \Rightarrow$$

$$r_{o,T5} \cdot R_4 \cdot R_{i,CE,T7} \cdot R_{i,CE,T8} =$$

$$R_4 \cdot R_{i,CE,T7} \cdot R_{i,CE,T8} + r_{o,T5} \cdot R_{i,CE,T7} \cdot R_{i,CE,T8} + r_{o,T5} \cdot R_4 \cdot R_{i,CE,T8} + r_{o,T5} \cdot R_4 \cdot R_{i,CE,T7}$$

$$= 6.3 \cdot 1.0 \cdot 10^4 \cdot 349 \cdot 261$$

$$5738607 \cdot 10^3 = 6.04 \Omega$$

The input impedance of the mixer transistors which are connected at the output of $T5$:

$$R_{i,T7} = Z_{\pi,T7} + r_{x,T7} = 236 + 113 = 349 \Omega$$

$$R_{i,T8} = Z_{\pi,T8} + r_{x,T8} = 132 + 129 = 261 \Omega$$

<table>
<thead>
<tr>
<th>Calculated values $T5$</th>
<th>BiCMOS 0.8 µm</th>
<th>SiGe</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_{i,CE}$</td>
<td>$3.45 \cdot 10^6$</td>
<td>$2.81 \cdot 10^2$</td>
</tr>
<tr>
<td>$R_{i,CB}$</td>
<td>$0.65 \cdot 10^1$</td>
<td>$2.96 \cdot 10^1$</td>
</tr>
<tr>
<td>$R_C$</td>
<td>$3.21 \cdot 10^2$</td>
<td>$1.47 \cdot 10^2$</td>
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<tr>
<td>$C_M$</td>
<td>$1.26 \cdot 10^{-13}$</td>
<td>$3.51 \cdot 10^{-11}$</td>
</tr>
<tr>
<td>$Z_\pi$</td>
<td>$4.99 \cdot 10^2$</td>
<td>$1.76 \cdot 10^{-1}$</td>
</tr>
<tr>
<td>$R_L$</td>
<td>$3.19 \cdot 10^2$</td>
<td>6.04</td>
</tr>
<tr>
<td>$K_{i,CE}$</td>
<td>$-48.6$</td>
<td>$-1.75$</td>
</tr>
<tr>
<td>$K_{i,CB}$</td>
<td>$-48.6$</td>
<td>$-1.75$</td>
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<table>
<thead>
<tr>
<th>Calculated values $T7$</th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_{i,CB}$</td>
<td>$1.04 \cdot 10^3$</td>
<td>$3.49 \cdot 10^2$</td>
</tr>
<tr>
<td>$C_M$</td>
<td>$1.25 \cdot 10^{-13}$</td>
<td>$2.65 \cdot 10^{-13}$</td>
</tr>
<tr>
<td>$Z_\pi$</td>
<td>$4.74 \cdot 10^2$</td>
<td>$2.36 \cdot 10^2$</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Calculated values $T8$</th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_{i,CB}$</td>
<td>$4.84 \cdot 10^2$</td>
<td>$2.61 \cdot 10^2$</td>
</tr>
<tr>
<td>$C_M$</td>
<td>$7.85 \cdot 10^{-13}$</td>
<td>$4.34 \cdot 10^{-13}$</td>
</tr>
<tr>
<td>$Z_\pi$</td>
<td>$7.49 \cdot 10^1$</td>
<td>$1.32 \cdot 10^2$</td>
</tr>
</tbody>
</table>
Output noise generated by $T5$:

\[ E_{no,T5}^2 = I_{R4}^2 \left( R_4 \parallel r_{O,T5} \right) + E_{nc,T5}^2 + \\
\left( E_{X,T5}^2 + \left( I_{nb,T5}^2 + I_{f,T5}^2 \right) r_{X,T5}^2 \right) K_{t,CE,T5}^2 + E_{nc,T6}^2 K_{t,CB,T5}^2 = \\
1.66 \cdot 10^{-24} \left( 1.0 \cdot 10^4 \cdot 6.26 \right) + 3.43 \cdot 10^{-21} + \\
\left( 7.27 \cdot 10^{-19} + \left( 1.74 \cdot 10^{-22} + 8.01 \cdot 10^{-25} \right) 43.9^2 \right) 1.75^2 + 1.69 \cdot 10^{-19} \cdot 1.75^2 = \\
1.04 \cdot 10^{-23} + 3.43 \cdot 10^{-21} + 3.26 \cdot 10^{-18} + 5.17 \cdot 10^{-19} \approx 3.76 \cdot 10^{-18} V^2 \]

The total output noise of the LNA:

\[ E_{no,T5}^2 = E_{no,T5}^2 + E_{no,T4}^2 K_{t,CE,T5}^2 = 3.76 \cdot 10^{-18} + 5.36 \cdot 10^{-11} \cdot 1.75^2 = 1.63 \cdot 10^{-10} V^2 \]

<table>
<thead>
<tr>
<th>Calculated noise values of fourth stage</th>
</tr>
</thead>
<tbody>
<tr>
<td>BiCMOS 0.8 µm</td>
</tr>
<tr>
<td>$E_{no}^2$</td>
</tr>
<tr>
<td>$E_{no}^2$</td>
</tr>
</tbody>
</table>
Appendix L

Noise in the entire LNA (BiCMOS and SiGe technology)

Equivalent input noise of entire LNA:

\[
E_{ni}^2 = \frac{E_{no\_T2}^2}{K_{t\_T2}^2} + \frac{E_{no\_T3}^2}{K_{t\_T2}^2 K_{i\_T3}^2} + \frac{E_{no\_T4}^2}{K_{t\_T2}^2 K_{i\_T3}^2 K_{i\_T4}^2} + \frac{E_{no\_T5}^2}{K_{t\_T2}^2 K_{i\_T3}^2 K_{i\_T4}^2 K_{i\_T5}^2} = \\
1.64 \cdot 10^{-13} + 3.80 \cdot 10^{-13} + 1.49 \cdot 10^{-17} + 3.76 \cdot 10^{-18} \\
\frac{279^2}{279^2} + \frac{279^2 \cdot 19^2}{279^2} + \frac{279^2 \cdot 19^2 \cdot 0.95^2}{279^2} + \frac{279^2 \cdot 19^2 \cdot 0.95^2 \cdot 1.75^2}{279^2} = \\
2.11 \cdot 10^{-18} + 1.36 \cdot 10^{-20} + 5.89 \cdot 10^{-25} + 4.89 \cdot 10^{-26} = 2.12 \cdot 10^{-18} V^2
\]

Noise figure of entire LNA:

\[
NF = 10 \log \frac{E_{ni}^2}{E_S^2} = 10 \cdot \log \frac{2.12 \cdot 10^{-18}}{8.28 \cdot 10^{-19}} = 4.08 dB
\]

<table>
<thead>
<tr>
<th>Calculated values of $E_{ni}$ and $NF$</th>
<th>BiCMOS 0.8 µm</th>
<th>SiGe</th>
</tr>
</thead>
<tbody>
<tr>
<td>$E_{ni}^2$</td>
<td>3.64 $\cdot$ 10$^{-18}$</td>
<td>2.12 $\cdot$ 10$^{-18}$</td>
</tr>
<tr>
<td>NF</td>
<td>6.43</td>
<td>4.08</td>
</tr>
</tbody>
</table>
Appendix M

The layout of the circuit designed in CMOS 0.6 µm technology