Cyclic ADC for Langmuir Probes in 180nm CMOS

Design of a 1V 14-bit 20kS/s 1.5bit-Cyclic ADC in XFAB 180nm CMOS Technology

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Thesis submitted for the degree of
Master in Electrical Engineering, Informatics and Technology
60 credits

Department of Physics
The Faculty of Mathematics and Natural Sciences

UNIVERSITY OF OSLO

Spring 2021

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http://www.duo.uio.no/

Printed: Reprosentralen, University of Oslo

Abstract

This thesis presents the design and implementation of a 14-bit 20kS/s Cyclic Analog to Digital Converter (ADC) in XFAB 180nm CMOS technology suited for sampling measurements from multi-Needle Langmuir Probes (m-NLP), which are instruments developed at the Department of Physics (UiO) to measure electron/ion densities in plasma, and are deployed on space crafts.
In an ongoing effort to miniaturize the instrument, the previously designed hybrid CR-SAR ADC, which is a hybrid architecture employing a resistor ladder and charge redistribution DAC, is to be redesigned with an alternative architecture that promises a more layout space conservative and more offset immune solution.
A 1.5-bit per phase Cyclic ADC, which requires smaller amount of analog circuitry and dissipates less power, and which is less prone to offset is designed . It has 12.25 ENOB and the power dissipation is 0.6mW. The XFAB 180nm technology has a high voltage transistor option that is required to bias the Langmuir probes and is compatible with IMEC's DARE (Design Against Radiation Effects) libraries of radiation hardened cells [6]. Unfortunately, 180nm XFAB has long turnaround times, which makes it unsuited for Master projects that actually produce silicon. Thus, this project is purely a design and simulation project, without ASIC production and testing. However, a part of the system is taped-out and sent for manufacturing on a shared chip with other student but it didn't return on the planned date to perform testing.

Keywords— Algorithmic, Cyclic, RSD, ADC, SC, DAC, m-NLP

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Preface

It has been a great privilege to be a graduate student at the Department of Physics, University of Oslo (UiO). My experience here has been full of opportunities to learn from the faculty staff and students with a wide and deep expertise in engineering, particularly in the field of CMOS technology. I am deeply grateful to all the people who, in one way or another, have helped me during my graduate study. Without their support and assistance, I could not have accomplished this.

First and foremost, I would like to express my sincere gratitude to my supervisor Prof. Philipp Häfliger at UiO for his continuous support, supervision and invaluable suggestions throughout the thesis work. I would also like to thank all the members of the bi-weekly supervision meeting group, the instructors and classmates, who have contributed a lot by sharing their knowledge and experience and providing valuable inputs during my two years study. A special thanks also goes out to those people in the department, who were particularly instrumental in facilitating the teaching and learning environment especially during the current pandemic.

Finally, I would like to express my heartfelt gratitude to my beloved parents for their motivation, support and guidance without which I would not have been able to reach this level.

Chapter 1

Introduction

1.1 Background

Multi-Needle Langmuir Probes (m-NLP) are sensors measuring electron or ion density in plasma that have been developed at the Physics Department, University of Oslo [1] under the 4DSpace-Strategic Research Initiative. The m-NLP comprises of four miniaturized cylindrical probes that perform a high speed electron density measurements without the need to know the spacecraft's potential and the electron temperature. Since 2008, it was deployed on different space crafts, i.e. in the ionosphere on sounding rockets or cubesats (e.g. the ICI-2, NorSat1 and QB50 missions)

In an ongoing effort to miniaturize the instrument, the Nanoelectronics group has already designed two iterations of mixed-signal systems on chip (SoC) to control and collect data from m-NLPs on a single integrated circuit (IC) in 180nm CMOS technology. The analog to digital converter (ADC) architecture, which is used for sampling measurements of the electrons drawn by the probes, in the previous iterations has been a hybrid Charge-Redistribution Successive Approximation Register (CR-SAR) ADC [11]. It's a hybrid architecture employing a resistor ladder and charge redistribution DAC.

This project explores an alternative ADC architecture and implementation in 180nm CMOS technology that promises to be more layout space conservative and more offset immune, a 1.5bit per phase cyclic ADC [2, 13, 16]. The design specification of the selected ADC is as shown in Table 1.1 below.

Table 1.1: Design specifications

Specifications	
Technology/Process	XFAB 180nm CMOS Technology
Resolution	14-bit
Sampling Rate	20kS/s
Power Supply	1.8V
Input Range	1V

1.2 Thesis Organization

This thesis describes the design and implementation of a 1.5bit per phase Cyclic ADC. It is arranged in to different chapters, each presenting specific topics. Following this Introduction, Chapter 2 discusses the different types of ADCs and their performance metrics. Chapter 3 presents the working principles of the different types of Cyclic ADC architectures. Chapter 4 deals with the system level design and implementation of the proposed 14-bit cyclic ADC in XFAB 180nm CMOS process. Chapter 5 describes the simulation and layout of the proposed topology. Chapter 6 summarizes this thesis and discusses the future work.

Chapter 2

Analog to Digital Converters and Performance Characteristics

2.1 Analog-to-Digital Converter (ADC)

An Analog-to-Digital Converter (ADC) is an electronic circuit that converts an analog electric signal (usually a voltage) into a digital bit corresponding to the magnitude of the input signal. The ADCs are usually at the front-end of many digital circuits that need to process continuous time and amplitude signals coming from the exterior component into a discrete digital signal that involves sampling, quantization and digital codes assignment. The Fig. 2.1 below shows the general block diagram of an ADC.

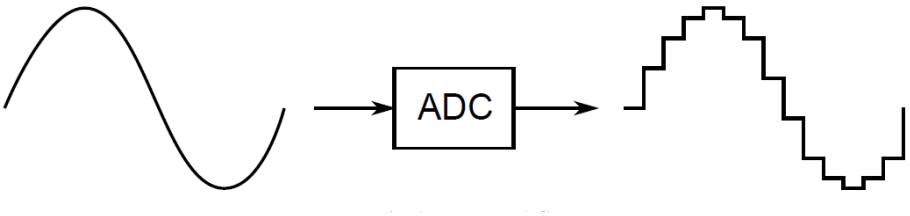

Figure 2.1: ADC block diagram

Analog-to-digital converters are the backbone of the modern digital systems and thus the design of a more compact and low power converters become the areas of interest for researchers. ADC can be roughly divided into three categories [16]: low-to-medium speed, medium speed, and high-speed converters with its corresponding accuracy as shown in Table 2.1 .

Table 2.1: Classification of ADC Architectures

Low-to-Medium Speed, High Accuracy	Medium Speed, Medium Accuracy	High Speed, Low-to-Medium Accuracy
Integrating	Successive approximation	Flash
Oversampling	Algorithmic	Two-step
		Interpolating
		Folding
		Pipelined
		Time-interleaved

Table 2.1: Classification of ADC Architectures

Some of these ADC architectures are explained below:

1. Integrating ADC

Integrating ADC is a popular approach for realizing high-accuracy data conversion on very slow signals. These types of converters have very low offset and gain errors in addition to being highly linear. A further advantage of integrating converters is the small amount of circuitry required in their implementation.

The Integrating conversion proceeds first by integrating the input for a fixed time period, then applying a known input to the integrator and measuring the time required for the integrator output to return to zero. It does not require accuracy in defining the integration time constant. Offset errors can be calibrated by performing an additional conversion using a known dc input quantity.

2. SAR (Successive Approximation Register) ADC

SAR ADC is a very versatile, capable of moderately high speed and accuracy with relatively low power. It has relatively simple circuits, in the simplest cases requiring only a single comparator, a bank of capacitors and switches, and a small digital logic circuit. Its biggest drawback is that it operates iteratively and therefore requires many clock cycles to perform a single conversion.

The accuracy of SAR is often determined by that of the DAC. In the case of charge-redistribution SAR, this role is played by a bank of comparators whose matching is important.

3. Algorithmic/Cyclic ADC

Algorithmic converters are similar to successive-approximation converters, except that instead of an accurate DAC or capacitor bank, these converters require an accurate gain of two in order to perform the iterative search for a digital code that represents the analog input.

Introducing redundancy in each cycle permits simple digital correction of any offset in the comparators. The detail will follow in the next chapter.

4. Pipelined ADC
Pipelined ADCs are similar to algorithmic converters, but employ multiple stages working on successive input samples simultaneously. Hence, they can complete a conversion on every clock cycle, providing higher throughput than algorithmic converters, but with the same latency.
Multiple bits can be resolved in each stage, with digital correction, in order to reduce the number of opamps in a pipelined converter and decrease the number of clock cycles required for each conversion.

5. Flash ADC
Flash converters are generally capable of the fastest conversion speeds of any ADC architecture. They convert analog to a digital signal by comparing the input with known reference values, and thus the more known references that are used in the conversion process, the more accuracy can be achieved. Therefore, their power consumption grows dramatically with the required resolution, so, they are usually reserved for converters where a high speed and low or modest resolution is sought.

2.2 ADC's Performance Characteristics

Some of the most commonly used terms for describing ADC's performances are defined below. [16].

Resolution
The resolution of an ADC is the total number of distinct analog levels corresponding to the different digital words. Thus, an N-bit resolution implies that the converter can resolve 2^N distinct analog levels. It cannot necessarily be an indication of the accuracy of the ADC, but instead it usually refers to the number of digital output bits.

Offset and Gain Error
An offset error is defined as the deviation of the output Vo from 1/2 LSB.The gain error is defined to be the difference at the full-scale value between the ideal and actual curves when the offset error has been reduced to zero.

Accuracy and Linearity
The absolute accuracy of a converter is defined to be the difference between the expected and actual transfer responses,and it includes the offset, gain, and linearity errors. The term relative accuracy is sometimes used and is defined to be the accuracy after the offset and gain errors have been removed.

Integral Nonlinearity (INL) Error
Integral nonlinearity is a popular measure of accuracy that specifies the deviation of a converter's input– output relationship away from the ideal, or least-squares fit, linear relationship.

Differential Nonlinearity (DNL)
Differential nonlinearity is defined as the variation in analog step sizes away from 1LSB typically, after the gain and offset errors have been removed.

Dynamic Range (DR)
The most common measure of accuracy at high input signal frequencies is dynamic range, often quantified by the maximum achievable signal to noise and distortion ratio (SNDR). The maximum input level in a system is limited by distortion whereas the minimum signal level that can be applied is limited by noise. This may be expressed in dB, or as an effective number of bits.

Chapter 3

Cyclic ADC Architectures

A cyclic ADC, also known as algorithmic ADC [2], is an evolution of pipelined ADC in which a single stage is reused for performing the remaining conversions. This makes the Cyclic ADC to achieve high resolution within a small die area. It operates in much the same way as a successive approximation converter (SAR) but, instead of halving the reference voltage in each cycle as in the SAR converter, the cyclic converter doubles the residue voltage while keeping the reference voltage unchanged [16]. Cyclic ADCs can be divided into two main categories: a 1-bit per cycle and multi-bit per cycle. In this chapter, the 1-bit and 1.5-bit cyclic ADC architectures are presented.

3.1 A 1-bit Cyclic ADC Architecture

The 1-bit cyclic ADC generates 1-bit at each conversion cycle and thus requires N clock cycles to complete the conversion. The block diagram of this 1-bit cyclic ADC [16] as shown in Fig. 3.1 below consists of a comparator, a digital to analog converter (DAC) switch, a summer and a multiply by two amplifier followed by a shift register.

At the beginning of the conversion, the input signal is first sampled and the sampled data V_{in} is compared to a threshold voltage in which a 1-bit digital output is generated. Depending on the value of this binary output, either a positive or negative reference voltage is selected by the DAC switch. Then a residue output voltage V_{i+1} is generated by subtracting the output of the DAC from the held input and amplifying it by two. For the next conversions, the residue voltage is fed back into the input node V_i. The cycle repeats for the same number of cycles as the desired number of bits, N, before starting a new conversion.

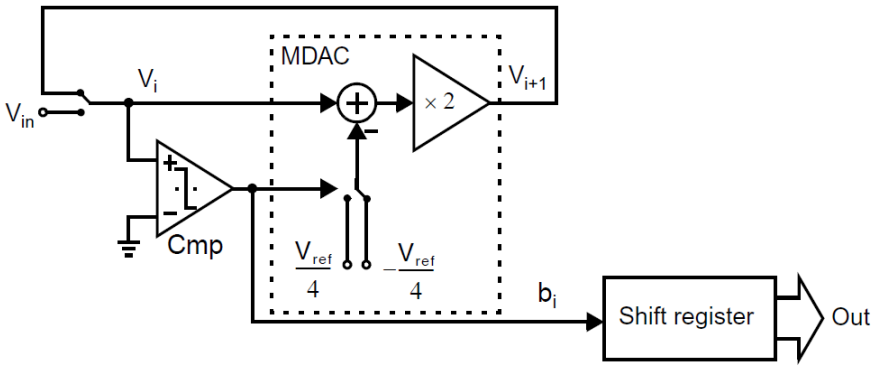

Figure 3.1: Cyclic/Algorithmic ADC block diagram

The flow graph for a signed algorithmic/cyclic conversion is shown in Fig. 3.2 below.
From the flowgraph, during the first cycle, the input voltage is sampled V_{in} and at the same time, it is compared to the reference voltage to generate a bit: b = 1 if $V_{in} > 0$, otherwise b = 0. This signal is passed to DAC switch, which generates the analog estimate of the comparator result. This estimate is subtracted from the signal that is held at the input to produce the analog residue voltage. This residue voltage is brought back to the full-scale reference level by a precise gain of two amplifier. The process is mathematically given by:

$$V_{(i+1)} = 2 \cdot V_{(i)} \pm \frac{V_{ref}}{2} \tag{3.1}$$

Where:

$V_{(i+1)}$ = is the output signal on i^{th} cycle
$V_{(1)} = V_{in}$ where V_{in} is the input signal
$\pm\frac{V_{ref}}{2}$ = the reference signal: subtract if $V_{(i)} > 0$ or add if $V_{(i)} \leq 0$

This 1-bit cyclic ADC suffers from comparator inaccuracies and loop offset errors [3]. The residue voltage must remain within the range of $[-V_{ref}, V_{ref}]$ to ensure convergence. Any shift in these values results in comparator offsets. In addition, the loop-offset errors also add up as a partial reminder at each conversion cycle. The other difficulties of such converters to achieve a high-precision result is the need of an accurate multiply-by-two gain amplifier. These errors can cause missing codes, integral and differential nonlinearities and as a result, the performance of the convertor degrades.

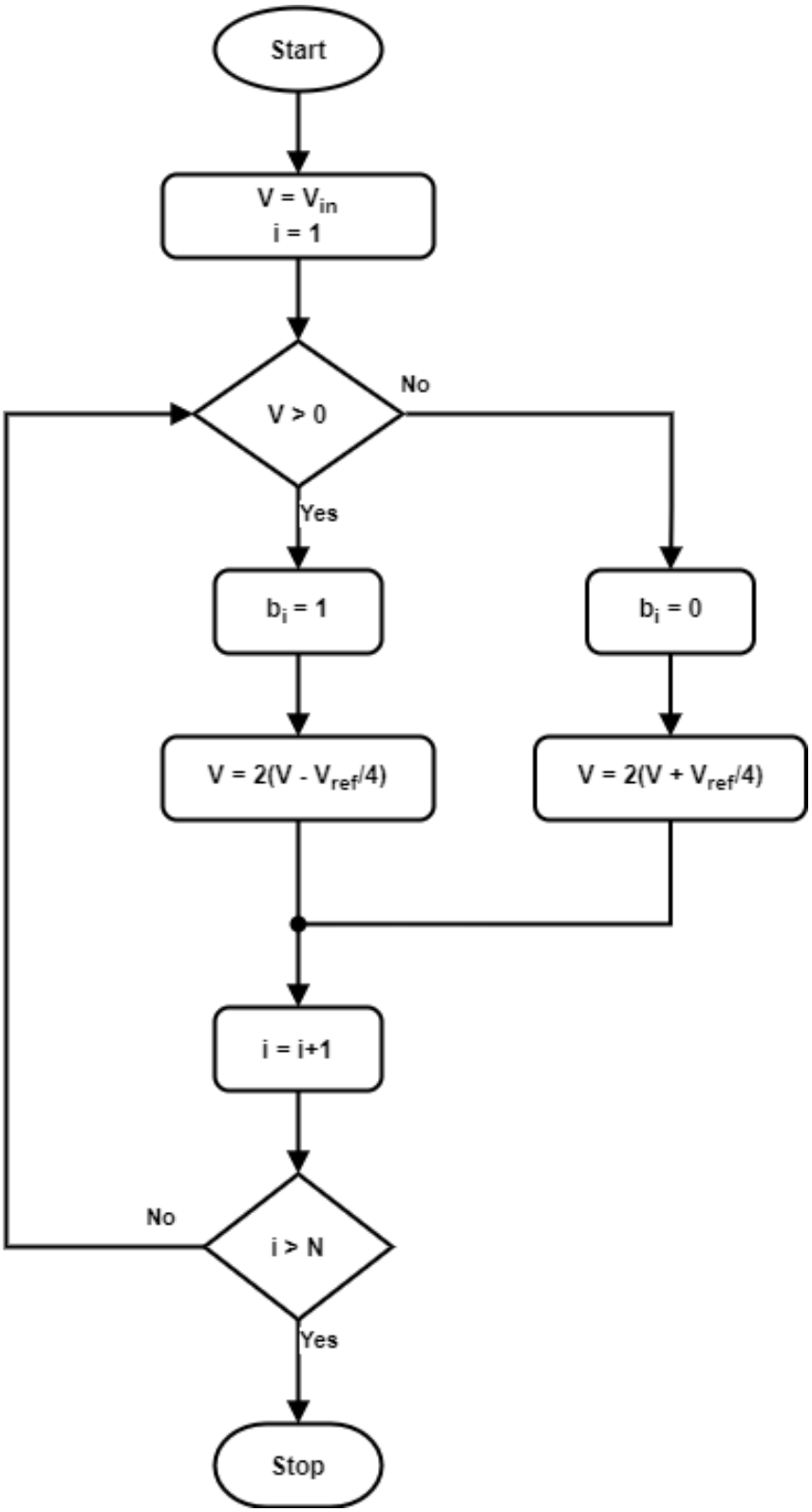

Figure 3.2: Flow diagram for 1-bit algorithmic converter(signed input)

3.2 A 1.5-bit Cyclic ADC Architecture

The 1.5-bit per phase architecture, which is often referred to as Redundant Signed Digit (RSD) Algorithm [2], is the most popular ADC type that employs a digital error correction algorithm to overcome the effects of comparator and loop offsets by introducing a second redundant comparator. This gives the sub-ADC three possible digital output codes (00, 01, 11), resulting in a 1.5bit per cycle (i.e $log_2(3) \approx 1.5bit$). [16]

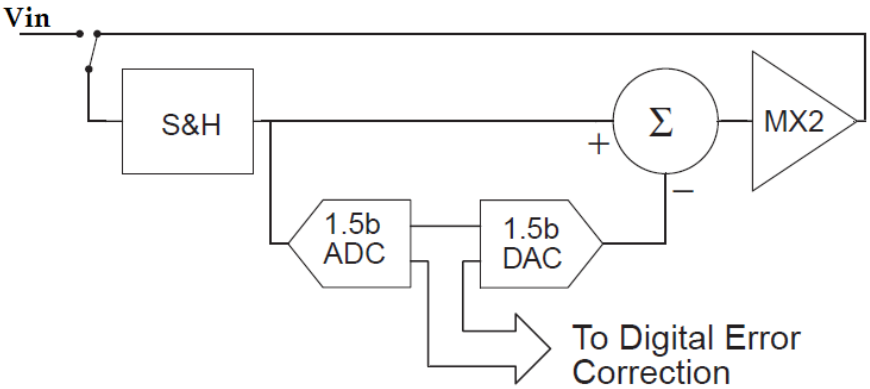

Figure 3.3: A 1.5 bit Cyclic ADC block

The 1.5-bit cyclic ADC stage shown in Fig.3.3 consists of a 1.5-bit sub-ADC and sub-DAC, a sample-and-hold (S/H), a summer and multiply-by-2 (MX2) blocks. The last three blocks listed above are later replaced by a single Switched Capacitor (SC) circuit.

3.3 The Operation of a 1.5-bit Cyclic ADC

The flow diagram of the 1.5-bit Cyclic ADC [2] is shown in Fig. 3.4 below.
The operational principle of the 1.5-bit algorithm is similar to the 1-bit converter but this time the sub-ADC has an additional comparator and its output becomes 2 bits, causing the sub-DAC output to have three different reference levels.
During the initial cycle, the input signal is sampled and compared with the two comparators' threshold voltages, $\pm\frac{V_{ref}}{4}$ and generate two bit codes. Depending on the combination of the codes generated, the sub-DAC connects to the corresponding reference voltages with the help of digital circuits. The resulting reference voltage is then summed to the input signal from the S/H. The result is then amplified (x2) to generate the residue voltage, which will be fed-back to the S/H for the next conversion cycle. This output residue voltage on the i^{th} cycle is expressed analytically by 3.2 [13] below.

$$V_{i+1} = 2 \cdot V_i + \mathbf{D}_i \cdot V_{ref}, \quad \mathbf{D}_i = \begin{cases} 1 & V_i \leq -\frac{V_{ref}}{4} \\ 0 & -\frac{V_{ref}}{4} < V_i \leq \frac{V_{ref}}{4} \\ -1 & V_i > \frac{V_{ref}}{4} \end{cases} \quad \text{i=1,2,... N} \tag{3.2}$$

Where:

$i =$ denotes the i^{th} conversion cycle
$V_{(i+1)} =$ the output signal on i^{th} cycle
$V_{(1)} = V_{in}$ where V_{in} is the input signal
$V_{ref} =$ the reference signal:
$N =$ denotes the resolution

The value of D_i in Eq.3.2 is determined by the three possible sub-ADC output codes which are either '00', '01' or '11', i.e. Di=1 when the output codes are '00', Di=0 when '01' and Di=-1 when '11'. The above process repeats until the last bit conversion is complete. Then, the two bits from sub-ADC outputs at the end of each clock phase are shifted til the end of the conversion and then, synchronized to have the final output bit in parallel in the form of an N-bit standard binary code.

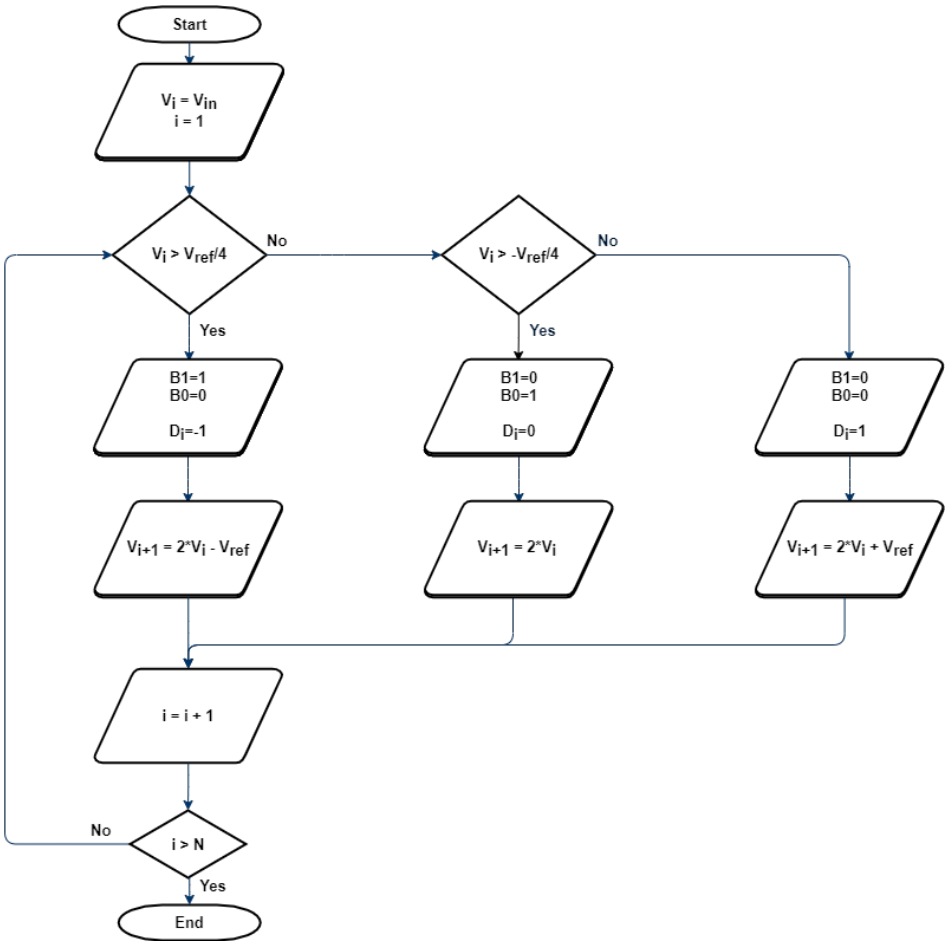

Figure 3.4: Flow diagram for 1.5-bit algorithmic converter

3.3.1 Mathematical Example

Assuming an input voltage $V_i = 0.8V$, the sub-ADC binary outputs, the corresponding sub-DAC reference voltage and its residue voltages are calculated as in the Table 3.1 below.

For an input range (peak-to-peak) $V_{pp} = 1V$, which is also referred to as the reference voltage V_{ref}, the threshold and reference voltages are computed as follows.

The sub-DAC outputs are:
Assuming the signal ground V_{cm} at:

$$V_{cm} = 0.9V,$$
$$V_{RH} = \frac{V_{ref}}{2} + V_{cm} = 0.5 + 0.9 = 1.4V$$
$$V_{RL} = -\frac{V_{ref}}{2} + V_{cm} = -0.5 + 0.9 = 0.4V$$

The sub-ADC's threshold voltages V_{th} values are:

$$V_{thH} = \frac{V_{ref}}{4} + V_{cm} = 0.25 + 0.9 = 1.15V$$
$$V_{thL} = -\frac{V_{ref}}{4} + V_{cm} = -0.25 + 0.9 = 0.65V$$

The new peak-to-peak input range of $V_{PP} = 1V$ is:

$$\begin{aligned} V_{pp} &= [-0.5, 0.5] \\ V_{pp-new} &= [-0.5 + 0.9, 0.5 + 0.9] \\ &= [0.4, 1.4] \end{aligned}$$

For this example, the unsigned input voltage $V_i = 0.8V$, where the input range is 0 to 1V, can be projected into the new input range 0.4 to 1.4V as:

$$V_{i-new} = 0.8V + 0.4V = 1.2V$$

The output residue voltage V_{res} is computed as:

$$\begin{aligned} V_{res} &= 2 \cdot V_i + \mathbf{D}_i \cdot V_{ref} \\ &= 2V_i - V_{DAC} \end{aligned}$$

Where: $\mathrm{V}_{DAC} = \begin{cases} V_{RL} = 0.4, & D = 1 \\ V_{CM} = 0.9, & D = 0 \\ V_{RH} = 1.4, & D = -1 \end{cases}$

The resulting outputs for the 14 cycles are shown in Table 3.1.

Table 3.1: A 1.5bit cyclic ADC

Cycle	Vi	sub-DAC	$\mathrm{V}_{res} =$	sub-ADC	
		V_{DAC}	$2\mathrm{V}_i - V_{DAC}$	B1	B0
1	1.20	1.40	1.00	1	0
2	1.00	0.90	1.10	0	1
3	1.10	0.90	1.30	0	1
4	1.30	1.40	1.20	1	0
5	1.20	1.40	1.00	1	0
6	1.00	0.90	1.10	0	1
7	1.10	0.90	1.30	0	1
8	1.30	1.40	1.20	1	0
9	1.20	1.40	1.00	1	0
10	1.00	0.90	1.10	0	1
11	1.10	0.90	1.30	0	1
12	1.30	1.40	1.20	1	0
13	1.20	1.40	1.00	1	0
14	1.00	0.90	1.10	0	1

From Table 3.1, the serial sub-ADC binary outputs B1 and B0 (B1 is the output from comparator with threshold voltage V_{RH} and B0 from the other comparator with threshold value of V_{RL}) are fed into the Digital Error Corrections (DEC) circuit comprising of shift registers and full adders to perform the serial to parallel bits conversion.

The outputs from all the cycles at which Cycle-1 to Cycle-14 represents the MSB to the LSB are delayed by shift registers to re-align the bits[16] so that the full adder performs the addition starting from the LSB(D0). Table 3.2 below shows the arithmetic operation of the DEC on the serial sub-ADC's binary outputs B1 and B0, where B0 is shifted so that B1(t) is added to B0(t+1) for all except the MSB (D13) bits.
The last bit of the sub-ADC binary output B0, which is represented as 'X' in Table 3.2, is ignored since we used both comparators to generate the 1.5bits for all the conversions, instead of using a separate 1bit sub-ADC for the last cycle as explained in [13].

Table 3.2: A 14-bit cyclic ADC output for $V_i = 1.2V$

sub-ADC output		Cyclic ADC	
B1	B0	Output	
1		**1**	D13 (MSB)
0	0	**1**	D12
0	1	**0**	D11
1	1	**0**	D10
1	0	**1**	D9
0	0	**1**	D8
0	1	**0**	D7
1	1	**0**	D6
1	0	**1**	D5
0	0	**1**	D4
0	1	**0**	D3
1	1	**0**	D2
1	0	**1**	D1
0	0	**0**	D0 (LSB)
	1	'X'	

Therefore, the 14-bits binary output corresponding to the input voltage $V_i = 1.2V$, where D13 is the MSB and D1 is the LSB, is '**11001100110010**'.

The simulation result for the input voltage $V_{in} = 1.2V$ is presented in Section 5.1.2 and the complete working procedures/algorithm in python code is attached in Appendix.

3.4 The Switched Capacitor (SC) Implementation

The basic building blocks of a SC network are: capacitors, opAmp, switches, and two-phase non-overlapping clocks. The multiply by two(amplification) of the cyclic ADC is the most important part that requires high accuracy to perform a precise conversion. The design of an opAmp that can perform this type of amplification is not realistic. The SC network is a popular and effective way of combining both the multiplication and subtraction modules of the converter.The SC Multiplying Digital-to-Analog Converter (MDAC) [8, 14] circuit combines the functions of DAC, S/H Amplifier, and subtracter and is therefore a good solution to perform both the digital-to-analog conversion and the subtraction of the resulting analog output from the analog input and multiplication by two.

The MDAC typically operates in a multi-phase clocking scheme, it samples the analog input signal during the first phase and then subtracts the analog output signal from the analog input signal during a second phase of the clock.
The MDAC performs both the sampling and the subtraction using either the same or different capacitors depending on the MDAC topology used. Moreover, SC circuits depend on the ratio of the capacitors and not on the absolute values of each capacitor, exceptions are when the ratios are not even necessary in the case of [9, 10]. Some of the different types of MDAC topologies [7] are described as follows.

3.4.1 Non-Flip-around topology

This topology is also called a Charge-redistribution (CR) MDAC and is shown in the Fig 3.5 [14]. The input signal is sampled on the Cs capacitor during the track phase, and transfers only the differential charge to the feedback capacitor during the hold phase.
During clock phase $\phi 1$, the input is sampled onto the Cs capacitor, and the feedback Cf capacitor is reset. On $\phi 2$, the Cs is connected to the Vref and Cf capacitor is connected to the output as a feedback.

Voltage multiplication by 2 occurs (C -> 2C) with the charge transfer of Q = Vo.2C of capacitor Cs=2C to the feedback capacitor Cf=C; initially discharged, via a virtual earth node to become 2Vo. This method is sensitive to the ratio of capacitors Cs/Cf.

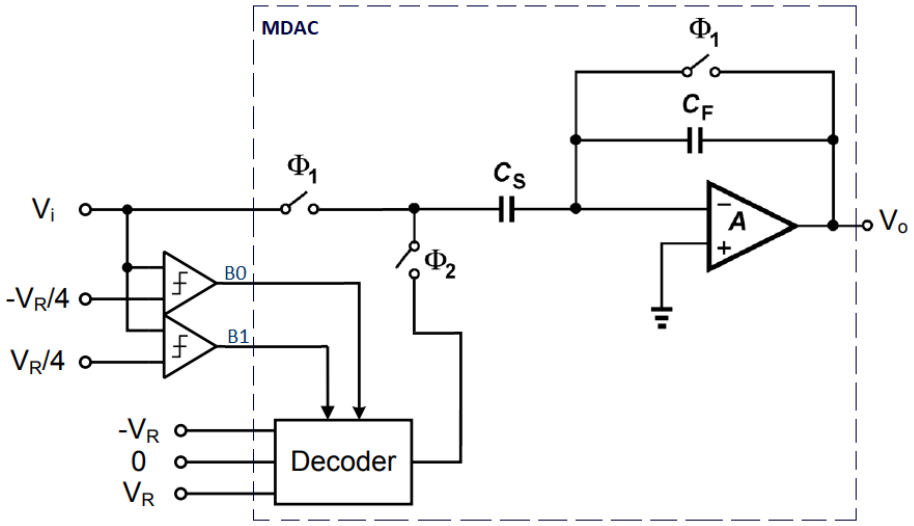

Figure 3.5: Non-Flip-around topology

3.4.2 Flip-around topology

The flip-around MDAC, which is an adaptation of the CR above, is the most widely used topology to perform the two mathematical operations, multiply by two and subtraction, of an algorithmic converters.
The input signal is first sampled on both C1 and C2 capacitors during the track phase, $\phi 1$, and then C1 capacitor flips to the output node while C2 is connected to either of $\pm V_{ref}, or 0$ during the hold phase, $\phi 2$, depending on the comparator outputs from the previous cycle.

This type of topology is also called a charge transfer with flip-around (C -> C), where both C1=C and C2=C are pre-charged with Vo; after which the charge on C2 is transferred to C1. A half a bit of extra accuracy can be achieved with the C -> C circuit compared to the C->2C circuit but in practical applications no better than 10 bits accuracy [13] is achieved in a standard CMOS processes.
There are two advantages of the flip-around architecture [17, 18]. The first advantage is lower power consumption. The second one is lower noise, the input-referred noise power reduction.

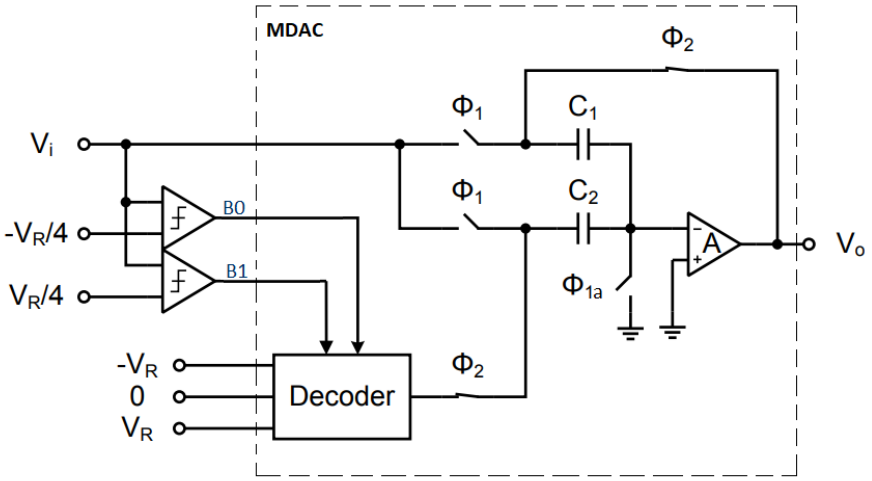

Figure 3.6: Flip-around topology

3.4.3 Capacitor matching insensitive topology

A new voltage adder concept (C + C), which is a new MX2 function [13], is based on a voltage addition. Capacitors can be used for addition, as demonstrated in Fig. 3.7, where instead of multiplying Vo by 2, voltage addition occurs by first charging each of capacitors C1 and C2 to Vo and then placing these capacitors end to end, with say the bottom plate of C2 connected to the top plate of C1.
Furthermore, to fulfill the 1.5-bit DAC function, the output can be easily level shifted by adding a voltage at bottom plate of C1.

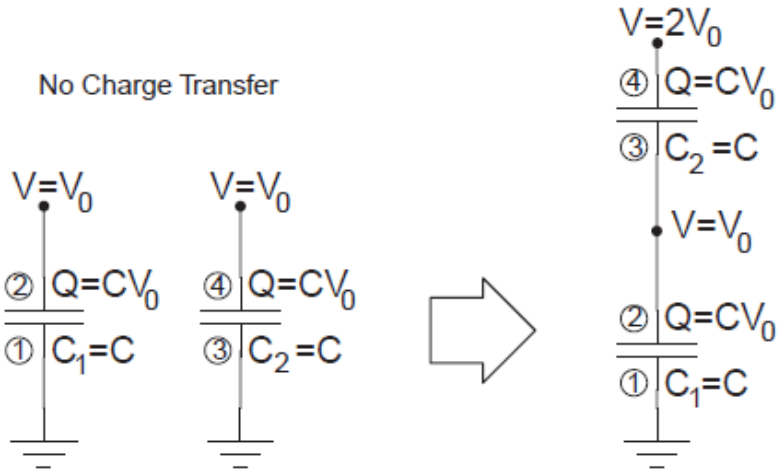

Figure 3.7: Voltage adder C+C [13]

Due to the parasitic coupling capacitance [9] on both terminals of C1 and C2, there is an inaccuracy in the MX2 function and therefore, the direct implementation of the C+C concept is only suitable for lower resolution ADCs of less than 8 bits.

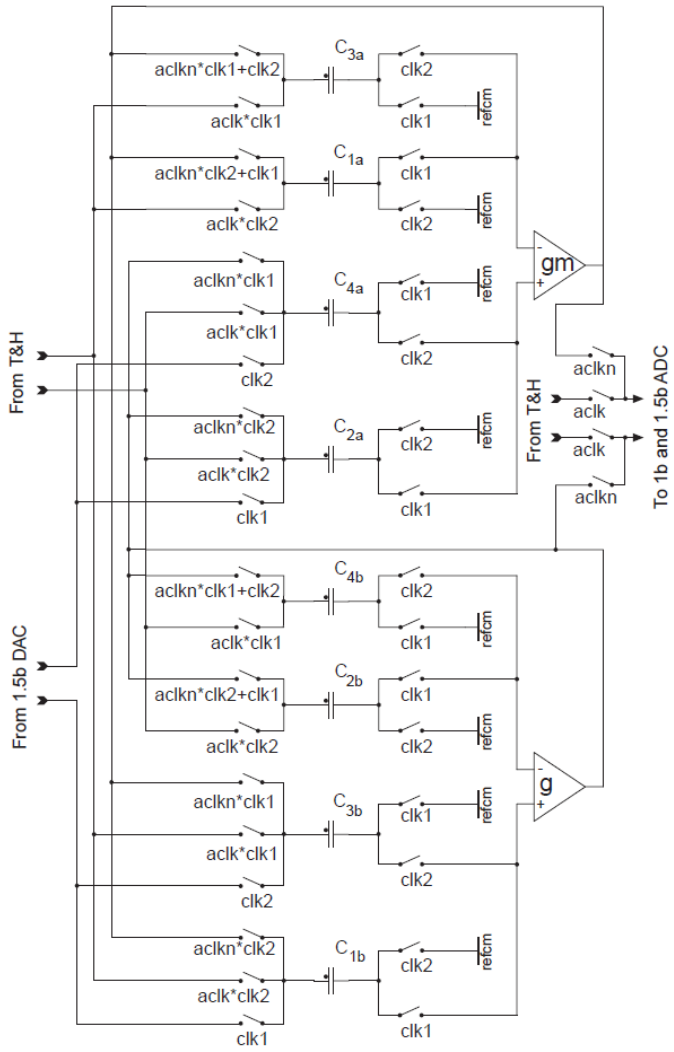

Figure 3.8: Capacitor matching insensitive C+C topology [13]

3.4.4 3-Caps topology

The 3-cap technique [5] is a modification of the flip-around configuration presented in the Section 3.4.2 above in which the capacitors are rearranged so that the opamp is used efficiently during both clock phases of the SC. Because of the fact that the the SC stage is not utilizing the opamp during the sampling phase, one can use the opamp for other operation(either sampling or amplification), by connecting an additional capacitor during the other clock phase. This makes the opamp to be used effectively in both clock phases resulting in not only the reduction of conversion time by half, but also saving both die area and power consumption.

This modification [4] also results in a considerable reduction of the opamp's load capacitance.

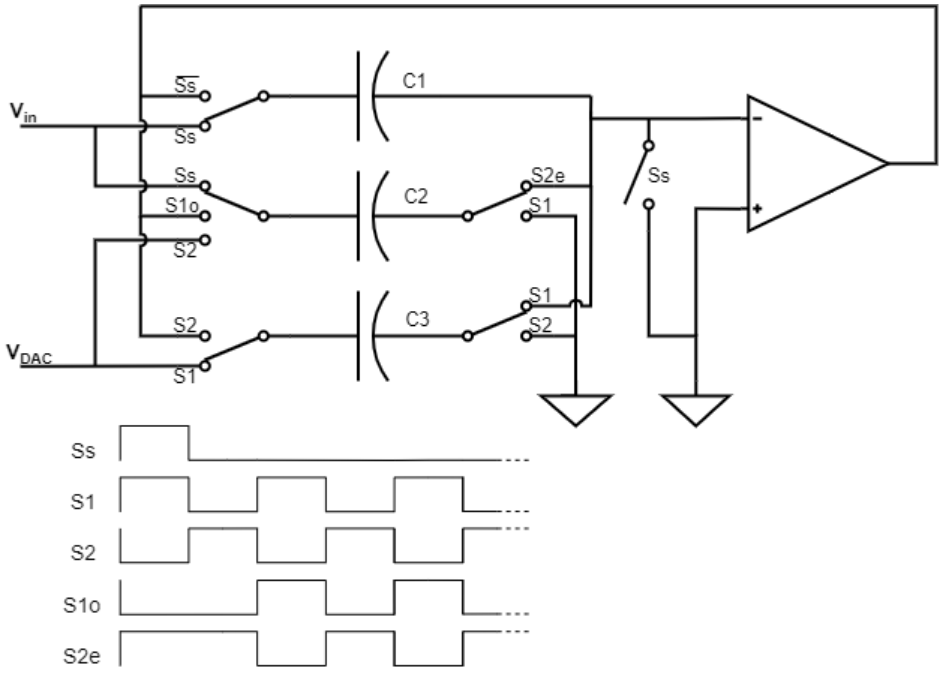

Figure 3.9: 3-Caps topology

The 3-caps topology operates in three different phases/stages to complete the conversion.

i) Initialization Phase
At the beginning of the conversion, V_{in} is sampled over C_1 and C_2 and C_3 is connected to the sub-DAC output, which is not yet computed. Therefore, the charge stored on these sampling capacitors is calculated as:

$$Q_{C1} = V_{in} \cdot C_1$$
$$Q_{C2} = V_{in} \cdot C_2$$

The total charge on both capacitors is:

$$\begin{aligned} Q_S &= V_{in} \cdot C_1 + V_{in} \cdot C_2 \\ &= V_{in} \cdot (C_1 + C_2 \\ &= 2 \cdot V_{in} \cdot C, \quad \text{Since } C_1 = C_2 = C \end{aligned} \tag{3.3}$$

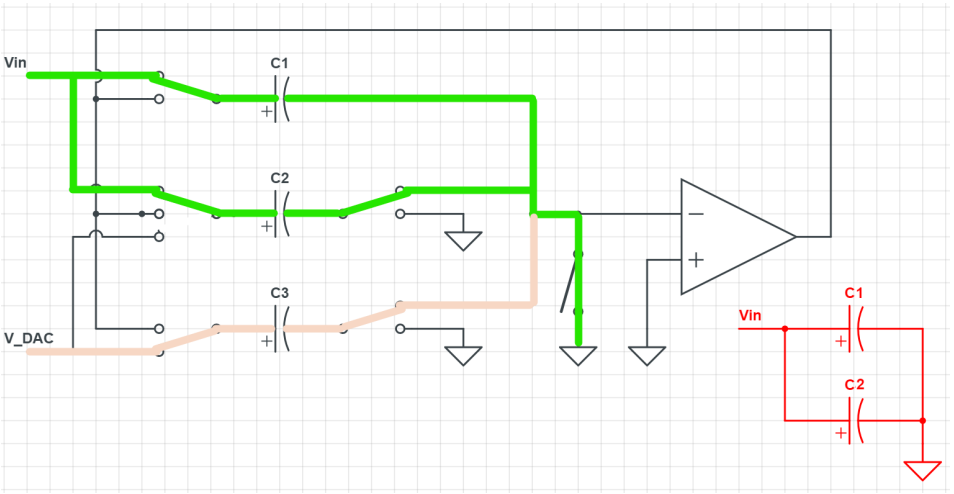

Figure 3.10: 3-Caps topology - initial state

ii) Even Phase

The input signal is disconnected from the MDAC circuit and instead the residue and the sub-DAC output computed in the previous initialization phase are connected. Capacitor C1 is connected to the opAmp output as a feedback while V_{DAC} is connected to C2 and the residue connected to C3. The Subtraction and amplification (Mx2) is performed on capacitors C1 and C2 while the resulting residue, at the same time, is sampled on C3.

$$\begin{aligned} Q_H &= V_{DAC} \cdot C_2 + V_{res(i+1)} \cdot C_1 \\ &= C \cdot (V_{res(i+1)} + V_{DAC(i)}) \end{aligned} \tag{3.4}$$

By conservation of charge and Eq. 3.3 and 3.4,

$$\begin{aligned} Q_H &= Q_H \\ C \cdot V_{in} &= C \cdot (V_{res(i+1)} + V_{DAC(i)}) \\ V_{res(i+1)} &= 2 \cdot V_{in} - V_{DAC(i)} \end{aligned} \tag{3.5}$$

In a similar manner, the charge on C3, on which the residue output is being sampled is:

$$Q_{C3} = V_{res(i+1)} \cdot C_3$$

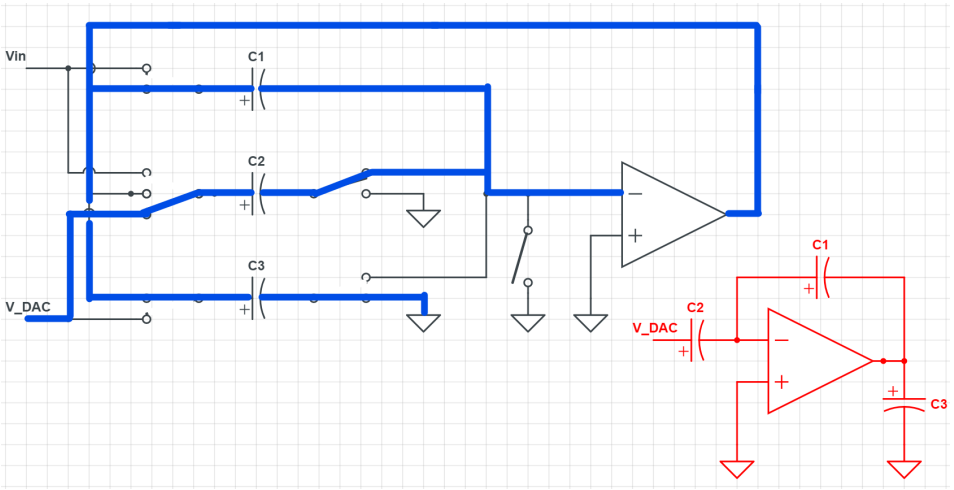

Figure 3.11: 3-Caps topology - even state

iii) Odd Phase
During this conversion phase, capacitors C2 and C3 interchange their purpose while C1 is kept as feedback capacitor. i.e. amplification is carried out using C1 and C3 capacitors and the resulting residue output, Vres,is sampled on and C2.
In the same way as the even phase above and since $C_1 = C_2 = C$,

$$V_{res(i+2)} = 2 \cdot V_{res(i+1)} - V_{DAC(i+1)}$$

Similarly, the charge on the residue sampling capacitor C2 will be:

$$Q_{C3} = V_{res(i+2)} \cdot C_2$$

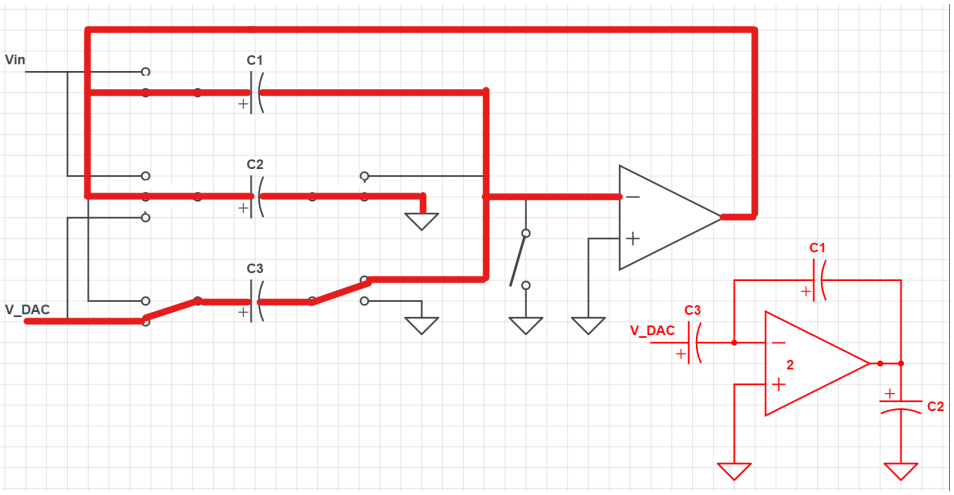

Figure 3.12: 3-Caps topology - odd state

The even and odd phases repeat until the start of the next conversion cycle, at which the initialization phase begins again.

The topologies presented in section 3.4.1 and 2 are capacitor ratio dependant while the 3rd one is capacitor matching incentive at the cost of conversion speed degradation for higher resolution[9, 10, 16].
The last one, 3-caps, is selected because of its low power and improved conversion clock by half, in addition to the capacitor mismatch cancellation scheme [2, 9] introduced by interchanging the functions of the two capacitors, C2 and C3, without any extra clock phases and hardware. The next chapter presents the implementation of the selected topology.

Chapter 4

A 1.5-bit Cyclic ADC Design and Implementation

4.1 System Level Design

4.1.1 1.5-bit Cyclic ADC Block Diagram

Fig. 4.1 shows the block diagram of the prototype cyclic ADC. The main building blocks comprises the cyclic ADC core, S/H, non-overlapping clock generator, and Digital Error Correction (DEC) logic. Each blocks are presented in the following sections.

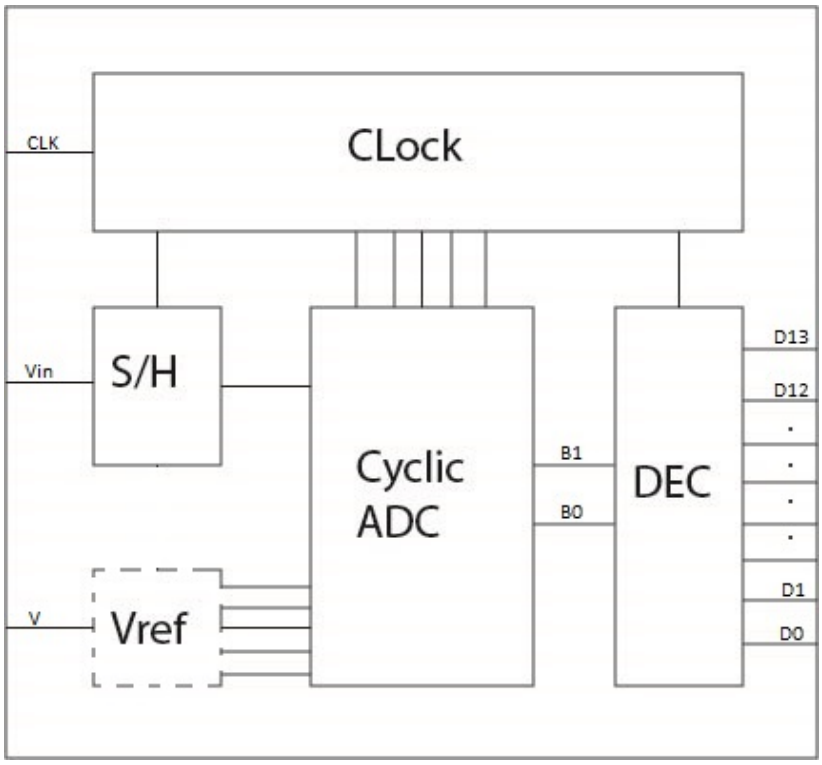

Figure 4.1: 1.5-bit Cyclic ADC Block Diagram

4.2 Sample and Hold (S/H)

An important analog building block, especially in data converter systems, is the sample and hold circuit. The use of a S/H (at the front of data converters) can greatly minimize errors due to slightly different delay times in the internal operation of the converter.
The simplest S/H circuit that can be realized using a CMOS technology was analyzed. It consists of a basic NMOS transistor switch (M1) and a dummy switch (M2) as shown in Fig.4.2. The addition of the dummy switch, which has a width one-half of the main NMOS switch, is used for clock-feedthrough cancellation [16].

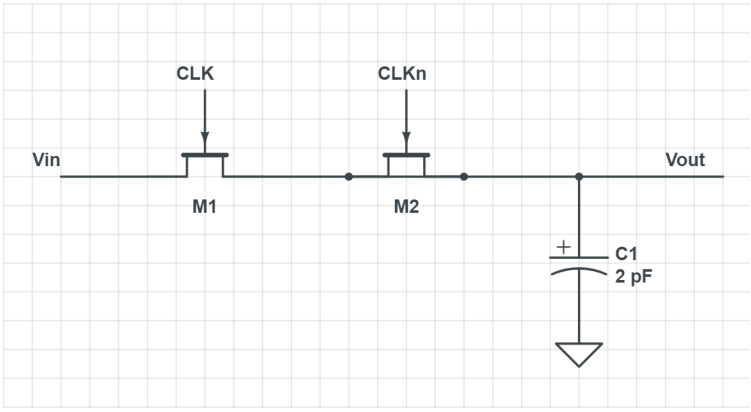

Figure 4.2: An open loop sample and hold circuit

The Switched Capacitor circuit used in this project does the sampling itself and makes a separate S/H circuit unnecessary.

4.3 Cyclic ADC

The 1.5-bit Cyclic ADC core block shown in Fig. 4.3 is composed of sub-ADC, Latch, sub-DAC, and Switched Capacitors circuits. The design of each blocks are explained in the following subsections.

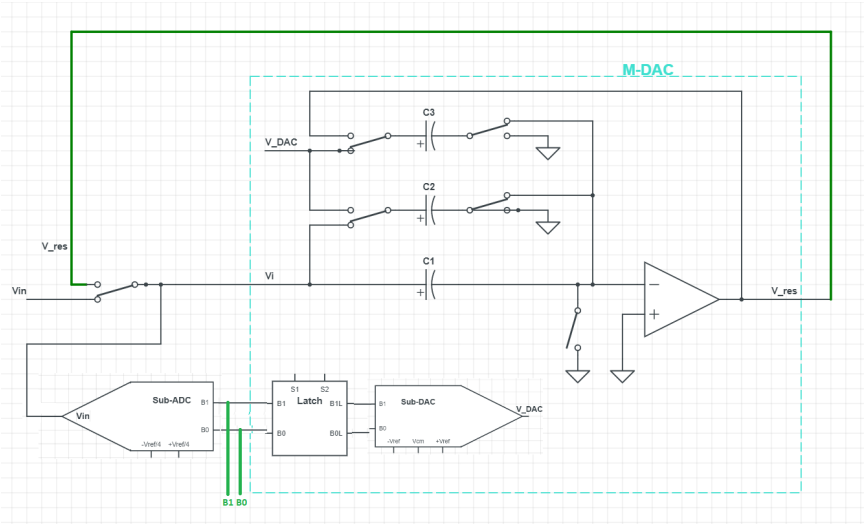

Figure 4.3: Cyclic ADC core

4.3.1 1.5bit Sub-ADC

Comparators are electrical circuits that compare two analog signals and output a binary signal based on the comparison, and thus called a decision-making circuits. They are one of the principal blocks of ADCs for the computation of the binary outputs.
Since the 1.5bit cyclic ADC does not require a high precision comparators, a simple three stages comparator is used in this project to keep the circuit less complex and compact. The first stage is a differential pair amplifier with an active load of pFET current mirrors. The second stage is a common source amplifier, which is used to boost the gain. The third stage is a buffer, which is an inverter, mainly converts the output of the decision circuit into a logic signals (GND=LOW or VDD=HIGH) and also increases the gain. The transistor level diagram of the comparator circuitry and its corresponding symbol is shown in Fig.4.4.

The sub-ADC is a combination of two comparators operating on two different threshold voltages so that two binary bits are generated as shown in Fig.4.5.

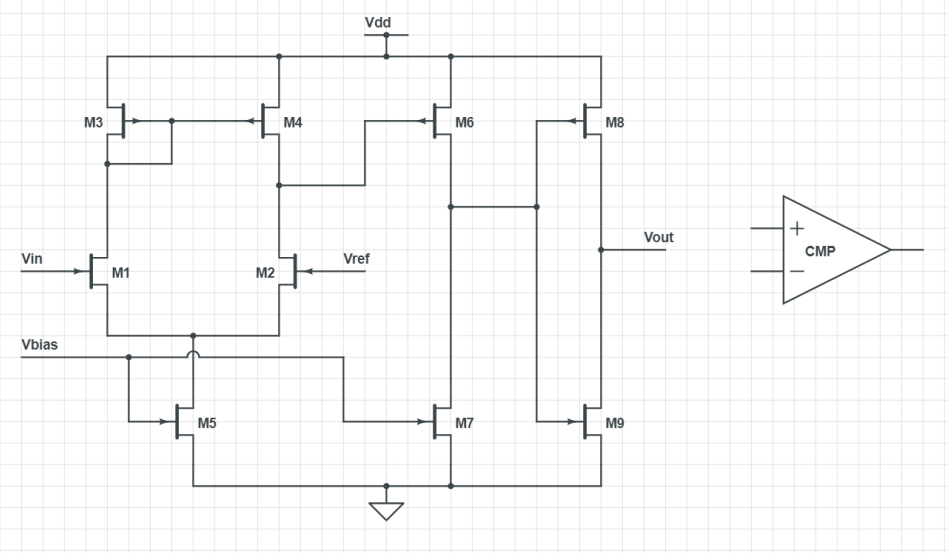

Figure 4.4: Three stage Comparator and its symbol

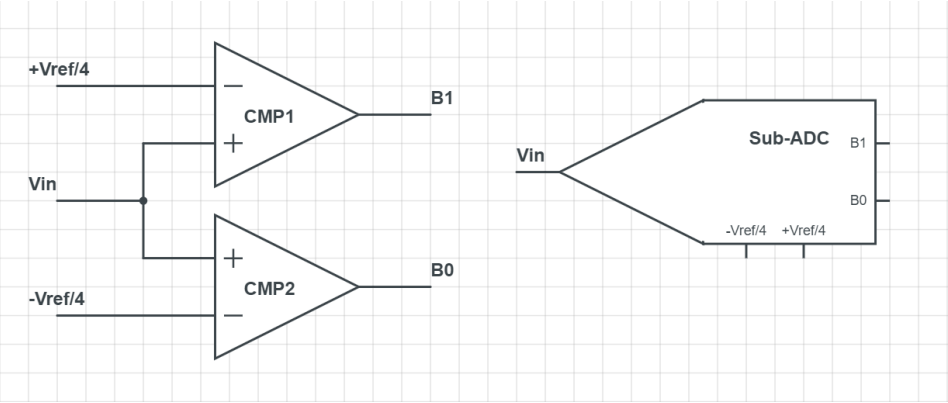

Figure 4.5: 1.5-bit sub-ADC and its symbol

The two bits generated by the sub-ADC above are then fed to a latch circuit, which holds the bits for one clock phase, and to the DEC block, after the '11'-bits are being adjusted to '10'-bits by resetting its least significant bit (LSB) using an XOR as shown in the Fig. 4.6 to make the full adder work properly.

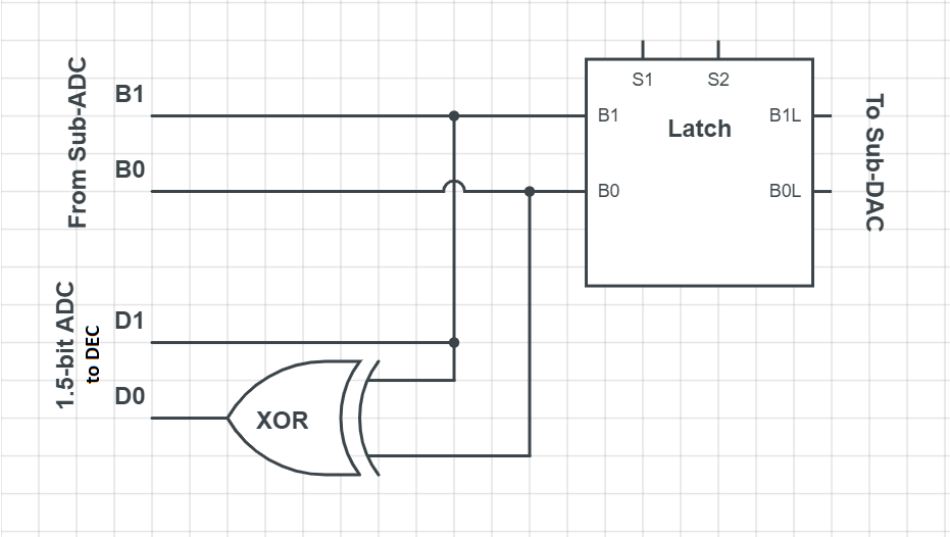

Figure 4.6: sub-ADC Latch

4.3.2 1.5bit Sub-DAC

The sub-DAC controls the voltage reference corresponding to the two bits generated by the sub-ADC after latched for one clock phase. The resulting voltage is then connected to the SC circuit for subtraction from the input signal hold at the sampling capacitor.

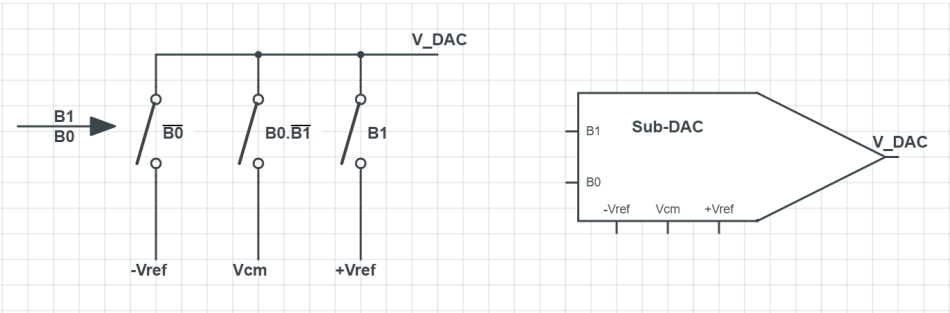

Figure 4.7: 1.5-bit sub-DAC and its symbol

4.3.3 Operational Amplifier (OpAmp)

Opamps are the most important building block in SC implementations for two basic tasks: 1) to accurately transport the signal charge from one capacitor to another capacitor and 2) to act as a buffer such that the voltage on the capacitors can be sampled without affecting the charge on the capacitors
To make the area consumption efficient, a very simple design of opamp, which is a two-stages amplifier [12] shown in Fig.4.8 is used. The first stage is a differential amplifier with an active load followed by the second stage

of a common source amplifier.

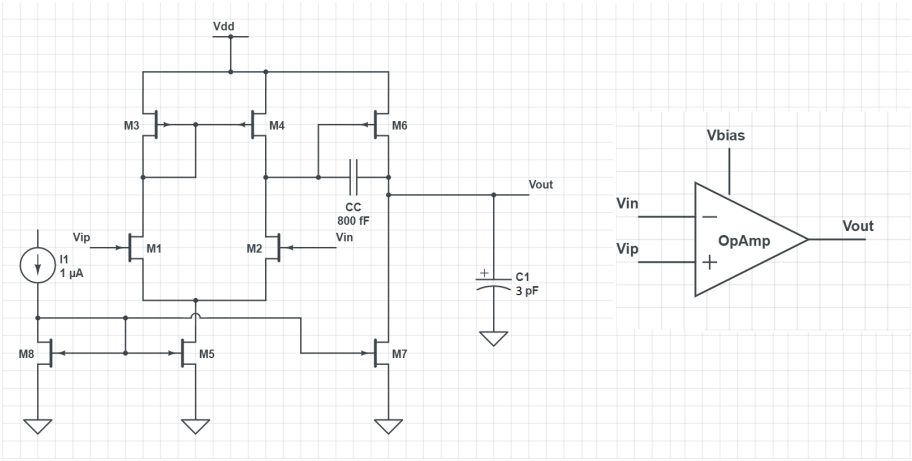

Figure 4.8: OpAmp and its symbol

4.3.4 Multiplying Digital-Analog Converter (MDAC)

The S/H, subtracter and amplifier components of the ADC are all replaced by a single SC circuit. The SC circuit is a combination of capacitors and an opamp interconnected by switches that are controlled by non-overlapping clock signals. The SC and sub-DAC circuits make the MDAC block which performs the arithmetic operations of the cyclic ADC. The MDAC interconnection of the proposed cyclic ADC is as shown in Fig. 4.9.

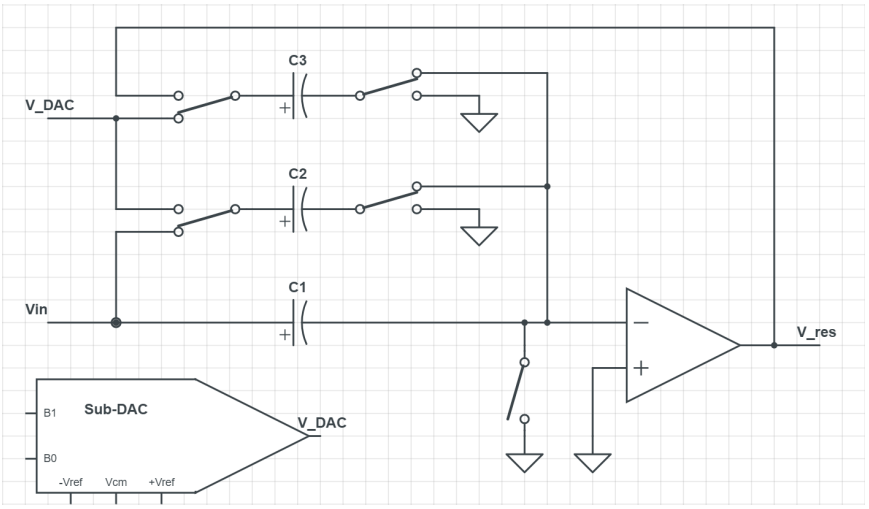

Figure 4.9: MDAC

4.3.5 CMOS Inverter

The basic CMOS inverter shown in Fig. 4.15 is used. Due to the weak mobility of PMOS transistors [15], the size(W/L) of the PMOS is taken to be 3 times wider than that of the NMOS transistor so that the inverter will have a symmetric transfer characteristic and equal current-driving capability in both pull-up and pull-down directions.

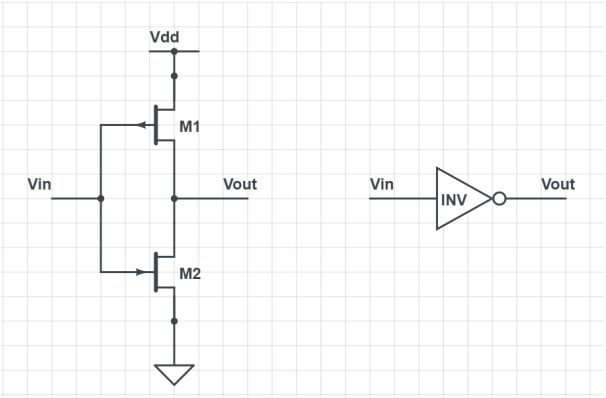

Figure 4.10: Inverter and its symbol

4.3.6 Transmission Gate (TGate) Switch

Most digital circuits' switches are realized by NMOS transistors because of their simplicity, circuit wise, and small silicon area. Despite these advantages, these kind of switches are exposed to signal-dependent charge injection and on-resistance variation resulting in signals distortion.

The transmission gate switch, which is a pair of complementary transistors connected in parallel as shown in Fig. 4.11, provides bidirectional current flow and exhibits an on-resistance that remains almost constant for wide ranges of input voltage. By keeping the size of the PMOS transistor the same as that of the NMOS transistor, then the charge injection due to each transistor will cancel when the transmission gate turns off.

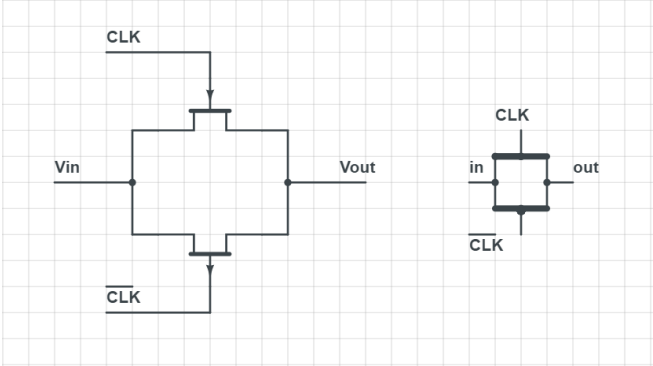

Figure 4.11: TGate-Switch and its symbol

4.4 Non-Overlapping Clocks

Non-overlapping clocks are the fundamental elements for switched capacitors to perform the basic functions: sampling, subtraction and amplification. The clock generator used in this project is shown in Fig. 4.12 below. The width of the inverter chains were adjusted to get the necessary delay that yields the required outputs.

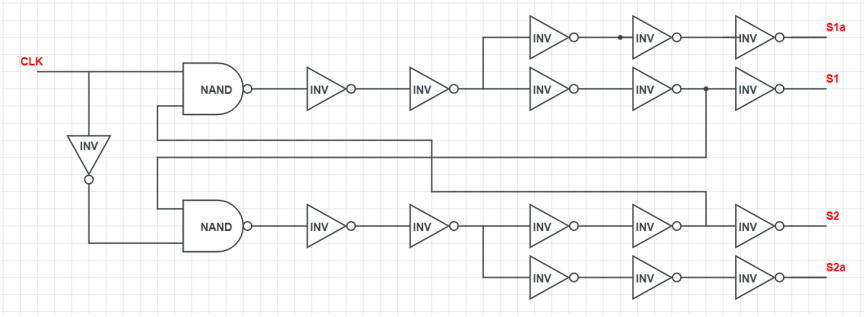

Figure 4.12: Non-Overlapping clock generator

4.5 Digital Error Correction (DEC)

The digital error correction logic has two main components: shift registers and full adder. The main goal of this block is code conversion, converting the two bits generated (1.5-bit) per phase into one bit and applying error correction which includes comparators and amplifier offsets, and amplifier gain error.

4.5.1 Shift Register

The two bits output from the sub-ADC are routed through a series of shift registers as shown in Fig. 4.13 to delay until the end of the conversion cycle.

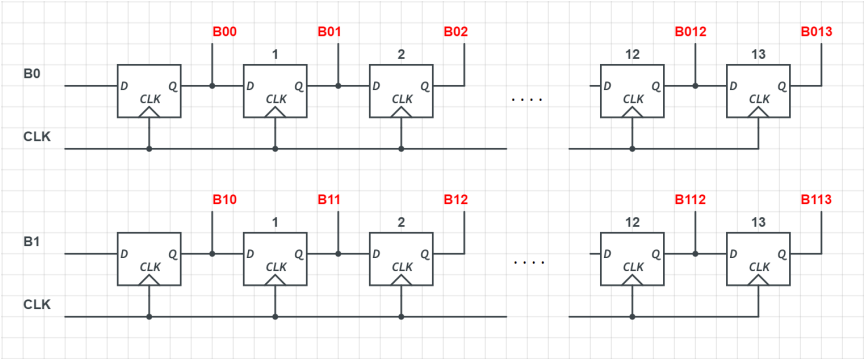

Figure 4.13: Shift Register

4.5.2 Full Adder

The full adder shown in Fig. 4.14 performs the code conversion and generates the final 14-bit output as explained in Section 3.3.1 above.

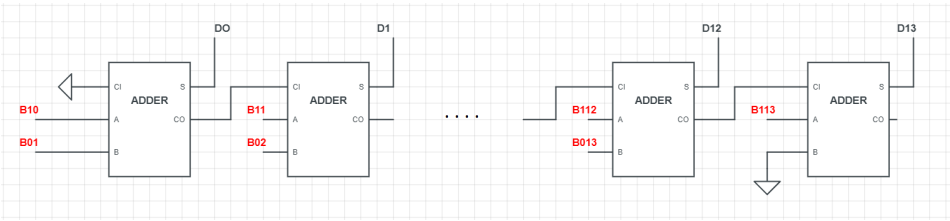

Figure 4.14: Full Adder

4.6 Implementation

The implementation of the designed ADC was not completed due to the limited resources during the current pandemic. From the whole system designed, the opamp used in this project was the only component that was taped-out and and sent for fabrication on a shared IC with another student. The fabrication of the chip is also delayed due to the pandemic and didn't return on the planned date. Therefore, the testing of the opamp is not carried out as planned.

The layout and the final chip sent for fabrication is shown in Fig. 4.15 to Fig.4.17 below.

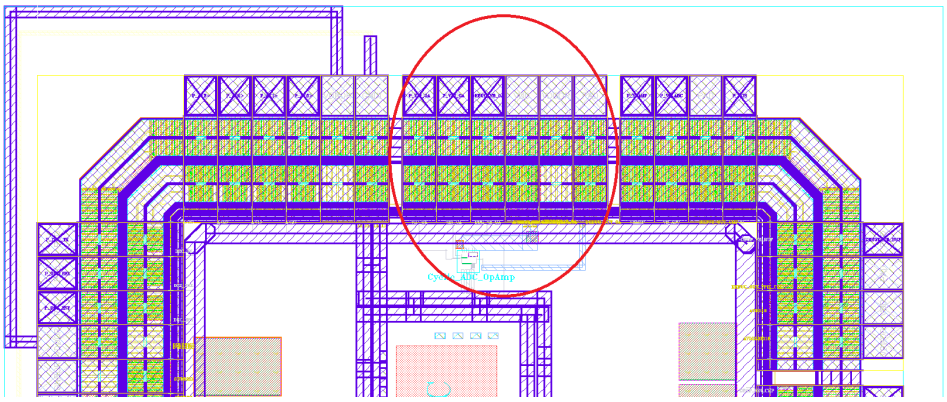

Figure 4.15: Portion of the Padframe corresponding to the OpAmp is circled in red

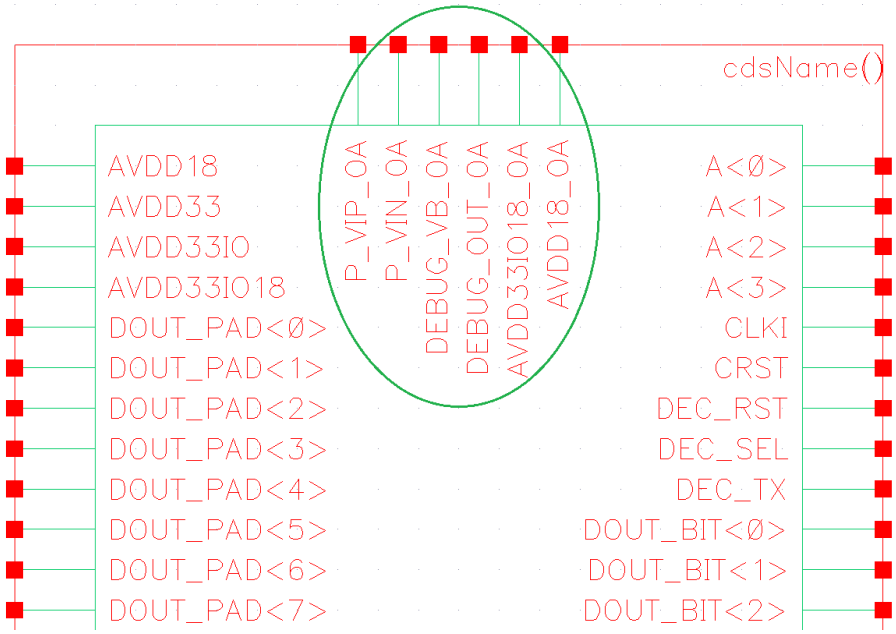

Figure 4.16: The OpAmp's pins on the chip are circled in green

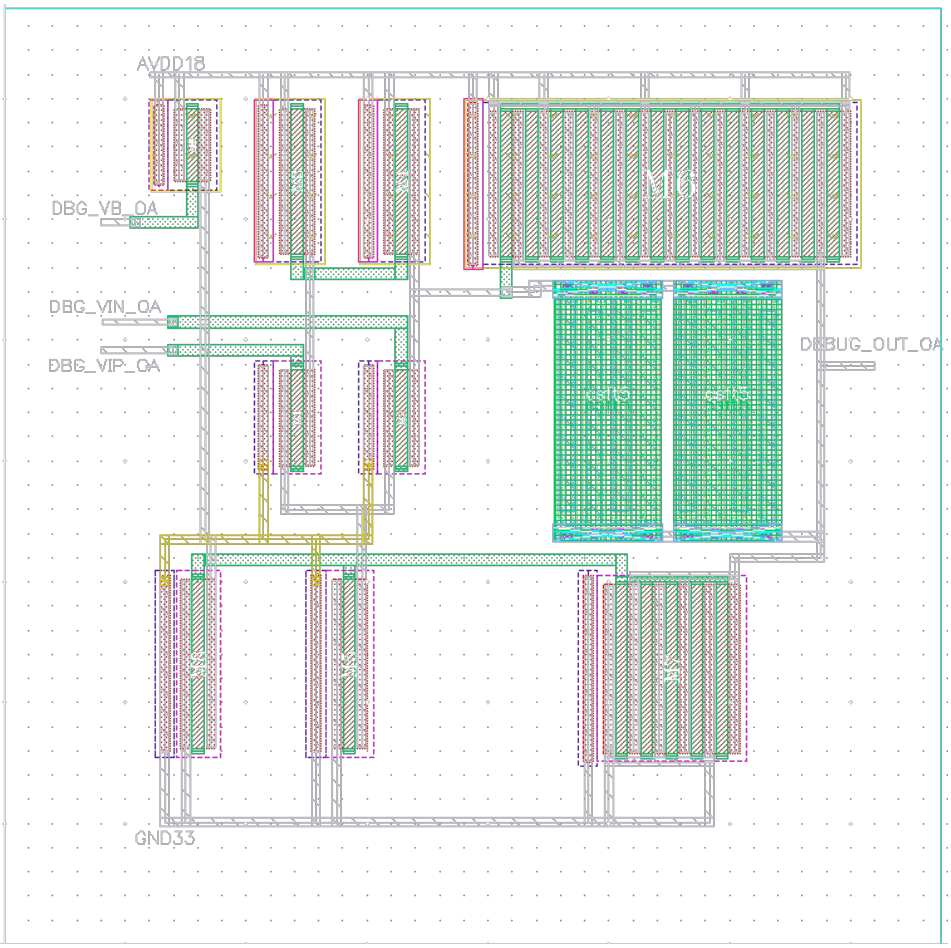

Figure 4.17: Layout of the OpAmp

Chapter 5

Simulation and Performance Evaluation

5.1 Cyclic ADC Simulation

5.1.1 OpAmp - AC Analysis

The opamp designed and used in the SC circuit has a gain of 61dB and a phase margin at 60°. A compensation capacitor, whose minimum value $C_c = 0.22C_L$ [12] is used to keep the phase margin at 60°. It has also a bandwidth of 20MHz as shown in Fig. 5.1.

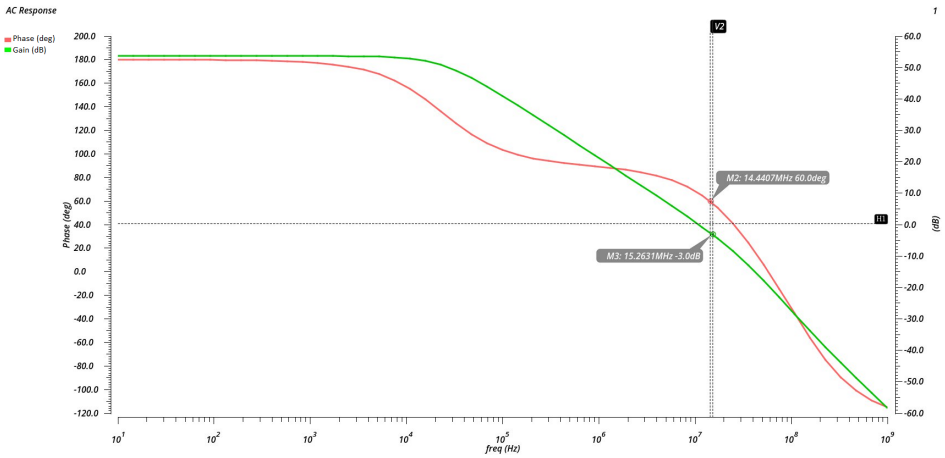

Figure 5.1: AC analysis of the opamp

5.1.2 Cyclic ADC - Transient Analysis

The clock signals used in the cyclic ADC are generated by the non-overlapping clock component and latching clock, which is provided from a direct voltage source. The clock signal for one complete conversion, i.e 14bit, is as shown in the Fig. 5.2. The CLKlat is used to delay the bits in the shift registers. The Ss is the sampling clock, 20kS/s, for the start of conversion and the S1 and S1o are the odd phase conversion clocks while the S2 and S2e are used for the even phase conversion. A non-overlap clock of 1ns delay was used.

Clock Signals

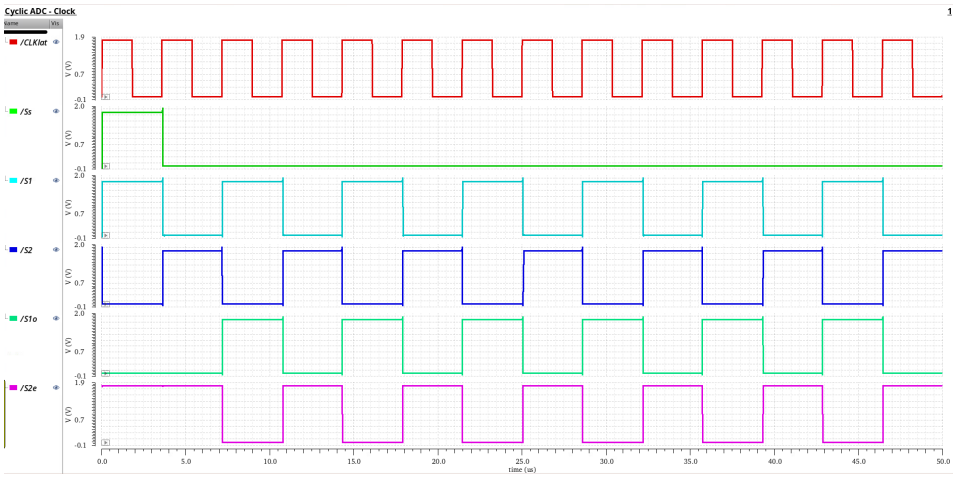

Figure 5.2: Non-overlapping Clock Signals

Clock signals and output bits

The example presented in section 3.3.1 for input voltage $V_in = 1.2V$ (circled in green) is presented in Fig. 5.3. The values enclosed in the red rectangle are the corresponding 14-bit output at which 1.8V represents the logic HIGH while the 4.3nV(0V) represents the logic LOW states.

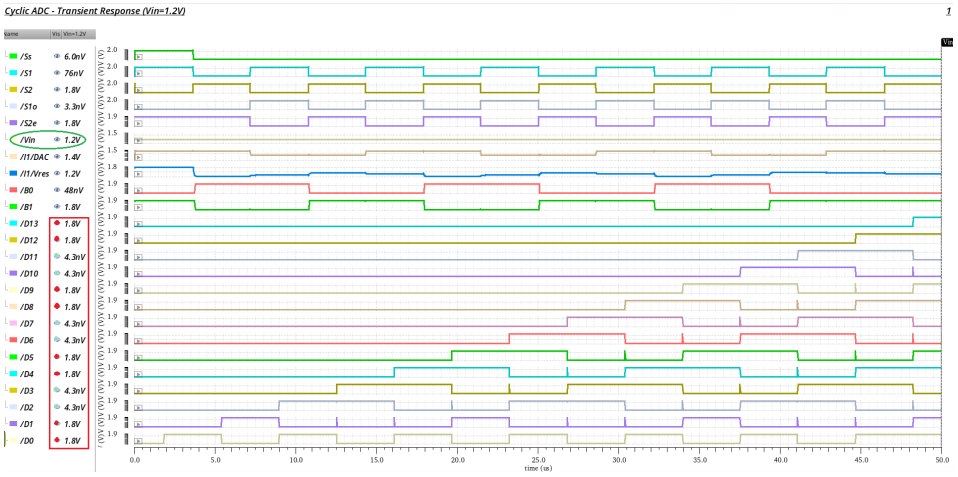

Figure 5.3: Clock signals and the 14bit output ($V_{in} = 1.2V$)

Residue voltage output per phase

The calculations presented in Table 3.1, its corresponding simulation results for an input voltage 1.2V is presented in Fig.5.4. The V_{DAC}, V_{res} and corresponding 1.5-bit sub-ADC outputs B0 and B1 for each conversion cycle are shown. Fig. 5.5 further shows the values of V_{res} outputs at each cycle.

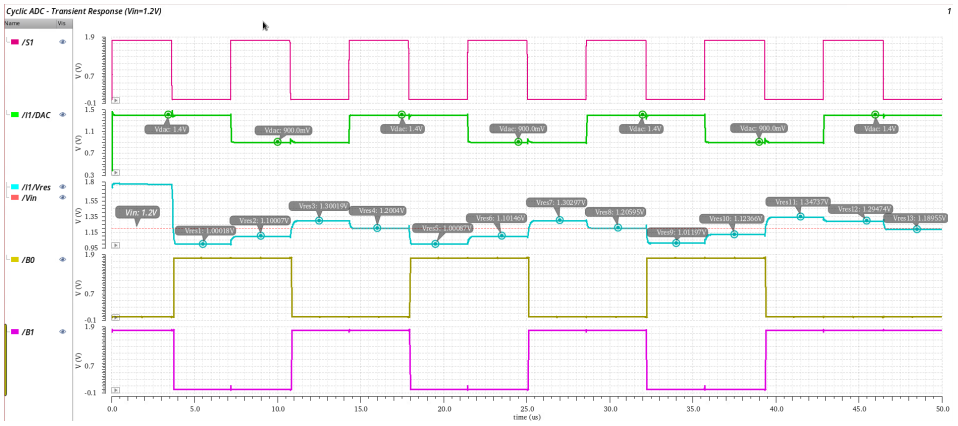

Figure 5.4: Residue and reference voltages ($V_in = 1.2V$)

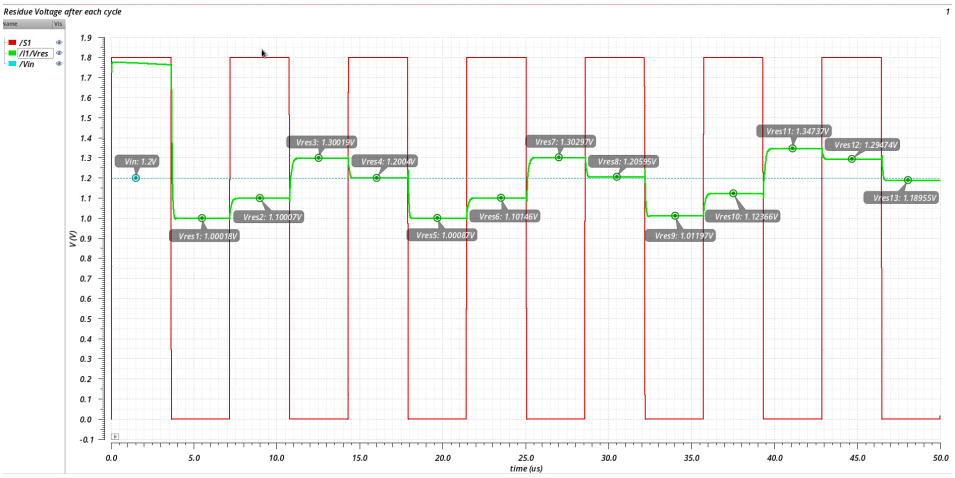

Figure 5.5: Residue Voltage after each cycle ($V_in = 1.2V$)

5.2 Cyclic ADC Performance Analysis

5.2.1 Linearity

The input-output characteristics of the 14-bit Cyclic ADC is shown in Fig.5.6 below using Python. The simulation was carried out on the input range 0.4V to 1.4V fro 40 sampling points. Due to the Linux server limited one-time login session of 8hours, it was not possible to run the simulation for each steps in an interval of 1LSB.

Cyclic ADC Transfer Function on a full-scale input range

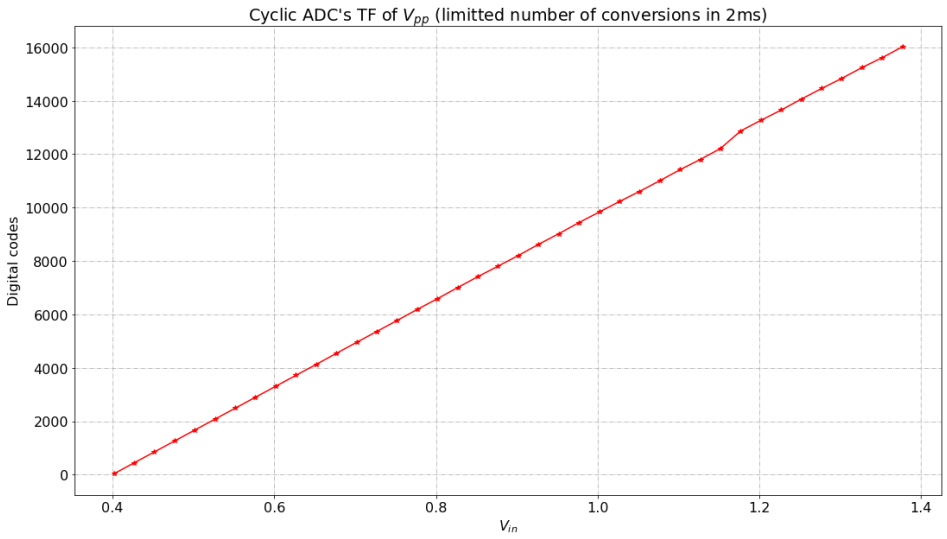

Figure 5.6: Transfer Function of full-scale ramp input

Cyclic ADC Transfer Function on a slow input ramp at 1LSB interval

Further simulation for a slow moving ramp input voltage was carried out around the middle of the input range, i.e, 20LSB to the left and 20LSB to the right of 900mV, to see its linear characteristics both at 1LSB steps and half-LSB intervals as shown in Fig.5.7 and Fig.5.8 below respectively.

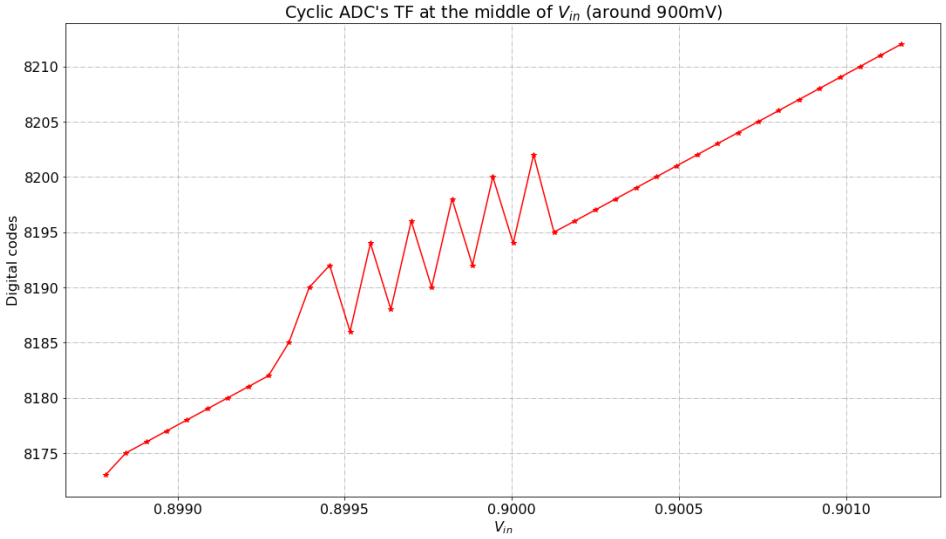

Figure 5.7: Transfer Function at 1LSB interval

Cyclic ADC Transfer Function on a slow input ramp at 1/2LSB interval

The input around the center was further zoomed for a 1/2LSB steps and the result is as shown in Fig.5.8.

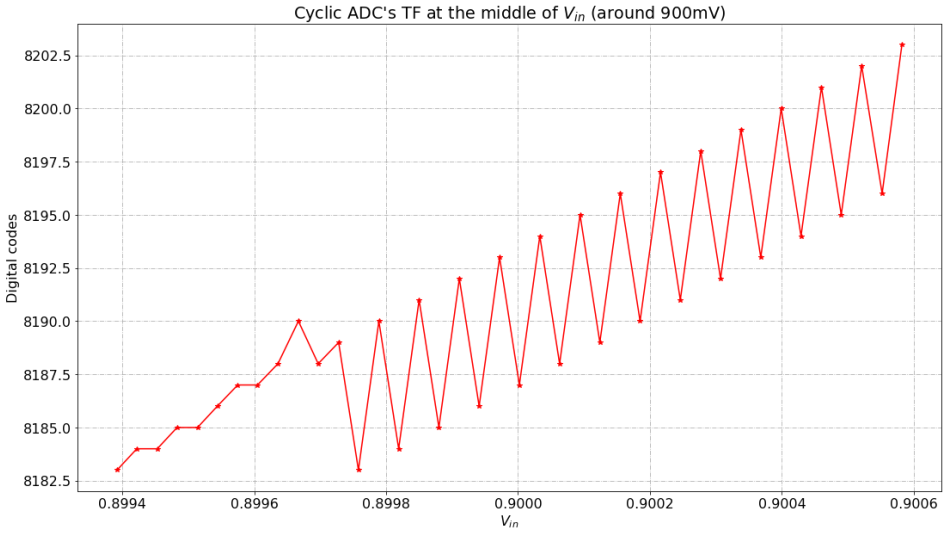

Figure 5.8: Transfer Function at half LSB interval

5.2.2 Effective Number Of Bits (ENOB)

From the data of the experimental and real transfer functions shown in Fig. 5.9, the effective number of bits are calculated at the middle, the input range at which the linearity behaves worst. The mean squared error (MSE) is obtained by subtracting the experimental values ($\tilde{Y}_i$) from the real one (Y_i) and then the differences are squared and then summed-up together and then the result is divided for the total number of samples (n).

$$MSE = \frac{1}{n}\sum_{i=1}^{n}(Y_i - \tilde{Y}_i)^2$$

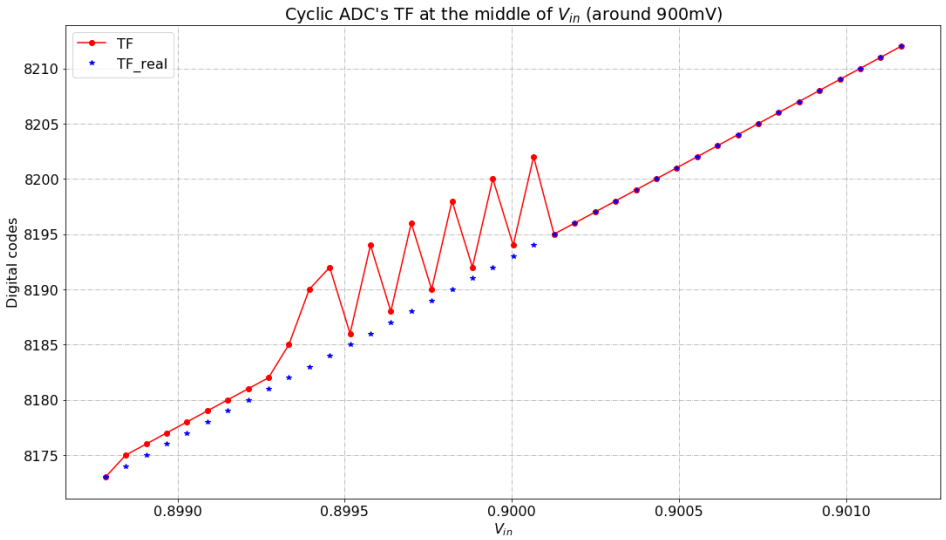

Figure 5.9: Transfer Function at 1LSB interval for both measured and real values

Then the Root Mean Squared Error (RMSE), which is the square root of the MSE is calculated so that the ENOB is calculated by the diffrence of the number of bits (N) and the $\log_2$ of the RMES.

$$RMSE = \sqrt{MSE}$$
$$ENOB = N - \log_2(RMSE)$$

The resulting ENOB is calculated to be 12.25 on the specified input range.

Chapter 6

Conclusion

A complete system level design and simulation of a 14-bit RSD Cyclic ADC intended for the use of sampling measurements of electron/ion density from m-NLP was carried out in XFAB 180nm CMOS Technology. The design focused on using very simple and basic components, which are smaller in number than the previously designed Hybrid CR-SAR ADC and also each component is kept at minimum size to attain the minimum die area while keeping the accuracy as close as possible to the requirement.

The Cyclic ADC dissipates 0.6mW power while achieving 12.25 ENOB at a sampling rate of 20kS/s . A thorough performance characteristics simulation was not carried out due to the limited hours (8hours) of the allowed one-time login session to Linux machines, and since the simulation of the whole peak-to-peak input range takes more than that.

Since practical realization of ADCs are affected by the finite gain of the opamp, comparator and opamp offsets, capacitors mismatch and the charge injection effect from CMOS switches, more improvements can be carried out mainly on the opamp and the comparators for a better accuracy and speed beyond the results of this thesis.

Bibliography

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Appendix A

Appendix

A.1 Python Code

The python code for the 1.5bit Cyclic ADC algorithm

```
######################## Import package
import numpy as np

######################## Define Function

def Conversion_14bit (Vi, Nbits, Vth, Vref):

    ######################## Initialize vector
    B1 = []
    B0 = []
    Vres = []        # Vres =2Vi-Vref =2Vi-Vdac
    Vdac = []        # {0.4, 0.9, 1.4}

    #Vi=[0.4, 1.4]
    #Vref={0.4, 0.9, 1.4}
    #Vth={0.65, 1.15}

    ######################## Conversion
    for i in range(Nbits):
        if Vi >= Vth[1]:                    #1.15
            B1.append(1)
            B0.append(0)
            Vdac.append(Vref[2])            #1.4
            Vres.append(2*Vi - Vref[2])

        elif Vi >= Vth[0]:                  #0.65
            B1.append(0)
            B0.append(1)
            Vdac.append(Vref[1])            #0.9
            Vres.append(2*Vi - Vref[1])
```

```
        else:                                   #Vi < 0.65
            B1.append(0)
            B0.append(0)
            Vdac.append(Vref[0])                #0.4
            Vres.append(2*Vi - Vref[0])

        Vi = Vres[i]        #input for next iteration

    #End For-Loop

    ######################## DEC - Shifting and Full-Adder
    D = ''          #store the 14bits
    c = 0           #carry

    for i in np.arange(Nbits-2,-1,-1):  #[12,11,...,2,1,0]
        sum = B1[i+1] + B0[i] + c
        if sum == 2:
            D = '0' + D
            c = 1
        else:
            D = str(sum) + D
            c = 0

    D = str(B1[i]+ c) + D   #binary digits
    b = int(D, 2)           #binary codes

    #print("\n ", Vi, " ", D, " ", b)

    return D, b, Vres

#End Function-Def.

######################## Define variables
Vi    = 1.2                 #[-Vref/2, Vref/2] = [0.4, 1.4]
Vref = [0.4, 0.9, 1.4]      #[-Vref/2, 0, Vref/2]
Vth   = [0.65, 1.15]        #[-Vref/4, Vref/4]
Nbits= 14                   #14-bit

######################## Calling the funtion for Vi
bin_d, bin_c, v_res = Conversion_14bit (Vi, Nbits, Vth, Vref)

######################## Print the outputs
#print("\n Vi         Binary       Codes ")
#print("\n", Vi, " ", bin_d, " ", bin_c)
```