Direct Synthesis of Carbon Nanotubes in CMOS – Layout of Micro-heaters

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***Abstract*—** Direct integration of Carbon Nanotubes (CNTs) in CMOS is important for commercially manufacturing low-cost CNT-based sensors. In such compact sensors, CNTs would act as sensing element, and CMOS circuits would process relevant signals from the CNTs. CNTs can be directly synthesized and integrated into CMOS by local thermal chemical vapor deposition (CVD), where a hot spot of ~ 900 ºC can be generated by CMOS microheaters. However, a sufficient thermal gradient between the micro-heaters and nearest CMOS devices is a prerequisite to ensure non-destructive temperature (< 300 ºC) in the electronic circuit regions. Our previous works have shown modelling and simulation of various CMOS micro-heaters that are promising for fulfilling these temperature requirements. In this paper, we investigate the layout designs of different metal and polysilicon micro-heaters using AMS 0.35µm CMOS process. Optical micrographs of the fabricated micro-heaters is also presented.

I. Introduction

Carbon nanotubes (CNTs) can be used as sensing material for gas, pressure, temperature and many other sensing applications [1], [2] due to their remarkable material properties [3], [4]. For mass production of compact CNT-based sensors, a cost-effective approach would be local synthesis and direct integration of CNTs on CMOS. Therefore, developing a standard process of direct CMOS-CNT integration is one of the main steps for commercially manufacturing sensors with CNTs as sensing element.

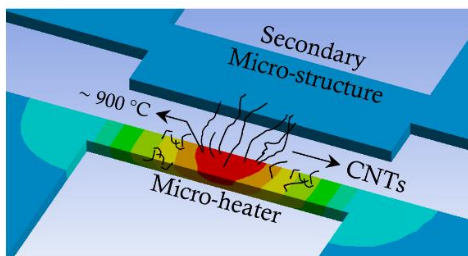

Figure 1. Concept of direct CNT-CMOS integration

In a CNT-based gas sensor, the electrical properties of CNTs change upon exposure to analytes. To maximize the effective surface area and electrical isolation, CNTs should be suspended between two electrodes as illustrated in Fig-1. In this arrangement, resistance of the suspended CNTs can be measured, hence, the change in resistance of the CNTs due to gas absorption or adsorption can be monitored. The resistance change can be correlated with the concentration of the target gas present in the environment.

CNT synthesis method using local resistive heating, developed by Englander et al. [5], is suitable for achieving electrode-CNTs-electrode configuration in CMOS. We have previously integrated MEMS-CNT using this method and demonstrated gas sensing [6], [7] where the positive results indicated possibility of direct CMOS-CNT integration, but implementation in CMOS is far more challenging in the processes currently available.

CNT synthesis process takes place in a CVD chamber where one electrode (micro-heater / CNT growth location) requires ~ 900 ºC temperature. This high temperature causes the thin catalyst layer (e.g. nickel, iron), pre-deposited on the surface of the micro-heater, to break down into nanoparticles. CNTs start to grow from the nanoparticles by a local thermal CVD process when a hydrocarbon gas (e.g. acetylene) is introduced. Details of this synthesis process can be found in one of our previous articles [8].

Joule heating is a suitable method for locally generating high temperature at a desired location for CNT growth. In CMOS, polysilicon and interconnecting metal layers can be used for the micro-heaters. High thermal gradient around the micro-heaters is necessary for CMOS compatible temperature (< 300 ºC) in the chip, which can mainly be accomplished by partially suspending the micro-heaters. Our simulation results support the achievability of such thermal requirements of the designed CMOS micro-heaters [8], [9].

AMS 0.35µm CMOS process has two polysilicon layers (Poly-1 & Poly-2) and uses aluminium (Al) for interconnecting metal layers [10]. We have designed various micro-heater layouts in Cadence Virtuoso using the polysilicon layers and top metal layer of this process. The designed micro-heaters are fabricated on 3 mm × 3 mm chips with the same CMOS process for the purpose of direct CNT synthesis in CMOS.

II. Design Approach

To design CMOS micro-heaters for our application, the most important aspect is to achieve high enough thermal gradient so that we get local hotspot (~ 900 ºC) for CNT synthesis while the circuit regions of the chip remain below 300 ºC. The micro-heater materials should have high melting point, as well as high electrical & thermal resistivity for efficient resistive heating.

The metal and polysilicon layers used for designing micro-heaters have dielectric layer beneath them, which conducts heat from the heaters to surrounding areas in the chip. Therefore,

surface area of the micro-heaters should be minimized to reduce the heater-dielectric contact area, thereby reducing heat conduction.

Microheaters need to be thermally isolated from the remaining chip area to achieve high thermal gradient. One of the most effective ways to obtain such thermal isolation is to suspend the micro-heaters by etching the dielectric material beneath them. However, suspended micro-heaters would be susceptible to mechanical deformation, mainly due to stiction and buckling during the dielectric etching and joule heating process. Compared to MEMS, CMOS structures are more vulnerable to the mentioned processes [11]. Therefore, we intend to perform limited dielectric under-etching on the CMOS micro-heaters to achieve required thermal gradient while maintaining necessary mechanical stability [9].

A. *Metal Micro-heaters*

Aluminium is not suitable as a micro-heater material for generating CNT synthesis temperature (~ 900 ºC) due to its low melting point (~ 660 ºC). Hence, tri-nickel aluminide (Ni_3Al) alloy is considered, which will involve nickel deposit on aluminium micro-heaters in post-processing of the CMOS chips. Based on relevant material properties, Ni_3Al alloy suits the requirements of micro-heater material better than the other Al alloys.

Compared to polysilicon, Al-Ni alloy has significantly lower electrical resistivity. Minimum width and thickness of the micro-heaters are limited by the CMOS process; hence, length of the metal micro-heaters has been extended to get sufficient micro-heater resistance.

Among the four Al interconnect layers in the AMS process, we have chosen the top layer to design the metal micro-heaters. Depending on the dielectric etching rate, etching duration can be set accordingly to get desirable partial suspension for these micro-heaters.

B. *Polysilicon Micro-heaters*

Microheaters have been designed using both polysilicon layers (Poly-1 & Poly-2). Poly-2 layer has higher resistivity than Poly-1 layer. In terms of material properties, polysilicon is more suitable as a micro-heater than metal [8], [9]. Due to high electrical resistivity, polysilicon heaters can have very short length. In our designs, polysilicon micro-heaters are more than 25 times shorter than metal micro-heaters; as a result, much lower heat would conduct to the layer beneath.

Relevant micro-heater designs include *in-situ* masks for partially under-etching the micro-heaters. These masks are designed using a top metal layer and vias. In CMOS, vias are used to interconnect different metal layers. All metal layers and vias are located above the polysilicon layers. In our polysilicon designs, we have utilized a top metal layer and/or vias as mask to define selective dielectric under-etching regions along the micro-heater. In some designs presented in *section III(B) & III(C)*, the metal layer and vias are placed in different positions near the micro-heaters to serve as built-in mask for protecting defined micro-heater areas from etching.

III. Results & Discussion

The layout designs and optical microscopy images of different fabricated micro-heaters are presented here. Design of the contact pads (required for electrical connections via wire bonding) are same for both metal and polysilicon structures. Thus, they are only shown in the metal designs.

A. *Aluminium Layer Designs*

Three Al micro-heater layouts are illustrated in Fig-2, with an overview of the system including the contact pads (Fig-2a). In design-1, the micro-heater is 200 µm long with uniform width of 0.7 µm. In design-2 (Fig-2b), the central portion (10 µm long) of the micro-heater has a width of 0.7 µm while the width of the remaining portion is 2.5 µm. This is to obtain higher temperature in central region. In design-3 (Fig-2c), the central portion has a rectangular wave shape to achieve a greater effective length compared to design-2.

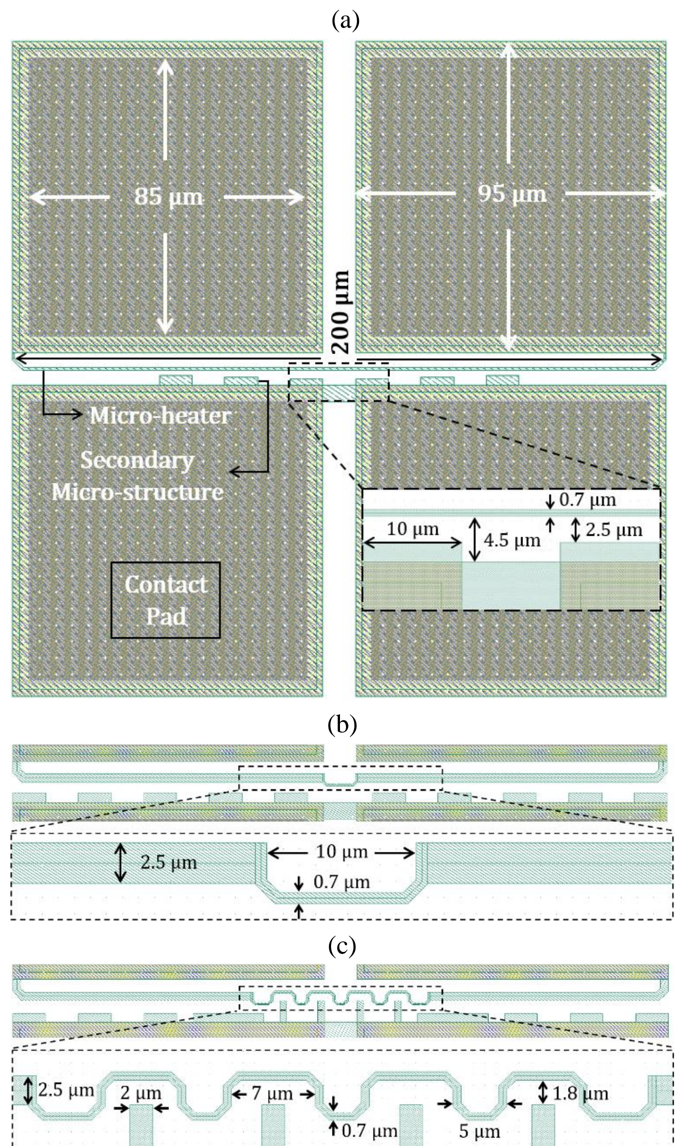

Figure 2. Aluminum micro-heater layout designs – (a) Design-1, micro-heater configuaration including contact pads; (b) Design-2 & (c) Design-3, reduced micro-heater effective length (without contact pads)

Electric field between the two electrodes (micro-heater & secondary micro-structure) along with diameter of the CNTs play an important role on the number of connected CNTs between the electrodes [12]. To vary this local electric field, spacing between the electrodes has been changed in different designs. Secondary electrodes in design-3 are narrower than the secondary electrodes of other Al layer designs.

Optical micrographs of the fabricated metal micro-heaters (design-2 & 3) are shown in Fig-3. Dimensions of all features in the fabricated chips match the designed values. The rhombus structure in the middle of the contact pads (Fig-3a) consists of an array of vias.

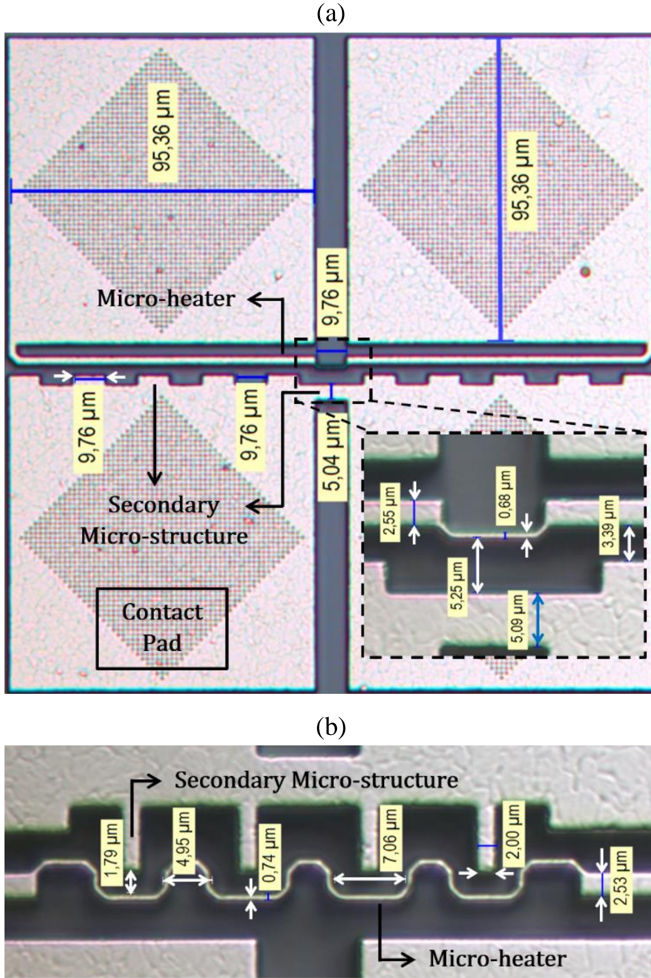

Figure 3. Optical micrographs of fabricated aluminum micro-heaters – (a) Overview of Design-2 including contact pads; (b) Design-3

B. *Poly-1 Layer Designs*

Micro-heater designs using Poly-1 are presented in Fig-3. A top metal layer (metal-1) is used to connect the micro-structures with contact pads. The designs shown in Fig-3a, b, & c use another metal layer (metal-2) as *in-situ* mask to prevent or limit dielectric etching from one side of the micro-heaters, thus improving mechanical stability of these heaters. Vias have also been used to protect from etching *(elaborated in section-II B)* in the designs shown in Fig-3b, c.

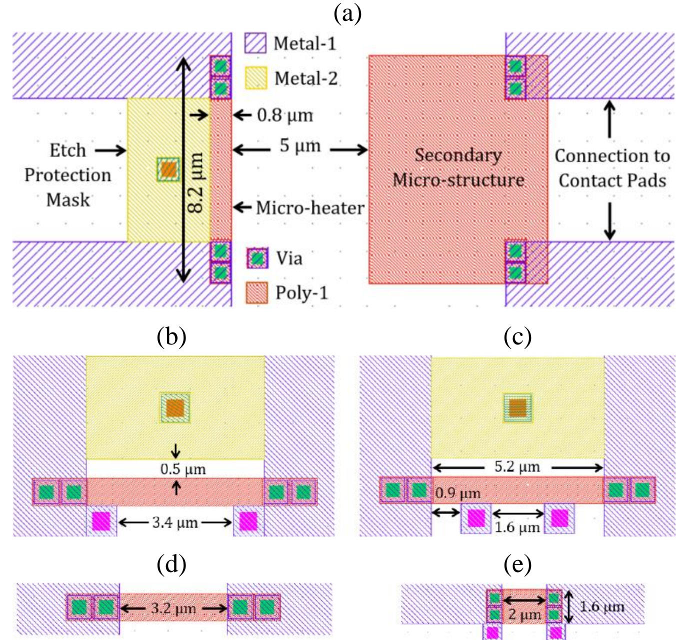

Figure 4. Poly-1 micro-heater layout designs (without contact pads) – (a) Design-1, detailed micro-heater overview; (b) Design-2 & (c) Design-3, micro-heater designs with metal-2 & vias as etching mask; (d) Design-4 & (e) Design-5, non-suspendable or fully suspendable micro-heater designs

In design-2 & design-3 (Fig-3b,c), a small gap of 0.5 µm was left between the micro-heater and the metal-2 etching mask to limit under-etching of that micro-heater side during the wet dielectric etching process. Micro-heaters in design-4 & design-5 (Fig-3d,e) are shorter than the previous designs, hence, they are more likely to meet the thermal gradient requirement even without any under-etching. Due to short length, these micro-heaters are likely to be sufficiently mechanically stable even if they are fully suspended.

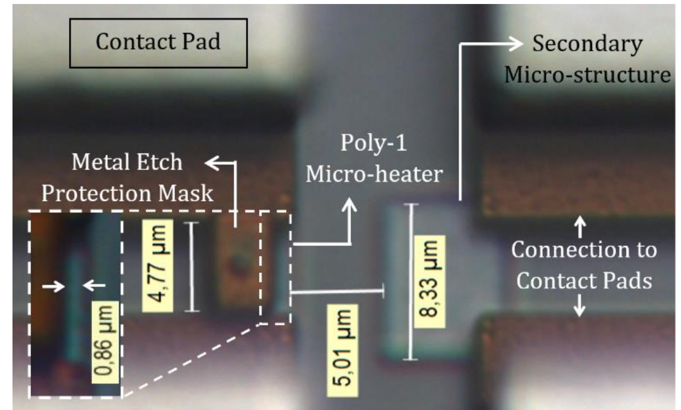

Figure 5. Optical micrograph of fabricated Poly-1 micro-heater in Design-1

The fabricated structures of design-1 (using poly-1 layer) is presented in Fig-5. Optical micrograph of this design can be easily associated with the layout shown in Fig-4a. Surface of the contact pads, connecting metal to the contact pads, metal layer for etch protection mask and polysilicon layer of the CMOS chips are situated at different heights. As a result, all features in Fig-5 are not equally focused.

C. Poly-2 Layer Designs

Micro-heater designs using Poly-2 layer are presented in Fig-6. Design-1 of both poly-1 (Fig-4a) and poly-2 (Fig-6a) have similar features with some minor changes in the feature dimensions. Only vias are used as etching masks in the designs shown in Fig-6b, c, & e. Placement of the vias (*in-situ* etching masks) is different in different designs in order to investigate the effect of vias in partial dielectric under-etching. Distance between the micro-heater and the secondary electrode, as well as the geometry of the secondary electrode has also been varied to achieve various electric field between the electrodes.

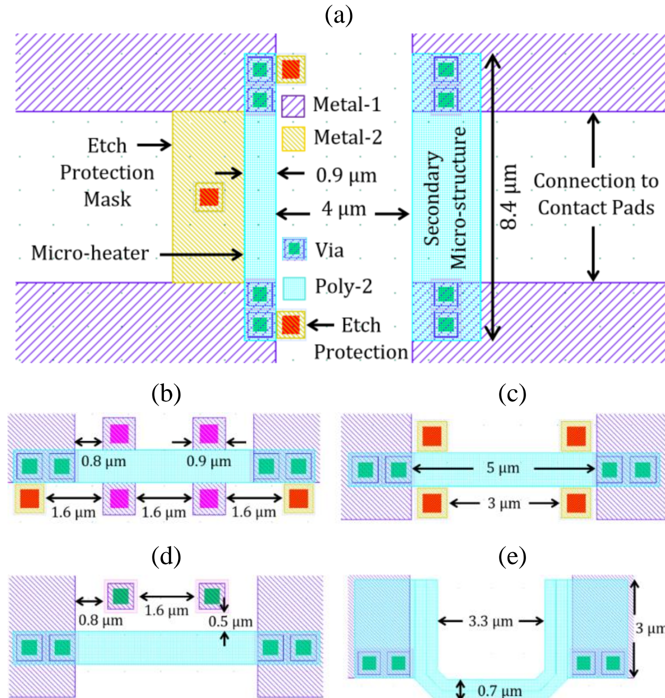

Figure 6. Poly-2 micro-heater layout designs (without contact pads) – (a) Design-1, detailed micro-heater overview; (b) Design-2, (c) Design-3 & (d) Design-4, micro-heater designs with vias as etching mask; (e) Design-5, non-suspendable or fully suspendable micro-heater design

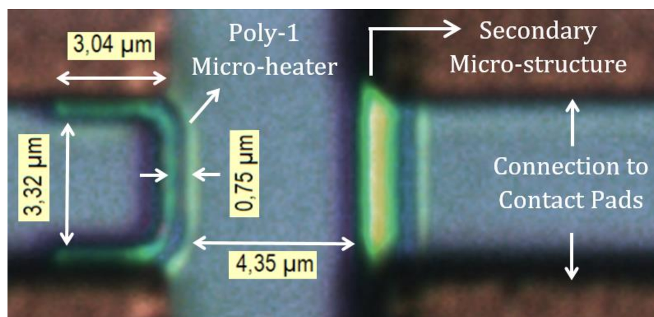

Figure 7. Optical micrograph of fabricated Poly-2 micro-heater in Design-5

An optical micrograph of design-5 (layout in Fig-6e) is shown in Fig-7. This design does not feature any etch protection mask. We intend to test this micro-heater without any under-etching (non-suspended) and also by completely etching the underneath dielectric layer (fully suspended), similar to the poly-1 designs in Fig-3d,e.

IV. Conclusion

This work demonstrates possible implementation of direct integration of CNTs in AMS 350 nm CMOS structures. Metal and polysilicon layers in CMOS are used for micro-heaters that would generate 900º C by resistive heating for CNT growth. To achieve required thermal isolation for CMOS circuits, vias or top metal layers are used to create *in-situ* masks for limited dielectric etching in CMOS post-processing, hence partially suspending micro-heaters. Layout structures presented here are found mechanically, electrically and thermally suitable for CMOS through simulations. A CMOS chip has been manufactured, with fabricated micro-structures accurately resembling the layout designs.

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