Exploring the SEU Dependence on Supply Voltage Scaling in 90 nm and 65 nm CMOS Flip-flops

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Contents

Acronyms

ABB	Adaptive Body Bias.
ADC	Ambipolar-Diffusion-with-Cutoff.
ASIC	Application Specific Integrated Circuit.
BSIM	Berkeley Short-channel IGFET Model.
CME	Coronal Mass Ejection.
CMOS	Complementary Metal-Oxide-Semiconductor.
DFF	Data Flip-flop.
DICE	Dual Interlocked Storage Cell.
DIBL	Drain Induced Barrier Lowering.
DFS	Dynamic Frequency Scaling.
DVS	Dynamic Voltage Scaling.
DVFS	Dynamic Voltage and Frequency Scaling.
EDA	Electronic Design Automation.
FSM	Finite-State Machine.
FWHR	Full Width Half Rail.
GCR	Galactic Cosmic Rays.
HVT	High Threshold Voltage.
IC	Integrated Circuit.
IoT	Internet of Things.
IRPP	Integral Rectangular Parallel-Piped.
LEAP	Layout Design through Error Aware Positioning.
LET	Linear Energy Transfer.

LVT	Low Threshold Voltage.
MEP	Minimum Energy Point.
MSV	Multiple Supply Voltage.
MTCMOS	Multi-Threshold CMOS.
NMOS	N-type Metal-Oxide-Semiconductor.
NWE	Narrow Width Effect.
PDA	Personal Digital Assistant.
PDK	Process Development Kit.
PMOS	P-type Metal-Oxide-Semiconductor.
PVT	Process, Voltage and Temperature.
RDF	Random Dopant Fluctuations.
RT	Radiation Tolerant.
SCE	Short-Channel Effect.
SEE	Single Event Effect.
SEFI	Single Event Functional Interrupt.
SEL	Single Event Latchup.
SER	Soft Error Rate.
SET	Single Event Transient.
SEU	Single Event Upset.
SoC	System on Chip.
SPE	Solar Particle Event.
SRAM	Static Random Access Memory.
SVT	Standard Threshold Voltage.
TCAD	Technology Computer Aided Design.
TDF	Temporal Dual-Feedback.
TMR	Triple Modular Redundancy.
ULP	Ultra Low-Power.

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Abstract

Down-scaling of the supply voltage is considered as the most effective means of reducing the power- and energy consumption of integrated circuits (ICs). Reduction in the power- and energy consumption is highly beneficial in aerospace and defense applications that have a constrained power budget. These applications include, but are not necessarily limited to, payloads in solar powered spacecraft and rovers. The benefits that can be harvested from reducing the power- and energy consumption in such applications are reduced weight, reduced mass and/or increased functionality for a given power budget. Although supply voltage scaling can improve the energy efficiency of ICs, radiation induced errors also tend to increase with decreasing supply voltage. In order to enable reliable operation in radiation-rich environments, radiation induced errors must be mitigated, preferably with minimum area, power and performance penalties.

In this thesis, the single event upset (SEU) dependence on supply voltage scaling is investigated for data flip-flops (DFFs) designed in 90 nm and 65 nm CMOS technology nodes. The radiation tolerance of the DFFs was characterized at supply voltages between 0.18 V and 1 V, and heavy ion radiation testing was performed using ions with linear energy transfer (LET) between $5.8\ \mathrm{MeV\text{-}cm^2/mg}$ and $68.8\ \mathrm{MeV\text{-}cm^2/mg}$. Both temporal and spatial hardening techniques are utilized as a means of mitigating SEUs, and the impact of drive strength and sensitive node separation is evaluated. The examined circuit-level hardening techniques include triple modular redundancy (TMR), dual interlocked storage cell (DICE) and temporal dual-feedback (TDF), as well as inverter-based and current starved delay elements for SET filtering purposes.

This study shows that radiation tolerant DFFs can offer soft error rate (SER) improvements of up to 55x, 121x and 600x, compared to a standard non-radiation tolerant DFF, when scaling the supply voltage down to 0.18 V, 0.25 V and 0.5 V, respectively. Simultaneously, by scaling the supply voltage down to 0.5 V and 0.25 V, radiation tolerant DFFs can achieve $\sim$3.9x and $\sim$12x higher energy efficiency, compared to when operating at a supply voltage of 1 V. Selective placement of high drive strength components showed to reduce the SEU sensitivity in DFFs by up to 112x, compared to DFFs utilizing standard drive strength. The impact of charge sharing was, on the other hand, increasingly challenging to mitigate with decreasing supply voltage. Nevertheless, based on the findings in this work, radiation tolerant DFFs operated at reduced supply voltage offer a clear advantage over standard non-radiation tolerant DFFs, and may therefore be suited for implementation in low power payloads, depending on the error rate requirements of the application.

In addition to investigating the SEU dependence on supply voltage scaling, this thesis also presents the design and performance of subthreshold to above threshold level shifters, and the characterization of the proton beam properties at the Oslo Cyclotron Laboratory (OCL).

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Chapter 1

Introduction

Ever since the early days of the integrated circuit (IC) industry, ICs played a key role in advancing research and development of aerospace and defense systems. In the 1960s, during the Space Race and the Cold War technological race, the aerospace and defense industry found ICs attractive since ICs could offer smaller size, lower weight and lower power consumption than the previously used discrete components [1]. One of the key enablers of technological advancements in the IC industry is the continuous scaling of transistor sizes. The down scaling of transistor sizes has increased the switching speed of transistors as well as enabled the integration of more transistors per unit area, leading to an exponential increase in performance of high-speed microprocessors over the last couple of decades. Simultaneously, the increase in performance has been accompanied by a comparable increase in power consumption and heat dissipation, making it difficult to meet the cooling requirements in many application areas. Over the last decade however, the power consumption of ICs has been stabilized in order to enable ICs to operate under practical thermal conditions [2]. Furthermore, the growing demand for portable devices has elevated the emphasis on low power consumption due to the limited power budget often found in such devices. In order to meet the low power requirements of portable devices and to increase the energy efficiency of ICs, circuit and microarchitectural optimizations have been vastly utilized [3]. Since many aerospace and defense applications also have a limited power budget, exploring techniques for reducing the power consumption is essential for optimizing the energy efficiency in high reliability applications. A reduction in the power consumption of ICs would enable to add additional functionality for a given power budget, and/or reduce the power budget, which could reduce size and weight of the system.

One of the most effective means of reducing the power consumption in ICs is to scale down the supply voltage. By scaling the supply voltage below the absolute value of the threshold voltages of complimentary metal-oxide semiconductor (CMOS) transistors, orders of magnitude reduction in the power consumption may be achieved [4, 5]. Due to the potential power savings, supply voltage scaling has been extensively researched for the purpose of maximizing energy efficiency in terrestrial applications which have a limited power budget [6, 7, 8]. While supply voltage scaling does contribute to substantial savings in power consumption, it is important to note that it also reduces the operating speed of the circuits, making the method suitable primarily for low to medium performance applications. Nevertheless, before this method can be applied to ICs in radiation-rich, high reliability applications, the radiation tolerance of the CMOS circuits operated at a wide supply voltage range, needs to be investigated.

Radiation hardening of ICs operated at nominal supply voltages have been extensively researched, and various hardening techniques have emerged as a result of the efforts. Such hardening techniques include, but are not necessarily limited to, triple modular redundancy (TMR) [9, 10], dual interlocked storage cell (DICE) [11, 12] and temporal redundancy [13, 14]. In this work, we investigate several of these radiation hardening techniques and their efficiency to mitigate radiation induced errors, while scaling the supply voltage as a means of reducing the power consumption. Supply voltage scaling has played a key role in the low-power revolution which occurred after the mid-1990s. The research efforts within the low power commercial industry have contributed to technological advancements giving us everyday products such as, smart-phones and tablets, Internet of things (IoT) gadgets and other portable devices. From an IC design perspective, common for all these devices is that they incorporate low-power design techniques which enable high energy efficiency. By tapping into the technological advancements made in the terrestrial low-power industry, low-power-, and even ultra low-power (ULP) radiation tolerant ICs may be realized, paving the way for new innovations within the aerospace and defense sector. However, several challenges related to radiation tolerance and supply voltage scaling need to be addressed before ULP, radiation tolerant IC are deemed reliable enough to meet the requirements of aerospace and defense applications.

1.1 Challenges in Low Voltage, Radiation Tolerant CMOS

The main reason for reduced power consumption, when scaling down the supply voltage, is the reduction of current flowing through the transistors. Reducing the supply voltage contributes to reducing both the dynamic (switching) and static (leakage) current, and thereby also the current drive capability of the transistors. Although this is favorable in terms of power consumption savings, a reduction in the current drive also contributes to increased vulnerability to radiation induced errors such as single event transients (SETs) and single event upsets (SEUs). Since the transistors ability to recover from SETs is heavily dependent on their current drive, reduction of the supply voltage causes the duration of SETs to increase, thereby making them more difficult to suppress. Moreover, the reduction of the supply voltage also contributes to lower charge being stored at each circuit node, leading to less radiation induced charge being necessary to create an SEU. As a consequence, circuits become more sensitive to particles with lower energy, and charge sharing induced SETs/SEUs become more pronounced as the supply voltage scales down.

Technology scaling also leads to increased vulnerability to radiation induced errors. The down-scaling of feature sizes has made traditional hardening techniques such as TMR and DICE less efficient since sensitive nodes are located closer to each other with each technology node, making the sensitive nodes more prone to charge sharing. The technology scaling impact on charge sharing is further magnified since the node capacitances are being reduced and less charge is being stored at each circuit node.

On top of the challenges related to supply voltage scaling, technology scaling and radiation tolerance, process variations also pose challenges in designing reliable low voltage ICs. The increased impact of variability at low voltages is acknowledged here since it plays a key role in low voltage IC design.

1.2 Thesis Outline

This thesis is based on a collection of papers related to the fields of low-power CMOS design and radiation tolerant CMOS design. The papers are listed below, organized in chronological order, where Paper II is a conference publication, while Paper I, III and IV are journal publications.

Paper I A. Hasanbegovic and S. Aunet, "Low-power subthreshold to above threshold level shifters in 90 nm and 65 nm process", *Microprocessors and Microsystems (MICPRO)*, vol. 35, pp. 1-9, Feb. 2011.

Paper II A. Hasanbegovic and S. Aunet, "Proton beam characterization at Oslo cyclotron laboratory for radiation testing of electronic devices", *IEEE 16th International Symposium on Design and Diagnostics of Electronic Circuits Systems (DDECS)*, pp. 135-140, Apr. 2013.

Paper III A. Hasanbegovic and S. Aunet, "Supply voltage dependency on the single event upset susceptibility of temporal dual-feedback flip-flops in a 90 nm bulk CMOS process", *IEEE Transactions on Nuclear Science (TNS)*, vol. 62, pp. 1888-1897, Aug. 2015.

Paper IV A. Hasanbegović and S. Aunet, "Heavy ion characterization of temporal-, dual- and triple redundant flip-flops across a wide supply voltage range in a 65 nm bulk CMOS process", *IEEE Transactions on Nuclear Science (TNS)*, vol. 63, pp. 2962-2970, Dec. 2016.

This thesis aims at investigating the radiation tolerance of low-power/low-voltage CMOS circuits, and for that reason, the paper contributions of this work originate from both the low-power/low-voltage CMOS field and the radiation effects field.

- Paper I presents the design and simulation results of subthreshold to above threshold level shifters in 90 nm and 65 nm CMOS process. Paper I is an extended journal version of a previously published conference paper [15].

- Paper II presents the characterization of a proton beam facility located at the University of Oslo. The purpose of the proton beam characterization was to investigate its suitability for radiation testing of ICs with proton energies below 30 MeV.

- Paper III investigates the SEU tolerance, primarily of a proposed temporal dual-feedback (TDF) data flip-flop (DFF) topology for a supply voltage range of 0.18 V to 1 V. The impact of temporal and spatial hardening is analyzed, and an evaluation of the potential energy savings offered by supply voltage scaling is given.

- Based on the findings in Paper III, extended experiments were conducted in Paper IV, which include a wider range of circuit hardening topologies, improvements in the circuit layout and an improved irradiation test campaign (wider LET spectrum, higher fluence, angled hits). In Paper IV, the radiation tolerance of six DFFs across a wide supply voltage range is presented and the improvement offered by temporal-, dual- and triple redundancy, compared to a standard DFF, is given. Additionally, the impact of drive strength in temporal redundant DFFs is also investigated.

The rest of this work is organized as follows: Chapter 2 is divided into two parts and presents a general overview of the background information related to Papers I-IV. The first part (Chapter 2.1) covers the basic principles in low-power CMOS design and ultralow-voltage operation. The second part (Chapter 2.2) gives an introduction to single event effects and the processes involved with charge generation and charge collection as a result of an inbound particle strike. Also presented in Chapter 2.2 is the soft error dependence on supply voltage, as well as a brief review of the previous work done within low-voltage, radiation tolerant circuit design. Chapter 3 gives a summary of each of the paper contributions of this thesis, while Chapter 4 aims at discussing the findings in the paper contributions beyond the discussions covered in the papers. Since the discussion is based on the paper contributions of this work, it is recommended to read the papers before reading the discussion. Finally, in Chapter 5, the conclusions of this work are given, as well as an outlook towards future research.

Chapter 2

Background

This chapter presents basic background information on the topics covered in the paper contributions of this thesis. The background information provides only a general overview over the most important concepts covered, and therefore does not serve as an extensive theoretical review. Additionally, short introductions may also be found in each of the respective papers.

2.1 Low-Power CMOS

Historically, for the vast majority of ICs, power consumption has not been a major concern until the 1990s. Before that, low power consumption was important only for a few niche applications, such as the wristwatches [4], hearing aids [16], pacemakers [17, 18] and pocket calculators [19]. The common requirement for these niche applications was portability, meaning they had to be battery powered. In the 1990s, after a steady performance increase, power consumption and heat dissipation also increased at an alarming rate, creating concerns about how to tackle future IC reliability- and cooling demands. Simultaneously, new application areas were emerging, such as cellular phones, notebooks and personal digital assistants (PDAs), which all required portability and thereby low power consumption. To meet the low power consumption requirements of these new applications, and to reduced the heat dissipation of ICs, low-power CMOS design became a significant part of mainstream IC development by the turn of the century.

Although not vastly researched prior to the 1990s, several of the design techniques enabling low power consumption in todays ICs have been known since the 1960s [4, 20]. These techniques include the reduction of the supply voltage for trading off speed for reduced power consumption, and concepts of reducing the standby power (back then, analog techniques were used to limit high power drain in bipolar digital circuits [20]). Since reduction of the supply voltage is one of the most powerful means of reducing the total power consumption of an IC, it is often utilized in conjunction with other low-power design techniques to achieve the highest possible power savings. These design techniques include, but are not necessarily limited to, clock gating, pipelining, parallelism, dynamic voltage and frequency scaling (DVFS), multiple supply voltage (MSV) domains and multi-threshold CMOS (MTCMOS). As a result of the new design techniques, new standard cells have also emerged, such as isolation cells, retention registers and level shifters. These cells are important for efficient implementation of the low-power design techniques. For example, in the case of MSV and DVFS, levels shifters are required for

interfacing the supply voltage domains. A typical requirement for the level shifters is to be able to cover a wide input range and also preferably a wide output range. As part of the work done in this thesis, an MTCMOS-based level shifter capable of converting subthreshold input signals to above threshold output signals has been presented (see Paper I [21]).

The efficiency of low-power design techniques in combination with supply voltage scaling has been demonstrated through numerous low-power and energy efficient IC implementations. For example, to support wireless sensor networks, a 16-b 1024-point processor operating at a supply voltage of 350 mV with a clock frequency of 10 kHz achieved 155 nJ/FFT, showing 8x improvement in energy efficiency compared to a low-power application specific integrated circuit (ASIC) implementation [6]. Furthermore, a variety of low-voltage microcontrollers and processors have been proposed [22, 23], such as the Sleep Walker, which achieves 7 $\mu\mathrm{A/MHz}$ using adaptive voltage scaling (AVS) between 0.32 V - 0.48 V while running at a frequency of 20 MHz [7]. Also, with the IoT demands of 10+ year battery lifetime, or even self-sustained operation, an energy harvesting system on chip (SoC) has been proposed for physiological sensing on the body [8]. The SoC is self-powered and contains its own power management, processing units and up-/downlink, and consumes 6.45 $\mu\mathrm{W}$ with its digital logic operating at a supply voltage of 0.5 V. Supply voltage scaling and body-biasing techniques have also attracted the attention of space electronics. The CMOS Ultra-Low Power Radiation Tolerant (CULPRiT) program found that up to 36x power savings were possible by scaling the supply voltage from 3.3 V to 0.5 V in a 0.35 $\mu\mathrm{m}$ CMOS technology [24]. A microcontroller designed using the CULPRiT techology showed up to two orders of magnitude better radiation tolerance than similar non-radiation tolerant microcontrollers, despite operating at a supply voltage of 0.5 V [25].

From (2.1) and (2.2)[26], it is very clear why supply voltage scaling is a popular methodology for reducing the power consumption of ICs.

$$P_{tot} = P_{sw} + P_{leak} \tag{2.1}$$

$$P_{tot} = \alpha \cdot C \cdot f_{clk} \cdot V_{DD}^2 + I_{leak} \cdot V_{DD} \tag{2.2}$$

The total power consumption (P_{tot}) of ICs is made up of a switching component (P_{sw}) and a leakage component (P_{leak}). Switching power depends on the activity factor (α), the total capacitance that needs to be charged/discharged (C), the operating frequency (f_{clk}) and the supply voltage (V_{DD}), while leakage power depends on the leakage current of transistors (I_{leak}) and the supply voltage (V_{DD}). From and (2.2), we see that supply voltage together with operating frequency offers cubic scaling in the switching power consumption and linear scaling in the leakage power consumption. Figure 2.1 shows the P_{sw}, P_{leak} and P_{tot} of a DFF, designed in a 65 nm CMOS process, as a function of V_{DD} between 180 mV and 1 V. The data presented is based on α = 0.025 and f_{clk}=f_{max}, where f_{max} is the maximum frequency. As seen in Figure 2.1, the switching power decreases by 6 orders of magnitude, while the leakage power decreases by 1 order of magnitude when scaling the supply voltage from 1 V to 180 mV. The observation that immediately stands out from Figure 2.1 is that P_{sw} in fact exhibits an exponential decrease with decreasing V_{DD}, when $V_{DD} < 0.5$ V, and that P_{leak} is not completely linear. These trends are attributed to the transistor subthreshold current characteristics and the transistor second order effects, which are not covered by the model in (2.2), and will be discussed in Chapter 2.1.1.

Nevertheless, the model does capture the effect of the leakage power becoming higher than the switching power at low supply voltages, limiting the decrease in total power consumption to approximately 5.5 orders of magnitude. The crossover between P_{leak} and P_{sw} is due to the increase in propagation delay and setup time in the DFF as a result of decreasing the supply voltage, which ultimately reduces the operating frequency (i.e., the time between switching operations) by 5.8 orders of magnitude. By decreasing α and/or f_{clk}, the contribution of the leakage power increases and thereby further limits the total power consumption savings at low supply voltages. In complex systems such as SoCs, leakage power is even more prominent due to low activity blocks such as static random access memory (SRAM) and process variation induced increase in delay (see Chapter 2.1.2).

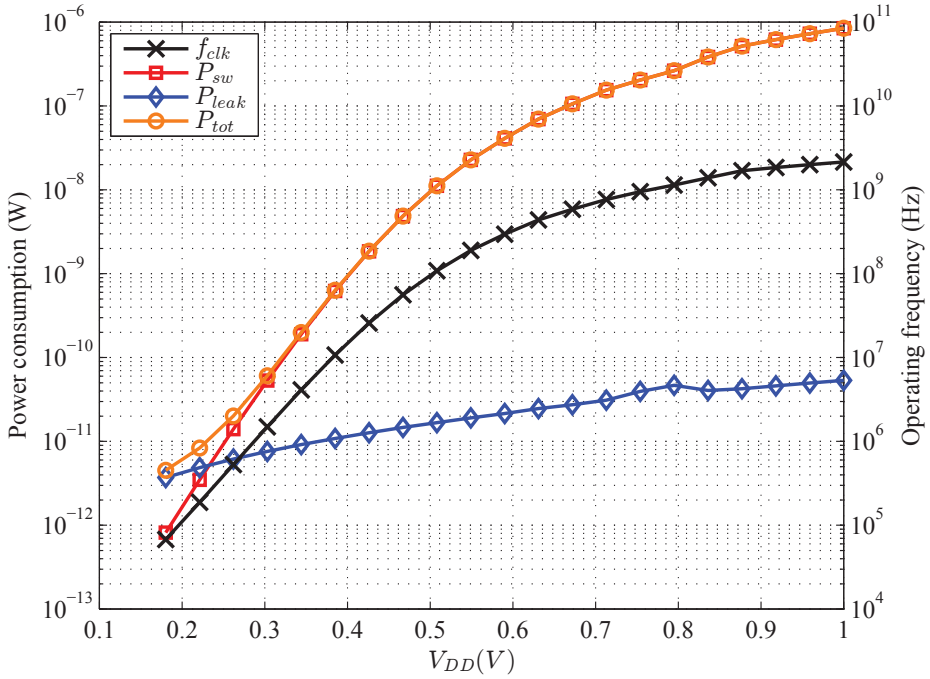

Figure 2.1: P_{sw}, P_{leak} and P_{tot} of a DFF implemented in a 65 nm low-power CMOS process. Based on post-layout simulations.

Although the power consumption metric provides information on the rate of energy dissipation, the energy consumption metric is perhaps even more important as it provides information about the energy efficiency of the circuit (i.e., the amount of energy needed to perform a switching operation). In energy constrained applications, it is important to minimize the energy consumption per cycle in order to maximize the number of operations/cycles that can be performed within a given energy budget. This typically comes down to finding a trade-off between the switching energy and and the leakage energy. Given a clock period $t_{clk} = 1/f_{clk}$, the total energy consumption (E_{tot}) per cycle can be modeled as (2.3), (2.4) and (2.5) [26]:

$$E_{tot} = E_{sw} + E_{leak} \tag{2.3}$$

$$E_{tot} = P_{sw} \cdot t_{clk} + P_{leak} \cdot t_{clk} \tag{2.4}$$

$$E_{tot} = \alpha \cdot C \cdot V_{DD}^2 + I_{leak} \cdot V_{DD} \cdot t_{clk} \tag{2.5}$$

In terms of E_{tot}, the switching component (E_{sw}) is not dependent on any time domain parameters, while the leakage component (E_{leak}) is increasing with the clock period. This is reflected in Figure 2.2, where leakage energy increases rapidly with decreasing supply voltage and becomes the dominating contributor of E_{tot} for V_{DD} < 260 mV. The point where dE_{tot}/dV_{DD} = 0 marks the minimum energy point (MEP) of the DFF, and sets a lower bound for the optimal supply voltage in terms of energy efficiency. Thereby, the maximum energy savings which can be achieved through supply voltage scaling, given α = 0.025, is 10x. This means that 10x more computations may be performed when V_{DD} = V_{DD}@MEP, than when V_{DD} = 1 V, given the same energy budget. Increasing the activity factor of the DFF would yield even higher reduction of E_{tot} and thereby push MEP lower in the supply voltage range. However, as mentioned previously, when considering process variations, complex systems with low activity factor components and longer combinational logic paths, the contribution of the leakage energy can increase and thereby move the MEP higher in the supply voltage range and reduce the potential energy savings.

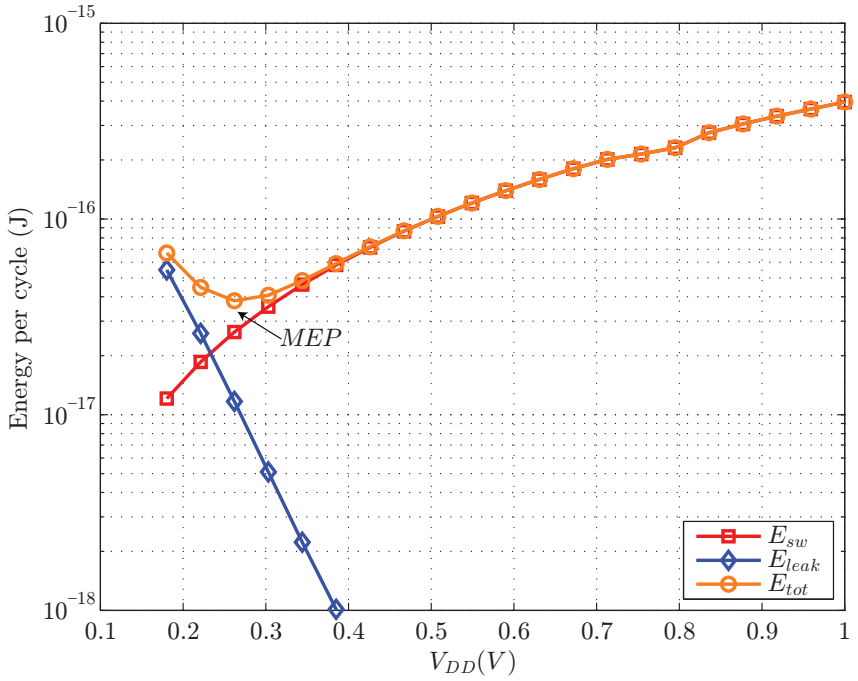

Figure 2.2: E_{sw}, E_{leak} and E_{tot} consumed per cycle by a DFF implemented in a 65 nm low-power CMOS process. Based on post-layout simulations.

2.1.1 Ultralow-Voltage CMOS

The performance and also the radiation tolerance of CMOS circuits are both dependent on the transistor current characteristics. As described in [27], the regions of operation of a transistor can be divided into three categories: (1) The superthreshold region (also know as 'above

threshold region') ($V_{GS} > V_{th}$), where the transistor channel is strongly inverted and the inversion charge density is larger than the substrate doping concentration, meaning that the carrier transport is dominated by drift. (2) The subthreshold region ($V_{GS} < V_{th}$), where the transistor channel is weakly inverted and the substrate doping concentration is larger than the inversion charge, meaning that the carrier transport is dominated by diffusion. (3) The near-threshold region ($V_{GS} \approx V_{th}$), where the transistor operates in moderate inversion and both drift and diffusion are contributing to the current conduction due to the inversion charge density and the substrate doping concentration being similar.

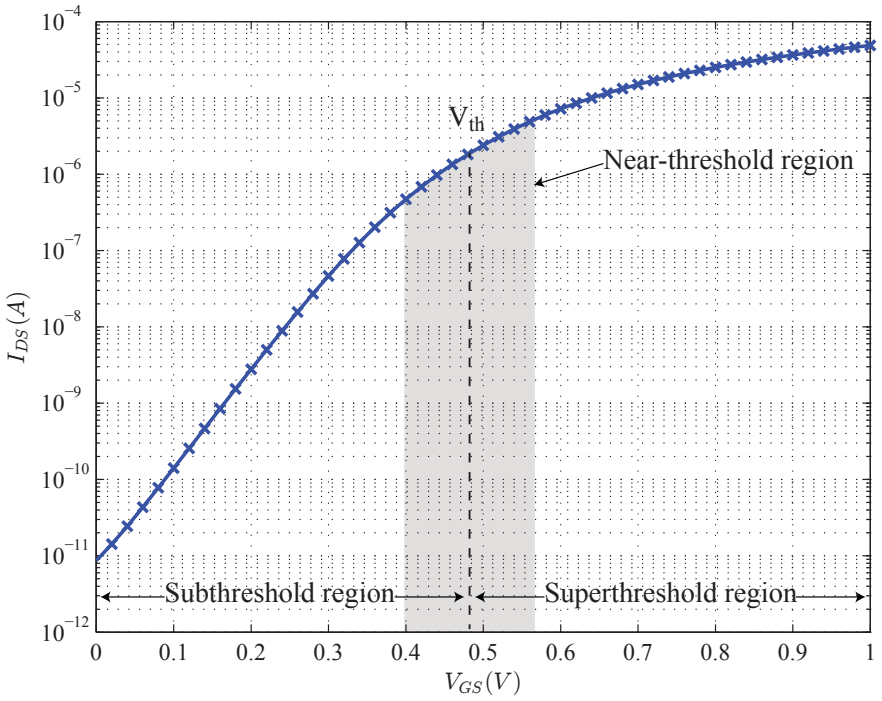

Figure 2.3: Simulated drain-source current (I_{DS}) as a function of gate-source voltage (V_{GS}) of a NMOS transistor (W/L=150 nm/100 nm), in a 65 nm low-power CMOS process.

As illustrated in Figure 2.3, the drain-source current in the superthreshold region scales roughly linearly with V_{GS} due to the inversion charge density being proportional to $(V_{GS}-V_{th})^{\alpha}$, where $1 < \alpha < 2$ for short channel devices as a result of velocity saturation. At the transition between superthreshold and subthreshold regions, a roughly quadratic to exponential trend may be observed as V_{GS} gets closer to, and below V_{th}. In the subthreshold region, the drain-source current (I_{DS-sub}) scales exponentially with V_{GS} due to the absence of a strong inversion region and due to the charge concentration being exponentially dependent on bias voltage [28]. The exponential dependence on bias is also reflected in (2.6), which is commonly used for modeling the current in the subthreshold region [29, 30, 31]:

$$I_{DS-sub} = \mu_{eff} \cdot C_{ox} \cdot \frac{W_{eff}}{L_{eff}} \cdot (n-1) \cdot U_T^2 \cdot exp\left(\frac{V_{GS} - V_{th}}{n \cdot U_T}\right) \cdot \left(1 - exp\left(\frac{-V_{DS}}{U_T}\right)\right) \quad (2.6)$$

where μ_{eff} is the effective mobility, C_{ox} is the oxide capacitance, W_{eff} is the effective

transistor width, L_{eff} is the effective transistor length and n is the subthreshold slope factor given by $(1 + C_{dep}/C_{ox})$, where C_{dep} is the depletion layer capacitance. U_T is the thermal voltage (kT/q), where k is Boltzmann's constant, T is the temperature and q is the charge of an electron.

From (2.6), it is evident that I_{DS-sub} is exponentially dependent on V_{GS} (V_{DD}), V_{th} and temperature. A favorable effect of the exponential dependence on V_{DD} is the high P_{sw} savings that can be achieved by scaling V_{DD} below V_{th}. This trend was shown in Figure 2.1, where P_{sw} showed exponential decrease with V_{DD} in the subthreshold region. Obviously, with exponential decrease in I_{DS-sub}, the propagation delay also increases exponentially since the delay is inversely proportional to I_{DS-sub}. This means that circuits operated in the subthreshold and near-threshold regions are primarily suited for low- to medium-speed applications.

For transistors operated in the subthreshold region, the subthreshold swing, S, is an important parameter:

$$S = 2.3 \cdot n \cdot U_T \tag{2.7}$$

The subthreshold swing is measure of the amount of V_{GS} needed to change I_{DS} by one order of magnitude (given in units of mV/decade). An ideal transistor achieves S=60 mV/decade at room temperature, however, a realistic value for S is typically between 70 mV/decade to 100 mV/decade in CMOS bulk technology. A small S is desired since it represents a high ratio between the on-current and the off-current. In digital circuits, the on-current, I_{on}, of a transistor is typically defined as the drain-source current, I_{DS}, when ($V_{GS} = V_{DS} = V_{DD} > 0$). Similarly, the off-current, I_{off}, is defined as I_{DS} when ($V_{GS} = 0, V_{DS} = V_{DD}$). I_{on} and I_{off} are thereby measures of the current drive and the leakage current, respectively. A high $\mathrm{I_{on}/I_{off}}$-ratio is desired since it yields a fast transistor when it is turned on and a low leakage transistor when it is turned off. Additionally, a high $\mathrm{I_{on}/I_{off}}$-ratio also contributes to better noise margins, making the circuit more robust against power supply noise, voltage drops and ground bounce. When optimizing the power consumption of a circuit by scaling down V_{DD}, I_{on} is inevitably scaled down, however, a low I_{off} is simultaneously desired for reducing the impact of the leakage current. Low leakage current reduces the impact of E_{leak} and thereby moves the MEP further down in the supply voltage range, enabling higher energy savings. Transistor sizing (particularly increasing L_{eff}) can to a certain degree be used to improve the $\mathrm{I_{on}/I_{off}}$-ratio. For example, at $V_{DD} = 250mV$, a minimum sized (W/L=120 nm/60 nm) NMOS has an $\mathrm{I_{on}/I_{off}}$-ratio of ~ 1100x, while an NMOS with W/L=150 nm/100 nm has an $\mathrm{I_{on}/I_{off}}$-ratio of ~ 1550x.

In addition to being a influential parameter when circuit speed and power are considered, I_{on} is also an important parameter when considering radiation tolerance. As charged particles pass in close proximity to sensitive circuit nodes, charge is is collected and thereby the voltage at these circuit nodes is altered. In order to prevent a radiation induced error from occurring, a high I_{on} is advantageous as it enables faster discharge of the collected radiation induced charge. Thus, scaling down V_{DD} entails not only reduction in the power consumption, but also an increase in the susceptibility to radiation induced errors. A more detailed discussion on radiation tolerance and supply voltage scaling is presented in Chapter 2.2.4.

In (2.6), it was also shown that I_{DS-sub} and thereby also I_{on} and I_{off}, are exponentially dependent on V_{th}. For long and wide channel transistors, assuming constant channel doping,

the V_{th} may be given as (2.8) [32]:

$$V_{th} = VTH0 + \gamma \cdot (\sqrt{\Phi_s - V_{BS}} - \sqrt{\Phi_s}) \tag{2.8}$$

where $VTH0$ is the threshold voltage at zero substrate bias ($V_{BS} = 0$), γ is the body bias coefficient, Φ_s is the surface potential and V_{BS} is the body-source voltage. On top of the body bias dependence, the geometrical parameters L_{eff} and W_{eff}, and bias conditions, V_{DS}, also contribute to determining V_{th}. The V_{th} dependence L_{eff} and W_{eff} was recognized several decades ago [33, 34] and is typically described through short-channel effect (SCE) for small L_{eff} and narrow-width effect (NWE) for small W_{eff}. In BSIM4 [32], these short- and narrow-channel effects contribute to either increase or decrease in V_{th} depending on the CMOS technology (e.g., well-engineering, doping, etc.), leading to a much more complex model than (2.8). Also covered by the BSIM4 model in [32] is the V_{th} dependence on V_{DS}, which is described through drain-induced barrier lowering (DIBL). DIBL causes V_{th} to decrease with increasing V_{DS}, giving rise to increased leakage currents. It is worth to note that DIBL is less pronounced in the subthreshold region than in the superthreshold region due to V_{DS} being below V_{th}. Nevertheless, for circuits operating a a wide supply voltage range, DIBL must be taken into consideration as it can contribute to increasing the leakage current when V_{DS} is high (e.g., non-linear P_{leak} in Figure 2.1). Since process variations cause variations in L_{eff} and W_{eff}, SCE, NWE and DIBL can have a magnified impact on V_{th} variations depending on transistor sizing. It is therefore favorable to size the transistors so that dV_{th}/dL_{eff} and dV_{th}/dW_{eff} are as small as possible, within the area, power and timing constraints.

2.1.2 Variability in Supply Voltage Scaled CMOS Circuits

Process variations pose one of the greatest challenges when it comes to designing reliable low-voltage circuits. It is therefore imperative that a great deal of attention is paid to variability in research and design of low-voltage SoCs [7, 35]. If not managed adequately, process variations can lead to over-design (e.g., wasted area, power, delay), reduced yield (e.g., timing violations) and/or failure of meeting the application requirements. Process variations can be divided into two categories: *Die-to-die* and *within-die* variations. Die-to-die variations are classified as the lot-to-lot and wafer-to-wafer variation which offsets all the transistor parameters (e.g., oxide thickness, L_{eff}, W_{eff}) on a single die, equally. On the circuit-level, this type of variations can be managed by utilizing adaptive body bias (ABB) [36] and AVS [37] globally on a die. Within-die variations have both a *systematic* and a *random* component which induce variations in transistor parameters across a die. Systematic variations are caused by gradients in the etching and lithography properties during fabrication. The systematic variations are deterministic and depend on the transistor location on the die and the transistor surroundings. Managing the systematic within-die variations may be accomplished using the same methods as for die-to-die variations, but using a certain granularity on the die (e.g., multiple supply voltage domains). Systematic within-die variations caused by layout dependent effects such as Well Proximity Effects [38] and Shallow Trench Isolation induced mechanical stress [39], can also be mitigated through careful layout techniques. Random variations, on the other hand, are probabilistic in nature and are caused by random uncertainties during fabrication. These include, but are not limited to, geometrical variations [40], local oxide thickness variations [41] and fluctuations

in the location and number of dopant atoms in the channel region [42], leading to identical transistors in close proximity exhibiting different electrical properties (i.e., mismatch). The impact of random variations can be reduced through utilizing increased logic depth [43], utilizing MTCMOS and through transistor sizing.

In general, random variations are regarded as a more problematic issue than systematic variations, since random variations are more difficult to suppress through design techniques. Out of the contributors to random variation, random dopant fluctuations (RDF) are considered to be the dominant source of mismatch in circuits operated in subthreshold region, especially as the transistor dimensions continue to shrink, and the number of dopants in the channel region continues to decrease [44]. The impact of random variations on V_{th} is traditionally modelled as (2.9) [45]:

$$\sigma V_{th} = \frac{A_{VT}}{\sqrt{W_{eff} \cdot L_{eff}}} \tag{2.9}$$

where A_{VT} is a the slope factor of σV_{th} which is inversely proportional to the square root of the transistor area. Several analytical models for A_{VT} have been proposed [46, 47], where the key features are linear dependence on the oxide thickness and fourth-root dependence on the channel dopant concentration. In 65 nm CMOS process, A_{VT} is typically ~ 3.5 (in units $mV \cdot \mu m$) for small-sized transistors suited for traditional digital logic implementation. Thus, a minimum sized NMOS transistor with $W/L = 120nm/60nm$ would have $\sigma V_{th} = 41.3mV$. Such large variations in V_{th} can have a significant impact on the circuit performance, depending on the transistors operating region.

Random variations in I_{on}, $\mathrm{I_{on}/I_{off}}$-ratio and inverter (INV) delay (t_{pd}) at multiple supply voltages were taken from the Process Development Kit (PDK) of a 65 nm CMOS process and are shown in Table 2.1. For minimum sized transistors operating in the subthreshold region (V_{DD}=0.18 V), $\sigma/\mu(I_{on})$ can be $>$ 10x higher than in the superthreshold region (V_{DD}=1 V). Increasing the transistor size reduces the impact of I_{on} variation in all regions of operation (as suggested by (2.9)), however this also increases the capacitive loading and thereby also the delay. For example, a $\sim 2x$ increase in area, reduces the I_{on} variation by $\sim 20\%$. A $\sim 2x$ increase in area improves also the $\mathrm{I_{on}/I_{off}}$-ratio by $\sim 30\%$ in the subthreshold region and by $\sim 80\%$ in the superthreshold region. However, in contrast to the I_{on} sensitivity to variation, the $\mathrm{I_{on}/I_{off}}$-ratio is more sensitive to variations in the superthreshold region than in the subthreshold region due to I_{on} having superthreshold sensitivity to variation and I_{off} having subthreshold sensitivity to variation. From Table 2.1 it can be seen that there is a dramatic decrease in the $\mathrm{I_{on}/I_{off}}$-ratio when scaling the supply voltage from V_{DD}=1 V to V_{DD}=0.18 V. This decrease can in fact become even more dramatic when both die-to-die and within-die variations are taken into account, which can lead to the $\mathrm{I_{on}/I_{off}}$-ratio being as low as 10x at V_{DD}=0.18 V, given 6σ variation. Also seen in Table 2.1 is the increase in inverter delay variations, where $\sigma/\mu(t_{pd})$ is $>$ 8x higher in the subthreshold region than in the superthreshold region. Random delay variations contribute to different components having different timing constraints. In order to meet the timing constraints of all components, the delay of the slowest component typically sets the maximum allowable clock frequency in synchronous designs. As a consequence of adhering to the timing of the slowest component, the impact of leakage current increases (i.e., E_{leak}) causing the MEP to move higher up in the supply voltage range. Figure 2.4 illustrates

this in the context of DFFs, however adding combinational logic to the equation would further increase the impact of E_{leak}, due to further reduced maximum frequency. As suggested by [43] and as seen in Table 2.1, the overall random delay variation in combinational logic can be reduced by optimizing the logic depth.

Due to the challenges imposed by operating in subthreshold region (e.g., low $\mathrm{I_{on}}$, low speed, high σ/μ), circuits are often operated in the near-threshold region, as it provides a trade-off between power saving, speed and manageability of process variations.

Parameter	Device	V_{DD}=0.18 V		V_{DD}=0.5 V		V_{DD}=1 V	
		μ	σ/μ	μ	σ/μ	μ	σ/μ
$I_{on}(A)$	NMOS (120/60)	1.121n	1.077	1.796μ	0.435	50.62μ	0.090
$I_{on}(A)$	NMOS (150/100)	817.9p	0.805	1.841μ	0.341	48.39μ	0.064
I_{on}/I_{off}	NMOS (120/60)	154.4	0.096	124.5k	0.340	3.245M	0.701
I_{on}/I_{off}	NMOS (150/100)	198.6	0.104	332.5k	0.236	5.894M	0.475
$t_{pd}(s)$	1x INV	532.3n	0.330	403.2p	0.216	20.37p	0.039
$t_{pd}(s)$	9x INV	5.191μ	0.191	3.773n	0.098	201p	0.019

Table 2.1: Mean (μ) and sigma/mean (σ/μ) values for I_{on}, $\mathrm{I_{on}/I_{off}}$-ratio and inverter delay (t_{pd}) as a result of random variations. Based on 200 samples.

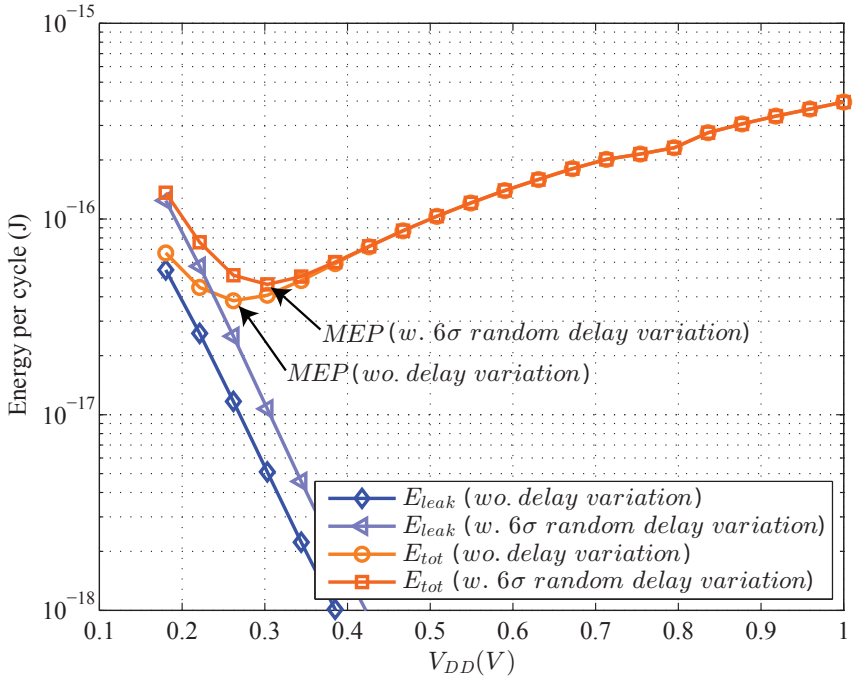

Figure 2.4: E_{leak} and E_{tot} with and without random delay variations for a DFF implemented in a 65 nm low-power CMOS process. Based on post-layout simulations.

2.2 Single Event Effects

Single event effects (SEEs) is a collective term used for describing radiation induced errors in digital electronics which are caused by single particle hits. SEEs are typically categorized in temporary, non-destructive errors and permanent, potentially destructive errors.

The subcategories of temporary, non-destructive SEEs are SETs, SEUs and single event functional interrupts (SEFIs). SETs are transient voltage fluctuations which are caused by charge collection, as a result of an inbound particle interacting with the sensitive nodes (typically reverse biased source/drain), in off-state transistors [48]. If an SET occurs internally in sequential circuits such as latches and flip-flops, or memory circuits such as SRAM, the SET may get latched and cause an SEU. An SEU can be defined as a change in the logic state of a memory element from a logic one to a logic zero or vice-versa. The SETs, although short in duration, can propagate through combinational logic and potentially get latched by latches or flip-flops and thereby cause erroneous logic states, also resulting in SEUs. SEFIs share similarities with SEUs, in terms of origin, as in both cases a storage element is affected by a particle hit. However, what distinguishes an SEFI from an SEU is that an error (i.e. an SEU) occurs in a control register which interrupts normal device operation for a prolonged time period [49]. Nevertheless, these errors (SET, SEU and SEFI) are considered to be temporary since the affected logic can be rewritten or reset to regain proper operational behavior.

Single event latchup (SEL) is a permanent and potentially destructive SEE where a parasitic thyristor structure is triggered by a high energy particle strike, forming a low impedance path between the supply voltage and ground. This leads to a high current state in the device and is typically corrected by turning the power supply off and back on in order to reestablish normal operation. If the SEL is left uncorrected for a longer time period, the high current path may result in a destructive IC failure.

With the continuous reduction of the supply voltage with technology scaling, SEL is becoming a lesser problem as it requires a high enough voltage differential (typically > 1.4 V) to turn on and maintain the parasitic bipolar devices. Since this work was based primarily on supply voltages of 1.2 V and below, SEL, although monitored, will not be a key topic and the primary focus will be on SETs and SEUs.

2.2.1 Radiation Environments

The most commonly associated radiation environment which electronic devices encounter is the naturally-occurring radiation environment in space. Electronic devices in space are exposed to primarily three sources of radiation: Galactic cosmic rays (GCRs), solar particle events (SPEs) and trapped radiation belts.

GCRs are energetic particles that enter the solar system from interstellar space (i.e., from outside the heliosphere). The GCR spectrum consists of most atomic elements, where hydrogen contributes to almost 90 % of the total composition. The particles are ionized, meaning they have been stripped of their electrons. As a result, the charged particles (protons and heavy ions) are affected by the solar wind and the magnetic fields of the sun and therefore the interplanetary and near-Earth GCR spectrum is modulated depending on the solar activity. Thus, for high solar activity, the GCR intensity decreases, and for low solar activity, the GCR intensity increases

[50].

SPEs also contribute to the interplanetary and near-Earth radiation environment. Solar particles originate from solar flares caused by energy build-up in the coronal magnetic field and from solar flares associated with Coronal Mass Ejections (CMEs) [51]. Of the two SPE mechanisms, CMEs are considered to be responsible for the major contribution of solar flare radiation in interplanetary space. Although these events are dominated by lighter particles (protons and electrons), the relatively smaller heavy ion contribution can still pose a threat to electronic devices [52, 53]. Figure. 2.5 shows the interplanetary radiation environment for nuclei ranging from hydrogen to uranium (Z = 1 to 92). The radiation environment is presented in the form of an integral linear energy transfer (LET[1]) spectrum[2] for GCR and worst week SPE conditions.

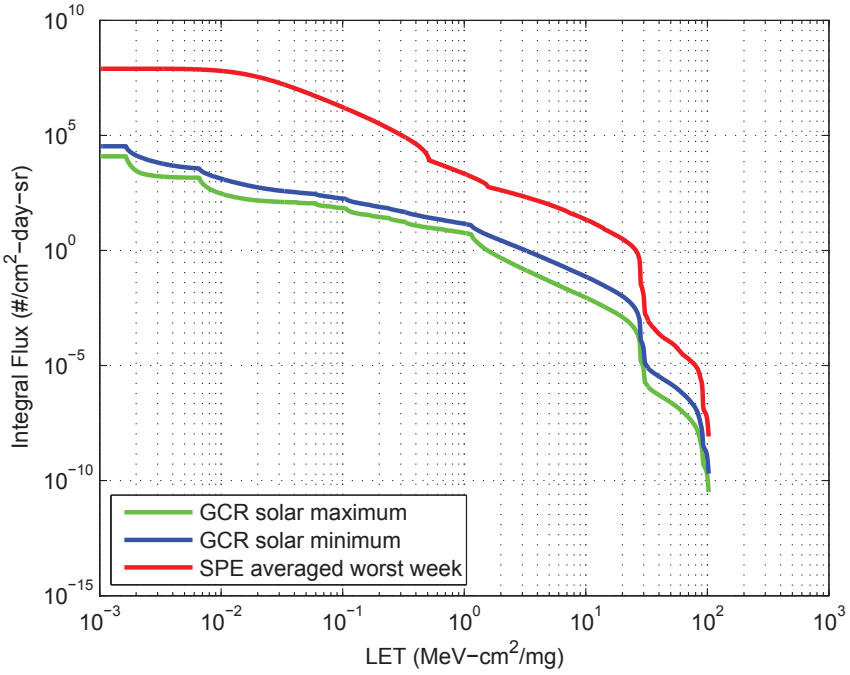

Figure 2.5: Integral LET spectra from CREME96 for interplanetary/geosynchronous orbit during maximum, during minumum and during worst week solar flare conditions. Based on 2.54 mm aluminum shielding.

While it is the GCRs and SPEs that pose the highest SEE threat to electronic devices operated in interplanetary/geosynchronous orbit, it is protons that pose the highest threat to electronic devices in low Earth orbit. Due to the Earth's magnetic field, GCR particle flux is attenuated, however, the magnetic field also contributes to trapping radiation (mainly protons and electrons) in what is known as the Earth's radiation belts. The intensity of the trapped radiation depends on the distance from the Earth's surface as well as solar activity, and the proton energy ranges between 1 keV - 300 MeV [51].

Electronic devices operated in the Earth's atmosphere can also experience SEEs. As GCRs penetrate into the Earth's atmosphere, interactions between the GCR particles and atmospheric

[1] A measure of energy loss of an energetic particle traversing a material. The concept of LET will be introduced in more detail in Chapter 2.2.2

[2] Integral LET spectra is the integral flux of all particles with LET values larger than the LET on the x-axis in Figure. 2.5

atoms cause secondary neutrons and protons which can occur down to sea level [54]. As with the radiation environment in space, the terrestrial radiation environment also depends on the altitude as well as the GCR modulation. Consequently, the impact of radiation is higher for avionics applications than for ground based applications, and the radiation intensity is typically lower during solar maximum than solar minimum [54]. Other terrestrial application areas where electronic devices are exposed to radiation environments include nuclear power plants, research (e.g., high energy physics) and defense systems.

Before electronic devices are deployed in a specific radiation environment, their radiation tolerance is often characterized by using particle accelerators. Particle accelerators mimic the radiation environment and the radiation tests are often performed with much higher flux than what would be encountered in the actual radiation environment in order to save time. One of the contributions of this thesis (Paper II [55]) deals with the topic of characterizing a particle accelerator for the purpose of radiation testing with protons, while two other contributions (Paper III [56] and Paper IV [57]) utilize heavy ion accelerators for characterizing the radiation tolerance of DFFs. After the radiation tolerance of a device has been characterized, radiation environment conditions such as the ones shown in Figure 2.5 may be used to estimate the error rate of the device.

2.2.2 Ionizing Energy Deposition and Charge Collection

Particle induced errors may be caused by either indirect or by direct ionization [58]. *Indirect ionization* is primarily caused by the lighter particles (e.g., protons and neutrons) through Rutherford scattering and/or nuclear reactions (elastic, inelastic). Charged particles interact primarily by Rutherford scattering (also known as Coulomb scattering) which occurs when an inbound particle passes within a short distance of an atomic nucleus of the target material an interacts with the nucleus through electromagnetic force. In such an event, equally charged particles would repel each other and can cause both excitation and liberation of atomic electrons [59]. For reduced distance between the particle and the nucleus, an elastic nuclear reaction may occur, creating a recoiling nucleus (i.e., Si recoil in a semiconductor). If the inbound particle interacts directly with the target nucleus, an inelastic nuclear reaction may occur, causing fragmentation and generation of potentially recoiling secondary particles. Any of the recoiling nuclei, either from elastic or inelastic nuclear reactions, can deposit energy along their path via direct ionization.

Direct ionization is when an energetic charged particle (e.g., heavy ion) traverses the target material and generates electron hole (e-h) pairs along its path, thereby ionizing the atoms in the target material. When a charged particle traverses matter, the charged particle loses kinetic energy and thereby also slows down, until it finally comes to a halt in the target material. The mechanisms involved in slowing down charged particles in matter are nuclear (i.e., nuclear interactions) and electronic (i.e., ionization) energy loss [60]. The electronic energy loss is used for describing the ionization caused by the interaction between charged particles and the matter which the particles traverse. The ionization is caused by the transfer of energy from the charged particle to the target nuclei, whereby bound electrons are freed and e-h pairs are generated.

The ionization potential of the material that a charged particle passes through is referred to as LET. The LET (2.10) approximates the amount of energy lost by the particle dE, per unit

length dx, per unit mass density ρ (often given in units of $\mathrm{MeV\text{-}cm^2/mg}$ in the field of radiation effects).

$$LET = \frac{dE}{dx} \cdot \frac{1}{\rho} \tag{2.10}$$

Based on the LET and the density of silicon ρ, the charge generated when the charged particle passes through silicon may be estimated for small path lengths by (2.11).

$$Q_{gen} = \frac{q \cdot LET \cdot \rho \cdot x}{E_{ehp}} \tag{2.11}$$

where, ρ is the material density, x is the path length, E_{ehp} is the energy required to produce a free e-h pair, and q is the elementary charge. If a sufficient amount of the generated charge is collected by a sensitive node in the semiconductor device, an error may occur as a result of the incident particle hit.

Charge collection occurs primarily through two fundamental carrier transport mechanisms: drift and diffusion. Charge collection through *drift* is highly dependent on the presence of an electric field. The presence of an electric field has an opposite effect on electrons and holes, causing electrons to move towards higher potential and holes to move towards lower potential. Thereby, e-h pairs located near an electric field will be separated and move in opposite directions. The drift current density of electrons ($J_{n,drift}$) and holes ($J_{p,drift}$) is given by (2.12) and (2.13), respectively [28]. The drift current density is proportional to the electric field (E), the carrier mobility (μ), the charge concentration (n for electron, p for holes) and the elementary charge (q).

$$J_{n,drift} = qn\mu_n E \tag{2.12}$$

$$J_{p,drift} = qp\mu_p E \tag{2.13}$$

Charge collection through *diffusion* is a slower process than charge collection through drift, and its current density is not determined by an electric field. Diffusion carrier transport is when carriers move from regions of high concentration to regions of low concentration. The diffusion current density for electrons ($J_{n,diff}$) and holes ($J_{p,diff}$) is given by (2.14) and (2.15), respectively [28]. The diffusion current density of electrons is proportional to the gradient of the charge concentration ($\frac{dn}{dx}$), the mobility and thermal energy dependent diffusion coefficient (D_n) and the elementary charge (q). Equivalent dependencies apply for the diffusion current density of holes.

$$J_{n,diff} = qD_n\frac{dn}{dx} \tag{2.14}$$

$$J_{p,diff} = -qD_p\frac{dp}{dx} \tag{2.15}$$

The total current density is thereby given by (2.16) for electrons and by (2.17) for holes [28].

$$J_n = qn\mu_n E + qD_n \frac{dn}{dx} \tag{2.16}$$

$$J_p = qp\mu_p E - qD_p \frac{dp}{dx} \tag{2.17}$$

The drift and diffusion equations presented here are only meant to illustrate the basic principles involved in the charge collection mechanism after a charged particle strike. In order to more accurately predict the magnitude and rate of charge generation and collection, three-dimensional (3D) technology computer aided design (TCAD) device simulators need to be utilized [61, 62]. These tools solve the Poisson-, current continuity [63] and the drift-diffusion equations in (2.16) and (2.17), all in a 3D-environment. In addition, the TCAD tools also incorporate other transport models such as hydrodynamic transport, which is more suitable for the state-of-the-art semiconductor devices than the drift-diffusion model [64].

One of the drawbacks with using TCAD is that it is highly computation intensive, making it time consuming to simulate large size circuits. In response to the challenges imposed by TCAD simulations, several charge collection estimation models have been proposed to speed up simulations of SEEs: integral rectangular parallelepiped (IRPP) [65], Messenger double exponential [66], electric-field funnel model [67] and ambipolar-diffusion-with-cutoff (ADC) model [68]. Each of the models have their limitations and requirements, and vary in terms of their applicability depending on technology, circuit size and required recourses. Nevertheless, several of these models have evolved to meet the challenges introduced by CMOS technology scaling, such as [68, 69], which model charge sharing and [69] which models parasitic bipolar effect.

2.2.3 Basic SEE Mechanisms in Latches and Flip-flops

The mechanisms leading up to a potential error as a result of an single charged particle passing through a radiation sensitive volume in a semiconductor device are shown in Figure 2.6[70].

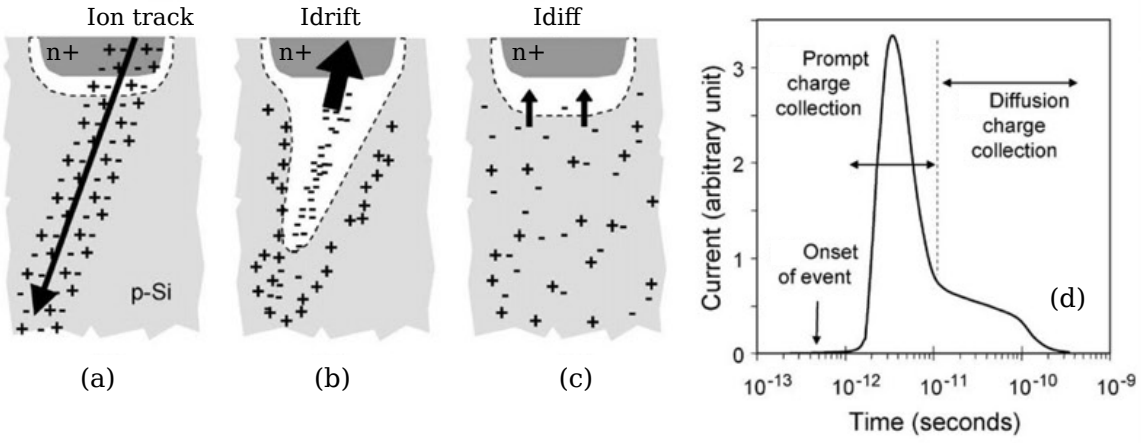

Figure 2.6: Conceptual illustration of eh-pair generation (a) as a result of a single charged particle strike, charge collection through drift (b), charge collection through diffusion (c) and the resulting current at the circuit node (d) [70].

When ionizing radiation particles such as alpha particles and heavy ions etc. pass through semiconductor material, e-h pairs are generated along its track (Figure 2.6(a)). A lot of the e-h pairs are recombined if located far away from electric fields. However, if the particle passes through a region with an electric field, such as a reverse biased pn junction, the electrons and and holes are separated and the free carriers are collected by the circuit node represented by the pn junction. In addition to prompt charge collection by the electric field, the ionization track also alters the shape of the electric field, forming a funnel which extends the area of the electric field and enhances the charge collection efficiency. This causes a rapid charge collection by drift, which has a duration in the picoseconds range (Figure 2.6(b)). Although not an initial dominant charge collection mechanism, the free carriers located further away from the electric field are also being collected, but through diffusion (Figure 2.6(c)). Since diffusion is a much slower carrier transport mechanism than drift, the charge collection by diffusion becomes more visible after the charge collection by drift has subsided, and has a duration in the nanoseconds range (for nominal supply voltages). On the circuit level, the particle induced charge collection translates into a current spike, which in turn, results into a temporary voltage spike (Figure 2.6(d)). This temporary voltage spike occurring in an internal circuit node due to a particle hit is classified as an SET.

If an SET occurs internally in sequential circuits such as latches and flip-flops, or memory circuits such as SRAM, the SET may get latched and cause an SEU. Furthermore, SETs can also propagate through combinational logic and potentially get latched by latches or flip-flops, thereby increasing the probability of SEUs. Figure 2.7 shows a DFF realized using standard latches in a master-slave configuration. In a standard latch topology there are two fundamental ways of getting an SEU, both occurring during the window of vulnerability (WOV) [71]. The mechanisms behind SEU occurrence are identical for both the master latch and the slave latch, however, for simplicity, the master latch will be used for describing SEU occurrence in latches.

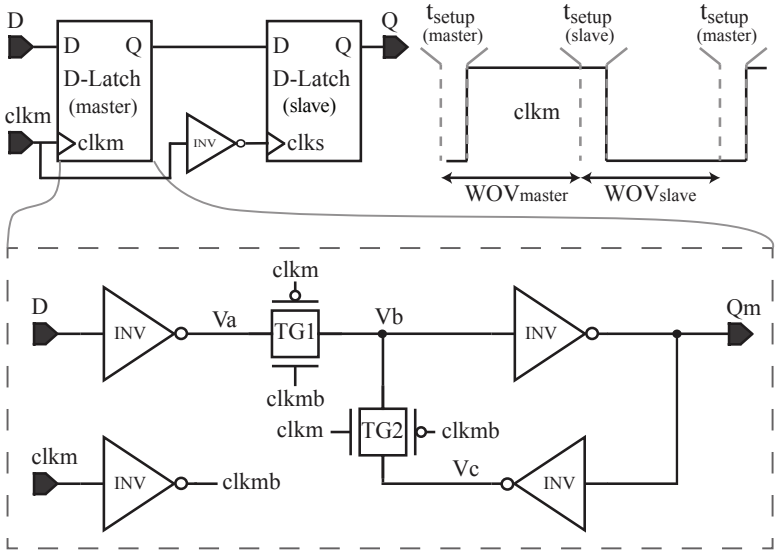

Figure 2.7: Standard master-slave DFF and illustration of the WOV for a DFF.

A requirement for a particle induced SET to occur is that the particle induced charge collection (Qcoll) is greater than the critical charge (Qcrit) of the node of impact. The critical charge of a node is the required charge to establish a voltage transient larger than the switch-

ing threshold of a logic element interconnecting to the node of particle impact. Thereby, given $\mathrm{Qcoll} > \mathrm{Qcrit}$, an SEU can occur in a latch when:

1) Particle induced charge collection appears in the latch feedback (nodes *Vb*, *Vc* or *Qm*) when TG1 is off and TG2 is on (during $\mathrm{WOV}_{\mathrm{master}} - \mathrm{t}_{\mathrm{setup\ (master)}}$). The resulting SET propagates through the feedback and replaces the original stored voltage with the value of the SET, creating an SEU.

2) Particle induced charge collection (i.e an SET) appears on the latch input (*D* or *Va*) at the rising edge clkm (during $\mathrm{t}_{\mathrm{setup\ (master)}}$), right before TG1 closes). The transient error propagates to node *Vb* through TG1, latching the SET instead of the correct voltage.

In master-slave DFF operation, when *clkm* is high the master latch is holding the DFF output value (*Q*) in its feedback, while the slave latch is transparent. On the other hand, when *clkm* is low the master latch is transparent, while the slave latch is holding the DFF output value (*Q*) in its feedback. Thereby, given that *clkm* is high, an SEU would occur in the master latch and be propagated to the slave latch when *clkm* goes low. When *clkm* is low, an SEU would occur in the slave latch, meaning that the SEU would last for only half a clock period. Furthermore, a DFF is also susceptible to SETs on *clkm*. For example, if an SET occurs at *clkm* after rising edge of *clkm*, and after the data input (*D*) has settled to a new value which is different from when *clkm* first went high, the new value at the data input would get latched, creating an SEU.

More information on how SETs and SEUs occur in standard non-radiation tolerant DFFs and radiation tolerant DFFs is given in Paper III and Paper IV.

2.2.4 Soft Error Dependence on Supply Voltage

Ever since the early adaptation of the Qcrit concept [72], in 1978, it was apparent that the the soft error sensitivity increases with decreasing supply voltage. Already back then it was predicted that the soft error sensitivity will increase with technology and supply voltage downscaling [73]. Consequently, supply voltage scaling has been investigated as a means for reducing the soft error sensitivity, by increasing the supply voltage of critical components [74]. However, since the technology scaling was inevitable, identifying the future challenges imposed by reduced supply voltages was also an important research area [75, 76]. As the supply voltages have scaled down, research efforts have led to the incorporation of error-correcting code (ECC) in radiation tolerant memory design [73, 77] as well as circuit-level and layout-level soft error mitigation techniques such as TMR [9, 78], dual redundancy [11], spatial hardening (e.g., charge sharing mitigation) and temporal hardening [13, 14].

As a first step towards describing the soft error dependence on supply voltage, we can look at the relationship between Qcrit and the electrical parameters, given by (2.18) (based on [79]):

$$Qcrit = C_n \cdot V_{trip} + I_r(V) \cdot t_{trip} \tag{2.18}$$

where, C_n is the total node capacitance and V_{trip} is the voltage swing required to produce an SET or an SEU, $I_r(V)$ is the restoration current (equivalent to the current drive) of the interconnecting transistor, which is dependent on the voltage across the transistor, and t_{trip} is time required until an SET or an SEU occurs. When determining Qcrit for an SET, t_{trip} is the

time required for the circuit node to charge up to the switching threshold of a logic element interconnecting to the node of particle impact. When determining Qcrit for an SEU, t_{trip} is the time required for the memory node to flip. Since technology scaling entails the reduction of nodal capacitance (C_n) and supply voltage reduction entails reduction of switching threshold (V_{trip}), it becomes evident that these two factors contribute to decreased Qcrit and thereby increased soft error sensitivity. Additionally, as seen in Chapter 2.1.1, reducing the supply voltage also reduces the current drive of the transistor, which reduces $I_r(V)$ and thereby causes a further decrease in Qcrit. Studies have shown that technology scaling alone (from 350 nm to 50 nm) has contributed to a 18x decrease of Qcrit in latches [80, 81]. Supply voltage scaling, on the other hand, has an even more adverse effect on Qcrit. By scaling the supply voltage from 1 V to 0.5 V in the 65 nm CMOS process used Paper IV, Qcrit is reduced by a factor of 9x. By scaling the supply voltage from 1 V to 0.18 V, Qcrit is reduced by a factor of 93x. Although the Qcrit methodology serves as convenient method for describing the radiation tolerance of a circuit or a circuit node, other effects such as *charge sharing*, *SET pulse widths* and *charge collection efficiency* also influence the radiation tolerance, especially in circuits employing radiation hardening techniques.

Both *charge collection efficiency* and the duration of the *SET pulse widths* are influenced by supply voltage scaling. Since the supply voltage has an direct impact on the strength of the electric field, charge collection efficiency will therefore also be affected. As seen in Chapter 2.2.2, the charge collection via drift is proportional to the strength of the electric field, indicating that charge collection via drift is reduced with decreasing supply voltage. This leads to the total charge collected as a result of a charged particle hit to be reduced by orders of magnitude, if the supply voltage is scaled down sufficiently (down to the subthreshold region) [82]. Furthermore, reducing the supply voltage also reduces the impact of *Parasitic bipolar effect* due to reduced voltage across the pn junctions in the transistors, making parasitc bipolare devices less efficient, leading to further reduction of the collected charge [82, 83]. On the other hand, reduction of the supply voltage also reduces the current drive of the transistors by up to several orders of magnitude, which contributes to slower recovery of the affected node and ultimately leads to increased SET pulse widths. By scaling the supply voltage from 1.2 V to 0.2 V, it was observed (using device simulation) that a reduction in the collected charge by 3 orders of magnitude, a reduction in the current drive by 6 orders of magnitude, which resulted in an increase in SET pulse widths by 3 orders of magnitude, for LET = 100 $\mathrm{MeV\text{-}cm^2/mg}$ [82]. Additionally, the SET pulse width dependence on LET was studied in [84], showing that the LET dependence decreases as the the supply voltage scales down. At a supply voltage of 0.2 V, there was no difference in the full width half rail (FWHR) SET pulse withs caused by LET = 1 $\mathrm{MeV\text{-}cm^2/mg}$ and LET = 100 $\mathrm{MeV\text{-}cm^2/mg}$.

Another supply voltage dependent mechanism which affects the soft error sensitivity is *charge sharing* [62, 85]. Charge sharing is when multiple nodes collect the charge generated by a single charged particle hit. When a charged particle strikes a sensitive area on the die, charge is generated in a radial proximity of the actual impact location. In addition to the struck transistor collecting the charge, also the adjacent transistors may collect portions of the generated charge, given short distance between adjacent transistors and high enough particle LET. Charge sharing mitigation is important when designing radiation tolerant circuits which incorporate redundancy. For example, TMR would be inefficient if 2 out of 3 memory nodes

experience charge sharing. Therefore, redundant nodes must have sufficient separation in order to mitigate charge sharing. When the supply voltage scales down, the adjacent nodes become more sensitive to charge sharing due to reduced Qcrit. As a result, the increased charge sharing sensitivity needs to be taken into account when designing redundancy-based radiation tolerant circuits which are aimed at operating at a wide supply voltage range.

Despite charge sharing being a potentially harmful charge collection phenomenon, charge sharing can also be exploited for increasing the single-event tolerance. One example is the layout principle called "Layout Design through Error Aware Positioning" (LEAP) [12, 86]. By using the LEAP principle, charge sharing between adjacent transistors cancels (partially or fully) the overall effect of the single event in the circuit. This is enabled by the transistors opposite reaction to the charge collection as a result of an particle hit. Recently, preliminary studies have shown that the LEAP principle provides increased SEU tolerance in supply voltage scaled DFFs [87].

Another single event mechanism exploiting charge sharing is *pulse quenching* [88]. Pulse quenching describes the effect of SET pulse width reduction as a result of charge sharing between adjacent transistors. For example, given two series coupled inverters, an ions strike at the first inverter will result in an SET with a pulse width proportional to the ion LET and that SET would propagate to the input of the second inverter. However, if the charge generated by the ion strike is also collected by the second inverter, the second inverter experiences a delayed charge collection. This delayed charge collection in the second inverter negates the SET from the first inverter and can thereby reduce the resulting SET pulse width at the output of the second inverter. Pulse quenching in conjunction with supply voltage scaling was studied in [82], showing that pulse quenching has the most noticeable effect at nominal supply voltage and for high LET. Nevertheless, as a result of pulse quenching, the SET pulse width as well as the LET dependence of the SET pulse width decreased at all supply voltages. On the other hand, Ahlbin et.al. [89] showed that pulse quenching was most noticeable at supply voltages between 0.7 V and 0.5 V, while no pulse quenching was observed at supply voltages above 0.8 V. Both these studies indicate that pulse quenching can be effective at several supply voltages, given that pulse quenching conditions (propagation delay and transistor spacing, charge collection efficiency, etc.) are met. However, the effectiveness of pulse quenching may vary when covering a wide range of supply voltages, due to large variations in propagation delay and charge collection efficiency.

In this thesis, the SEU mitigation efficiency of DFFs employing TMR, DICE, temporal-, spatial-, and drive strength hardening is investigated at a supply voltage range between 0.18 V and 1 V, using heavy ion irradiation with LET = 5.8 - $68.8\ \mathrm{MeV\text{-}cm^2/mg}$. In Paper III, the SEU mitigation efficiency of temporal- and spatial hardening is examined in a temporally redundant DFF topology. As shown in [82], by scaling down the supply voltage, the delay of CMOS circuits increases at a faster rate than the SET pulse width. Consequently, temporal redundancy is an interesting SEU mitigation technique at low supply voltages since the performance penalty induced by SET filters may be lower at reduced supply voltages than at nominal supply voltages. In Paper IV, the SEU mitigation efficiency of the commonly used hardening techniques TMR, DICE and temporal redundancy are investigated. The SEU mitigation efficiency of the hardening techniques is compared. Additionally, the impact of drive strength hardening is also presented.

Chapter 3

Summary of paper contributions

This chapter presents summaries of each of the paper contributions of this thesis. The paper contributions include subthreshold to above threshold level shifter design (Paper I), characterization of the proton beam at OCL (Paper II), and the design and radiation tolerance characterization of DFF topologies aimed at operating at a wide supply voltage range for optimizing power- and energy consumption (Paper III and Paper IV). In addition to summaries of the paper contributions, supplementary information is also given in this chapter for some of the papers. The purpose of the supplementary content is to provide further information on the topics covered in the papers, and to add information that is relevant to the thesis (e.g., information that did not fit the page limit of the papers).

3.1 Paper I : Low-power subthreshold to above threshold level shifters in 90 nm and 65 nm process

3.1.1 Introduction

Many low power applications require ICs to be flexible in terms of the trade-off between power consumption and performance. In order to achieve such flexibility, methods such as dynamic frequency scaling (DFS) and dynamic voltage scaling (DVS) are often used. Additionally, ICs can also utilize MSV domains, where low power sections of the ICs are supplied by a low supply voltage (VDDL), and where high performance sections are supplied by a high supply voltage (VDDH). MSV domains are also commonly used in AVS schemes for managing the impact of process-, voltage- and temperature (PVT) variations, and in order to interface the different supply voltage domains, level shifters are required.

Paper I [21] (see reprint on p. 55) presents a level shifter topology aimed at converting subthreshold signals to above threshold signals. Conventional level shifters are not suited for converting subthreshold signals as they suffer from an uneven pull-up/down ratio. This is due to the conventional level shifter having weak pull-down transistors, which are controlled by subthreshold signals, and strong pull-up transistors, which are controlled by above threshold signals.

In order to mitigate the uneven pull-up/down ratio, the proposed level shifter uses multi-threshold CMOS (MTCMOS) design technique. The weak pull-down transistors are replaced

with low threshold voltage (LVT) transistors, while the strong pull-up transistors are replaced with high threshold voltage (HVT) transistors. Furthermore, diode-connected and off-biased PMOS transistors are utilized in the pull-up paths, thereby limiting the current and making it possible to optimize the pull-up/down ratio for the intended digital input voltage range.

3.1.2 Summary of results

Two versions of the proposed level shifter were designed in a 90 nm bulk CMOS process, one for high speed (MDCVSHS) and one for low power (MDCVSLP). Additionally, one version was also designed in a 65 nm bulk CMOS process (MDCVS65). All the level shifters were extensively verified across process- and mismatch variations. The MDCVS65 was also verified using a temperature range between -40 °C and 150 °C.

The MDCVSHS level shifter achieved a propagation delay of 32 ns, energy consumption per transition of 17 fJ and static power consumption 2.5 nW, while converting 180 mV digital input signals to 1 V digital output signals. The transistors in the MDCVSLP version of the level shifter were sized to reduce the static power consumption of the MDCVSHS level shifter. The MDCVSLP version achieved a propagation delay of 120 ns, energy consumption per transition of 21 fJ and static power consumption 1 nW, under the same input and output conditions as the MDCVSHS level shifter.

Since the 65 nm version of the level shifter (MDCVS65) was designed using a low power process, the threshold voltages of the 65 nm transistors were generally higher than the threshold voltages of the 90 nm transistors. As a result, lower static power consumption was achieved at the expense of increased minimum input voltage. The MDCVS65 level shifter performs with a propagation delay of 64 ns, energy consumption per transition of 23 fJ and static power consumption 84 pW, while converting 350 mV digital input signals to 1.2 V digital output signals.

All level shifters are designed with sleep-mode and isolation capability while making use of a single dual-height cell physical implementation strategy.

3.2 Paper II :Proton beam characterization at Oslo Cyclotron Laboratory for radiation testing of electronic devices

3.2.1 Introduction

Electronic devices utilized in space applications are often exposed to various types of ionizing radiation which can both cause permanent damage to the device and/or cause the devices to malfunction. Since protons are one of the main radiation sources in space, accelerated proton testing is an important part of radiation assurance for electronic devices. Having access to such irradiation facilities is therefore of great advantage for space related research activities conducted at a research institute.

Since the University of Oslo has a cyclotron with a proton beam, work was initiated for evaluating its beam properties for the purpose of using the beam for radiation testing of ICs. Paper II [55] (see reprint on p. 66) presents the proton beam characterization, with focus on determining the accuracy of the proton flux and fluence, as well as investigating methods for beam-to-target alignment. The methods used for the beam characterizations are also evaluated for the purpose of providing dosimetry during radiation testing. This work was conducted using 30 MeV protons, with a future goal in mind of using proton energies between 1 MeV to 30 MeV. Within this energy range, it is especially the lower part (1 MeV - 2 MeV) which is of high interest for radiation testing of both contemporary and future CMOS circuits, due to proton direct ionization being high in this particular energy range.

3.2.2 Summary of results

The proton beam characterization provided initial insight in the beam properties of the proton beam at the Oslo Cyclotron Laboratory (OCL). The flux and fluence were characterized by utilizing two particle detectors, placed on the outskirts of the beam line, which measured the scattered protons. Prior to each irradiation run, the particle detectors need to be calibrated. During calibration, a Faraday cup was placed in the center of the beam line for calibrating the ratio of direct protons detected by the Faraday cup to the scattered protons detected by the particle detectors. For calibration of the particle detectors, it was found that calibration runs of 240 s were sufficient for reducing the axial gain error (i.e., the uncertainty of the detector calibration) to 1.22 %. After calibration, the Faraday cup can be removed, and a DUT can be inserted for irradiation. The detectors can then be used for monitoring the on-line flux. In Paper II, the on-line flux was monitored with 40 second intervals.

In order to determine the beam-to-target alignment, a beam profile measurement method was utilized. The proposed method makes use of dosimeter film, which is sensitive to radiation dose, which in turn is proportional to proton intensity. By utilizing the dosimeter film in conjunction with a collimator, the location of the DUT can be located in the beam profile. The location of the DUT was identified by comparing the dosimeter films in front and behind the collimator. Furthermore, a more accurate assessment of the average flux at the DUT could also be made since the location of the DUT in the beam profile could be identified. During beam profile measurements, it was discovered that it may be difficult to align a potential DUT to the center of the beam. Measurements showed 23 % lower average flux observed at the DUT, compared

to the average flux observed at the center of the beam.

Although the particle detectors and the dosimeter film provide the means of average flux measurements, the method is not suitable for accurate on-line flux measurements at the DUT, due to the need of processing the dosimeter film after each irradiation run. Since the dosimeter film needs to be processed after each run, temporal resolution of the flux is lost, and only the average flux (fluence/irradiation time) can be derived form the detector counts and the dosimeter film processing.

Beam stability characterization was also performed. Here, it was discovered that the beam intensity variation can have and relative standard deviation of 4.78 %. Furthermore, it was also discovered that the beam tends to slightly drift in space.

Finally, preliminary electrical tests were performed using low voltage digital CMOS circuits operated in the subthreshold region ($\mathrm{V_{DD}} = 0.35\ \mathrm{V}$). The tests showed that the CMOS circuits were susceptible to the noise in the cyclotron environment, which was sufficient to cause erroneous behavior in the circuits.

3.3 Paper III : Supply Voltage Dependency on the Single Event Upset Susceptibility of Temporal Dual-Feedback Flip-Flops in a 90 nm Bulk CMOS Process

3.3.1 Introduction

With the continuous scaling of CMOS technology and with an increasing demand for low power consumption, CMOS devices will be required to operate at much lower supply voltages than in the past. Terrestrial applications, such as portable devices, battery powered devices, IoT gadgets etc., have greatly benefited from CMOS technology scaling and low power CMOS design techniques. Since many spacecraft utilize solar power as their main source of power, it is therefore important to investigate the radiation tolerance of supply voltage scaled CMOS circuits in order to increase the power efficiency of the circuits utilized in space applications.

DFFs are one of the most important sequential building blocks used for realizing digital functionality in ICs. In Paper III [56] (see reprint on p. 73), four radiation tolerant DFF topologies are investigated in terms of their radiation tolerance against heavy ions, across a wide supply voltage range (0.18 V to 1 V). The DFFs have been designed and fabricated in a low-power commercial 90-nm bulk CMOS process and were tested using heavy ions with LET between $8.6\,\mathrm{MeV\text{-}cm^2/mg}$ and $53.7\,\mathrm{MeV\text{-}cm^2/mg}$. Three of the TDF (Temporal Dual-Feedback) DFFs employ a proposed temporal hardening topology while the forth DFF is based on the DICE topology. The proposed topology is presented in detail with charge injection simulations, and the impact temporal and spatial hardening has on the SEU sensitivity is analyzed. Furthermore, a performance comparison of the DFFs i performed and an evaluation of potential energy consumption savings offered by supply voltage scaling is also presented.

3.3.2 Summary of results

In this work, supply voltages of 0.5 V and below were of highest interest since it was expected that the TDF DFFs would exhibit low radiation tolerance due to short SET filter delay at $\mathrm{V_{DDL}} = 1\mathrm{V}$. The highest radiation tolerance achieved in this work was by a TDF DFF, which achieved an SEU cross-section below $1.9 \cdot 10^{-10}\mathrm{cm^2/bit}$ (no SEUs detected) at $\mathrm{V_{DDL}} = 0.5\mathrm{V}$, $4 \cdot 10^{-10}\mathrm{cm^2/bit}$ at $\mathrm{V_{DDL}} = 0.25\mathrm{V}$, and $2 \cdot 10^{-9}\mathrm{cm^2/bit}$ at $\mathrm{V_{DDL}} = 0.18\mathrm{V}$. The general observation was that the SEU sensitivity increases as the supply voltage decreases. A comparative study of temporal- and spatial hardening showed that temporal hardening (i.e., longer SET filter delay) is a more efficient SEU mitigation technique than spatial hardening (i.e., wider sensitive node spacing) for the TDF DFFs at $\mathrm{V_{DDL}} = 0.5\mathrm{V}$. As the supply voltage decreases and the LET increases, the impact of charge sharing becomes more dominant, making temporal hardening less efficient and spatial hardening more important. By increasing the sensitive node spacing, a higher radiation tolerance is achieved at low supply voltages, given that the SET filter delay is long enough to filter out the occurring SETs.

In terms of potential energy consumption savings, when scaling the supply voltage from 1 V down to 0.5 V, 0.25 V and 0.18 V, the proposed DFFs achieve at least -72 %, -92.5 % and -95 % (respectively) reduction in energy per transition compared to a DICE DFF when operated

at a supply voltage of 1 V.

Although the first prototype of the TDF DFF showed low SEU sensitivity, particularly at $\mathrm{V_{DDL}} = 0.5\mathrm{V}$, further investigation is needed. Further work includes exploring the SEU dependence on angled hits, reducing the area, improving the performance and improving the SEU tolerance at $\mathrm{V_{DDL}} = 1\mathrm{V}$. These aspect are looked into in Paper IV.

3.3.3 Supplementary content: SET filter delay measurements

In Paper III, Table II, the feedback delay of TDFCS is only slightly longer (4% - 8 %) than that of the TDF4D. Such a small increase in delay does not match the improvements in SEU cross-section offered by the TDFCS compared to TDF4D. Therefore, it is suspected that for the prototype IC used during irradiation, the SET filter delay of the TDFCS was in fact relatively longer than that of the TDF4D. The reason behind this assumption is that the delay values in Table II are based on post-layout simulations which do not account for noise sources and process variations. In reality, the bias node *biasN* was coupled to V_{DDL} using a long cable, which made the bias signal susceptible to noise. Any noise signal which would drive the the bias node *biasN* down, would also result in driving the bias node *biasP* up, causing an increase in the delay. When operated in the subthreshold region, the delay becomes even more sensitive to noise due to the subthreshold current sensitivity (as shown in Chapter 2.1.1). Moreover, process- and mismatch variations can cause additional shifts in the device parameters, resulting in large delay variations, especially when subthreshold operation is taken into account (discussed in Chapter 2.1.2).

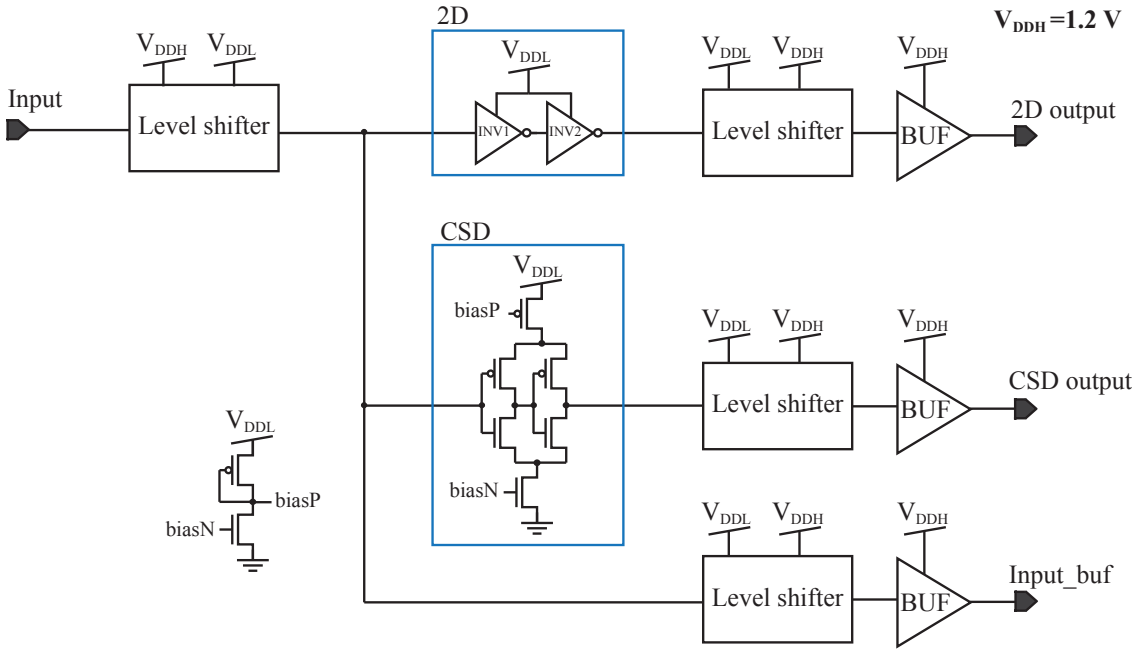

Figure 3.1: Illustration of the test structures used for delay measurements.

Based on the suspicions described above, the delay of the current starved inverter delay element (CSD) and the delay of a delay element composed of two inverters (2D) was investigated[1].

[1]Measurements were performed February 12th, 2017.

The prototype IC had a test structure which consisted of these two delay elements (shown in Figure 3.1). Figure 3.2 shows the measurement results for $\mathrm{V_{DDL}} = 0.25V$ and $\mathrm{biasN} = 0.25V$. By comparing the delay in Table II (Paper III) to the delay in Figure 3.2, the 2D delay is 1.45x longer than predicted by post-layout simulations and the CSD delay is 3.97x longer than predicted by post-layout simulations. By extrapolating the measurement results of the 2D delay to the 4D delay (as in the feedback delay of TDF4D), the 4D delay is only 1.03x longer than predicted by post-layout simulations. This confirms that the SET filter delay of TDFCS was significantly longer than that of the TDF4D. Based on the delay measurements, the feedback delay of TDFCS was ∼650 ns, while the feedback delay of TDF4D was ∼200 ns, at $\mathrm{V_{DDL}} = 0.25V$. The feedback delay of the TDF8D can also be extrapolated form these results, resulting in ∼400 ns, meaning that the feedback delay of TDFCS was also longer than that of the TDF8D at $\mathrm{V_{DDL}} = 0.25V$.

Also shown in Figure 3.2 is that $biasN$ is ∼0.225 V at the IC pin, even though the applied voltage is 0.25 V. This voltage drop also contributes to increased delay in CSD delay element. Figure 3.3 shows a scenario where $\mathrm{V_{DDL}} = 0.25V$ and $\mathrm{biasN} = 0.5V$. It can be observed that the delay of CSD is reduced by almost a factor 2 compared to when $\mathrm{biasN} = 0.25V$. By setting $\mathrm{biasN} > V_{DDL}$, the bias circuit receives a better controlled input voltage, resulting in a reduction in the CSD delay.

The delay was also measured at $\mathrm{V_{DDL}} = 0.18V$ and $\mathrm{V_{DDL}} = 0.5V$, where the same trends were observed as for $\mathrm{V_{DDL}} = 0.25V$, meaning that the feedback delay of TDFCS is longer than that of TDF4D and TDF8D.

Taking the delay measurements into consideration, the conclusions presented in Paper III are still valid: Temporal hardening has an increasing impact on the SEU sensitivity of the proposed DFF with increasing supply voltage and decreasing LET. Spatial hardening has an increasing impact on the SEU sensitivity of the proposed DFF with decreasing supply voltage and increasing LET.

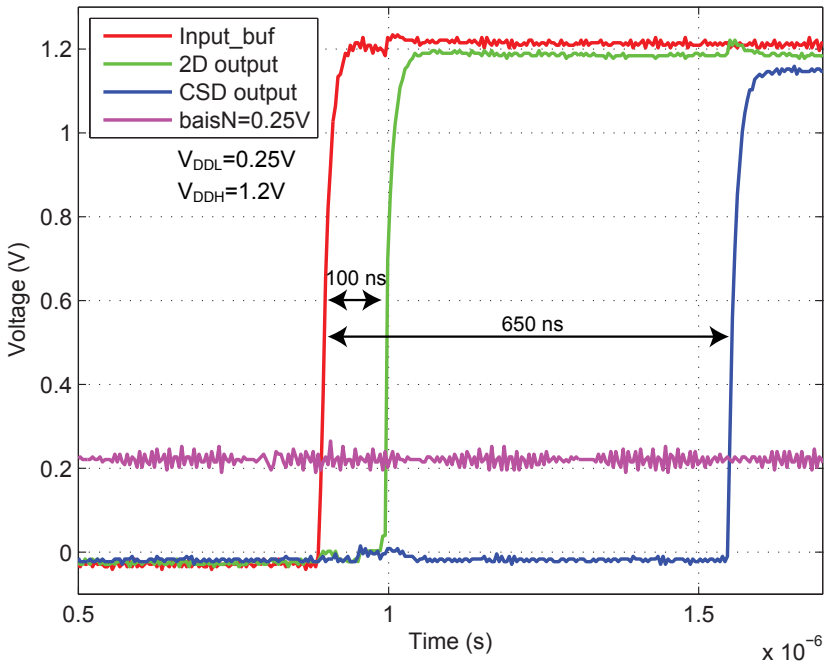

Figure 3.2: Delay of 2D and CSD at $\mathrm{V_{DDL}} = 0.25V$ and $\mathrm{biasN} = 0.25V$.

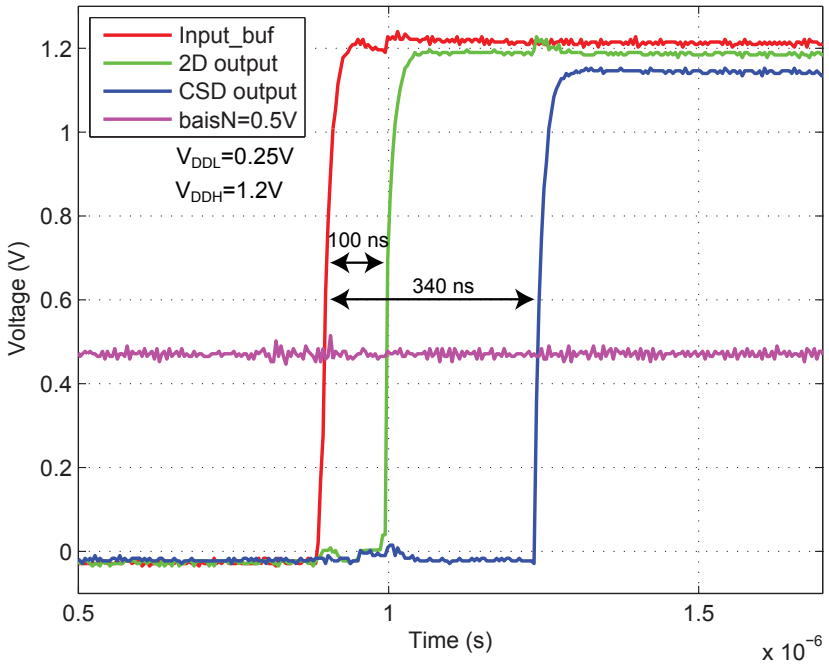

Figure 3.3: Delay of 2D and CSD at $\mathrm{V_{DDL}} = 0.25V$ and $\mathrm{biasN} = 0.5V$.

3.4 Paper IV : Heavy Ion Characterization of Temporal-, Dual- and Triple Redundant Flip-Flops Across a Wide Supply Voltage Range in a 65 nm Bulk CMOS Process

3.4.1 Introduction

Paper IV [57] (see reprint on p. 85) aims at furthering the research conducted in Paper III [56], by testing and comparing a wider range of DFF hardening techniques. For this purpose, five radiation tolerant DFFs, employing temporal-, dual- and triple redundancy were designed and fabricated in a low-power commercial 65 nm bulk CMOS process. The radiation tolerance of the hardened DFFs is compared to the radiation tolerance of a standard, non-radiation tolerant DFF.

The DFF topologies, layout and sensitive node spacing are presented in detail. In this work, three temporal redundant DFFs are used, where two of the DFFs utilize current starved inverter based delays for SET filtering, and one DFF utilizes inverter based delays for SET filtering. The two first DFFs (TDFCS/TDFCSLT) offer a performance improvement compared to the proposed DFF topology presented in [56], while the latter DFF (TDF) is identical to the most radiation tolerant DFF (TDF8D) in [56], for comparison. Additionally, a DICE DFF and a TMR DFF are also examined. The SEU tolerance of the DFF topologies is evaluated at supply voltage range of 0.18 V to 1 V, using heavy ions with LET between $5.1\,\mathrm{MeV\text{-}cm^2/mg}$ and $99.1\,\mathrm{MeV\text{-}cm^2/mg}$.

3.4.2 Summary of results

The results show that radiation tolerant DFFs offer 14x to 1328x improvement in the SEU sensitivity compared to a standard DFF, depending on the supply voltage, heavy ion LET and angle of incidence. Temporal hardening showed to be an efficient SEU mitigation strategy at supply voltages between 1 V and 0.5 V, given that the SET filtering delay is sufficiently high. However, as supply voltage scales below 0.5 V, the SEU mitigation efficiency decreases due to reduced SET recovery efficiency. Additionally, results show that utilizing high drive strength components in temporal redundant DFFs can offer an improvement in the SEU rate of 3x to 112x over temporal redundant DFFs utilizing standard drive strength components, for supply voltages of 0.5 V and below.

Hardening techniques such as the DICE can also be efficient SEU mitigation techniques at supply voltages between 1 V and 0.5 V, however, sensitive node spacing showed to have a major impact on the SEU rate with decreasing supply voltage and with increasing LET. At the lowest supply voltage (0.18 V), the TMR DFF showed the best SEU tolerance among the tested DFFs. Thus, the indication is that employing three independent storage elements may be a more efficient SEU mitigation strategy at very low supply voltages than being reliant on state restoration (DICE) or SET recovery/filtering (TDF, TDFCS and TDFCSLT).

3.4.3 Supplementary content: SER improvement offered by RT DFFs

In Paper IV, the soft error rate (SER) improvement offered by the radiation tolerant (RT) DFFs compared to the standard (STD) non-RT DFF (C2M DFF in Paper IV) was shown only for $\mathrm{LET} = 13.9\,\mathrm{MeV\text{-}\,cm^2/mg}$ and $\mathrm{LET} = 68.8\,\mathrm{MeV\text{-}\,cm^2/mg}$. In order to evaluate the SER improvement based on the entire LET spectrum used in Paper IV, and based on a typical radiation environment, (3.1) may be used.

$$SER = \int_{LET_{min}}^{LET_{max}} cs(LET) \cdot \Phi(LET)\, dLET \tag{3.1}$$

where LET_{min} is the minimum LET, LET_{max} is the maximum LET, $cs(LET)$ is the SEU cross-section of a DFF as a function of LET and $\Phi(LET)$ is the differential LET spectrum. The differential LET spectrum may be acquired through numerical differentiation of the integral LET spectrum (such as the ones shown in Chapter 2.2.1). The SER improvement offered by the RT DFFs compared to the STD DFF is given by (3.2).

$$SER_{STD/RT} = \frac{SER_{STD}}{SER_{RT}} \tag{3.2}$$

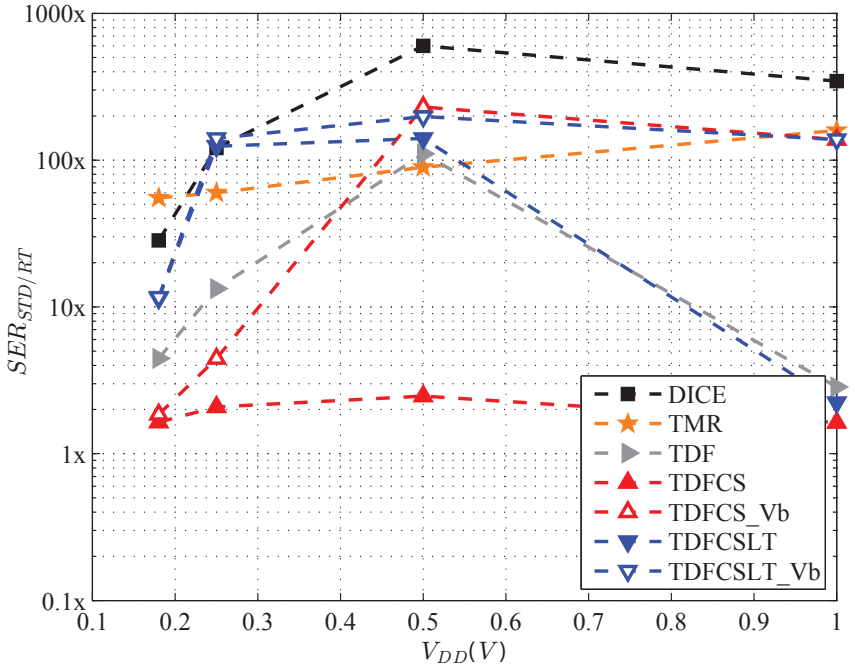

Figure 3.4: SER improvement offered by the RT DFFs compared to the STD DFF as a function of V_{DD}.

Figure 3.4 shows $SER_{STD/RT}$ as a function of V_{DD}, for $\mathrm{LET} = 5.8 - 68.8\,\mathrm{MeV\text{-}\,cm^2/mg}$ and for a GCR solar minimum LET spectrum. The upper bound of the 95 % confidence interval of the SEU cross-section is used as $cs(LET)$ input for (3.1). From Figure 3.4, the DICE is the most radiation tolerant DFF when taking the supply voltage range between 0.25 V and 1 V into consideration. The DICE achieves 121x, 600x and 345x SER improvement compared

to the STD DFF at $V_{DD} = 0.25V$, $V_{DD} = 0.5V$ and $V_{DD} = 1V$, respectively. The TDFCS* DFFs achieve >120x SER improvement compared to the STD DFF in the supply voltage range between 0.25 V and 1 V, depending on the configuration (SET filter delay, LVT transistors vs. standard threshold voltage (SVT) transistors). At $V_{DD} = 0.25V$, the TDFCSLT_Vb[2] achieves an SER improvement of 141x, slightly higher than the DICE. At $V_{DD} = 0.18V$, the TMR shows the highest improvement, achieving 55x SER improvement compared to the STD DFF. The SER improvement offered by the TDF DFF was generally lower than that of the other RT DFFs.

It should be noted that the results in Figure 3.4 are based on the radiation data available in Paper IV. Since the DICE, TDF and TMR had more irradiation runs than the TDFCS* DFFs, the DICE, TDF and TMR gain an advantage because their upper limit of the 95 % confidence interval, for when no SEUs are detected, is lower than that of the TDFCS* DFFs. Moreover, by including ions with $\mathrm{LET} < 5.8\,\mathrm{MeV\text{-}\,cm^2/mg}$, the results in Figure 3.4 may be altered. For example, if the SEU cross-section of the STD DFF decreases faster than the SEU cross-section of the RT DFFs, with decreasing LET, the SER improvement offered by the RT DFFs will decrease because there is a higher abundance of ions with $\mathrm{LET} < 5.8\,\mathrm{MeV\text{-}\,cm^2/mg}$ compared to ions with $\mathrm{LET} > 5.8\,\mathrm{MeV\text{-}\,cm^2/mg}$ in the GCR spectrum. For the same reason, the radiation data in Paper IV does not provide the necessary information for performing good SER predictions since the LET spectrum below $5.8\,\mathrm{MeV\text{-}\,cm^2/mg}$ was not investigated, and since the DFF SEU sensitivity to tilt- and roll-angles was assessed only for 30-degree and 45-degree tilt. Therefore, the results in Figure 3.4 are meant to illustrate the SER improvement offered by the RT DFFs compared to the STD DFF, specifically for $\mathrm{LET} = 5.8 - 68.8\,\mathrm{MeV\text{-}\,cm^2/mg}$.

3.4.4 Supplementary content: Energy consumption comparison

In Paper IV, there was limited focus on the performance of the evaluated DFF topologies because the investigation of the radiation tolerance of primary concern. In order to supplement the findings in Paper IV, an energy consumption comparison is included in this thesis for the sake of assessing the potential benefits offered by supply voltage scaling.

The energy consumption comparison of the DFFs in Paper IV is based on post-layout simulations at a temperature of 25 °C. For each of the DFFs, the simulation includes the DFF and a combinational logic path, which model worst-case path delay in a synchronous system (e.g., a pipeline or an finite-state machine (FSM)). V_{DD} was scaled from 1 V to 0.18 V. No process and mismatch variations were taken into consideration, however, a somewhat over-exaggerated worst-case logic path delay of 60 inverter gates was used to compensate for the lack of variation. The activity factor was 0.1. The energy consumption is monitored of the DFFs only.

Figure 3.5 shows the energy per cycle of the DFFs. Only a subset of the DFF configurations are included. Several of the DFF configurations with $V_b < V_{DD}$ (TDFCSLT_0V3, TDFCSLT_0V2, TDFCS_0V2, TDFCS_0V15 and TDFCSLT_0V15) are not included due to their limited impact on the SEU sensitivity. Given that these configurations were plotted, their energy consumption would be similar to TDFCS and TDFCSLT for appropriate V_{DD} settings. This can be observed in TDFCS_0V3, which is plotted for $V_{DD} = 0.5V - 0.18V$.

[2]TDFCSLT_Vb is equivalent to the TDFCSLT_0V2 in Paper IV, when $V_{DD} = 0.25V$.

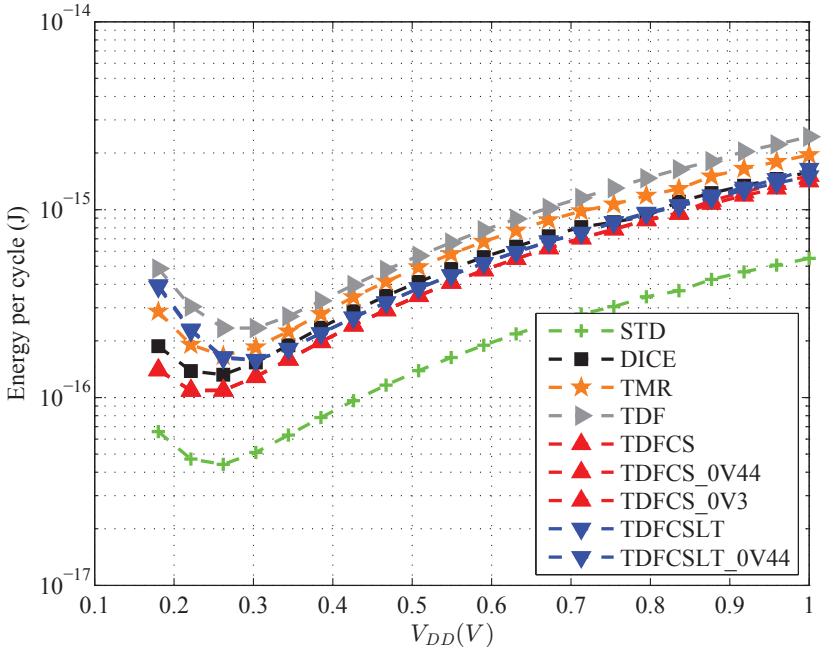

Figure 3.5: Energy per cycle of the DFFs in Paper IV.

From Figure 3.5 it is evident that the RT DFFs have a higher energy consumption than a standard STD DFF. All the RT DFFs incorporate some form of redundancy which requires a higher transistor count than what is required in a STD DFF. As a result, both the switching and the leakage energy increases in the RT DFFs. Furthermore, the MEP is also affected, depending on the DFF, where the DFFs with higher leakage have a MEP higher in the V_{DD}-range than DFFs with lower leakage.

Figure 3.6 shows the energy per cycle comparison between the RT DFFs and an STD DFF. The RT DFFs consume between 2.2x to 7.4x more energy than an STD DFF, depending on V_{DD} and RT DFF topology. The lowest energy consumption penalty is achieved by TDFCS, followed by TDFCSLT (for $V_{DD} > 0.35V$) and DICE. The TDFCS and TDFCSLT have an advantage over the DICE because they incorporate fewer pull-up/pull-down paths and more transistor stacking than the DICE, leading to lower energy consumption. The TDF DFF consumes the highest energy due to high transistor count and due to the inverter based delay elements. The TMR has also high energy consumption due to employing a high degree of redundancy. In the subthreshold region ($V_{DD} < 0.4V$), the energy consumption of the TDF and TDFCSLT increases rapidly due to increased impact of E_{leak}. In the case of the TDF DFF, high path delay in combination with high P_{leak} in the DFF topology dominate the E_{leak} contribution. Similarly, in the case of the TDFCSLT, the utilization of LVT transistors contributes to high P_{leak}, which in combination with high path delay increases E_{leak}.

Figure 3.7 shows how much energy savings can be achieved in the RT DFFs by scaling their V_{DD} compared to an STD DFF operating at $V_{DD} = 1V$. By scaling V_{DD} down to 0.65 V to 0.5 V, the RT DFFs achieve the same energy efficiency as the STD DFF. For the purpose of narrowing the discussion on energy savings, only the most radiation tolerant DFFs from Paper IV are considered. Recalling from Chapter 3.4.3, the DICE was the most radiation tolerant DFF when considering the supply voltage range between 0.25 V and 1 V and the TMR was

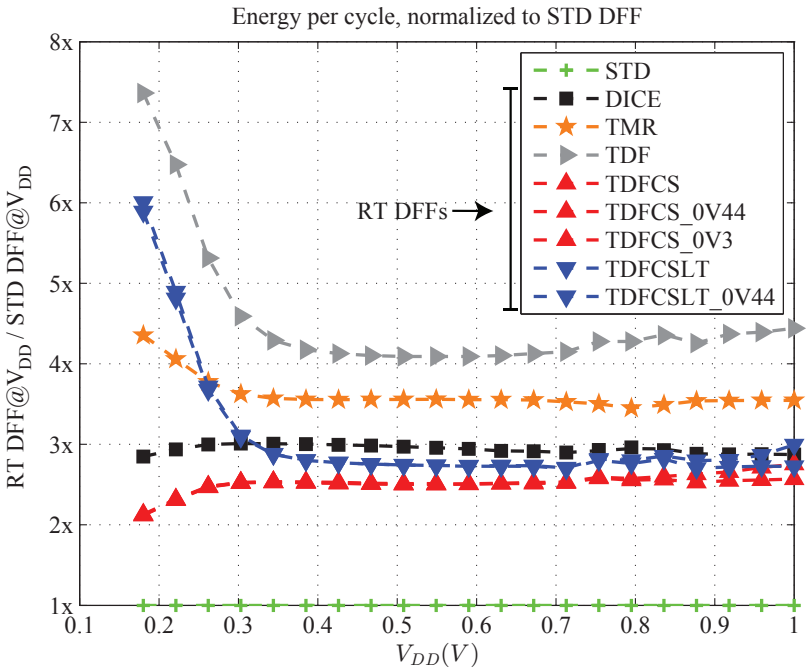

Figure 3.6: Energy per cycle of RT DFFs compared to the STD DFF vs. V_{DD}.

the most radiation tolerant at $V_{DD} = 0.18V$. Given that V_{DD} is scaled down to 0.5 V and 0.25 V, the DICE is ∼1.4x and ∼4.1x more energy efficient than a STD DFF operated at 1 V. At $V_{DD} = 0.18V$, the impact of E_{leak} reduces the benefits of scaling down the supply voltage, leading to TMR DFF being only ∼1.9x more energy efficient than the STD DFF. Based on these observations, it is safe to say that supply voltage scaling can enable the RT DFFs to operate with higher energy efficiency than the STD DFF (operated at $V_{DD} = 1V$), while simultaneously providing higher radiation tolerance.

So far we have looked at the energy savings that can be achieved in RT DFFs compared to STD DFFs. However, supply voltage scaling can enable even higher energy savings when RT DFFs are compared to RT DFFs. Figure 3.8 shows the amount of energy savings can be achieved in the RT DFFs by scaling their V_{DD} compared to a DICE DFF operating at $V_{DD} = 1V$. By scaling the supply voltage to 0.5 V and 0.25 V, the DICE DFF is ∼3.9x and ∼12x more energy efficient than a DICE operated at $V_{DD} = 1V$. As seen previously, E_{leak} limits the energy savings at $V_{DD} = 0.18V$, nevertheless, the TMR achieves ∼5.5x lower energy consumption than a DICE operated at $V_{DD} = 1V$.

While taking the aforementioned simulation constraints into consideration, RT DFFs can reduce the energy consumption by a factor of 12x by scaling the supply voltage down to the MEP. Even higher energy savings are possible for higher activity factor and shorter worst-case delay paths. On the other hand, reduced activity factor and longer worst-case delay paths increase the impact of E_{leak}, reducing the benefit of scaling down the supply voltage. In other words, the energy savings are dependent both on the implementation and operating conditions such as operating frequency.

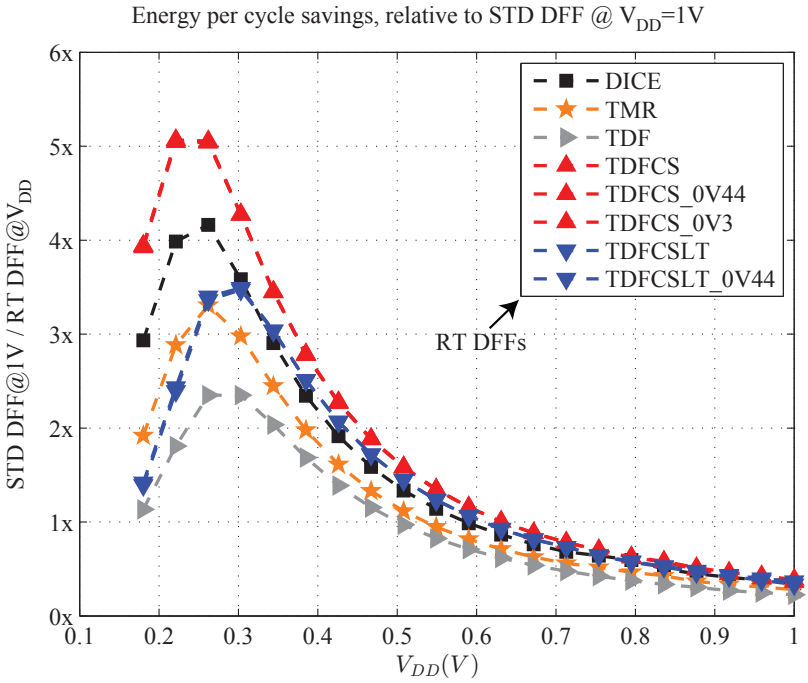

Figure 3.7: Energy savings of RT DFFs compared to the STD DFF @ $V_{DD} = 1V$.

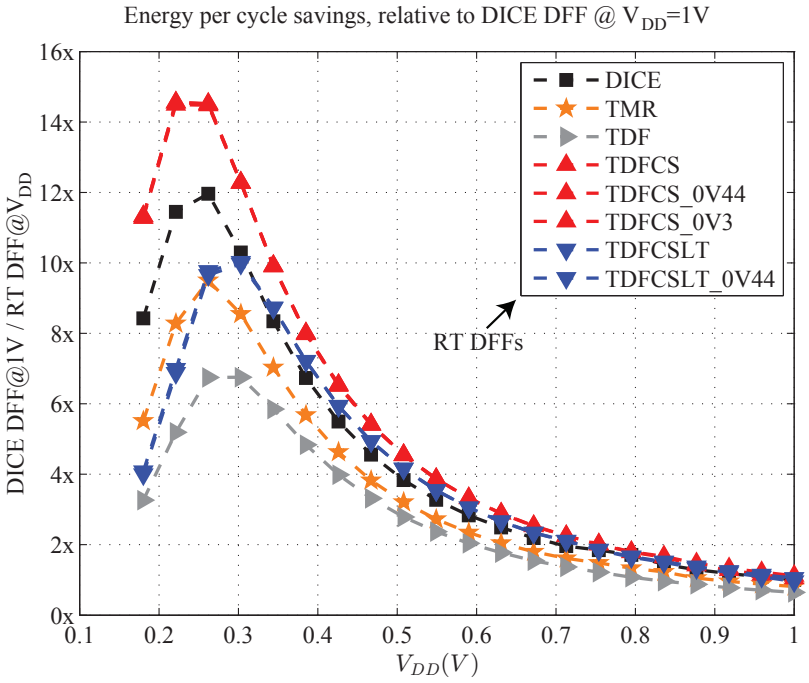

Figure 3.8: Energy savings of RT DFFs compared to the DICE DFF @ $V_{DD} = 1V$.

Chapter 4

Discussion

4.1 Subthreshold to Above Threshold Level Shifters in 90 nm and 65 nm CMOS

Supply voltage scaling has remained a central topic within the field of low-power CMOS design. Accompanying this trend is also the continued research on level shifters as they are an indispensable part of ICs employing MSV domains [90, 91]. The level shifters presented in Paper I were designed to offer a trade-off between speed, power- and energy consumption. This was achieved through a combined utilization of MTCMOS, diode-connected PMOS, off-biased PMOS transistors and transistor sizing. By utilizing transistor sizing, a certain optimization range can be achieved and increased static power may be traded for reduced propagation delay (e.g., MDCVSLP vs MDSVSHS). MTCMOS, diode-connected PMOS and off-biased PMOS transistors help with optimizing the contention between the pull-up and pull-down ratio and thereby also contribute to reducing contention-induced energy consumption. However, diode-connected PMOS and especially off-biased PMOS do infer additional propagation delay. The off-biased PMOS transistors limit the pull-up network to being driven by leakage current and therefore it is important to choose both the appropriate transistor type and size to obtain the desired delay, power/energy consumption and VDDL/VDDH scalability.

When compared to some of the similar recently published level shifter topologies in 90 nm and 65 nm CMOS process technologies [92, 93, 94], the proposed level shifter topology shows comparable and often lower energy- and static power consumption. However, the proposed level shifter topology does generally exhibit somewhat higher propagation delay compared to similar works. The higher delay in the level shifters in Paper I is not necessarily a limitation, especially since the level shifter delay is comparable to the delay of a subthreshold logic gate. In a typical MSV scenario where a signal path consists of logic operated at both subthreshold and superthreshold supply voltages, the total propagation delay can easily become dominated by the subthreshold logic delay. For example, given a subthreshold and superthreshold logic depth of >10 SVT gates, MDCVSLP as interfacing level shifter, the level shifter contributes to less than 13 % of the total delay. Furthermore, if MDCVSLP was changed with MDCVSHS, the level shifter delay contribution would be less than 5 %. In other words, for subthreshold logic depth of > 10 gates, the level shifter topology in Paper I is well suited, however, for smaller logic depths, a faster level shifter topology may be better suited.

4.2 Proton Beam Characterization at OCL

Having easy access to a radiation facility is a major benefit to researchers working within the field of radiation effects. Therefore, proton beam characterization was performed at OCL as a first step towards providing a radiation test facility for our low-power, radiation tolerant IC design activities at the University of Oslo. As part of this work, methods for on-line flux measurements and beam-to-target alignment were investigated. The beam characterization showed that the combined utilization of plastic scintillator detectors and dosimeter film provide means of on-line flux monitoring and determination of DUT location in the beam. However, the flux at DUT and the DUT location in the beam could not be determined until after the dosimeter film has been processed, which is only possible after an irradiation run has been completed. This means that only the average flux (fluence/irradiation time) at the DUT can be extracted by using this method. Furthermore, using this method for dosimetry purposes during irradiation testing has its limitations since the fluence at the DUT can only be determined after the dosimeter film has been processed. Post-processing of the dosimeter film showed (Fig. 5 in Paper II) that is was difficult to achieve good beam-to-target alignment due to the beam profile being relatively narrow. The average flux at the DUT was 23 % lower than the average flux at the beam center, and that the average on-line flux measured by the detectors only, was 33 % lower than the average flux at the DUT.

The methods used in Paper II for measuring the flux and the beam profile have previously been used at other facilities. For example, particle detectors measuring scattered protons have been used for flux measurements at the Radiation Effects Facility at Texas A&M University (TAMU)[1], and dosimeter film has been used by the TRIUMF Proton Irradiation Facility [95] for beam profile measurements. In Paper II, only two particle detectors were used in comparison to the four particle detectors which are used at the TAMU facility. At least four detectors are necessary for detecting spatial beam drifts. With only two horizontally aligned detectors in use, the beam can drift in the vertical direction and thereby completely miss the DUT during an irradiation run.

By using the characterization setup described in Paper II, the beam intensity was found to vary with a relative standard deviation of 4.78 %, which results in 24 % when 5 standard deviations are considered. The horizontal drift appeared to be much smaller than the drift in beam intensity, as shown in Fig. 7 in Paper II. Even though the vertical drift could not be monitored by the detectors, the vertical drift was assumed to be similar to the horizontal drift, which is confirmed by the uniform beam profile (Fig. 3 and Fig. 6 in Paper II). The impact of spatial beam drift was underestimated in Paper II, however, after further analysis, it was discovered that spatial beam drift has a significant impact on the flux variation. Analysis showed that beam drift varies with a relative standard deviation of 0.64 % in the horizontal direction. This translates into a beam drift of $\pm$ 3.1 mm from the beam center, given one standard deviation. Given that the DUT is perfectly aligned in the beam center, a drift of $\pm$ 3.1 mm would result in < 5 % flux variation. However, if the DUT is located at the edge of the beam profile, like in Paper II, the impact of drift is magnified and a drift of $\pm$ 3.1 mm results in flux variation of $\sim$ 30 %. In other words, since perfect DUT alignment to the beam center cannot be guaranteed, and if worst case conditions (e.g., 5σ) are taken into consideration, the beam

[1] http://cyclotron.tamu.edu/ref/measurements.php

can occasionally drift as much as ± 15 mm from the beam center, leading to a flux variation of > 95 %. It should be noted that the observations made in the beam stability- and the drift properties of the cyclotron in Paper II are only based on one intensity setting. Several beam intensity settings must be used to get a clearer picture of how the beam intensity impacts the beam stability and drift.

The methodology used for flux measurements and beam-to-target alignment were sufficient for uncovering some of the limitations (w.r.t. radiation testing purposes) of the proton beam at OCL. The beam profile was shown to be relatively narrow and as a consequence, beam drift has a significant impact on the flux (> 95 %, 5σ taken into account). Furthermore, electronic interference caused subthreshold CMOS logic to malfunction in the OCL environment. Due to the high flux variations and noise issues, the proton beam at OCL (in the condition it was in during the experiment) was not well suited for the radiation test requirements in this thesis since higher predictability was desired. To substantially reduce the impact of the beam drift, the beam profile must be broadened and potentially collimated one more time. This can be achieved in several ways, for example by using scattering foils or by installing an xy-wobbler [96]. Given that the beam is broadened sufficiently and by using two additional detectors, the flux can be monitored without the utilization of the dosimeter film. The dosimeter film can however be used for further beam characterization and for checking the beam uniformity occasionally. There was also observed some beam instability, however, a 24 % variation (5σ taken into account) is acceptable for many radiation test requirements. Furthermore, since there is little demand for proton energies around 30 MeV for SEE test purposes, the next step in the beam characterization should also be investigate methods for reducing the energy, preferably below 0.5 MeV (at the sensitive volume). This does however require significant investments of new equipment, such as vacuum chamber, ionization chamber and silicon detectors [97].

While taking the limitations of the proton beam at OCL into consideration and the time it would take to obtain stable operation of a low energy proton beam, it was determined that the cost, risk and workload was too high to continue. Work on the OCL was thereby suspended, and alternative solutions were sought out for radiation testing of ICs. The choice was then made to pursue utilization of the heavy ion beams at the Heavy Ion Irradiation Facility (HIF) at the Université catholique de Louvain (UCL) in Belgium, and later at the Radiation Effects Facility (RADEF) at the University of Jyväskylä, Finland. These two facilities were used for evaluating the heavy ion induced SEU dependence on supply voltage of DFFs in 90 nm and 65 nm bulk CMOS processes.

4.3 SEU Dependence on Supply Voltage Scaling in 90 nm CMOS Temporal Redundant DFFs

It has been shown in this thesis that supply voltage scaling is a powerful tool for reducing the energy- and power consumption of ICs. If radiation tolerant ICs are to exploit supply voltage scaling as a means of reducing the energy- and power consumption, their radiation tolerance must be examined at a wide supply voltage range before they can be utilized in high reliability applications.

In Paper III, four DFFs were irradiated with heavy ions at supply voltages of 1 V, 0.5 V,

0.25 V and 0.18 V. Among the tested DFFs, three were based on a proposed temporal redundant topology, the TDF, and one was based on the well-known DICE topology. Since the TDF is vulnerable to both SETs and charge sharing, their SEU tolerance is dependent on both temporal hardening (i.e., SET filter delay) and spatial hardening (i.e., separation between sensitive nodes). By performing a comparative study on the SEU sensitivity of the TDF DFFs to supply voltage and LET, the impact of temporal and spatial hardening was analyzed.

Comparison of the TDF DFFs showed that their SEU sensitivity is more dependent on temporal hardening than on spatial hardening at $\mathrm{V_{DDL}} = 0.5\mathrm{V}$. On the other hand, for decreasing supply voltages and increasing LET, their SEU sensitivity was more dependent on spatial hardening due to increased impact of charge sharing. This observation was made by comparing the SEU cross-section TDFCS and TDF4D (Fig. 9, Paper III). The TDFCS had a longer SET filter delay, but shorter sensitive node separation than the TDF4D (3.5 μm vs. 4.2 μm). As a result, the TDFCS had a lower SEU cross-section than TDF4D at $\mathrm{V_{DDL}} = 0.5\mathrm{V}$, for the entire LET spectrum, despite having shorter sensitive node separation. However, as the supply voltage scaled down, the SEU cross-section of the TDFCS approached that of the TDF4D. At the lowest supply voltage ($\mathrm{V_{DDL}} = 0.18\mathrm{V}$), the TDFCS even exhibits a higher SEU sensitivity than the TDF4D for LET $\geq 38.8\,\mathrm{MeV\text{-}cm^2/mg}$. These findings indicate that the impact of charge sharing becomes more severe as the supply voltage scales down, which is also expected from theory (see Chapter 2.2.4). Nevertheless, temporal hardening showed to have a higher impact on SEU mitigation than spatial hardening for $\mathrm{LET} \leq 19.4\,\mathrm{MeV\text{-}\,cm^2/mg}$, even at supply voltage down to 0.25 V. Since the TDF is dependent on both temporal- and spatial hardening, the TDF must have both sufficient SET filter delay and sufficient sensitive node separation, in order to provide a low SEU sensitivity.

The last of the TDF DFFs, the TDF8D, was designed with an increased minimum sensitive node spacing (1.5x wider than TDF4D) and increased SET filter delay ($\sim$1.8x higher than TDF4D). In light of the recent findings related to the SET filter delay in TDFCS (presented in Chapter 3.3.3), the TDF8D had a shorter delay than the TDFCS. Nevertheless, the SET filter delay in the TDF8D was sufficient for filtering out the majority of the SETs, particularly at $\mathrm{V_{DDL}} = 0.5\mathrm{V}$. As a result, the TDF8D experienced no SEUs at $\mathrm{V_{DDL}} = 0.5\mathrm{V}$, exhibiting an SEU cross-section of $1.9 \cdot 10^{\text{-}10}\mathrm{cm^2/bit}$ ($7 \cdot 10^{\text{-}10}\mathrm{cm^2/bit}$, 95 % confidence level taken into account). The results thereby showed that an input- and feedback delay of $\sim$2.69 ns and $\sim$4.83 ns, respectively, were efficient to filter out SETs, and that sensitive node spacing of 6.4 μm was efficient for mitigating charge sharing caused by perpendicular ion hits, for $\mathrm{V_{DDL}} = 0.5\mathrm{V}$. As the supply voltage was lowered to 0.25 V and 0.18 V, the TDF8D also experienced SEUs, however, its SEU cross-section was lower than that of the other TDF DFFs. An interesting observation was made at a $\mathrm{V_{DDL}} = 0.18\mathrm{V}$, where the TDF8D showed almost one order of magnitude lower SEU cross-section compared to the other TDF DFFs. This observation confirmed that the additional temporal and spatial hardening reduces the SEU cross-section, even at ultralow supply voltages. Even though the TDFCS had longer SET filter delay than the TDF8D at $\mathrm{V_{DDL}} = 0.18\mathrm{V}$, the lower SEU cross-section of the TDF8D emphasizes the importance of charge sharing mitigation at ultralow supply voltage.

In Paper III, a brief performance comparison between the TDF DFFs and a DICE DFF was given. The TDF DFFs consumed up to 2x more area, up to 1.5x more energy and had 0.32x maximum frequency compared to the DICE DFF. Despite these performance penalties, a

TDF8D operating at a supply voltage of 0.5 V, 0.25 V and 0.18 V still offers -72 %, -92.5 %, -95 % (respectively) reduction in energy consumption, compared to a DICE operating at a supply voltage of 1 V. This shows that even though radiation tolerant topologies are designed with performance penalties compared to well-rounded topologies (in terms of radiation tolerance and performance) such as the DICE, supply voltage scaling can still offer significant energy savings. Moreover, several improvements with regards to the TDF performance were recognized in Paper III. These improvements were incorporated in the TDF DFFs presented in Paper IV.

The radiation tolerance of a DICE DFF was also characterized in Paper III. Since interleaving of sensitive nodes was performed on the latch-level for all the DFFs in Paper III, the sensitive nodes of the DICE DFF were spaced very close to each other due to the DICE topology allowing for a more compact layout than for example the TDF. The short sensitive node spacing caused the DICE DFF to exhibit a higher SEU sensitivity then expected. Furthermore, the DICE DFF also failed to function correctly at $\mathrm{V_{DDL}} = 0.25\mathrm{V}$ and $\mathrm{V_{DDL}} = 0.18\mathrm{V}$. Due to the shortcomings of the DICE implementation in Paper III, its radiation tolerance was not compared to the radiation tolerance of the TDF DFFs as it would be an unfair comparison. The same DICE topology was re-implemented in Paper IV with DFF-level sensitive node interleaving, showing a significant improvement in both its ability to operate at low supply voltages and its ability to withstand radiation hits.

4.4 SEU Dependence on Supply Voltage Scaling in 65 nm CMOS Temporal- Dual- and Triple Redundant DFFs

Based on the findings in Paper III, an extended experiment was conducted in Paper IV, evaluating the radiation tolerance of a wider variety of DFFs at a supply voltage range of 0.18 V - 1 V. The hardening techniques evaluated in Paper IV are DICE, TDF, TMR, TDFCS and a non-radiation tolerant DFF. The electrical performance of TDFCS in Paper IV was improved compared to that of the TDFCS in Paper III. In Paper IV, the sensitive node spacing was increased for all the reoccurring DFF topologies (e.g., DICE, TDF) compared to the sensitive node spacing used in Paper III. The increased sensitive node separation improved the radiation tolerance of the DICE DFF. However, in the case of the TDF, the radiation tolerance showed to be highly dependent on both sensitive node separation as well as drive strength, especially at supply voltages below 0.5 V.

The SEU cross-section of the DFFs is shown in Fig. 4 and Fig. 6, in Paper IV. The DICE DFF experienced no SEUs at $\mathrm{V_{DD}} = 1\mathrm{V}$ for the entire LET spectrum, and at $\mathrm{V_{DD}} = 0.5\mathrm{V}$ for LET $\leqslant 36.6\ \mathrm{MeV\text{-}cm^2/mg}$, given perpendicular ion hits and 30-degree Ar hits. The DICE DFF showed also a low SEU cross-section at $\mathrm{V_{DD}} = 0.25\mathrm{V}$. This made the DICE DFF the most radiation tolerant DFF when considering the supply voltage range of $\mathrm{V_{DD}} = 1\mathrm{V} - 0.25\mathrm{V}$. However, for 45-degree tilted Xe hits the DICE showed a high sensitivity to angled hits at $\mathrm{V_{DD}} \leqslant 0.5\mathrm{V}$. The high sensitivity to angled high LET hits is relatively expected since the DICE topology is known for being vulnerable to angled hits, even at nominal supply voltages [98, 99]. It should be noted that the SEU response to angled Xe hits is a worst-case scenario and it has little impact on the SER of the DFF due to the low abundance of Xe ions in typical interplanetary space environments. A more interesting investigation is to use steeper angles with

LET $\leqslant 30.0\,\mathrm{MeV\text{-}cm^2/mg}$ as such ions are more frequent. For $\mathrm{V_{DD}} \leqslant 0.25\mathrm{V}$, the DICE DFF experienced SEUs for the entire LET spectrum, and its SEU susceptibility had a relatively high LET dependence. The high LET dependence at such low supply voltages is due to increased charge sharing sensitivity as a result of decreasing Q_{crit} with decreasing supply voltage.

The temporal DFFs TDFCS_0V44 and TDFCSLT_0V44 also showed good radiation tolerance at $\mathrm{V_{DD}} = 1\mathrm{V}$ when $\mathrm{V_b} = 0.44\mathrm{V}$ was applied to the current starved SET filter delay elements. The TDFCS_0V44 and TDFCSLT_0V44 experienced only one SEU at LET $= 66.8\,\mathrm{MeV\text{-}cm^2/mg}$ with a SET filter delay of 3.4 ns. The SEU is assumed to have occurred due to SET propagation, since a configuration with $\mathrm{V_b} = 0.35\mathrm{V}$ resulted in no errors detected in TDFCS and TDFCSLT (not discussed in Paper IV). Other works have shown that a SET filter delay of $\sim$ 600 ps is sufficient to filter out SETs in 65 nm technology at $\mathrm{V_{DD}} \approx 1\mathrm{V}$ [100, 101]. However, the necessary SET filter delay to fully suppress the occurring SETs is highly dependent on the SET filter delay topology as well as the CMOS fabrication technology (high speed vs low power), where both have an impact on the SET recovery efficiency. For example, inverter based delay elements have better SET recovery efficiency than current starved delay elements due to the limited drive strength in current starved delay elements. On the other hand, current starved delay elements consume less area and power than inverter based delay elements. Additionally, current starved delay elements are more flexible in terms of user controlled delay, which may be beneficial when operating at a wide range of supply voltages. In terms of SET recovery efficiency dependence on CMOS fabrication technology, high speed technologies have higher drive strength than low power technologies, leading to better SET recovery efficiency in high speed CMOS technologies.

The impact of drive strength was investigated in Paper IV, where the TDFCSLT utilized LVT transistors in its multiplexer for better SET recovery efficiency, compared to TDFCS. Previous studies have shown that reduction of the threshold voltage reduces the SET pulse widths and increases Q_{crit} at nominal supply voltages in 90 nm and 65 nm CMOS technologies [102, 103]. A similar observation is made in this work for supply voltages below the nominal supply voltage. The TDFCS and TDFCSLT had identical topologies and layout implementations, and despite the TDFCSLT having shorter SET filter delay, the TDFCSLT showed up to 112x improvement in the SEU sensitivity compared to TDFCS at $\mathrm{V_{DD}} \leqslant 0.5\mathrm{V}$. This study shows that increasing the drive strength of key components in a temporally hardened latch topology can have a high impact on the SEU response even at low supply voltages. The TDFCSLT achieved an SEU cross-section below $1 \cdot 10^{-9}\mathrm{cm^2/bit}$ with the minimum SET filter delay at $\mathrm{V_{DD}} = 0.5\mathrm{V}$ and $\mathrm{V_{DD}} = 0.25\mathrm{V}$ for LET $\leqslant 66.8\,\mathrm{MeV\text{-}cm^2/mg}$. Furthermore, the TDFCSLT was also the least SEU sensitive DFF at $\mathrm{V_{DD}} = 0.25\mathrm{V}$. Perhaps equally important as increased drive strength is the lack of sufficient drive strength. The TDFCS showed very poor ability to filter out SETs at all supply voltages, making it one of the most SEU sensitive DFFs. At $\mathrm{V_{DD}} \leqslant 0.25\mathrm{V}$, the TDFCS_0V2 and TDFCS_0V15 had very limited ability to filter out SETs due to limited SET recovery efficiency. However at $\mathrm{V_{DD}} = 0.5\mathrm{V}$, the TDFCS_0V3 exhibited the second best (after the DICE) radiation tolerance since the supply voltage was high enough to enable more efficient SET filtering than what was achieved at lower supply voltages.

At $\mathrm{V_{DD}} = 0.5\mathrm{V}$, the TDFCSLT_0V3 was more sensitive to SEUs than TDFCS_0V3. This was unexpected since it was foreseen that higher drive strength in TDFCSLT_0V3 would provide better SET filtering efficiency, and that the equal sensitive node spacing would ensure sim-

ilar charge sharing sensitivity. Increasing the SET filter delay by setting $\mathrm{V_b} = 0.25\mathrm{V}$ caused no reduction in SEU sensitivity of the TDFCSLT and a minor reduction (not discussed in Paper IV). Although this observation received limited attention in Paper IV, further investigations indicate that the SEU cross-section of TDFCSLT_0V3 was limited by charge sharing. Since the TDFCSLT utilizes LVT transistors, it is suspected that device engineering contributes to increased charge sharing sensitivity in the TDFCSLT. One common method used for decreasing the threshold voltage of transistors is reduction of the doping in the channel region. In addition to contributing to increased carrier mobility, a decrease in doping levels also contributes to increased charge collection efficiency [104] and increased diffusion length (i.e., the distance a carrier will travel before recombining) [105]. The utilization of LVT transistors may therefore increase charge sharing sensitivity. However, the advantages of LVT transistor utilization still outweigh the disadvantages, especially at $\mathrm{V_{DD}} \leqslant 0.25\mathrm{V}$, where the TDFCSLT showed a lower SEU sensitivity than the TDFCS/TDFCS_Vb.

At $\mathrm{V_{DD}} = 0.18\mathrm{V}$ all DFFs experience a high increase in the SEU sensitivity due to increased sensitivity to charge sharing as a result of a low Qcrit. The TMR DFF showed the best radiation tolerance among the tested DFFs despite suboptimal sensitive node spacing, indicating that it may be beneficial to utilize topologies with multiple independent storage elements at low $\mathrm{V_{DD}}$. It should however be noted that the SEU tolerance of the TMR is also dependent on the readout procedure. Around nominal $\mathrm{V_{DD}}$ ($\pm$ 20 %), high frequency dynamic readout procedures are considered to emulate worst-case conditions due to increased vulnerability to SETs at the input [78]. With decreasing $\mathrm{V_{DD}}$, SETs at the input have decreasing impact because the operating frequency decreases at a much higher rate than the SET pulse width increases [82]. Although the semi-static readout procedure used in Paper IV mimics a very low frequency, the worst-case test procedure of a TMR DFF at low $\mathrm{V_{DD}}$ is fully-static (i.e., no clock running). By having a clock running, single DFF upsets in a TMR topology get corrected at rising edge of the clock, possibly contributing reduced sensitivity to multiple ion hits. In the absence of a clock, the probability of SEUs due to multiple ion hits increases as no corrections are made over the course of the irradiation run. Such considerations need to be taken into account depending on the purpose of the TMR DFF (e.g., clock gated configuration register vs. data path register).

Chapter 3.4.3 presented the SER improvement offered by the radiation tolerant DFFs compared to the standard DFF, and Chapter 3.4.4 presented the energy savings comparison between all the DFFs tested in Paper IV. By combining these findings, the SER and energy savings dependence on $\mathrm{V_{DD}}$ scaling can be determined. The combined results show that a DICE operated at $\mathrm{V_{DD}} = 0.5\mathrm{V}$ is $\sim$3.9x more energy efficient than a DICE operated at $\mathrm{V_{DD}} = 1\mathrm{V}$. At $\mathrm{V_{DD}} = 0.5\mathrm{V}$, the DICE offers an SER improvement of 600x over a standard DFF. When $\mathrm{V_{DD}} = 0.25\mathrm{V}$, the DICE is $\sim$12x more energy efficient than a DICE operated at $\mathrm{V_{DD}} = 1\mathrm{V}$, while offering an SER improvement of 121x compared to a standard DFF. At $\mathrm{V_{DD}} = 0.18\mathrm{V}$, the TMR was the most radiation tolerant, offering a 55x SER improvement compared to the standard DFF, while operating at $\sim$5.5x higher energy efficiency than a DICE at $\mathrm{V_{DD}} = 1\mathrm{V}$. As mentioned in Chapter 3.4.3, the SER data presented in this thesis is based on $\mathrm{LET} = 5.8 - 68.8$ $\mathrm{MeV\text{-}\ cm^2/mg}$. A more complete view of the SER improvement offered by the radiation tolerant DFFs would be enabled if SEU cross-section data for $\mathrm{LET} < 5.8\ \mathrm{MeV\text{-}\ cm^2/mg}$ and the SEU cross-section data for a wider range of tilt- and roll-angles was available. Furthermore, as mentioned in Chapter 3.4.4, different implementations and operating conditions may yield

different energy savings results.

Although the DICE showed the highest SER improvement compared to the standard DFF, the TDFCS* DFFs should not be dismissed as inferior when radiation tolerance and energy efficiency is concerned. The TDFCS* DFFs can offer lower energy consumption than the DICE for $\mathrm{V_{DD}} > 0.35\mathrm{V}$, meaning they can potentially (depending on implementation and operating conditions) provide higher energy savings than the DICE. With further charge sharing mitigation, both the DICE and the TDFCS* DFFs stand to improve their radiation tolerance. As mentioned in Chapter 3.4.3, the DICE did receive an advantage compared to the TDFCS* DFFs due to having more irradiation runs, leading to the DICE exhibiting much lower SER than the TDFCS* DFFs.

Chapter 5

Conclusion

In this thesis, the feasibility of utilizing supply voltage scaling as a means of reducing power- and energy consumption in radiation tolerant CMOS circuits was investigated. The topics covered in this thesis include subthreshold to above threshold level shifter design for interfacing supply voltage domains, proton beam characterization for radiation testing, and the design and radiation tolerance characterization of DFF topologies aimed at operating at a wide supply voltage range for optimized power- and energy consumption.

The implementation consideration, performance and reliability of subthreshold to above threshold level shifters in 90 nm and 65 nm CMOS process was presented in Paper I. The level shifters offered lower power and energy consumption than several of previously published level shifters, as well as lower power consumption than several of the recently published level shifter topologies in 90 nm and 65 nm CMOS process. The level shifters are well suited for the purpose of subthreshold to above threshold conversion and are compatible with supply voltage scaling. However, if subthreshold operation is not of concern, or if maximizing the operating frequency is a primary requirement, an alternative level shifter topology may be better suited for implementation.

The proton beam properties at OCL were characterized in Paper II for the purpose of radiation testing of electronic devices. The proton beam characterization showed that the beam profile was relatively narrow, and that the beam stability and the spatial beam drift can cause significant (> 95 %) drops in the proton flux. Several measures for improving the flux variations have been proposed, which may be useful for further work on the OCL proton beam. The proton beam showed promise with regards to its usability for radiation testing of electronic devices, however the required work to improve its usability was out of the scope of this thesis. As a result, other facilities were pursued for the purpose of radiation testing.

The SEU dependence on supply voltage was investigated in Paper III and in Paper IV. In Paper III, three different configurations of a proposed TDF DFF topology were designed in a 90 nm CMOS process. The radiation tolerance of the TDF DFFs was examined at supply voltages between 1 V and 0.18 V, for perpendicular ion hits with LET between $8.6\,\mathrm{MeV\text{-}cm^2/mg}$ and $53.7\,\mathrm{MeV\text{-}cm^2/mg}$. To the author's knowledge, this work was the first to investigate the impact of temporal and spatial hardening techniques on the heavy ion induced SEU sensitivity in radiation tolerant DFFs, from the deep-subthreshold region to the nominal supply voltage. The TDF DFF with the widest sensitive node separation and the longest SET filter delay exhibited the lowest SEU sensitivity. Experimental results showed that the TDF could operate at a supply

voltage of 0.5 V without experiencing any SEUs (SEU cross-section of $1.9 \cdot 10^{-10}\mathrm{cm}^2/\mathrm{bit}$). The radiation tolerance of the TDF DFFs was explored down to a supply voltage of 0.18 V, where it was observed that the level of SEU hardening (i.e., the distance between sensitive nodes, SET filter delay) can have a significant impact on the SEU sensitivity. Charge sharing was found to be an increasing cause of SEUs with decreasing supply voltage, meaning that the sensitive node separation needs to be increased for improving the radiation tolerance at reduced supply voltages. Furthermore, current starved delay elements for SET filtering purposes should be used with caution. At low supply voltages, process variations and/or noise can lead to higher delays than expected (from the simulations performed in this work), introducing higher performance penalty. Based on the experimental results and DFF performance evaluations, it was observed that supply voltage scaling down to 0.5 V can enable the TDF to operate at higher energy efficiency than a DICE DFF operated at 1 V. The finding thereby confirm that supply voltage scaling can be used to reduce the power- and energy consumption of radiation tolerant DFFs, while still maintaining a high degree of radiation tolerance.

In Paper IV, the SEU dependence on supply voltage was investigated for a wider variety of DFF topologies designed in a 65 nm CMOS process. The radiation tolerant DFFs showed generally an increase in their SEU sensitivity with decreasing supply voltage. Nevertheless, several of the DFF topologies demonstrated a low SEU rate at reduced supply voltages, exhibiting a clear advantage, in terms of radiation tolerance, over a standard non-radiation tolerant DFF. A DICE DFF showed the best radiation tolerance at a supply voltage of 0.25 V, 0.5 V and 1 V, exhibiting an SER improvement of 121x, 600x and 345x, compared to a standard non-radiation tolerant DFF. Certain configurations of the TDF DFF also showed good radiation tolerance in this supply voltage range. To the author's knowledge, this is the first study to investigate the impact of utilizing LVT transistors for SET/SEU mitigation in temporal redundant DFFs operated at low supply voltages. Utilization of LVT transistors for increased drive strength showed to improve the radiation tolerance in the TDF DFF, without significantly impacting the power consumption for supply voltages above 0.35 V. The radiation tolerance improvement enabled by LVT transistors was achieved with minimum SET filter delay settings in TDF DFFs, indicating that SET recovery efficiency may be more important than SET filter delay at low supply voltages. A correlation between the utilization of LVT transistors and increased SEU sensitivity was observed in one of the TDF DFFs, suggesting that LVT transistors may contribute to increased sensitivity to charge sharing. At a supply voltage of 0.18 V, a TMR DFF showed the best radiation tolerance, achieving a SER improvement of 55x, compared to a standard non-radiation tolerant DFF. Consequently, employing three individual storage elements may offer the best radiation tolerance when operating in deep-subthreshold region. Based on the findings in Paper IV, supply voltage scaling offers up to 12x energy savings in radiation tolerant DFFs while achieving > 120x SER improvement compared to a standard non-radiation tolerant DFF. This assessment is based on perpendicular ion hits and 30-degree Ar hits with LET between $5.8\,\mathrm{MeV\text{-}cm}^2/\mathrm{mg}$ and $68.8\,\mathrm{MeV\text{-}cm}^2/\mathrm{mg}$, and supply voltages above 0.25 V. A more complete view of the SER improvement offered by the radiation tolerant DFFs can be acquired by investigating ion hits with $\mathrm{LET} < 5.8\,\mathrm{MeV\text{-}\,cm}^2/\mathrm{mg}$, at steeper tilt- and roll angles, because charge sharing was considered to be the highest contributor to SEUs in the radiation tolerant DFF topologies, especially for decreasing supply voltage. Given that charge sharing is mitigated further, the SER of the radiation tolerant DFFs can be reduced additionally.

5.1 Recommendations for Further Work

As the device dimensions continue to decrease, directional ion hits and charge sharing are becoming an increasing issue. Thereby, thorough radiation tolerance characterization of contemporary electronic circuits requires radiation testing using a range of tilt- and roll angles in order to characterize the radiation tolerance to worst case directional hits. Incorporating all the test parameters (e.g., frequency, tilt, roll) is already a challenge for devices only characterized at nominal supply voltage, due to the high cost of beam time. By adding a wide supply voltage range to the test parameters, the number of irradiation runs is multiplied by the number of supply voltages, leading to even higher characterization costs. To reduce the amount of beam time needed to characterize the radiation tolerance of electronic devices, and to mitigate design errors during development, simulation tools should be utilized prior to characterizing the radiation tolerance in a beam. Simulation tools which can model radiation effects are either already developed or in continuous development [106, 107, 108]. By calibrating the charge collection models to be compatible with a wide supply voltage range, and by verifying the model correspondence to experimental results, a powerful tool for design of low-power radiation tolerant circuit design may be realized.

Given that access to sophisticated radiation effects modeling tools is not available, an interesting approach to mitigating charge sharing is to utilize multi-bit standard cells. This approach enables wide separation between sensitive nodes and is supported by current place and route tools [109]. Even if multi-bit cells are used for charge sharing mitigations, models identifying sensitive nodes should be developed in order to minimize the risk of bad cell placements.

Since the University of Oslo does have a cyclotron with a proton beam, furthering the work presented in Paper II might be of interest for researchers working within the field of radiation effects. Here, the main goal should be to investigate the possibilities of using the proton beam with proton energies below 0.5 MeV (at sensitive volume) in order to study SEUs caused by direct ionization. Recent studies have indicated that low energy protons do not have a high impact on the total on-orbit SEU rate when operated at nominal supply voltages [110]. However, when the supply voltage is scaled down to 0.5 V, the SEU rate contribution of low energy protons can be as high as 91 %, depending on CMOS technology, radiation environment and shielding [110]. Further work on the proton beam would entail procuring additional equipment. A vacuum chamber would be beneficial for limiting the spread in proton energy. Silicon detectors are needed for characterizing the proton energy, energy straggling and for low intensity flux measurements. Ionization chamber is needed for allowing flux and fluence measurements at higher intensities. Additionally, methods for beam energy selection/degrading and for achieving good beam homogeneity are also needed.

Publications

Paper I

Low-power subthreshold to above threshold level shifters in 90 nm and 65 nm process

Journal publication printed in Elsevier Microprocessors and Microsystems,
Volume: 35, Issue: 1, Feb. 2011.
Bibliography reference [21].

Paper II

Proton beam characterization at Oslo Cyclotron Laboratory for radiation testing of electronic devices

Conference publication presented at the IEEE 16th International Symposium on Design and Diagnostics of Electronic Circuits & Systems (DDECS), April 10, 2013. Publication date: 1. July, 2013.
Bibliography reference [55].

Paper III

Supply Voltage Dependency on the Single Event Upset Susceptibility of Temporal Dual-Feedback Flip-Flops in a 90 nm Bulk CMOS Process

Journal publication printed in IEEE Transactions on Nuclear Science,
Volume: 62, Issue: 4, Aug. 2015.
Bibliography reference [56].

Paper IV

Heavy Ion Characterization of Temporal-, Dual- and Triple Redundant Flip-Flops Across a Wide Supply Voltage Range in a 65 nm Bulk CMOS Process

Journal publication printed in IEEE Transactions on Nuclear Science,
Volume: 63, Issue: 6, Dec. 2016.
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