Design and test of a 128x128 Pixel Global Shutter CIS with HDR Support

A camera suitable for capturing scene with fast moving objects and/or unstable illumination sources

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Abstract

A 128×128 5T-pixels CMOS Global Shutter with HDR support is designed, implemented and tested in cooperation with Marius Lunder Lillestøl[11]. The design is done in Cadence with the process AMS OPTO $0.35\mu m$. For test and verification, a PCB is created with a simple camera control system in FPGA and a user interface for configuration. Partial of the design reuses parts previous master students, Mathias H. F. Wilhelmsen[22] and Stian Hjorteset[7], made. The global shutter mechanism results are compared with a rolling shutter. HDR skimming scheme is compared with images taken without skimming.

Image Sensor	
Package	JLCC84 (84 I/O Pads)
Chip Size	$5.6mm^2$
Power Supply	3.3V
Power Consumption	Approx. 11.5mW
Pixel Fill Rate	19.75%
Resolution	128×128 (QVGA)
Output Signals (2)	Analog
Technology	AMS OPTO $0.35\mu m$ process
Shutter	Global Shutter
Noise Reduction Technique	non-true CDS
Control System	External
Configurations	Exposure time Tx pulse time Bias voltages

Table 1: Image Sensor Properties

Preface

This thesis summarizes project work and has been written to complete the M.Sc Degree in Informatics: Nanoelectronics at the University of Oslo. This was done in cooperation with Marius Lunder Lillestøl and together we've encountered numerous of challenges and was capable of overcoming these.

Photography has always been an interest of mine and after finding out that it was possible to write a master thesis dedicated to image sensors, I decided to apply for the master studies. Adjunct Professor Johannes Sølhusvik contributed in defining a suitable master thesis based on Event Based image sensor, but was later found to be a complicated task to proceed. Later, an available master thesis on Global shutter image sensor is presented and I applied for it.

I want to thank Marius Lunder Lillestøl for accompanying me and his endless support, I certainly wouldn't be able to overcome the challenges on my own, and for all the times he played his 90s/80s songs(or something) from his Spotify account. I want to thank our supervisor Johannes for sharing his knowledge within this domain, his enthusiasm and guidance. A huge thank previous master students Mathias H. Wilhelmsen and Stian Sumstad for sharing their experience with us and allowing us to reuse their design for this project. A huge thank to Olav Stanly Kyrvestad, Senior Engineer at NANO Resarch Group and Philipp Dominik Häfliger, professor at the NANO Resarch Group, for answering our questions and guidance.

I want to thank my sister, Iman, for her endless support and nagging at home. If it weren't for her, I wouldn't be able to get up in the morning. I want to thank Karl Magnus for going through my thesis and constantly giving me advices. Also, I want to thank Bård-Kristian for buying me a coke on the actual day of the deadline.

Last, but not least I want to thank my moka pot that never failed at making a delicious good cup of coffee every morning. It saved me a lot of money.

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Chapter 1

Introduction

The very first Complementary-Metal–Oxide–Semiconductor (CMOS) and Charged-Coupled Device (CCD) were invented in 1963[13] and 1970[19] respectively. CCD image sensors dominated within the digital imaging field for its small pixel size, high quantum efficiency and low noise compared to CMOS image sensor. CCDs were produced massively from 1980s to 1990s and these were mainly used for scientific purposes, industrial applications and high-end cameras. However, CCDs structure requires special manufacturing process, high voltage for charge transfer and has limiting readout speed and special process when integrated on-chip.

Before the invention of CCDs, integrated circuit(IC) designers have reported progresses with CMOS image sensor, such as Horten in 1964 [8], Schuster in 1966 [17] and Wreckler in 1967 [21], where the challenges consist of improving photon sensing unit along with the read out mechanism and electron storage. Despite these progresses, CMOS image sensors were incapable of providing the same image quality as CCDs and therefore produced only for applications where image quality wasn't prioritized. IC designers continued on developing CMOS image sensors because of their simple production process and low power consumption.

The passive pixel sensor, introduced by Weckler, has no active component in the pixel architecture, hence the name, and contains a switch for both reset and readout. This structure suffers from noise and additional processing techniques are required to cancel these out. The term Active Pixel Sensor (APS) is first introduced by Noble in 1968 [16] with an in-pixel amplifier. Later Tsutomu Nakamura proposed a new readout operation in 1985 [15] with it and APS with an intra-pixel charge-transfer techniques was invented by Fossum in 1993 [2]. This structure was able to reduce fixed pattern and temporal noise and capable of providing good image quality with a high readout speed. In 1997, a pinned photodiode in CMOS pixel architecture was introduced by Guidash [6] and this technique allowed CMOS image sensor to provide image quality on the same level as CCDs. Along with it's advantages mentioned earlier, IC desginers and

researchers started to invest more of their efforts in CMOS image sensors. In 2000s, CMOS image sensors have replaced CCD in many applications because of it's performance.

CMOS image sensor has grown rapidly and numbers of architecture are invented and presented, but the system itself is complicated. The improvements for the device, pixel architecture, process and readout circuits are still developing. The most common exposure mechanism a CMOS image sensor has is a rolling shutter, which is shown to be insufficient in the rapidly growing technology world where high sensitivity and precision is demanding. For capturing objects in fast motion or under pulsed light illumination, many researchers have shown their interest in image sensors with a pixel architecture with supports global shutter mechanism.

In CCD image sensors, interline transfer CCD in a global shutter mode is common. The same shutter mechanism for CMOS image sensors was less preferable because it required additional area for memory frame circuitry in the early generation. This increases the cost of the production and the structure is prone to dark current and stray light on the memory lane. This application also reduces the fill factor and affects the quantum efficiency which is why rolling shutter mechanism is the most common approach.

Despite the disadvantages, CMOS image sensor with a global shutter technology is still desirable. The advantages that follows with a global shutter is preventing the artifacts a rolling shutter technology produces; motion blur when capturing images of objects in motion, see figure 1.1, or nonuniform lightning with varying light intensities sources. Other artifacts one can reduce with global shutter technology are smear, wobble, skew and partial exposure.

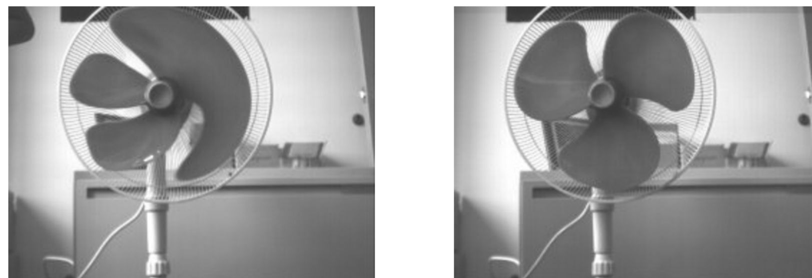


Figure 1.1: (Left) Image taken with a rolling shutter (Right) Image taken with a global shutter [5]

As mentioned earlier CMOS with global shutter was not of main focus, but with the pinned photodiode invention and an active pixel structure it's possible to suppress the disadvantages. Invention of CMOS image sensors with global shutter have been reported lately, such as by Wany in 2003 [20] and Furuta in 2007 [3]. This improvement alone is not sufficient for

scenes with a wide range of light intensity. Having a high dynamic range (HDR) is necessary in fields such as automotive cars, security systems and medial applications. To improve precision in image, many researches have incorporate numbers of technique and architecture to achieve a higher dynamic range to avoid over- and under saturated scenes. Some are designed specifically for this purpose and a variation of sampling methods have been presented, such as the dual sampling method by Fossum in 1997 [23].

1.1 Pixel

Pixels are the main circuity in image sensors and modern pixels typically consist of a photodiode and several transistors, but in some architectures a pixel can contain 2 or more photodiodes, capacitors and even noise reduction circuitry. In this chapter, photodiode will be described along with it's noise characteristics and common architectures are mentioned.

1.1.1 Photodiode

A photodiode converts light into voltage or current and is the main component in an image sensor. The general structure consists of two differently doped semiconductor types, p- and n-type, in one single semiconductor crystal and a window for the light to access through. The semiconductors are doped to achieve excesses of electrons and electron holes and when placed together they will flow towards the opposite type while leaving behind positive donor ion and negative acceptor ion. When in contact, diffusion occurs and will create a depletion area, an electric field, where no more electron or hole can travel to the other side without sufficient energy, see figure 1.2. Silicon is the common semiconductor material used for detecting visible light because of it's favourable bandgap energy, E_g, which limits the wavelength range.

Photodiode is constructed to operate in the reverse bias condition, the n-type is connected to the positive terminal while p-type is connected to ground. When the depletion area is exposed to light electrons and electron holes get excited and will flow to the positive side and ground respectively instead of towards the opposite type. This effect is known as photoelectric effect and produces photocurrent. This occurs only if the energy of the light is sufficient to excite a single electron, see equation 1.1.

$$E_{photon} = \frac{hc}{\lambda} \tag{1.1}$$

λ, h and c is the wavelength, Planck's constant and speed of light respectively. For silicon the desired wavelength will be between $190 - 1100nm$ and any wavelength outside of this range is invisible to silicon,

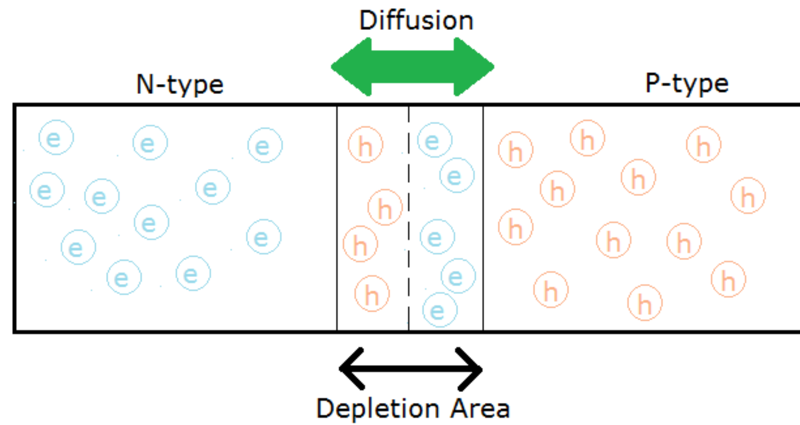


Figure 1.2: Semiconductor

while the visible light is $390 - 700nm$. These charges are then collected and read out. Although a photodiode in general contains doped semiconductor they still vary in structure. There are 3 main types P-N, PIN and pinned photodiodes. P-N junction type is the simplest structure and consist only of an n- and p-type, see figure 1.3. PIN photodiode contains an intrinsic semiconductor between the n- and p-type. This region is a pure semiconductor and is beneficial during reverse biased due to it's lower capacitance. The intrinsic area is almost the whole depletion region and, hence, much larger and has a nearly constant-size compared to a P-N diode. In this sense, this structure increases the volume of electron-hole pairs capable of being generated by a photon. Despite this, increasing the size of the intrinsic region increases the parasitic resistance and affects it's performance during low frequency. A pinned photodiode includes a shallow p-type implant on top of the n-type layer and p-type layer at the bottom, creating a sandwich. This additional top layer provides a complete charge transfer and reduces the transfer noise. Other conventional properties includes suppressing dark current and reset noise, has higher sensitivity and better stabilization of the photodiode electrically. Today a pinned photodiode is the primary photodetector used in both CMOS and CCD image sensors due to its properties.

Prior to the invention of pinned photodiodes, P-N photodiode was widely used in CMOS image sensors. The fabrication process is similar to a CMOS process and with some modifications in IC circuit schematics, it's possible to produce it in a general IC design environment. P-N photodiode is therefore used for low cost image sensors or small image sensors. Also, it has a large full-well capacity, which defines how much charge a pixel can hold until saturation point is reached. The only cons with P-N photodiode is dark current and thermal noise during reset mode.

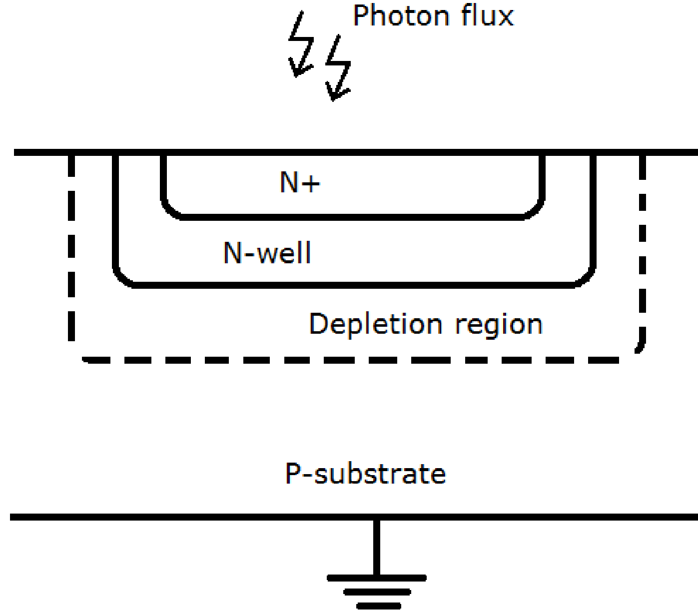


Figure 1.3: Reverse biased photodiode (P-N junction type)

1.1.1.1 Full Well Capacity

Full well Capacity(FWC) is another term necessary to determine how well an image sensor operates and it determines the range of the analog to digital converter (ADC). A photodiode has a limited amount of accumulated charges on its capacitance and the signal based on it is described in the equation 1.2

$$N_{sat} = \frac{1}{q} \int_{V_{reset}}^{V_{max}} C_{PD}(V) \cdot dV[electrons] \tag{1.2}$$

where N_{sat} is the maximum amount of charge that can be accumulated, C_{PD} and q is the photodiodes capacitance and charge of an electron(coulomb) respectively. The term in general defines when a photodiode goes into saturation. V_{max} and V_{reset} varies and depends on the structure of the photodiode and the operating conditions.

1.1.1.2 Conversion Gain

Conversion gain $(\mu V/e^-)$ is the term use to describe the change on voltage by a single electron at the conversion node

$$C.G = \frac{q}{C_{FD}}[\mu V/electron] \tag{1.3}$$

C_{FD} is the node connected to the well where the accumulated charges flow and is known as the charge-to-voltage conversion capacitance and q is the elementary charge(Coulombs). The previous equation is used to

calculate the input conversion gain, but since this point is never measured and to calculate this and compare it with a measure value the output conversion gain is used instead

$$C.G_{output} = A_V \cdot \frac{q}{C_{FD}} \tag{1.4}$$

1.1.1.3 Fill Factor

In general fill factor defines the ratio of total pixel's light sensitivity area versus its total area, $AREA_{PD}/AREA_{pixel}$. This definition is required due to additional components are present in a pixel while the photodiode is the only component which contributes in converting light and therefore the photosensitive area is unequal to the total pixel area. The additional components are such as transistors and capacitors. The effective fill factor applies when a microlens[1] is in use. Microlens increases the light sensitivity of a pixel by concentrating the light from the whole area to the the photodiode. Often, the effective fill factor can be increased by nearly 100%.

1.1.1.4 Quantum Efficiency and Responsivity

Quantum efficiency(Q.E) gives the ratio of amount of current in one pixel given by a number of incident photon. This relation is the most important parameter used to evaluate the quality of the sensor and in image sensor it is usually described with the equation 1.5

$$Q.E(\lambda) = N_{sig}(\lambda)/N_{ph}(\lambda) \tag{1.5}$$

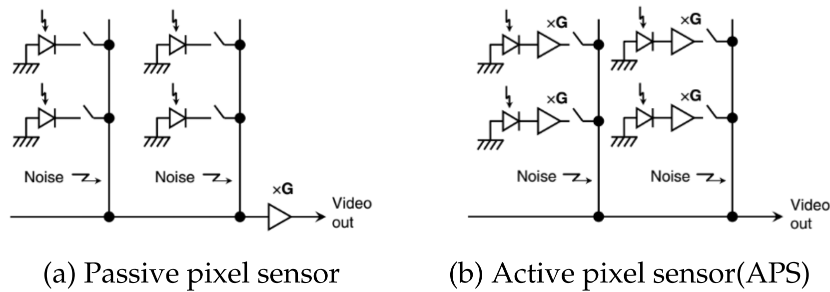
where N_{sig} and N_{ph} are the generated signal charge in a pixel and number of incident photons per pixel, respectively. This term is necessary due to, as mentioned earlier in fill factor, some photons can be absorbed or reflected by the metal structure around a photodiode and effective fill factor and charge transfer efficiency are the terms included in this definition.

1.1.2 Architectures

A passive pixel architecture consist only of a single switch compared to the active pixel architecture which has an amplifier, see figure 1.4. In CMOS pixel structure it's also known as 1T-pixel. An active pixel consists of more transistors for controlling readout, exposure time and amplification of signals. In this section 3T-, 4T- and 8T-pixel architecture will be mentioned briefly.

---

[1] Microlens[14] is a small lens, commonly in μm, and is usually fabricated in array on the chip. The size are chosen based on the pixel size and structure. A small pixel requires a smaller pitch between the pixel and the lens to reduce shading.



(a) Passive pixel sensor (b) Active pixel sensor(APS)

Figure 1.4: Passive pixel and active pixel [14]

1.1.2.1 3T-Pixel

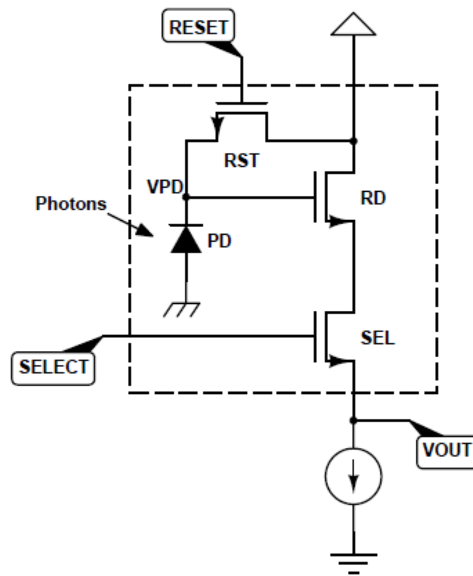


Figure 1.5: A 3T-pixel architecture[22]

The 3T-pixel is the standard APS configuration. The architecture consist of a diode, reset transistor, source-follower and select transistor. The operation for this structure is as follow: the diode is reset through the reset transistor. After reset mode, the diode then starts collecting charges generated from light source for a given integration and read out time when the select transistor is on. The full well capacity of this structure is the photodiode and has no other limitation than itself, and the conversion gain is proportional to the well. The downside with this structure is that during reading mode the diode continues to collect charges and is unsuitable to perform a global shutter.

1.1.2.2 4T-Pixel

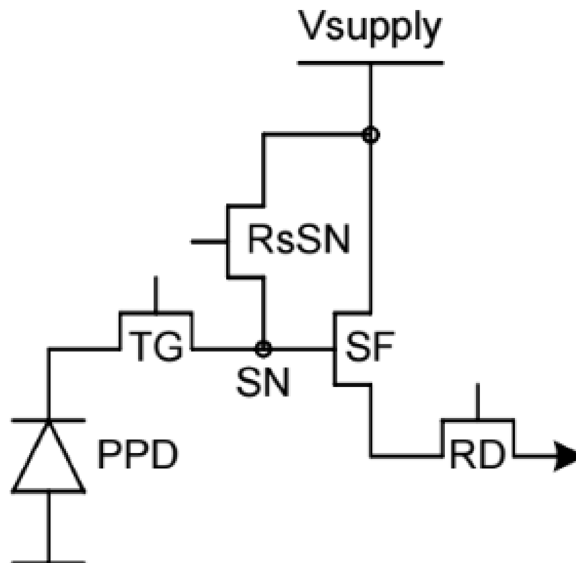


Figure 1.6: A 4T-pixel architecture [10]

The 4T-pixel architecture is similar to the 3T-pixel, but with an additional transistor between the photodiode and reset, a transfer transistor, and creates storage area FD, the floating diffusion node[2]. The operation for this configuration is similar to a 3T-pixel, but T_x is on during reset mode and sampling mode for charge transfer. This structure is beneficial due to charge collection and readout are separated which makes it possible to sample the reset signal as well as a reference signal to cancel out the reset noise. 4T-pixel is suitable for memory storage for a small period of time and is suitable for precision imaging. This is due to the capacitance for charge storage no longer depends on the photodiode itself, but on the FD node as well, which is adjustable. A high conversion gain is possible and the pixels sensitivity increases.

1.1.2.3 8T-Pixel

A variant of an 8T-pixel structure has been invented[4]. The specific scheme in figure 1.7 is designed to perform global shutter with a sample and hold circuitry within each pixel, hence the capacitors in the pixel architecture. The storage capacitors in series, parallel configuration is also possible, stores both the converted current to voltage signal and reference

[2]The origin of floating diffusion node derives from CCD. After accumulating charges, these are dumped at the floating diffusion node connected to an amplifier for further readout. APS copied the concept with the built-in source-follower and hence the name. The term "floating" mean the node is isolated.

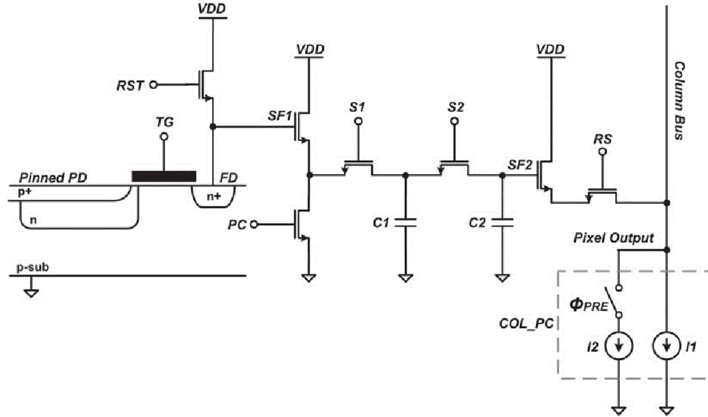


Figure 1.7: A 8T-pixel architecture[4]

signal. CMOSIS [4] is still developing the 8T-pixel by improving the structure and size.

1.2 Noise

Noise is inevitable and limits the imaging performance. An image sensor captures information and represents it as a 2 dimensional image. Noise, in this field, appears as a signal variation and reduces the quality of the representation. Noise has two categories; Fixed Pattern Noise(FPN) and temporal noise. As the name "fixed" applies, these noise appears at fixed positions and because it's fixed in space, FPN can, in theory, be removed either through signal processing or noise reduction circuits. Temporal noise, unlike fixed-pattern noise, varies in time and is frozen when an image is captured, therefore this noise is fixed spatially, yet varies in sequential shots.

1.2.1 Fixed Pattern Noise

FPN main components are dark current non-uniformity, performance variation of the pixel's source-follower, also known as the active transistor, and offset found in columns [14]. These arises due to imperfections in components in each pixel and therefore causes a noise pattern. Dark current is apparent during no illumination and is treated as an offset between each pixel, hence the name, and is proportional to the integration time and dependent of the temperature. These dark charges affects the usable dynamic range and the no illumination reference value used for the image. Dark current caused by a transistor in an active pixel is due to hot-carrier from the gate to the drain area, also known as current leakage. Other causes of dark current are local heat source which excites

the electron-pair and inclined light ray from micro-lens. The last two causes creates shading, a spatial frequency output variation.

1.2.1.1 Shading

Shading describes fading light observed at the edges of an image. It's also occurs as a low variation and the source for this noise can be dark current or the affect of an unsuitable microlens.

1.2.2 Temporal Noise

As mentioned thermal noise is random and varies in time. There are 3 fundamental temporal noise components in optical systems: thermal noise, shot noise and flicker noise[14]. Other significant noise components in image sensors are kT/C noise, smear, blooming, shading and image lag.

1.2.2.1 Shot Noise

Shot noise is the main noise factor during medium to high illumination level and limits the signal-to-noise ratio and dynamic range of the sensor. This noise occurs when semiconductor devices generate currents, such as in transistors and diodes, and can be modeled by Poisson probability distribution.

1.2.2.2 Thermal Noise

Thermal noise, as it's name indicate, is caused by heat. This produces thermal agitation of electrons within a resistance and can be represented with the power spectral density in form of voltage

$$S_V(f) = 4kTR[V^2/Hz] \tag{1.6}$$

where k is Boltzmann's constant, T is temperature and R is the resistance. This noise contributes to dark currents, currents that are not generated through photon absorption.

1.2.2.3 kT/C Noise

kT/C, also known as reset noise (thermal noise in capacitor), are random fluctuations in voltages when reading from the capacitor or FD-node in pixels. This occurs during pixel reset due to bidirectional movement between the diode and reset voltage node and thermal noise from the switch when on. The noise is then sampled and stored until readout. The kT/C noise can be reduced by using a soft reset, but at the same time introduces image lag. Preferably, one should sample the reset signal and use Correlated Double Sampling to reduce this. In the equation k,

T and C are Boltzmann's constant, absolute temperature and capacitance respectively.

1.2.2.4 Flicker Noise

Flicker noise is proportional to $\frac{1}{f}$ and is only needed to be considered during low frequencies since its noise contribution drops below thermal noise in higher frequencies. In a CMOS image sensor, the amplifier in a single pixel suffers from $1/f$ and can be suppressed by using Correlated Double Sampling circuitry as long at the sampling interval between reset and signal is short enough to consider it as an offset.

1.2.2.5 Smear and Blooming

Smear and blooming are noises which arise when the image sensor is exposed under strong illumination and the amount of generated charges exceeds the pixels full-well capacity. Smear appears as a straight vertical white lines and is usually seen in CCDs because of it's the vertical shift registers. The excesses of charges may diffuse into the shift register. Smear can also be the cause of stray photons, and both cause deterioration to the image. Blooming is seen as a bright circle on the images from the light source since the charge leaks to adjacent pixels.

1.2.2.6 Image lag

Image lag occurs when previous frame leaves residual. This may be the cause of incomplete charge transfer or soft reset with a voltage below threshold voltage and results in an incomplete reset. This is known as electrical shading and the term covers pulse delay, parasitic effect and voltage drop across switch transistors.

1.3 Global Shutter

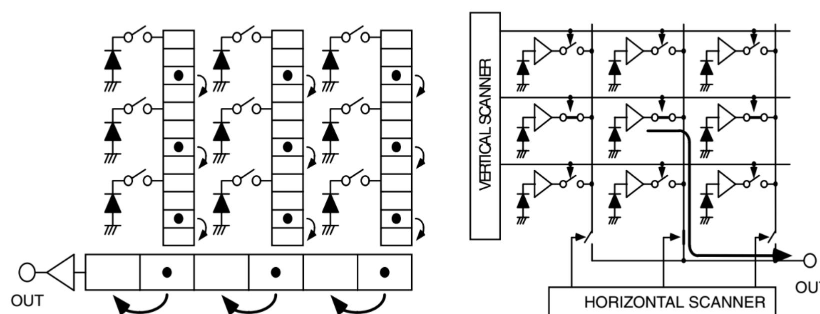


Figure 1.8: (Left) CCD with shift registers (Right)CMOS image sensor[14]

In digital image sensor world, the comparison between rolling shutter and global shutter is often discussed. In a global shutter mode, all pixels are exposed to light and blocked simultaneously. Rolling shutter allows exposing a single pixel row simultaneously and read out, and when it's done, the next row starts, hence the name. CCDs interline transfer, see figure 1.8, is the most known image sensor with global shutter, but because of it's disadvantages mention earlier in the Background section, developing CMOS based image sensor with global shutter is preferable. Global shutter mode can be achieved either mechanically or electronically. Mechanical shutter is not a pixel design configuration, but is instead a device composed by curtain that quickly expose and shield the sensor from incoming light. It has several types, such as leaf, focal or diaphragm shutter, and many modern camera uses the combination of both mechanical and electronic shutter. The project main focus is global shutter with electronic shutter and therefore mechanical shutter will not be discussed.

1.3.1 Electronic global shutter

An electronic global shutter is used to achieve an identical start and stop of integration time for all pixels. The advantages with a electronic global shutter instead of a mechanical shutter is that it's faster, both in exposure time and readout speed. Implementing an electronic global shutter have two approaches:

1. Memory-in-pixel
2. Frame-memory

1.3.1.1 Memory-in-pixel

Memory-in pixel scheme has been used earlier in CMOS sensors, but only for high frame-rate applications where the accumulated charge and readout operations are performed individually. The 4T-pixel and 8T-pixel architecture are examples of such configuration. The downside by using this application is when a pixel is exposed to bright illumination source leakage can occur during the storage time and affect the storage signal and in return deteriorates the image in form of blooming.

1.3.1.2 Frame-memory

Frame-memory is an additional circuity found in a CMOS image sensor. The signal from each pixel is transferred as fast as possible into a frame memory row by row after exposure and the readout scheme is then done by scanning the memorized signals from the frame instead of the actual pixels. To avoid any leakage, the frame memory is covered by a metal

to shield light. This method is advantageous by achieving a non-leakage configuration, but a large pixel array can cause differences in exposure time for each row and achieving a low-noise readout signal from the pixels array is challenging. Another drawback is the additional on-chip memory, as mentioned earlier, and this causes additional cost.

1.4 Sample and hold

A sample and hold circuitry is designed to store the analog signal from a single pixel unit for further read out. This inclusion allows the signal to be independent of time and prevents any further affection of the photodiode. This is composed of a switch, capacitor and an amplifier, commonly a source follower. A sample and hold circuitry can be composed within each pixel unit or each column. This circuitry can further consist of more transistors to preform noise reduction operations, such as Correlated Double Sampling(CDS) and Differential Delta Sampling(DDS).

1.4.1 Correlated Double Sampling

The CDS technique is the most common noise reduction operation used in CMOS image sensors and has the exact same structure as a simple sample and hold circuitry, but with an additional branch see figure 1.9. This technique reduces kT/C noise, thermal noise, flicker noise(1/f) and FPN caused by process variation in the source follower of an APS. The general process consist of sampling the reset signal of the FD-node before exposure and then the signal accumulated from the photodiode after the exposure. Both signals travels through the exact same signal path and any mismatch and process variation along this specific path are therefore identical. By subtracting the reset voltage with the signal voltage, the noise is then canceled and the output voltage will contain only of the differences between the two, which is the actual voltage drop. This structure can further be expand by adding a branch with the same circuitry. This structure allows a faster sampling time since the process of sampling the reset signal has no need to wait for the signal capacitor to be empty.

1.4.2 Differential Delta Sampling

As mentioned in previous section, a CDS with an additional branch results in a slightly different travel path between the reset and voltage drop signal and since CDS has amplifiers of it's own it introduces new noises. The noise occurs because of the threshold offset of the pMOS used as a source follower and it causes vertical FPN. DDS is another noise suppression technique beneficial for reducing the newly introduced noise, see figure 1.10. This configuration requires a new switch, PCB_{switch}. After both

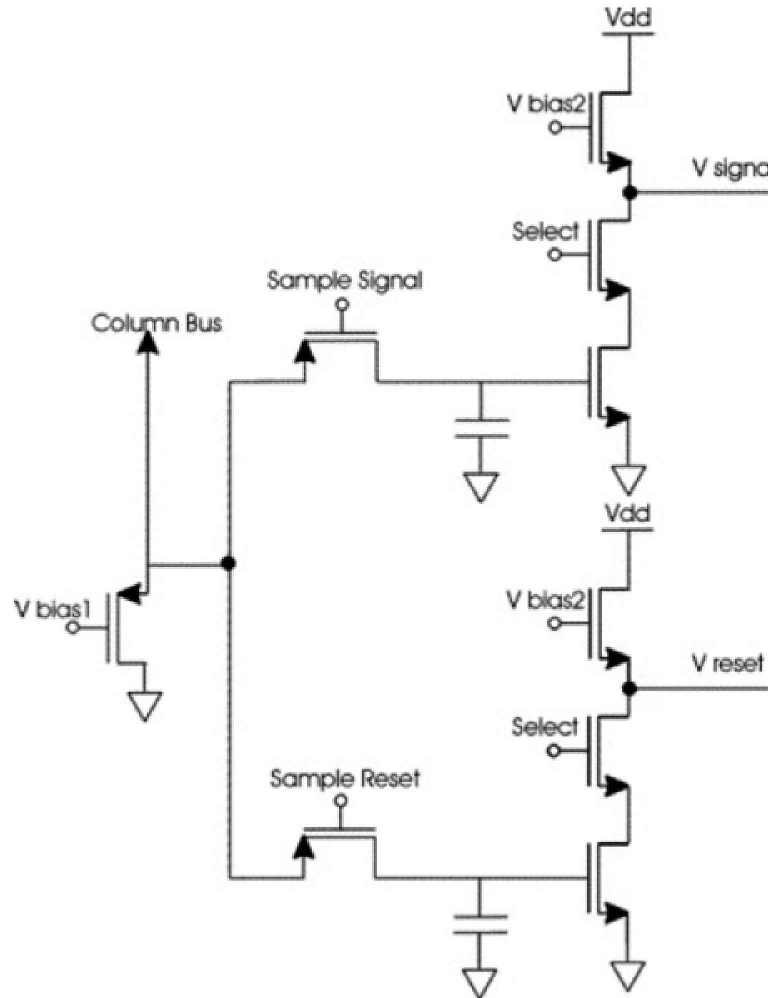


Figure 1.9: Correlated Double Sampling Circuit

signals has been sampled and held on the storing capacitors, horizontal scanning begins. When the column is selected, the two source follower are activated and generate a difference in the output signal that corresponds to reset and voltage signal. After reading the sampled signals out, the column select turns off. The new switch turns on and shorts the storing capacitors, also known as the crowbar operation. When shorted, the voltage signal will change until reaching the same potential. This signal is then read out when selected with the column signal, amplified by the same pMOS. The differential signals are buffered by different gains, the signals occurring after the crow bar operation defines the difference in gain. With this information, the gain mismatch can be suppressed and reduce the vertical FPN.

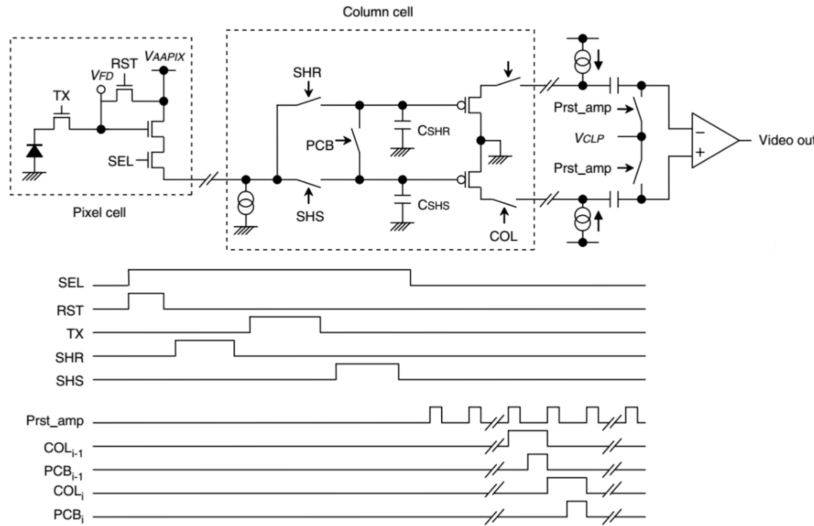


Figure 1.10: Differential Delta Sampling [14]

1.5 High Dynamic Range

Dynamic range(DR) is, in imaging, used to measure the ratio between largest and the smallest detectable light or the ratio between the full well capacity and the noise floor. When the input signal exceeds this range, information is either lost or produces an image dominated by noise. An image sensor can increase this ratio and is known as high or wide dynamic range. An example of a scene which requires a higher dynamic range can be a chair illuminated by the sun, while the background with a plant is covered in shadow. With a short exposure time, the sensor is incapable of detecting the plant in the shadow. A medium exposure time can still detect the chair, but some saturated areas are present and the plant is slightly visible. A long exposure time can leave half of the image saturated while the plant becomes clearly visible. HDR is capable of mapping the scene so that both the chair and plant is visible without any saturation.

The common techniques for achieving high dynamic range are skimming, staggered and split diode[18]. Skimming is obtained by pulsing the transfer gate with a mid-level voltage while the charges are still accumulating. The period of the pulses has to be one short and long, and the ratio between the exposures defines the dynamic range. The mid-level voltage marks the barrier on the transfer gate and any charge above this barrier is skimmed, hence the name, to the supply voltage.

Staggered is the method where the scene is captured multiple times. The readout scheme is staggered, which means right after the long exposure is done, the short one starts immediately. The signal from the long exposure time is stored in line buffers until the signal from the same pixel in the short exposure time is complete. The images are then

combined in the digital domain.

The split diode is a technology developed for automotive applications. The pixel architecture has two diodes, one large and one small, and both diodes are exposed simultaneously. This structure is beneficial because it removes motion artifacts which the splitting exposure times, skimming and staggered, can be prone to. This scheme is also suitable to combine with a global shutter, but in term of size, it's a drawback because of a additional diode. The signals are converted into digital domain and processed there to achieve a higher dynamic range

1.6 Motivation

We are surrounded by image sensors, in DSLRs, cellphones, personal computers, cars and even out in space, such as Hubble and Curiosity Mars Rover. As mentioned, image sensors technology has developed rapidly since the early 1970s and done major achievements. Starting with something as simple as detecting light, image sensor have now become a highly complex system. Despite the accomplishments of the last generation, improvements are still necessary. The demand for image sensors capable of capturing objects in motion and under varying light scenes is increasing due to machine vision, compensating for flickering LED lights and usage within medical field. The popularity of using rolling shutter in these areas has been reduced because of it's artifacts, and integrated circuit designers have turned to global shutter concepts to develop improvement. A CMOS global shutter image sensor to prevent motion artifacts with the combination of HDR support is desired to resolve the problem.

1.7 Thesis Outline

In this thesis a CMOS global shutter image sensor with HDR support is presented and tested. The thesis provides the design process of the image sensor and layout, followed by the design of the PCB and test and verification of the ASIC by using FPGA and GUI for data extraction, see figure 1.11. MATLAB is used for analysing and evaluating the extracted data. At the end of the thesis, future work and conclusion will be discussed.

The design phase is done together with Marius L. Lillestøl to ensure both partner fully understands the circuit, while the layout is divided between us. The test system is divided where I was responsible of the PCB and Marius is responsible of the FPGA. Lastly, I coded the MATLAB code used for evaluating the data. A simple overview of the work distribution is listed in the table 1.1. It should be noted that both contributed to each

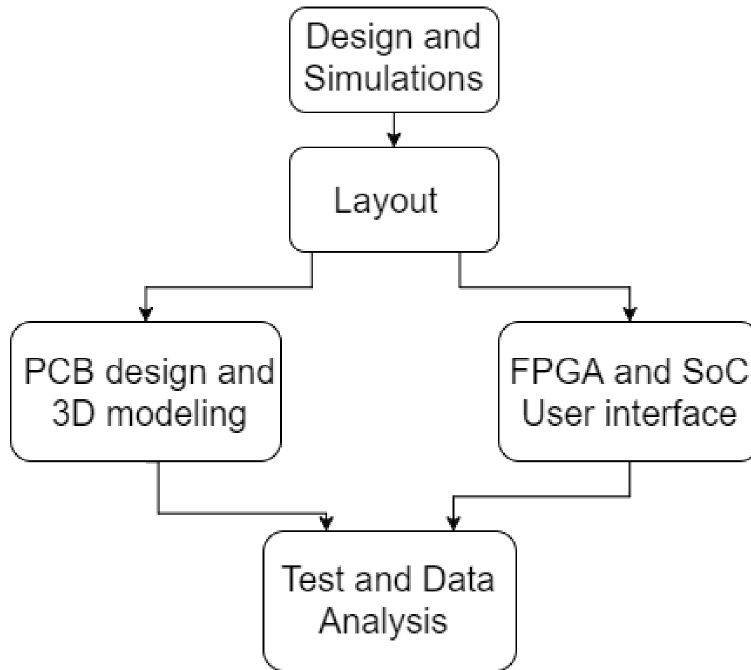


Figure 1.11: Thesis outline

others task, but the work distribution is listed to show who should be credited for the task.

<table>
<tr><th>Marius</th><th>Soman</th></tr>
<tr><td colspan="2">Planning</td></tr>
<tr><td colspan="2">Schematics</td></tr>
<tr><td>Pixel LO</td><td>Row Decoder LO</td></tr>
<tr><td>TX-control LO</td><td>Column Decoder LO</td></tr>
<tr><td></td><td>Output buffer LO</td></tr>
<tr><td colspan="2">Sample & Hold LO</td></tr>
<tr><td colspan="2">M1 buffer LO</td></tr>
<tr><td colspan="2">TOP and Padframe LO</td></tr>
<tr><td>FPGA and VHDL</td><td>Printed Circuit Board</td></tr>
<tr><td>C program</td><td>Lens mount</td></tr>
<tr><td>PC and Java</td><td>Matlab code</td></tr>
</table>

Table 1.1: Work Distribution. LO=Layout

Chapter 2

Design

The design of a CMOS global shutter image sensor with HDR support will be described in this chapter. The implementation of the chip is done with Cadence IC with the process AMS OPTO 0.35um and simulated with ADE XL. The chip fabrication is done through EUROPRACTICE with their design rules. The image sensors main and the most critical parts are the pixel unit and pixel array. The design process begins therefore with this section and continues with the sample and hold circuitry with CDS support, followed by the row and column decoder. Both decoders are based on the design a previous master student, Mathias Wilhelmsen[22], had created because they're suitable in form of specifications and is more efficient to reuse existing circuits due to restricted time. A control circuit for the transfer transistor for HDR support is included and the design process ends with a buffer for M1 and adding input and output pads at the top hierarchy. The estimated restricted chip area is $5mm^2$ and this value is given based by the institutes budget.

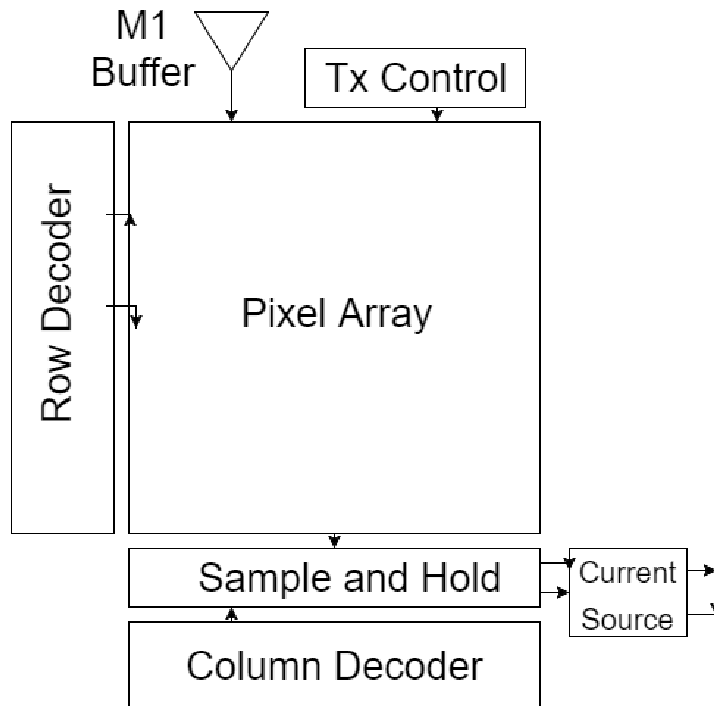


Figure 2.1: Overview of the chip

2.1 5t- Active Pixel Sensor

The condition of collecting the accumulated charges from the photodiode simultaneously of all pixels unit, a storing node is necessary and needs to be separated from the photodiode in order to perform an electronic global shutter. A 4t-pixel is a suitable and simple architecture for this purpose. To maintain a low noise pixel, a pinned photodiode should be used. This component is unavailable and one must design its own photodiode by the cost of the probability of a faulty product, hence a regular photodiode provided by the process is used. A possible incomplete charge transfer from the photodiode to the FD-node is to be expected. With the photodiodes built in guard rings, a single diode occupies an area up to $7\mu m \times 7\mu m$ where only 66% of the area is photosensitive, see figure 2.4b. To ensure the size of the chip remains within the restricted total area the pixel array contains only of 128×128 pixels.

A simple 4t-pixel configuration suffers from image lag. This is the effect of the reset transistors incapability of resetting the photodiode to it's full potential due to the voltage drop over the transfer transistor, Tx. Over time the storing node, FD-node, is affected by the signal from the photodiode since it's still generating charges during the readout process, assuming there's no mechanical shutter. This is most noticeable with the signals from the last row as their read out process has a larger time gap after exposure before it begins. As a global shutter, it's necessary to store

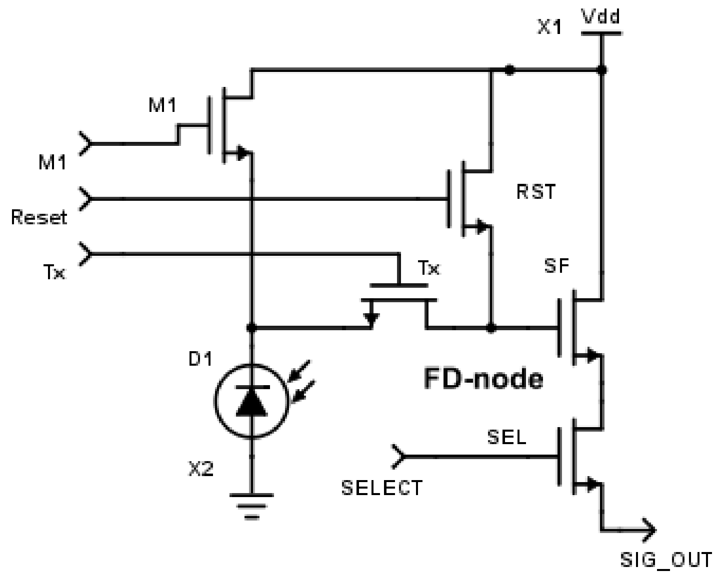


Figure 2.2: Schematic of the 5t-pixel

the accumulated charges until the readout process begins without being corrupted. If the storing node is affected by the continuously exposure and charges are able to travel through Tx transistor despite being switched off, the photodiode needs to be reset and maintain its potential without resetting the storing node itself. To prevent this, an additional transistor, M1, is introduced. M1 is connected directly between the photodiode and the power source, VDD. The structure improves photodiode reset and expands the interval of totals charges being accumulated. During readout, this transistor can be switch on to prevent the photodiode from generating more currents and ensure that the storing node is not corrupted. This solution is inspired by the paper presented by Lauxtermann[10]. The basic timing diagram is presented in figure 2.3

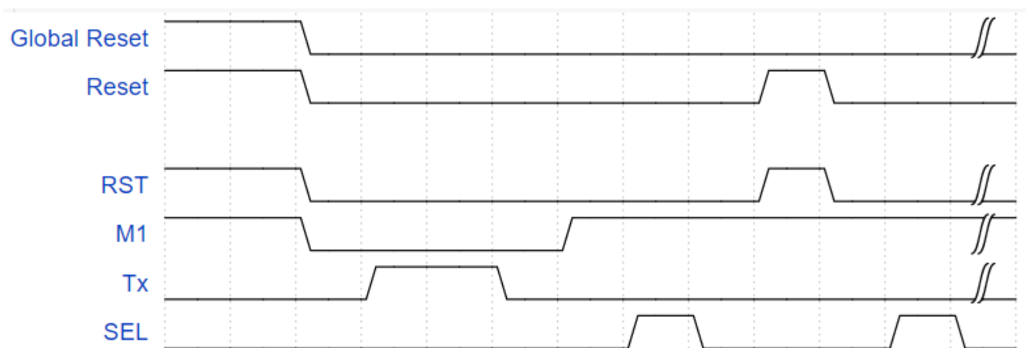
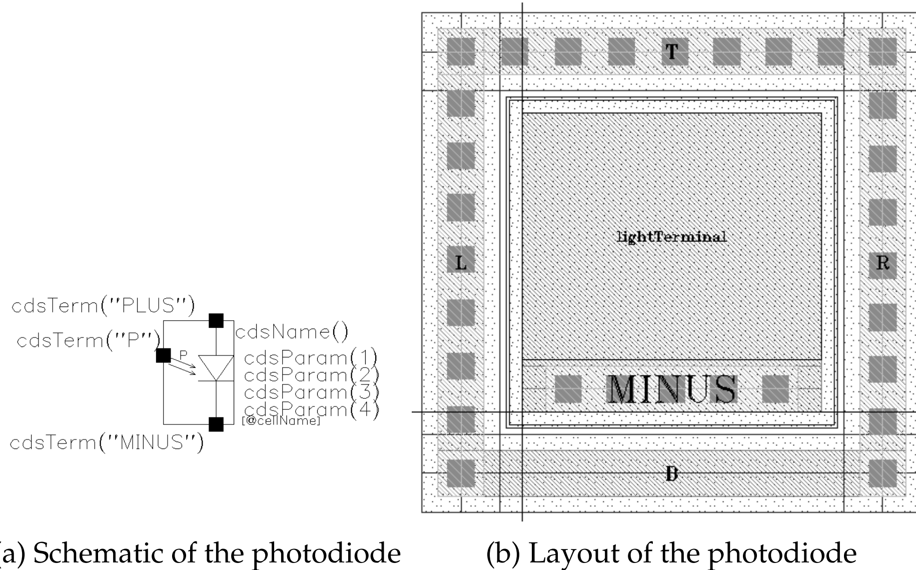


Figure 2.3: Basic timing diagram of the pixel without HDR

2.1.1 Photodiode



(a) Schematic of the photodiode (b) Layout of the photodiode

Figure 2.4: The photodiode provided by the process

The photodiode PHDNW850 provided by the process is with an N-Well and includes anti-reflection coating. A circuit is available to use as an approximation and behaves identically as their photodiode for simulation usage. The input voltage range used is between 1uV and 100nV. The parasitic extraction listed its total capacitance to be $11fF$.

2.1.2 Possible configuration

As the pixel architecture is as now, it's impossible to perform a true CDS due to the reset signal. Instead of sampling it before the exposure, it needs to be sampled afterwards, especially if it's for a global shutter scheme. This reduces the CDS ability of reducing kT/C because the reset level will not be the same as the one the signal drop begins from. CDS still reduces FPN, but is known as a non-true CDS. A possible configuration would be to add an additional transistor between Tx and the photodiode, a Tx_2.

With this structure, one can sample the reset signal beforehand and store it at the FD-node. After the exposure, the accumulated charges can transfer over Tx_2 and store it in the node between this and Tx_1. The CDS will be able to sample the reset signal of the FD-node first. Tx_1 turns on for charge transfer over to the FD-node and the reset signals drops. The signal sampled at this rate is then the true signal drop from the same reset signal sampled earlier, and true CDS is then performed. This configuration is not implemented due to the additional transistor would increase the pixel size and if done the quantity of pixels would most likely be reduced.

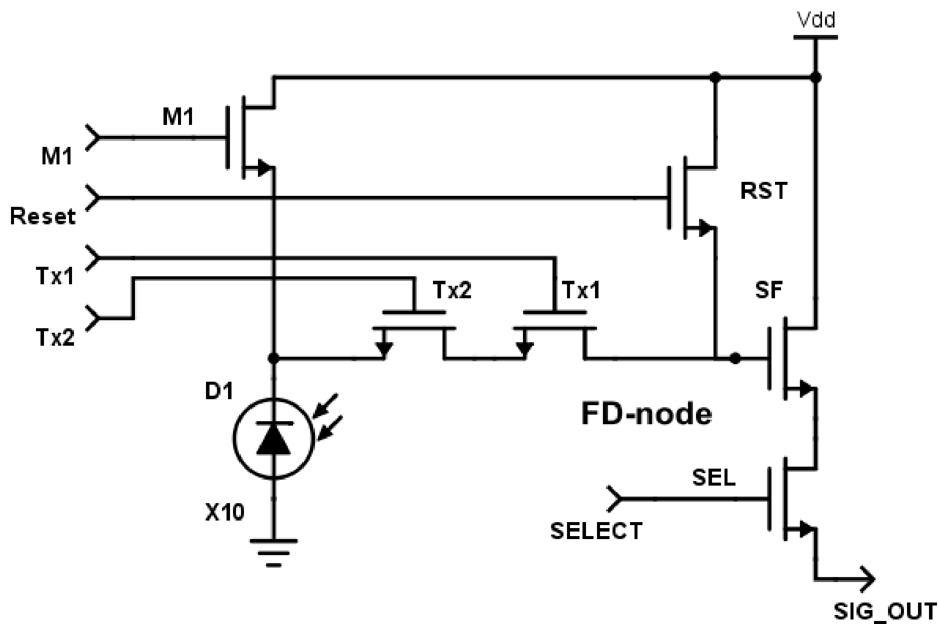


Figure 2.5: A 6T-pixel architecture

2.2 M1 buffer

The gate signal to the transistor M1 in the pixel is used by all pixel units simultaneously. Since the array consist of long metals path and vias, extracting the parasitic RC values are necessary to find an appropriate buffer for M1 signal. After layout extraction, the parasitic capacitance is around 50pF and the resistance is calculated by finding the total resistance of a single path and calculated as a parallel connection. The final design of the entire chip will consist of input and output pads and each of these pads has a buffer of their own and are included in the test bench. The test bench consist of the different predefined buffers and pads found in the library, see figure 2.6.

Assuming the image sensor captures 15FPS(frames per second) with 128×128 pixel units. Each frame get $66ms$ for exposure and read out. Assuming the exposure time is 5ms, a single pixel has a readout time of $\frac{66ms - exposure_time}{128 \times 128} = 3.7\mu s$. Within this period, M1 needs to be turned on right after exposure. The approximated time for possible exposure and readout is in μs and so M1 should not have a rise or fall time longer than this. According to the simulation, a BUFX32 seems to be sufficient enough for a rise and fall time around 54.7ns and 35ns respectively.

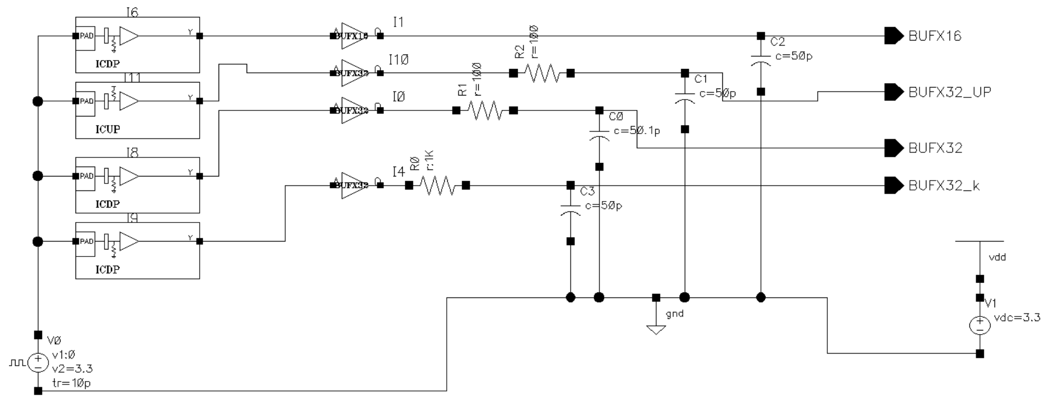


Figure 2.6: Schematic of M1 buffer test bench

2.3 Tx control

The design has incorporated a control circuitry for the transfer gate, Tx, in order to perform the skimming technique. The main aspect of this circuitry is to provide Tx different voltage levels, with the range 0V to 3.3V, from external voltage sources through switches and a decoder to control these, see figure 2.7. The implementation is beneficial for pulsing Tx with different voltages in a short amount of time, reducing delay and including the decoder in the chip will provide a faster and accurate switching instead of feeding in an AC voltage signal externally.

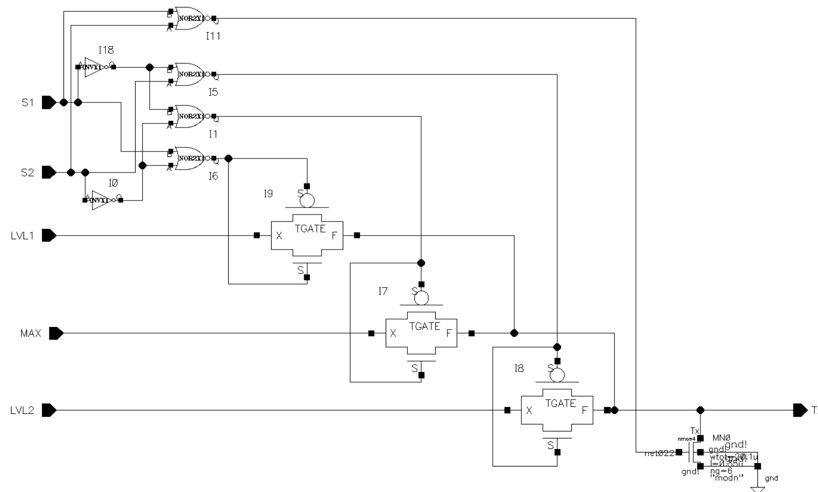


Figure 2.7: Tx control schematic. The decoder is to the upper left

The switch used in this scheme is a transmission gate, also known as an analog switch. The switch is made up of an nMOS and pMOS transistors. The two transistor are connected in parallel by their drain and source terminals and their gate receives the same signal, where one of them is inverted. Their substrates, nMOS and pMOS, are connected to ground and

power supply voltage respectively. With this switch, it can effectively pass both logic low and logic high signal and is able to use the entire voltage range compared to a single MOS switch. The sizes of these transistors are increased to achieve a bigger channel between source and drain. The size of the pMOS is doubled compared nMOS to match the pull up and pull down effect. This configuration is necessary considering the signal will need to be forked out to the entire pixel array and the extracted parasitic capacitance is approximately 50pF.

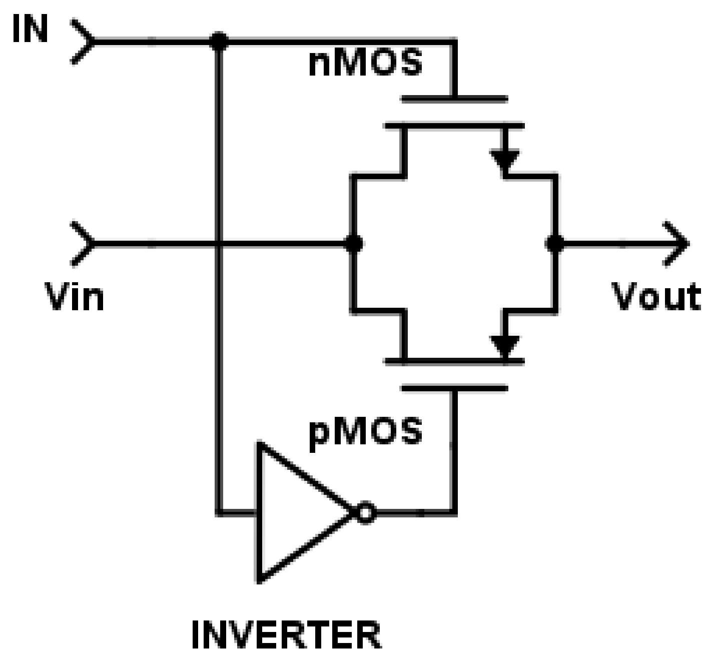


Figure 2.8: The transmission gate

The decoder for controlling the switches receives two external digital signal, S1 and S2, and produces 4 outputs. The table for the S1 and S2 and their outputs selection in plotted in table 2.1. The decoder itself is small and therefore uses regular binary counter compared to the addressing decoders and consists of a combination of NOR and inverters to achieve the outputs, see figure 2.9. This configuration can simply be adjusted into Gray Code if hazard were to occur during chip test by adjusting the input voltages and VHDL code. The transistor sizes are set by simulating multiple tests with an output load of 50pF and 100Ω, which is the total parasitic capacitance and resistance of the Tx metal path into each pixel unit.

S1	S2	Voltage level
0	0	0
0	1	LVL1
1	0	LVL2
1	1	MAX

Table 2.1: Table of the Tx decoder

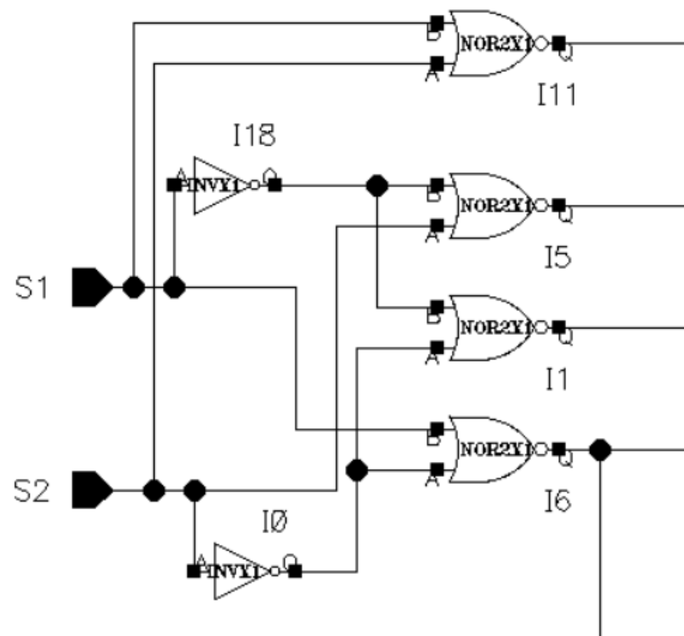


Figure 2.9: Close up of the Tx decoder

2.4 Sample and Hold Circuitry

A simple sample and hold circuitry with a non-true CDS technique, see figure 2.10. This is to utilize the CDS theory as much as possible by sampling the reset signal shortly after the voltage drop has been sampled to prevent any noise that might occur during time.

A common CDS uses capacitors, but the layout of a single capacitor occupies a large area, see figure 2.11, and considering the photodiode in use, the chip exceeds the restricted total area. For this reason, a MOS capacitor[9] is used instead due to its thin-oxide. The project has chosen to use nMOS because it requires less space in layout compared to pMOS. The drain and source terminals are connected to ground along with the bulk. A common capacitance value for storage capacitors is approximately 600fF and to achieve the same capacitance with a MOS capacitor, it's width and length must assign accordingly. To find the appropriate values for the size, the equation 2.1 is used.

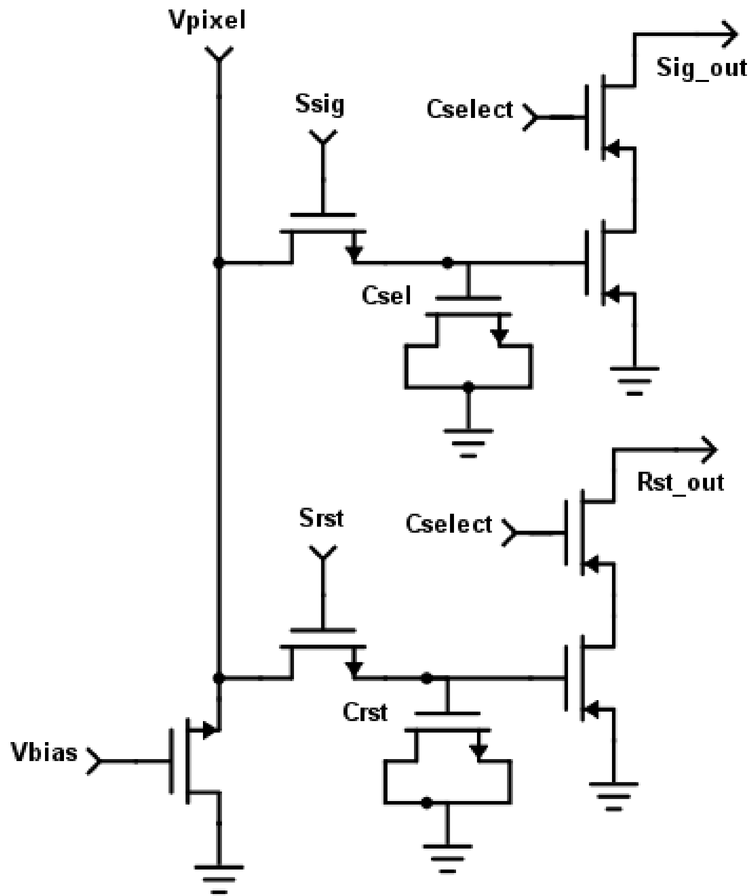


Figure 2.10: Correlated Double Sampling circuit

$$C_{MOS} = W \times L \times Cox \quad (2.1)$$

Cox($fF/\mu m^2$) is the MOS gate capacitance[1] per area, W and L is the width and length respectively. According to the datasheet, the nMOS Cox is around $4.54 fF/\mu m^2$ and with W/L = $15\mu m/10.25\mu m$ the MOS will gain a capacitance around $698 fF$. This value is only valid if the gate voltage exceeds the V_{th}.

The readout process starts with selecting a row of pixels, allowing the voltage drop signal to travel down to their respectively CDS, while the S_{sig} is high to store the signal in C_{SIG}. After this is completed S_{SIG} turns off and the pixels, at the same row, resets it's FD node. Once again, the row

[1]MOS transistor has several parasitic capacitance due to it's structure. Cox, capacitance of the oxide layer, is the capacitance between the gate and the channel(assuming a channel has been formed). This value varies and depends on the dielectric($\epsilon_{ox} \times t_{ox}$) material used

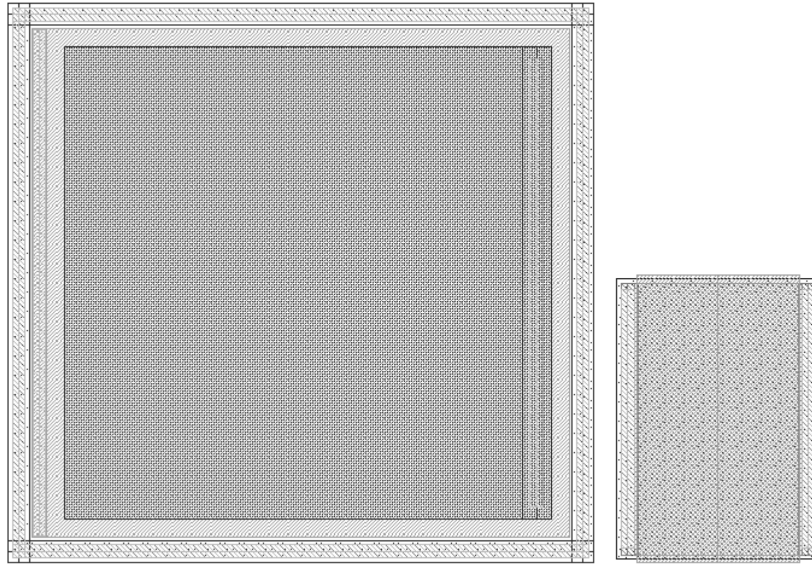


Figure 2.11: Poly-poly capacitor VS MOS capacitor with the same capacitcane

gets selected and S_{RST} goes high to samples the reset signal to C_{RST}. At the end of the CDS circuit, a second set of transistors are present which operates as a current source. These two pMOS are common for the entire array and are biased with an input voltage range of 2.2-2.6V, see figure 2.12.

As mentioned in the Background chapter, CDS has transistors of their own and mismatch occurs among these components as well and produces column FPN. The configuration DDS was considered, but due to limited area, this isn't implemented. The priority of the project is to complete CDS in the layout beforehand and the remaining free area should be used by enlarging the storage capacitor to improve signal accuracy and longevity.

2.5 Decoders

An image sensor with global shutter could use a shift register due to it's low power consumption and since there's no special addressing requirements to complete the exposure and readout this method is quite suitable. In this project this structure is incompatible due to the requirement of supporting the skimming technique and the use of CDS. Addressing to a specific pixel during exposure and readout becomes necessary and for this purpose binary decoders are required. Decoders are digital circuits and operates by receiving multiple input signals and has multiple outputs. Each combination of the input signal converts to a specific output state and it's common to have enable signals, which can be used to disable the decoder and resulting low output signals, preferably

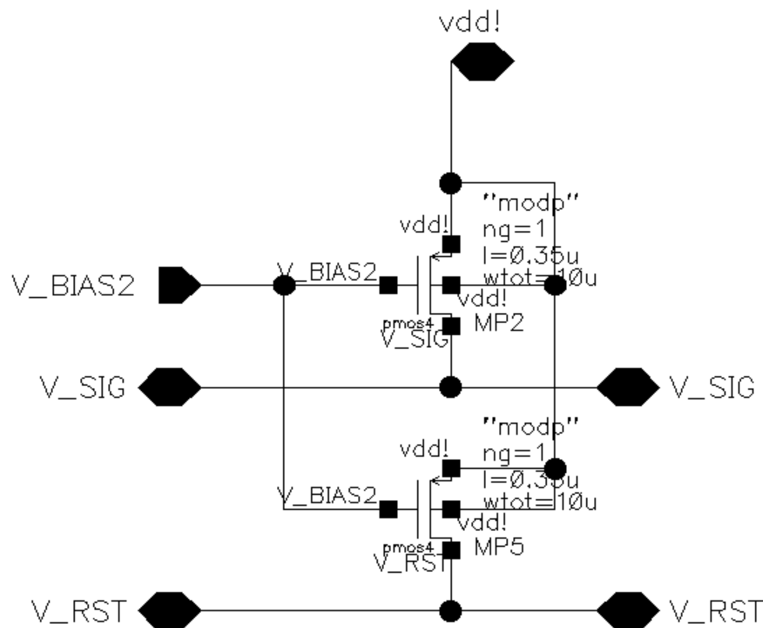


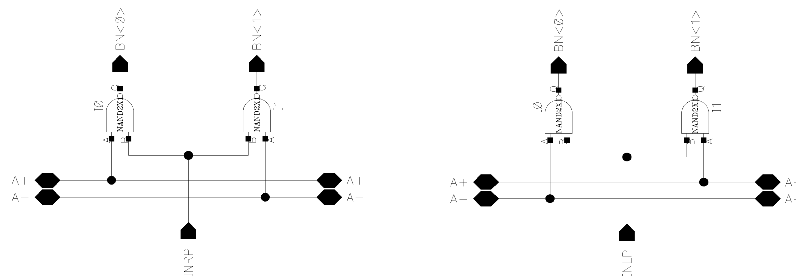
Figure 2.12: Current source at the end of the CDS circuit

zero. The decoders in this project converts n numbers of input signals to 2^n output signals. Commonly, decoders uses natural binary codes format, but using Gray Code format or also known as Reflected Binary Code (RBC) is more preferable. Gray Code changes only one single bit at a time when incrementing or decrementing a specific value and this trait reduces the total bit being toggled. This scheme reduces power consumption, prevents possible glitches and is able to provide a more accurate addressing, a small example is given in table 2.2. As mentioned, these decoder are the same as the ones design by Mathias Wilhelmsen and slight modifications are done for the decoders to be usable for this project. For more details of the creation can be read in his paper[22].

Both decoders are divided up into hierarchies and built up in a symmetrical binary tree. The simplest block of the hierarchy consist of a pair of NAND or NOR gates to create a 1-2 decoder, see figures 2.13 and 2.14. Since NAND and NOR are complementary of each other this feature is taken into account by building alternating layers of these gates and within each layer the blocks expects a positive or negative input interchangeably and produces negative or positive outputs respectively. Also the use of address signal within each block of a single layer, A+ and A-, are swapped. Further details of design process of the decoders can be found here [22].

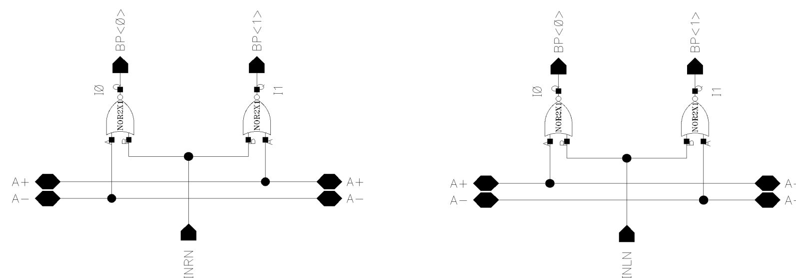
b[0:3]				g[0:3]			
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	1
0	0	1	1	0	0	1	0
0	1	0	0	0	1	1	0
0	1	0	1	0	1	1	1
0	1	1	0	0	1	0	1
0	1	1	1	0	1	0	0
1	0	0	0	1	1	0	0

Table 2.2: Binary code vs Grey code



(a) NAND gate with negative input (b) NAND gate with positive input

Figure 2.13: NAND gates



(a) NOR gate with negative input (b) NOR gate with positive input

Figure 2.14: NOR gates

2.5.1 Row Decoder

The original row decoder has 8 addressing signals and produces 256 select and reset signals. This number exceeds the requirements and needs to be reduced. The method of reduction is to half the binary tree, both within the first single 4-16 decoder and the quantity of the 4-16 decoders. The result is a single 3-8 decoder and 8 quantities of 4-16 decoder, see figure

2.15 and 2.16.

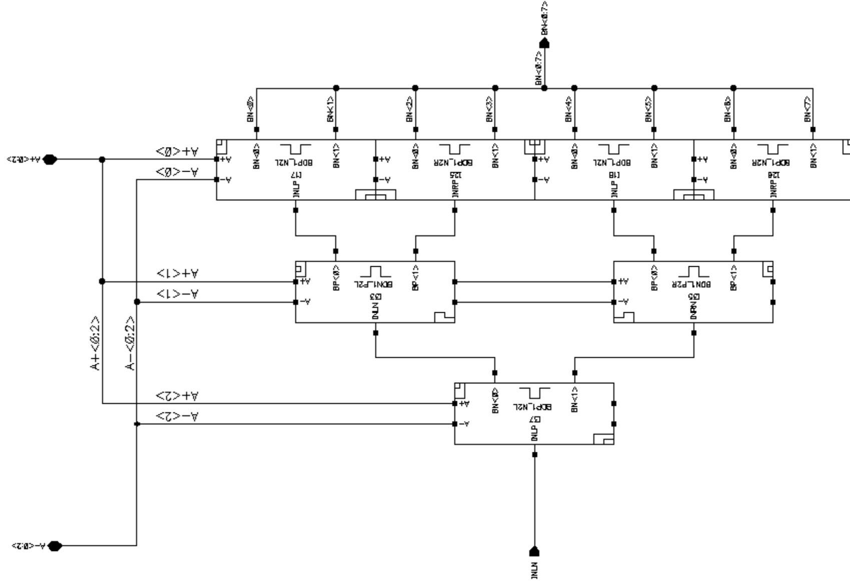


Figure 2.15: 3-7 decoder

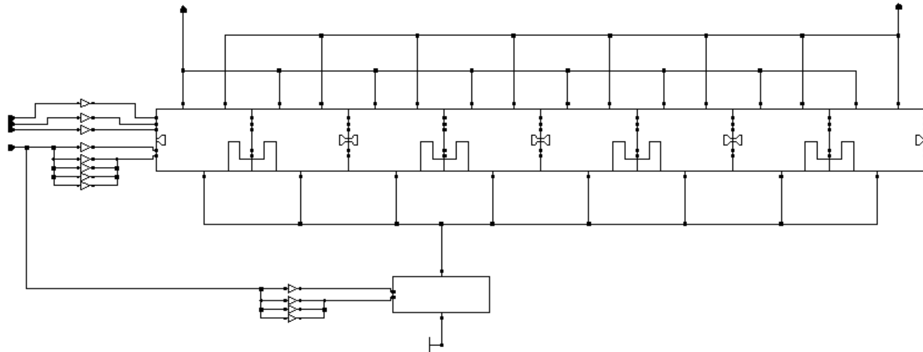


Figure 2.16: Row decoder: a single 3-8 decoder and 8 4-16 decoders

Row decoder has incorporated an extra NOR and inverter gate at the last layer of logic blocks to override the regular reset and select signals with a global reset signal. The global reset signal is the signal used to initialize the exposure process and applies to all reset transistor in the pixel array. The global reset differs from the general reset signal in form of the reset signal will only reset the FD-nodes of a single row of pixel. This can certainly be done in a much simpler approach, such as connecting the global reset directly into the reset transistor, but to prevent inaccuracy which may appear during test phase with the FPGA, this signal is included in the decoder. The logic operation for this is included in the last layer to reduce the amount of path the signal need to travel and for simplicity, see figure 2.17

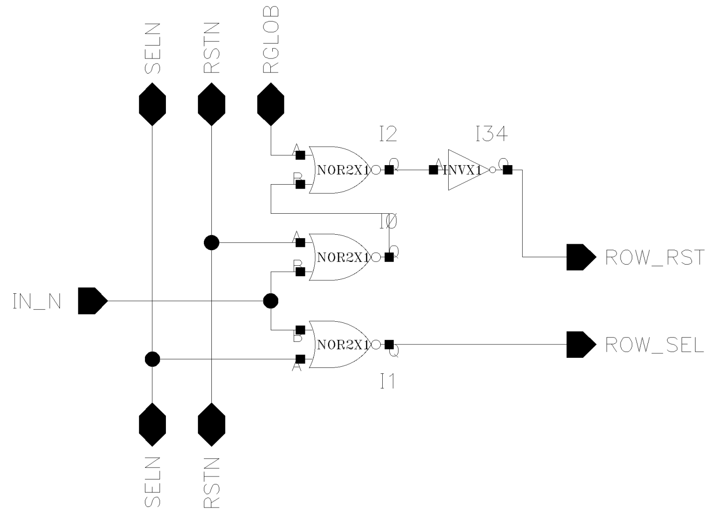


Figure 2.17: Last section logic circuit with global reset signal

2.5.2 Column Decoder

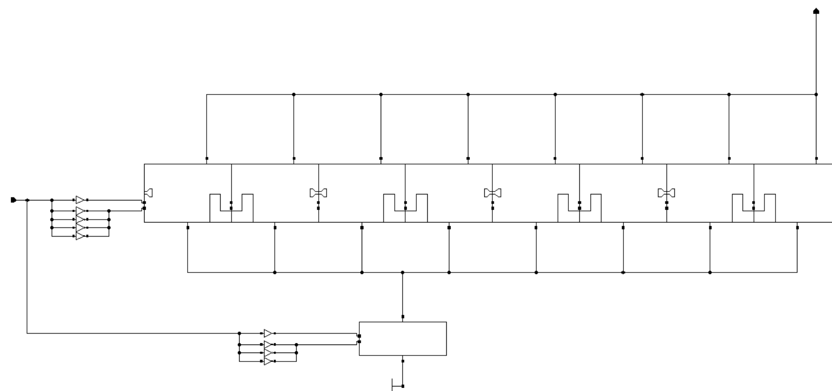


Figure 2.18: Column decoder with a single 3-8decoder and 8 4-16 decoder

The column decoder is a direct copy of the row decoder. The pixel array is square and therefore the 7-128 decoder used for selecting rows is compatible as a column decoder. The only difference between the two is the last layer of the logic, designed for the select enable, reset and global reset signals, is excluded.

2.6 Top

The top level schematic connect all units together, see figure 2.19. A minor mistake is done at this level and needs to be taken account for. The sample signals for sampling reset and voltage drop are swapped. The mistake

isn't devastating since the path and bias voltage used for both branches are identical, but this mistake can affect the result by inverting the image, assuming the analog to digital expects a differential input with reset as the reference signal.

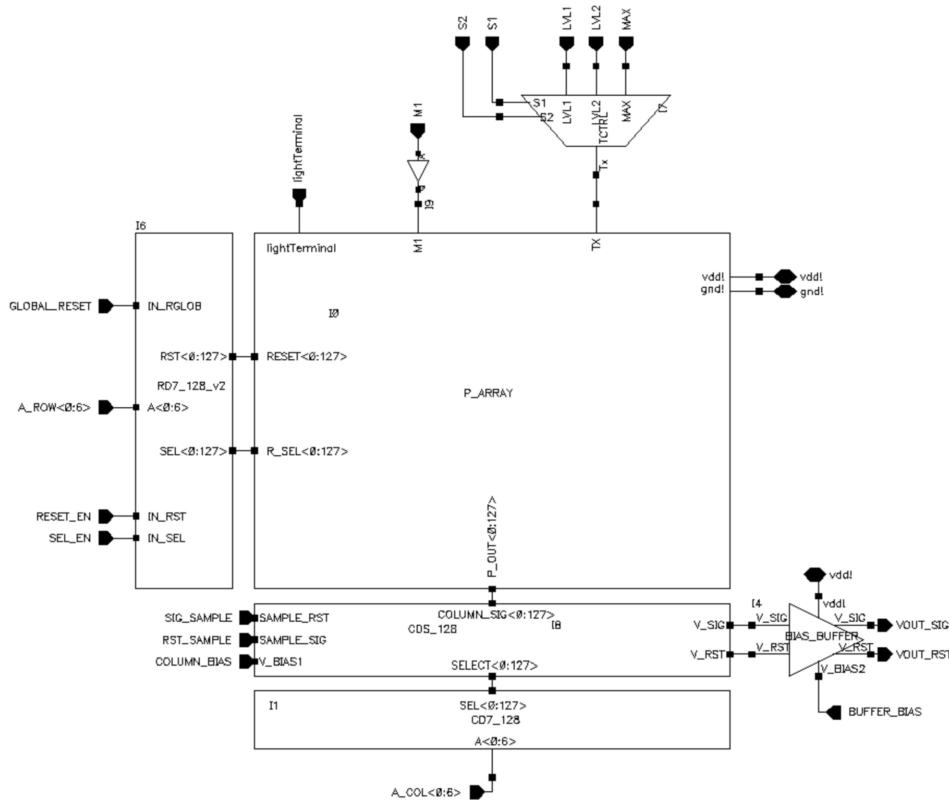


Figure 2.19: Top hierarchy of the chip

2.7 Layout Preparation

The total size of the chip was later expanded to include an additional ASIC design provided by another master student, Espen Klein Nilsen. For this purpose and to reuse the pad frames assembled by Wilhelmsen[22] and Stian Hjorteset[7], it was decided to use the JLCC84 pin package, having a total of 84 available I/O pins. Several of the pins are allocated to ground and power around the pad frame, with a spacing of $100\mu m$ between as a rule of thumb, to prevent potential ESD[2] damage. The pads were

[2]Electrostatic discharge is the term used when two differently-charged electric objects come in contact and the flow of electricity occurs. This can cause an electrical short and damaged the objects

available from foundry, with ESD protection included, and has analog or digital types, where the digital pads can either have a pull up or pull down ability. The available pads are distributed between the two ASIC, reducing the quantities of available pads for this project and test pads are limited. Including routing the I/O signals, some pads are connected to parts of the chip to observe its responsivity. The main objective is to validate it's functionality and enable simple debugging. Three test pads are added; row<1>, columns<16> and the output signal of the first column of the pixel array. The row and column are connected to verify its period corresponds to the code from the FPGA and to inspects their rise and fall time. The output of a row of pixels are connected to validate the signal change with the illumination and reset. More test pads should be added for verification and testability check, but due to limited pads, these are excluded.

2.8 Simulations

Design phase consists, not only of the schematic design, but simulation tests were done as well. Test benches were designed specifically and various of these have been set to test specific unit created for finding suitable transistor sizes, confirming each units functionality and adjusting the design accordingly. Row and column decoder have never been tested together with other units due to the simulation is time consuming, but instead they're tested separately to verify their functionality. The top test bench contains only of a 4×4 pixel array for simplicity and the same quantity of CDS as well, and not 128×128. The bias voltages for column current source and output current source are simulated with varying bias voltages and these ranges are noted down for further test of the image sensor chip. The functionality test of the top version is design for global shutter, but skimming method simulation test was never performed. The final test bench included the output capacitance and resistance of the pads to perform a simulation as realistic as possible.

Chapter 3

Layout

The layout design for the chip will be mentioned in this chapter. All units have passed Layout vs Schematic and Design Rules Check simulations. The extracted parasitic capacitance are taken into consideration and schematics have been modified to compensate for these. The design is divided into parts, in the same manner as the schematic design, allowing straightforward routing, convenient modifications and makes revising warning and errors of each design easier. The division of the parts are distributed between Marius and I to route, which is beneficial with limited time, and complete the design as effectively as possible. Some units have been modified by both, but the one who completes the final layout has the parts listed as their work, see table 3.1.

Soman Cheng	**Marius L. Lillestøl**
Row Decoder	Pixel and Pixel Array
Column Decoder	Tx Control
Bias Buffer	CDS
Top	M1 buffer
	Top

Table 3.1: Work distribution

The units implemented by Marius L. Lillestøl will be mentioned briefly and the scheme is explained. Further details of the actual approach to the final design are not described and one must refer to his paper[11].

3.1 Pixel and Pixel Array

The layout of pixel is created with the idea of keeping the structure as compact as possible and a high fill rate is desirable. Several attempts have been done to keep this ideal. The very first implementation was done to keep the total area to be as minimal as possible, but this layout didn't take the input signals nor routing into consideration, resulting overlapping

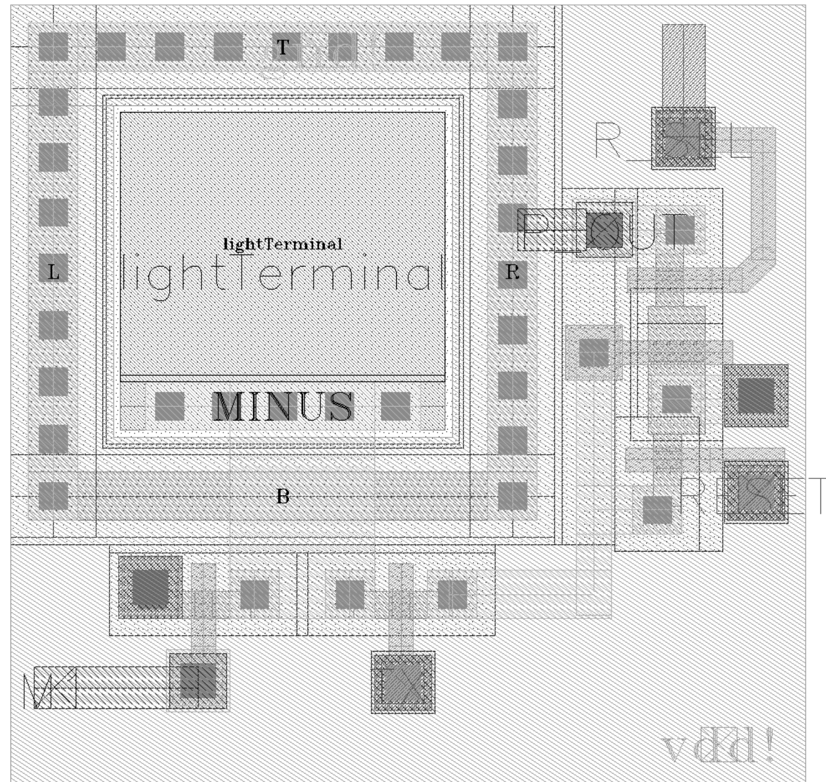


Figure 3.1: Layout of a pixel unit

metals and an increment use of vias. The later layouts were done not only to keep the total area minimal and square, but also to provide a simple routing system between all pixels without unnecessary use of vias. The final layout establishes a good base for further implementation of the pixel array. The progress went on to creating a pixel array with 128×128 pixel units. This is done by first copying the pixel unit, with the desired quantities of it and assigning the pitch size, which is the same as the width or length of the pixel unit itself, and placed under the first pixel to create a single column. The same method was done to create the input and output pins, but with a varying number, such as SE. No routing was done because a single pixel unit has already routed the signal path all the way to the edges and by placing the units next to each other, these path are automatically connected. The row was done with the same strategy, but instead of copying a single pixel, the whole columns was copied. Figure 3.2 is small section of the total pixel array.

MET4 with sloths are placed on top of the pixel array. The sloths are the opening for the photodiode to detect light, otherwise the rest of pixel array is fully covered. This is to shield the FD-node, transistors and signal paths from being exposed and affected by incoming light sources. The shielding is important to obtain a high shutter efficiency[1], especially

[1]Shutter efficiency described how much the stored pixel value is affected by incoming

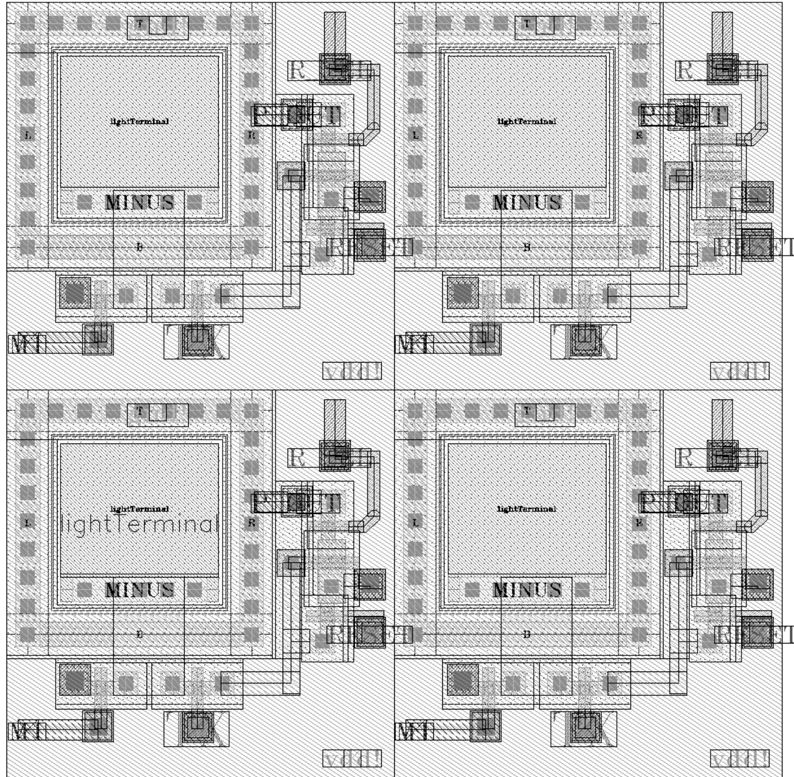


Figure 3.2: Layout of a 2x2 pixel

for a global shutter image sensor because obtaining accurate information without artifacts is the top priority. The extracted capacitance of the FD-node is approximately 0.7fF and combined with the gate capacitance of the source follower[2], the total capacitance is approximately 1.97fF. Compared to the photodiode, which has a capacitance of 11fF, the FD-node has a much lower value and will not be able to fully utilize the photodiode. The calculated fill factor for a pixel unit can be found in equation 3.1

$$FF = \frac{5\mu m \times 5\mu m}{11.25\mu m \times 11.25\mu m} \times 100 = 19.75\% \tag{3.1}$$

Lastly, a guard ring connected to ground is placed around the entire array. This is to protect the sensitive circuit from the neighboring ones in terms of voltage and current. A ground-connected ring allows easier ground routing for the pixel array as well as providing a stable ground network and multiple connection to reduce impedance.

light and distorts the information when awaiting for readout. The incoming light is unrelated to the exposure period and is typically unwanted

[2]calculated its capacitance in the same manner as with the MOS capacitor

3.2 Tx control

Tx logic is built around the transmission gates due to their large sizes. The N-well and P-well of both transistors requires a minimum spacing between them and are therefore placed with a distance between.

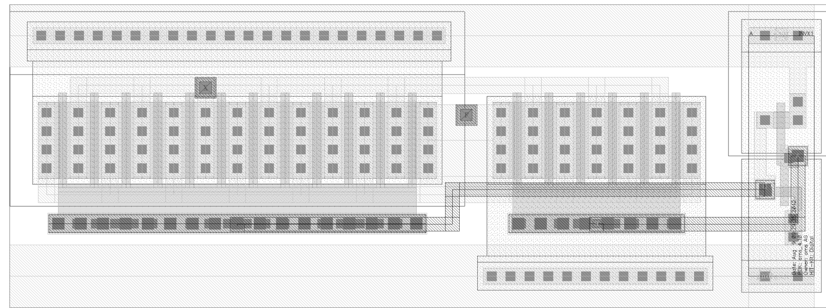


Figure 3.3: Layout of a single transmission gate (left) pMOS (middle) nMOS (right) inverter

The NOR gates are placed closely to their respectively transmission gate for shorter signal path to reduce resistance and capacitance. The inverters for these NOR gates are done in the same manner. The most suitable placement for the unit will be on top of the pixel array and so the length of this unit can be disregarded due to the length of the pixel array dominates. The components are therefore placed horizontally to minimize the total width. The scheme results in a width and length of $13\mu m$ and $140\mu m$ respectively, see figure 3.4.

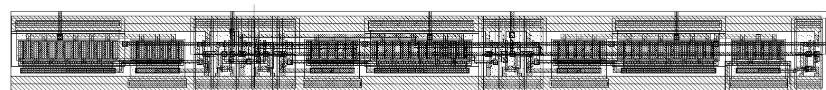


Figure 3.4: Layout of the Tx control

3.3 CDS

The CDS array is placed below the pixel array and above the column decoder. The layout was made with the calculated size of the MOS capacitor, but to maintain the simple routing scheme, the length of a single CDS unit should be the same as the pitch of the pixel array, which is $11.25\mu m$. This size is too small to place the components horizontally and instead needs to place vertically. Since the pitch is slightly larger than the width of the MOS capacitor, this allows a slight size increment. The transistors are placed between the two MOS capacitors. This is to reduce the possibility of crosstalk, see figure 3.5.

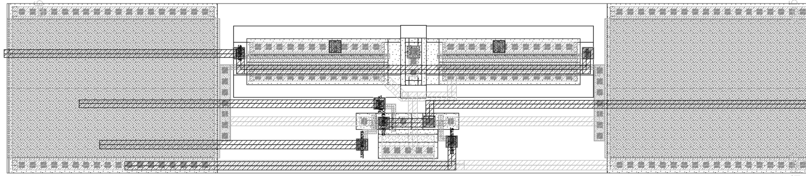


Figure 3.5: Layout of a single CDS (Rotated)

In this unit, the second largest components are the pMOS used as coloumn select switch and source follower, and these in general requires quite an amount of spacing and the minimum required space between their NTUB[3] and the NTUB used for nMOS needs to be fulfilled. The sample switches are less critical, but the path between them and the MOS capacitors should have the same length to keep both branches as identical as possible. In the final layout, the select and source follower shares a single contact, snapped together in the layout, and are placed on the left side. In total, there are 4 pMOS, the select and source follower of each branch. The nMOS switches are placed in the middle and the last nMOS transistor used as a current source are placed to the right. The two branches are symmetrical, except for the path connecting from the MOS capacitor and their respectively source follower. The differences lies in one of them are routed with a 90 degree turn, while the other one has a 45 degree turn. Figure 3.6 shows how the CDS are connected together. The MOC capacitor shares their drain and source terminal which are connected to ground. The signal path on the left side beginning from the top are select, bias voltage, and sampling signals. The signal path from the left side is connected to the output of the pixels.

3.3.1 Output Current Source

The output current source consist of two pMOS, both having their source terminal connected to the power supply, their drain terminal to their respectively inputs and their gate terminal to an external voltage. To maintain identical travel path for reset and voltage drop signal, the two transistor shares their source terminal, by snapping their contacts together, and adding a single via connected to VDD. Their gate are connected together on the left side with a via, their drain terminal are faced outwards which allows the path to route straightforward without having any turns. This is one of the simplest layout implemented, see figure 3.7.

[3]NTUB is the n-well. For transistor, one usually adding an implant mask above it, either a P or N-type

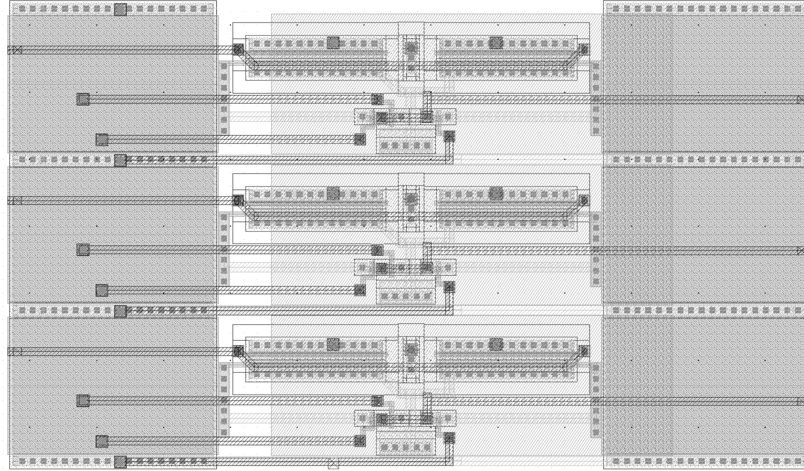


Figure 3.6: Layout of 3 CDS (Rotated)

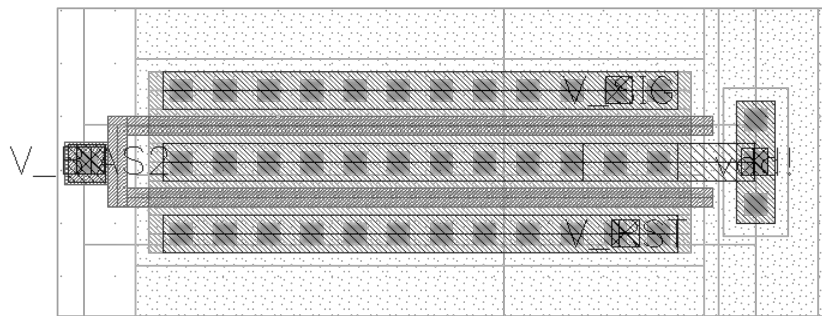


Figure 3.7: Layout of the pMOS current source

3.4 Decoder

The layout of decoder are huge and consists of many sub-modules. The main challenges of this part is to route between these parts correctly and maintaining equal path length. Despite the modules are repetitive, their signal path varies and routing them needs to be done carefully to avoid wrong inputs and outputs. The NOR and NAND pairs are the base logic block and need to be made without a specific routing path. This provides additional space to route at the upper level without the need of avoiding higher level metals. This reduces routing complication and avoid usage of more metal layers and vias than necessary. This, besides the pixel, is the first layout implemented and both decoders are implemented several times before achieving the most optimal structure.

3.4.1 Row Decoder

The process of row decoder implementation started with the logic block with the reset, select and global reset signal as the input. The outputs,

reset and select signal, are fed to the pixel array. The layout of the logic gates are pre-made and only needed to be placed together and routed.

3.4.1.1 First Design

The original thought was to have all the gates share their respective VDD and GND contacts for simple power and ground routing at the higher level by placing them right beside each other. This structure provides additional space for routing signals around the contacts and was assumed to be beneficial at the upper-level, see figure 3.8

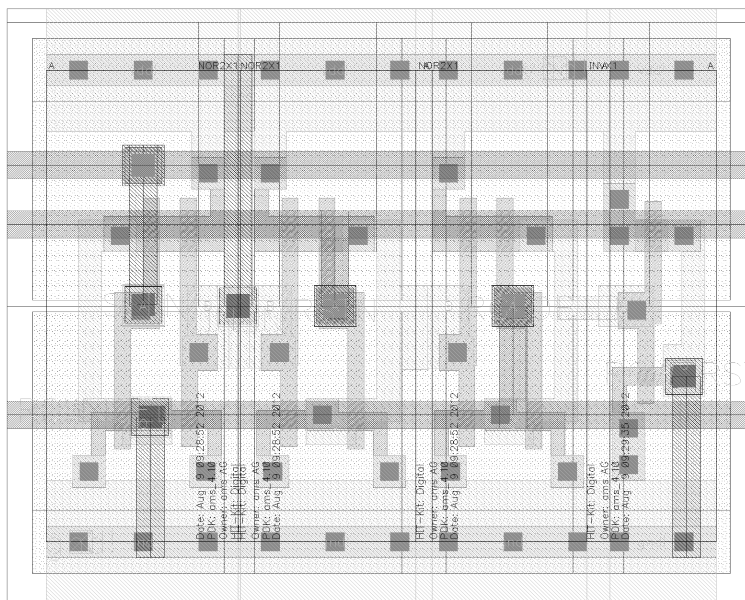


Figure 3.8: First layout of the last logic

By studying the layout closely, there is a minimal spacing between the logical gates due to a DRC rule that gave an error message regarding contacts used for power connections. A general logic gate is implemented with VDD contacts at the top and GND at the bottom. For better connection in case of defected vias and to fully utilize the power and ground potential, it's common to use more than one via for connection. Although, placed with the same orientation, the error occurred when the gates are too close, despite having the same potential. To evade the DRC error, they were placed further away with the minimal required distance. Rest of the NAND and NOR pair blocks were implemented in a similar manner. Vias were added in these blocks to specify where the inputs and outputs are and provide a routing guide. The vias used are from MET1 to MET2 and these seems to be the most natural via to use since MET2 path are not present in this sub-hierarchy. This allows the signals to be routed freely with MET2 to their respective pins. The routing scheme at

the upper level was done by making sure the length of the signal path from each logic block to their respective logic blocks is the same to avoid mismatch in terms of delay. The paths are routed as short as possible to reduce parasitic resistance and capacitance. Some of these blocks are flipped and rotated to share their VDD or GND with their neighboring blocks and, if possible, moving their gate terminal closer to the signal. The first design is shown to be inefficient. The total length of the decoder exceeded the requirements for the chip and the main issue was the first logic block implemented because it contains 3 NORs and a single inverter. Another factor that contributed to a poor layout design is the MET1-MET2 via used in the sub-hierarchy. The blocks are repetitive and assigning a specific via on all input and output caused collision during routing with MET2 layer.

3.4.1.2 Second Design

In the previous design, the length of the first logic block was too large and needed modification. To avoid the contact error with the powers, partial of the component were overlapped. This fixed the DRC error and it didn't respond with any warning. The other logic blocks were done in the same manner.

This design created a more compact unit and the distance between them decreased. The units were placed more strategically as well by having 3 columns of logic units. The first column consist of the 3-8 decoder, buffers, inverters and some logic units of the 4-16 decoders, a collection of 7 NOR and NAND pair units. The first decoder, 3-8 decoder, is placed in the middle to separate the other gates that had no connection and the next gates were placed as so. This placement strategy allows a simple routing method and majority of the paths were routed vertically, either up or down to their respective gates. Few needed to overlap more than a single unit. The second column consist of the last 8 4-16 decoders and the last column consist only of the logic blocks for controlling the signals to the pixel array. The routing scheme is done by making the paths forked out from a logic block as symmetrical and as short as possible to their next logic blocks. The vias used are planned more thoroughly, assigning MET1-MET2 to be the input or output vias from a logic block to next and MET1-MET3 vias are used for the addressing signals forked out from the buffers and inverters. The buffers and inverters are placed at the first column and because the signals need to travel through the entire logic. The signal paths between the logic blocks are routed horizontally with MET2 and addressing signals from the buffer and inverters are routed vertically with MET3. Several signal paths were routed on the left side from top to the end for connecting the addressing signals from the pads. These are placed there so the path doesn't need to route to a specific area.

Despite creating a unit which was more compact than the previous

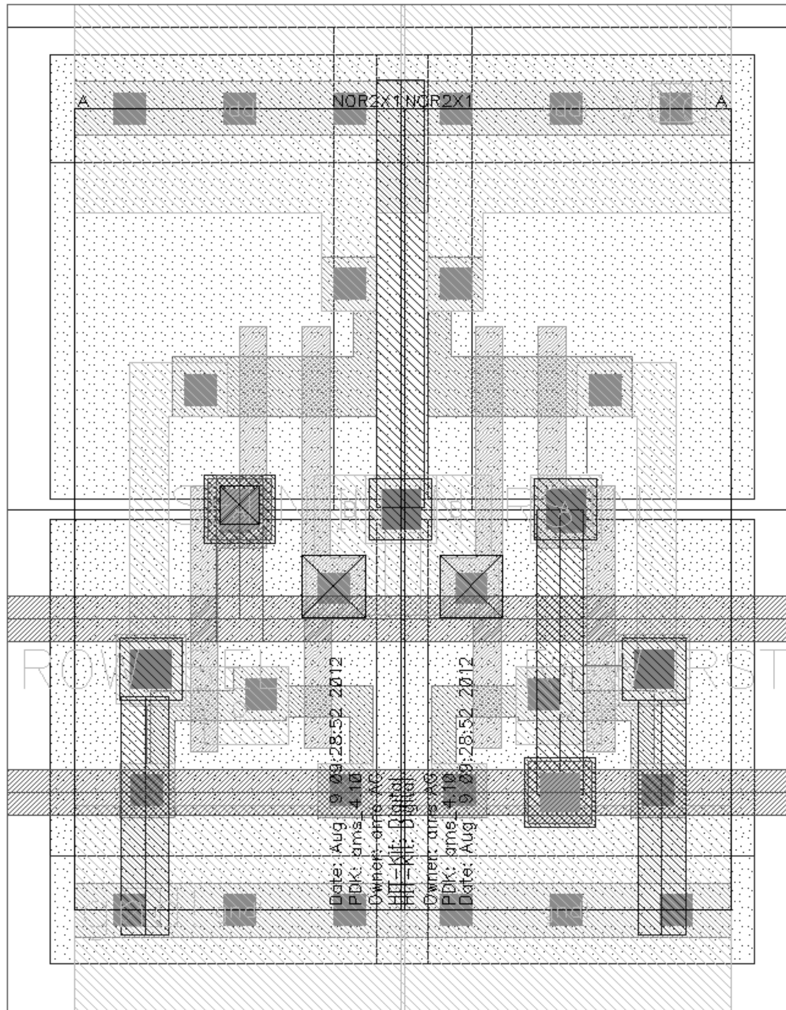


Figure 3.9: Second layout of the last logic (only partial of the layout is included)

design and the length was within the requirements, this design was still inefficient. The attempt of routing the reset and select signals to the pixel array was inefficient. The design didn't take the pixels size into consideration and routing all the signals were nearly impossible. The use of vias were enormous and the routing itself occupied a space even larger than the width of the decoder itself. This routing suffers from crosstalk and parasitic capacitance and resistance. Due to this, this design is abandoned.

3.4.1.3 Final Design

The final design took the pixel size into consideration and the pitch of each reset, select and between the reset and select were measured. These measurements are used in the select and reset logic. The final

design allows non-complex routing into the pixel array and vias weren't necessary.

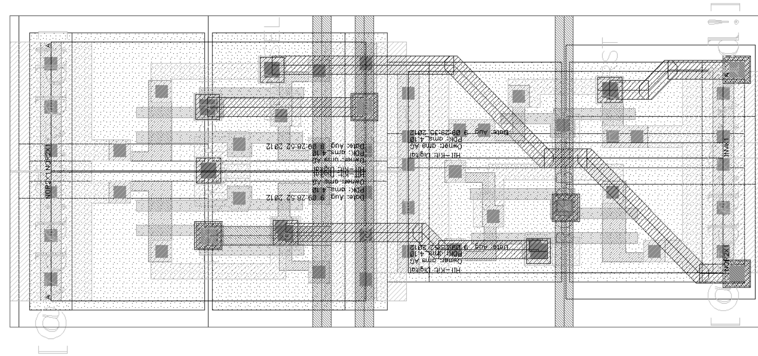


Figure 3.10: Final layout of the last logic

To achieve this, the component placements needed adjustment. The figure 3.10 shows the final structure of the select and reset logic. The two NOR gates for reset and select are placed to the left while the NOR for global reset and the inverter are placed on the right side, closer to the pixel array. This is due to the reset and select signal depends on the input signal from the previous logic, compared to global reset. As shown, the pins are placed with the correct pitch between reset and select as measured in a single pixel unit. At the upper level, the pitch between the reset to the next reset and the select to the next select, needs to have the same pitch as the pixel size itself, but the width of a single unit is too small and empty areas are present. These empty spaces caused error because of the NTUB and needed to be filled. Further implementation of the row decoder remains the same as mentioned in previous section by following the same strategy because the changes of the last logic doesn't affect the rest. Although, the placement of the buffers and inverters are changed. Instead of placing them on the top of the row decoder, they were placed as closely as possible to their respective logic units. The issue with this structure is that the length of the signal path from the buffer is no longer the same for all logic blocks and this may cause mismatch. A possible way of resolving the problem is to add additional buffers and inverters, and route the addressing signal from the pads directly to these as well.

The signal paths for incoming addressing bits are routed from the top and all the way to the bottom with MET1 and MET3 interchangeably, see figure 3.11. This allows them to be placed much closer compared to using a single metal due to the minimal required spacing between the same metal type. The length of these signals path are later shortened depending on where the addressing signal path enters from the pads since there is no need to route all the way, see figure 3.12. The final layout of the row decoder has a length around $1400\mu m$. Partial of the row decoder layout can be seen in figure 3.13.

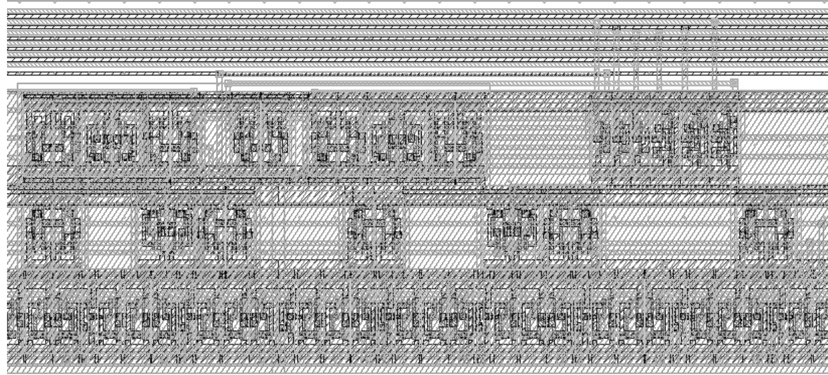


Figure 3.11: (TOP) Signal path dedicated to the incoming addressing bits

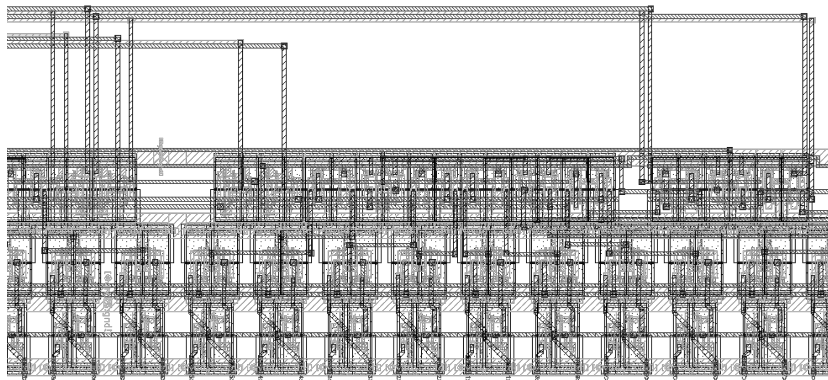


Figure 3.12: The signal path dedicated to the incoming addressing bits is shorten

Figure 3.13: (TOP) 3-7 Decoder (MIDDLE) 2 4-16 Decoders (BOTTOM) Reset and Select Logic (Rotated image)

3.4.2 Column Decoder

Column decoder differs from the row decoder in respect of the final logic with the select/reset signals. Excluding those gates decreases the length size in general. The first design did not take the pixels size nor pitches into account and the decoder was implemented as small as possible. The result was an incompatible size compared to the pixel array and the CDS array. The problem was the same as the row decoder encountered during its second design, the routing scheme was complex, abundant of vias were

required and the total area for routing the signals itself was larger than the decoder. After implementing the final row decoder layout, the scheme and idea are reused in implementing the column decoder as well. Precautions were taken during the second design by following the pitches from the mentioned circuits. The placements of 3-7 decoder, 4-16 decoders, buffers and inverters and the routing scheme are the same as row decoder, but instead of having 3 columns of logic blocks, the column decoder only has 2. A small section of the layout is shown in figure 3.14.

Figure 3.14: A small section of the column decoder

3.5 Top

The top level design consist of the combined units and the additional ASIC. The process of placing the units together required routing and adding dummy structures, specifically poly and MET4, to avoid minimum density area[4] error by the DRC. The additional ACIS is placed on the right side of the chip. See Appendix B for the full image of the image sensor chip.

3.5.1 Routing

The routing process connects the units together by drawing a metal path between their respective inputs and outputs. The units has the same pitch between their input and outputs, and by aligning them properly the path can be routed without bending them.

3.5.2 Pads

The pad frame includes, APRIO1K, APRIO200, VDD3RP, GND3RP, VDD3ALLP, GND3ALLP and ICDP. The power pads, VDD3LLP and GND3ALLP, along the frame with 100μm pitch are not connected to the chip itself. These are used for ESD protection and flows through the entire pad frame. Due to the additional ASIC, using these pads as power source for the chip will affect both ASICs and deactivating one-another during

[4]All metals in the layout has a minimum amount required by the process for proper fabrication. If density rule is not meet, partial of the wafer can be over etched and cause uniformity problem. Isolated metals are weaker and can be damaged when exposed to extreme temperature. Poly needs a minimum of 15% and MET4 need a minimum of 30%

use is impossible. Therefore, these pads are not connected and are purely used as dummies. APRIO1K and APRIO200 are analog pads with $1k\Omega$ and 200Ω respectively. The one with higher resistance is used for connecting the external bias voltages and the lower ones are used for analog outputs from the chip and the single column test point. ICDP are digital pads with a pull down effect. This is desirable to ensure that the signal is low if glitches were to occur. These are also used for connecting the test signals row<0> and column<16>.

3.5.3 Dummies

As mentioned earlier, additional dummy structures are required to evade minimum density error. MET4 is the ASICs power plane, VDD, and is used to cover the entire chip. It's structure is not uniform, but perforated to prevent stress and create openings for the photodiodes. This structure also acts as a shield and prevents transistors and signal paths from being affected by light. Poly structures are filled around the actual chip in form of squares.

Chapter 4

Printed Circuit Board

A Printed Circuit board is presented in this chapter. Both schematic and layout is created with the program CadSoft EAGLE. Requirements are minimal because the main objective is to design a simple PCB capable of powering, running and extracting results of the image sensor chip for testing. The design revolves around a suitable ADC, bias voltages, receiving and sending signals from FPGA, power supply circuit and ground. Previous master students, Hjorteset [7] and Wilhelmsen [22], have created a PCB dedicated to an image sensor and their design is used as a guidance and inspiration for this project. The procedure of creating a PCB is shown in figure 4.1.

4.1 PCB Design

The PCB schematic and board layout are shown in figure 4.2 and 4.3 respectively. The design and components choice are discussed in this section.

4.1.1 Analog to Digital Converter

The most important component on the PCB is the ADC. The ADC is necessary because the image sensor itself doesn't contain one and the existing ADC on the FPGA is unsuitable because of a long travel path going through vias, making the signals vulnerable to noise. The desired ADC should have a differential input to compare the reset and signal voltage because these are the outputs from the chip, instead of including an additional differential amplifier. Parallel digital outputs for data extraction is desirable due to the project will be reusing the code Mathias[22] has written. According to the simulations done in Cadence, the maximum difference between reset and signal is 0.8V and a quantization bit of 14, which will provide a quantization of 256 steps, is desired to fully differentiate the voltage levels. In the design

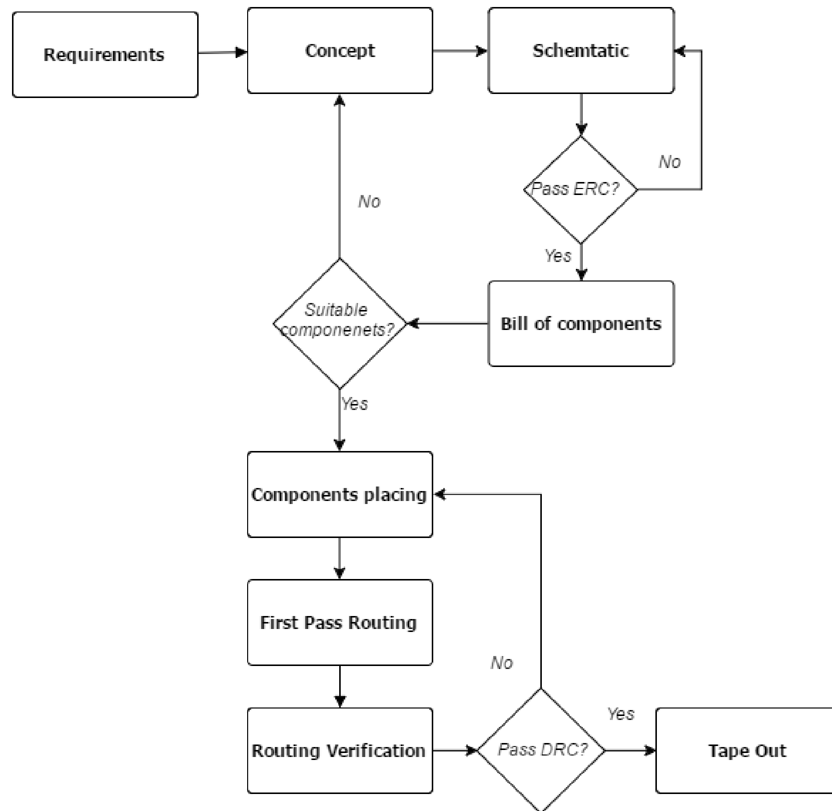


Figure 4.1: Designing PCB approach

phase, a minimum of 15FPS is possible and the ADC should have a minimum sample rate of $15fps \times 128^2 = 0.25MS/s$. A suitable ADC, LTC1746, fulfills the requirements and was used by Wilhelmsen[22] and Hjorteset[7]. The table 4.1 has listed some of the ADCs features.

LTC1746	
Sample Rate	25MSPS
Input Range	$\pm 1V$ or $\pm 1.6V$
Resolution (bits)	14
Voltage Supply	5V
Power Consumption	390mW

Table 4.1: Specifications of the LTC1746

The ADC is placed as close as possible to the image sensor output signals and bypass capacitors are place accordingly to the data sheet. Since capacitor sizes are not given, capacitors of the imperial size 0608 are used. This is to avoid complications during placement due to small size, see figures 4.4 and 4.5 for the schematic and layout.

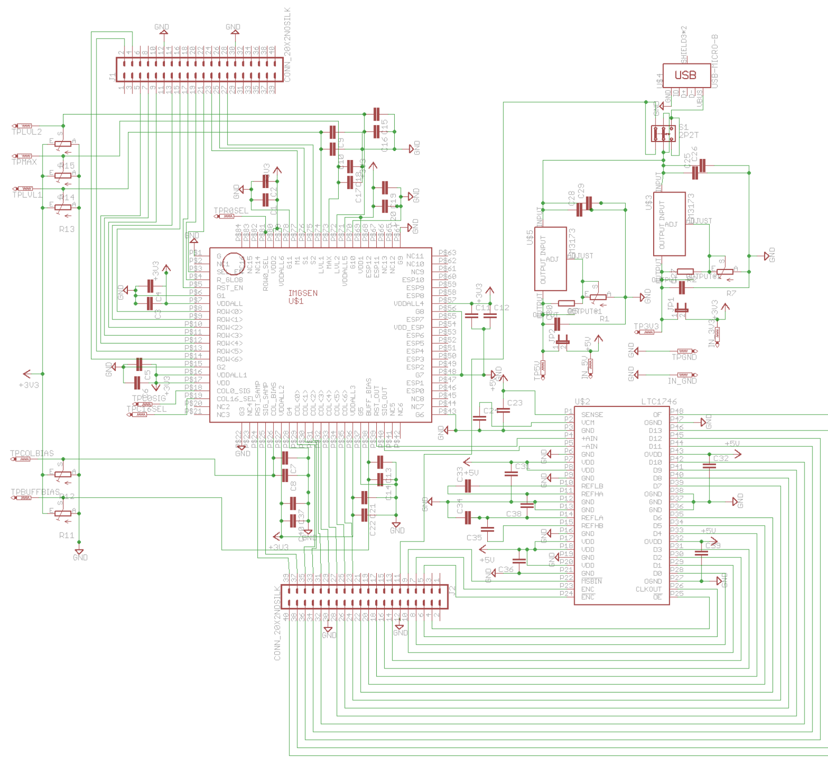


Figure 4.2: Schematic of the PCB

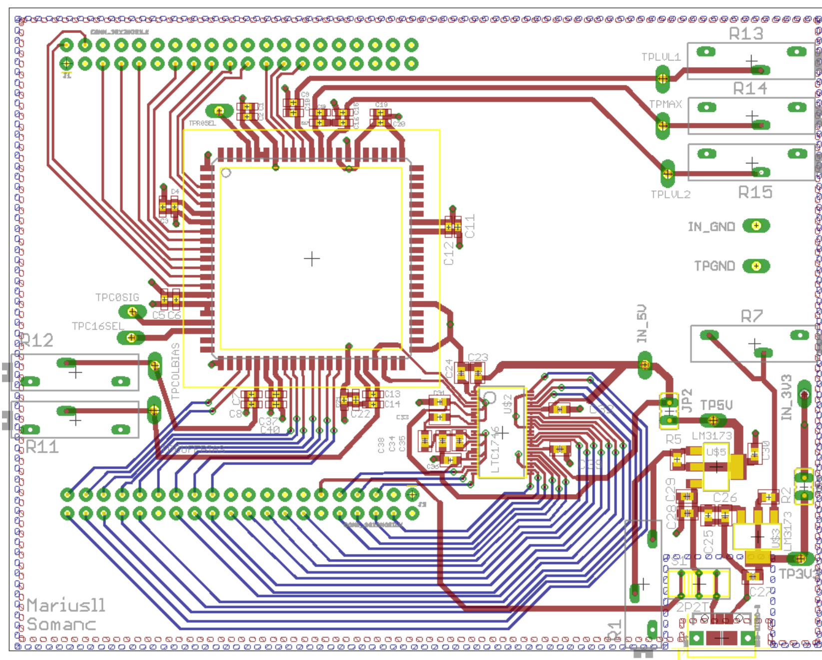


Figure 4.3: Layout of the PCB

4.1.2 Power and Ground

Eagle provides multiple layers PCB design and, with this opportunity, two inner layers, 2 and 15, are dedicated to power and ground respectively,

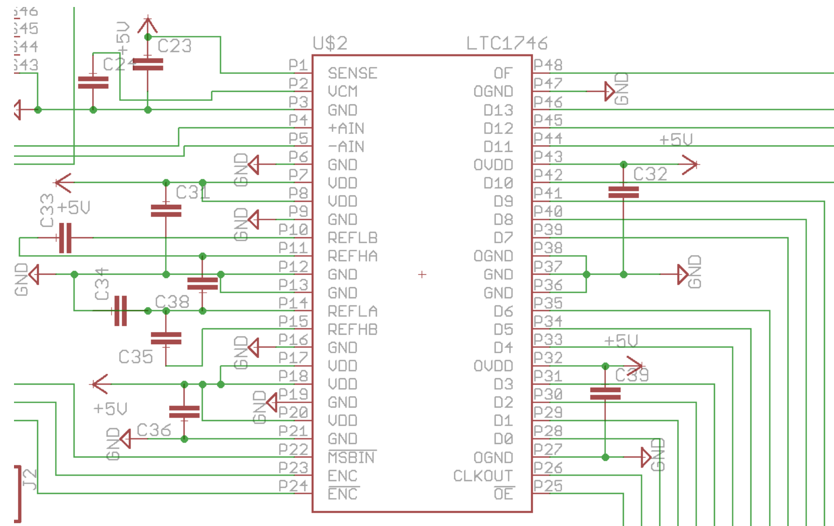


Figure 4.4: Schematic of the ADC

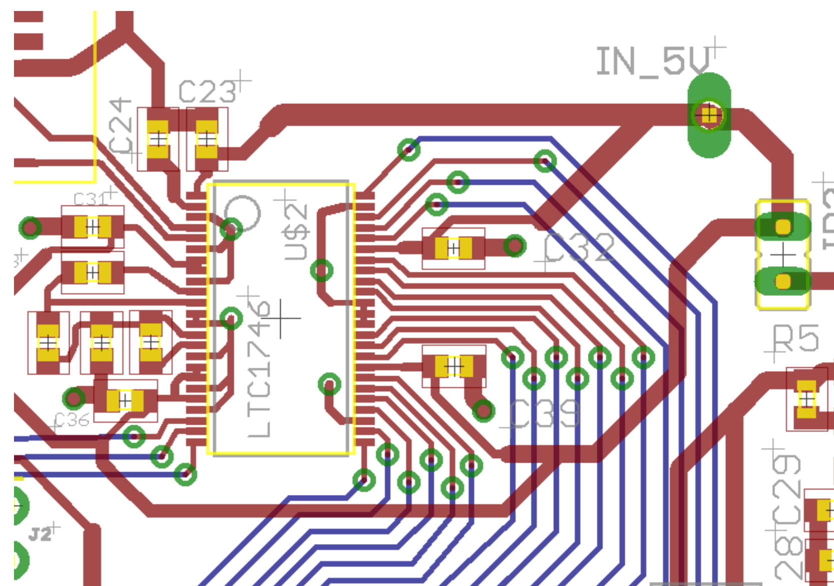


Figure 4.5: Layout of the ADC

see figures 4.6 and 4.7. This scheme allows a simplified power and ground routing to the targeted areas compared to having them on the outer layers where routing and surface mount component(SMT) placements need to be taken into consideration. The power and ground planes creates two plates with opposite voltage and produces a capacitive effect. This effect allows the power plane to feed more current if necessary without experiencing a voltage drop and this can also be achieve by placing bypass capacitors. For the ground plane, it's potential will have a better chance of remaining the same "ground" throughout the PCB and is better at dissipating heat. The inner layers also works as an isolation between the two outer layers,

so the routed signals won't affect each other.

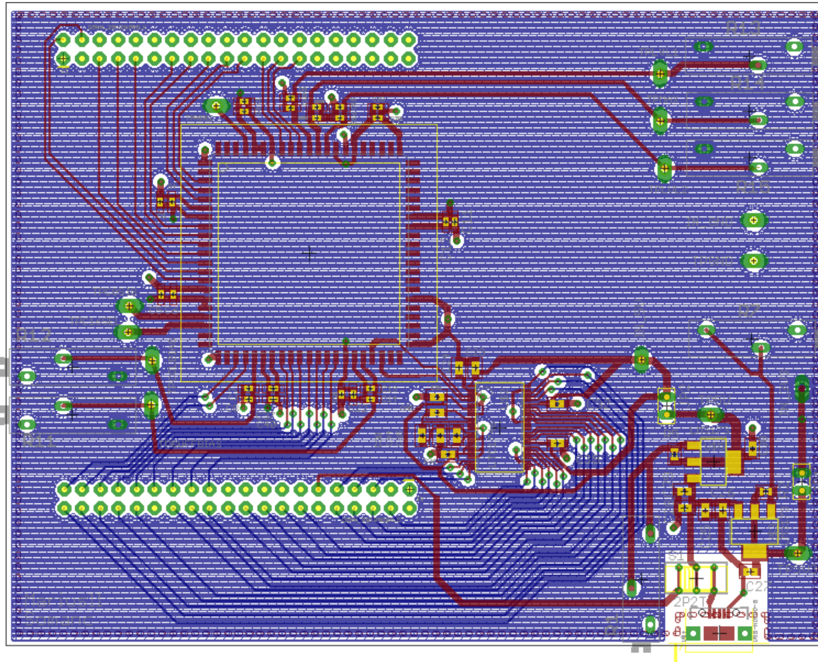


Figure 4.6: Layout of the power layer

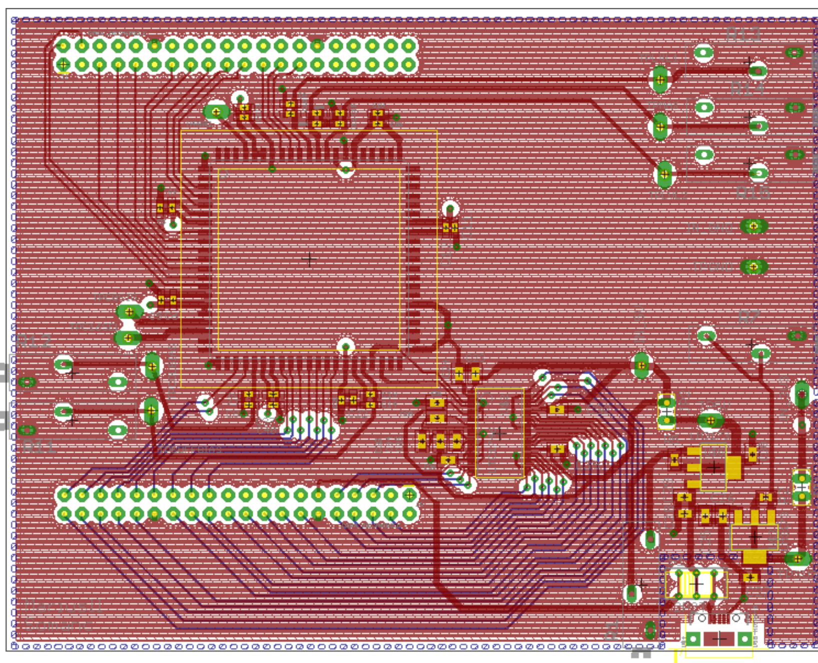


Figure 4.7: Layout of the ground layer

Two alternatives for powering up the PCB is available, either through a micro USB connection or from the FPGA and both provides 5V. The

power supply can be chosen manually with a switch. To ensure the voltage is correct and stable, adjustable voltage regulators are used. Voltage regulator is an integrated circuit used mainly to keep the output voltage stable regardless of changes in input voltage and output load. To adjust the voltage, resistors are connected on the feedback loop and their values are chosen depending on the desired output voltage, see figure 4.8. Jumpers and extra pins are added for manually powering up the PCB with external power in case of shortening. LM317AEMP/NOPB[1] is the voltage regulators used in this project and according to the datasheet the values for the resistors can be calculated by using the equation 4.1.

$$V_{out} = 1.25V(1 + \frac{R_2}{R_1}) + I_{ADJ}R_2 \tag{4.1}$$

Since an adjustable output voltage is desired, the setup follows the data sheets recommendation by using a resistor with the value of 240Ω and a potentiometer with $5K\Omega$ at the feedback, see figure 4.8.

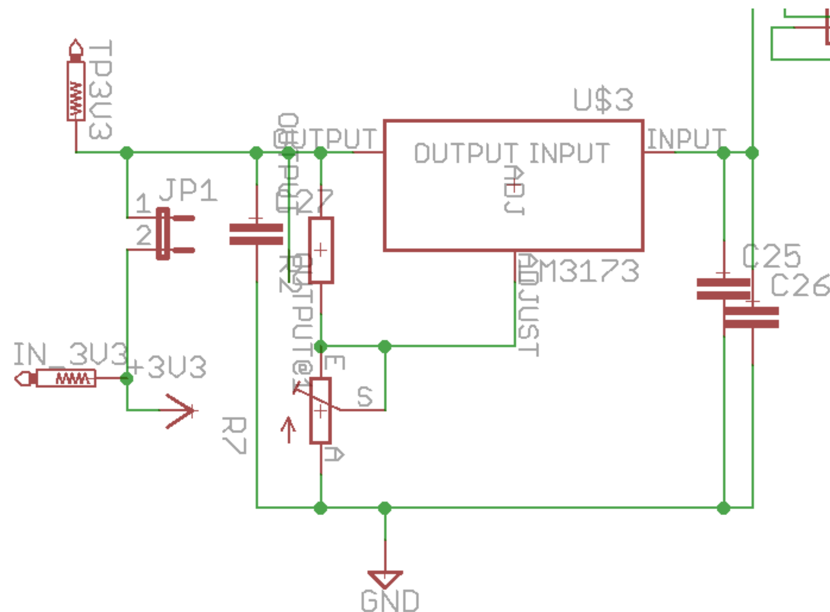


Figure 4.8: The setup of a voltage regulator

The overall PCB requires a voltage around 3.3V and the ADC requires 5V supply, therefore two voltage regulators are used where one feeds 3.3V to the power plane and the other 5V to the ADC. Routing power signal to the ADC required a bit more effort because the power signals shouldn't go through vias and also the trace needs to be slightly thicker for the current.

4.1.3 Bias voltages

In the image sensor, several bias voltages are required and these will be adjusted during the testing phase. To ensure the opportunity for adjustments, a total of 5 potentiometers are included. These are connected directly to power supply and ground, and their output are routed to the socket. To ensure a stable voltage, bypass capacitors of $0.1\mu F$ and $1\mu F$ are placed near the input to cancel out any AC signals.

4.1.4 Bypass capacitors

Bypass capacitor is mentioned earlier and the main reason for including these components in the PCB is because of its ability to eliminate voltage drops by storing electric charges and releases to compensate for voltage drops. The value and size chosen for the bypass capacitor are based on the operating frequency range and application. Since the PCB is for test usage only, ceramic capacitor[1] are used. These are inexpensive and has a large range of values and sizes available at the market. The physical size of the capacitor isn't a critical factor, but in some application needs to be considered due to their equivalent series inductance and series resistance, see figure. The packages used in the project is a mixture of the imperial size 0402 and 0603. The sizes are chosen regardless of the series resistance and series inductance because the resistance and inductance arises only when the operating frequency is above 50MHz, which is irrelevant in this project. The 0402 capacitors are placed around the image sensor chip to minimize the distance to the chip and increase total free area to route other signals due to the small pitch distance between each pins and while 0603 capacitors are used otherwise for simpler assembling.

The values chosen for the bypass capacitor are the common values $1\mu F$ and $0.1\mu F$. The idea behind these chosen values are based on the operating frequency, where smaller values handles high frequencies and larger values handles lower frequencies and high current issues. The image sensor chip doesn't run at specifically high nor low frequencies, and therefore the chosen capacitors has typical values. Since the operating frequency is uncertain and needs to tested after fabrication, two capacitors are used to cover a larger range of frequencies. Bypass capacitors are placed as close as possible to the pins because additional trace lengths contributes in impedance and inductance. See figure 4.9 too see the layout of the bypass capacitors of the image sensor chip.

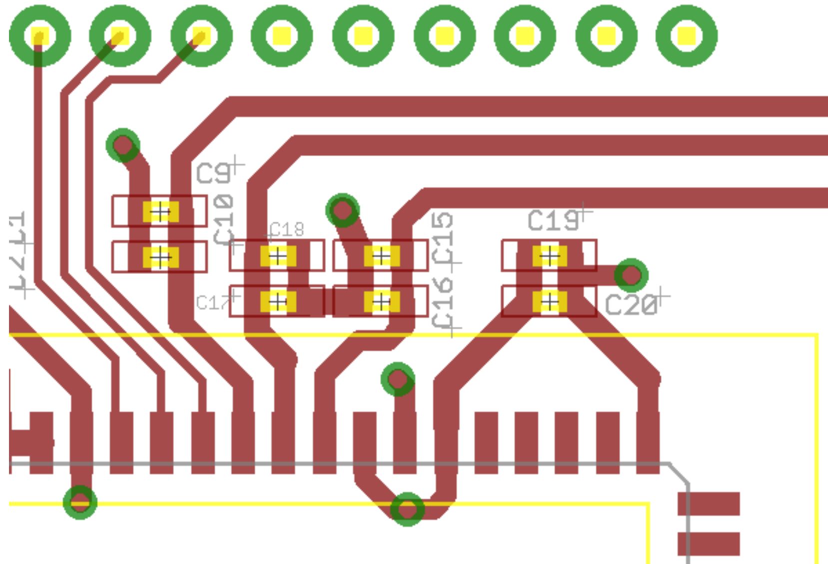


Figure 4.9: Bypass capacitor of size 0402 near the socket

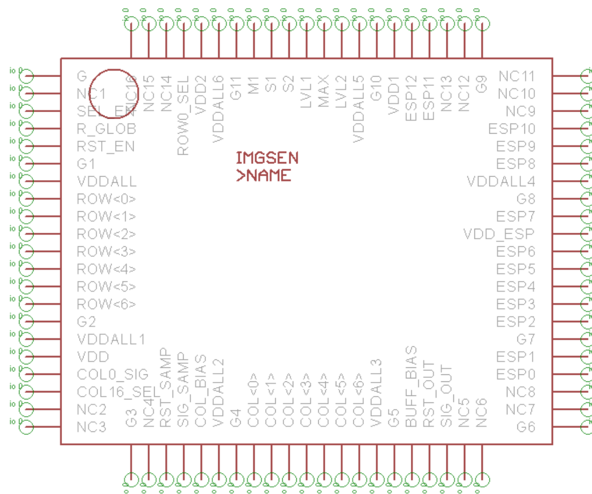


Figure 4.10: The symbol used for the chip

4.1.5 Socket and Board to Board Connectors

The package of the ASIC is the same as the one Wilhelmsen[22] and Hjorteset[7] had and for simplicity their footprint for the ASICs socket is reused. The footprint has 84 contacts with 1.27mm pitch and therefore the surface mount socket used in this project has the same feature. A surface mount chip carrier socket, Multicomp PLCC Socket, with tin-plated contacts is chosen and has slots for easy device extraction. A silkscreen is included and drawn around the pins with the size of 36 ×

[1] Ceramic capacitors has large value range, cheap and suitable for multiple applications

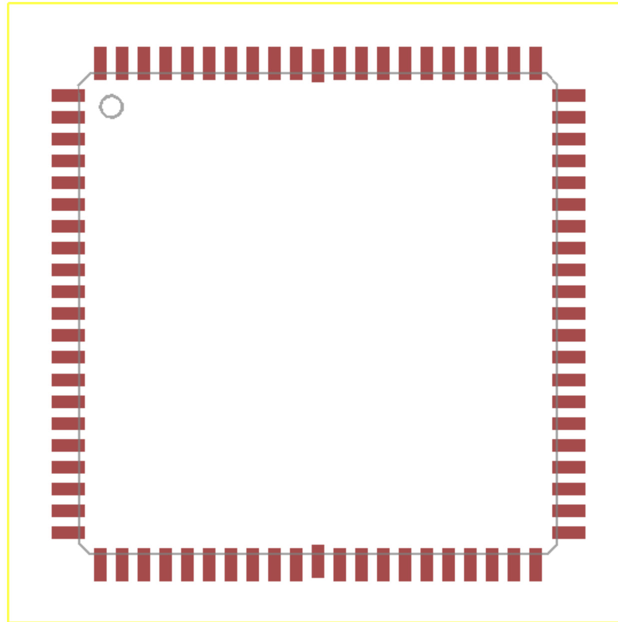


Figure 4.11: Layout of the PLCC socket with silkscreen

36*mm* to specify the physical frame of the socket used, see figure 4.11. The symbol drawn for the chip is shown in figure 4.10.

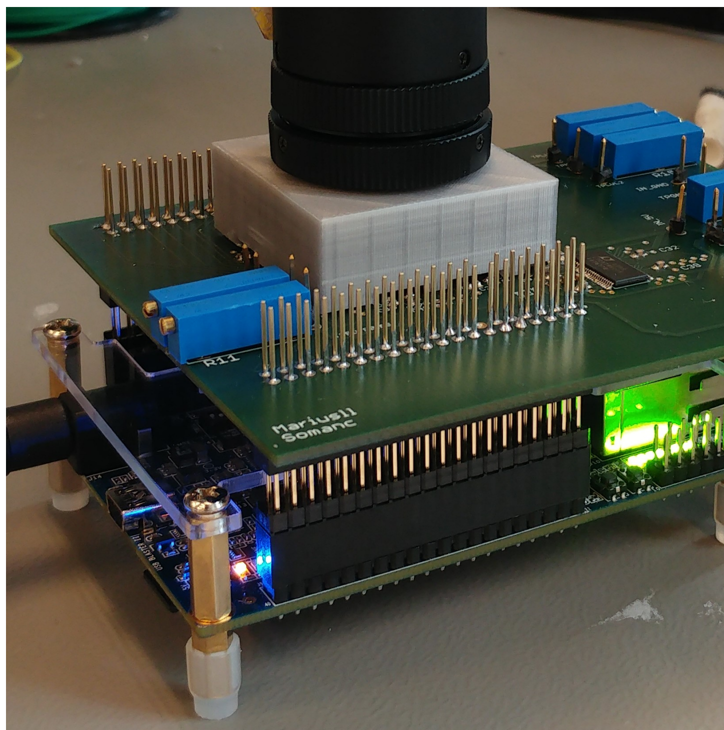


Figure 4.12: PCB with it's connectors

The developer board used for this project has I/O pins available for

connection. It has two 2×20 GPIO[2] expansion headers, each has 36 user pins with a pitch of 2.54mm and 4 pins assigned to ground, 5V and 3.3V. The two headers has a spacing of 60.45mm between. Vias are made in the layout and board-to-board connectors with the same quantities of pins and pitch are used. Each side uses two of these connectors to built up some height due to a single one doesn't have the required body height for connecting to the developer board because of its protection glass on the top, see figure 4.12.

4.1.6 Lens and Lens Socket

Monofocal, Manual Iris	
Model	T0412FICS
Mount	CS Mount
Focal Length	4mm
MAX Aperture Range	1:1.2
Focus	0.2m - ∞

Table 4.2: Lens Specification [12]

This project borrowed a lens[12] from Phillip Haflinger during test phase, as the previous master students did, and reuse the lens socket design, originally made by Lukasz Farian and modified by Wilhelmsen[22], which is calibrated to fit the lens and its focus point precisely. Some modifications is done for the socket to fit the designed PCB by taking the SMT components placement into consideration. Instead of having a solid frame, indents were made at the bottom. The width, length and height of the sockets "legs" are measured and cut with the program Solidworks and 3D printed, see Appendix A for socket details. See figure 4.13. Details of the lens is listed in table 4.2

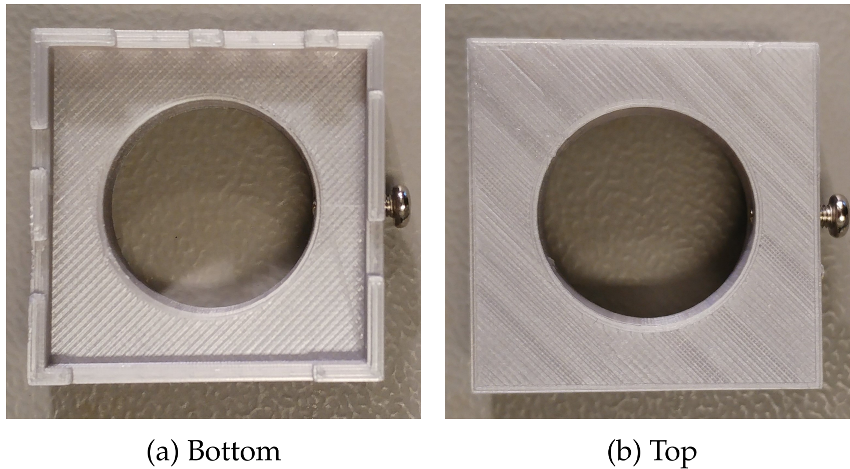
4.2 Assembling and Testing

The assembling process is done several times and tested to verify its functions. 3 PCB are made in total, but only the second one is used.

4.2.1 Components

The 0402 capacitors are small and when trying to place them on the PCB it seems as if the ends could nearly touch the pads. The first PCB is made without using the 0402 capacitors to ensure that they are soldered on properly to the pads. The first PCB didn't pass the test due to the chip

[2]General Purposes input/output



(a) Bottom (b) Top

Figure 4.13: Lenssocket

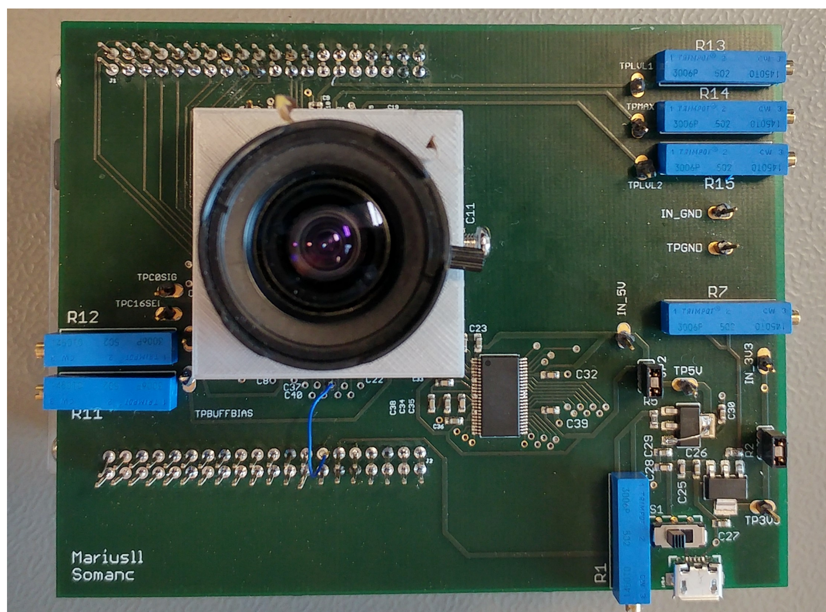


Figure 4.14: The second PCB

socket was bended during the reflow soldering process and more than half of the pins didn't had proper connection to the PCB pads. Instead of trying to solder them on manually, a second PCB is made. The second assembling used the 0402 capacitors because the lens socket was design with it's height taken into consideration and for the socket to sit properly on the PCB, the height in the capacitors need to be the same as 0402, which is 0.5mm. The silkscreen of the capacitors are not included and this caused wrong placement problems. These were removed with desoldering braid and soldered on again with solder lead manually. This process was time consuming and could have been avoided by included the silkscreen.

4.2.2 ADC

The ADC has no shorted pins and is connected properly to the pads of the first assembled PCB. The second PCB encountered problems. Some of the I/O pins of the ADC was shorted and this was confirmed by measuring the resistance between each pins. Excess solder paste was removed, in the same manner as with the capacitor, to create an open circuit. This procedure of removing excess solder paste might burn the ADC in the process and a new PCB was made to resolve the problem if the ADC isn't functional. The pins of the third assembled PCB is tested and is verified. Adjusting ADC SENSE pin is shown to be applicable during the test process, but unfortunately it's connected directly to the power supply. In the datasheet it's noted that an input range between $\pm 1.6V$ or $\pm 1V$ will limit the differential input and provide a specified input range, for example an input voltage of 1V with provide a differential input range of $\pm 1V$ and this is more preferable for this project since the output range of the image sensor is around 0.8V. This is to fully utilize the quantization bits of the ADC and to receive a finer representation of the differences between reset and signal. To support this adjustment, a potentiometer is required.

4.2.3 Power Circuit

The voltage regulator used in this design has a voltage drop of 0.7V and is proved insufficient for the ADC. The ADC requires a total of 5V and that's what the USB and the FPGA feeds. Along with the voltage drop, the output of the voltage regulator is 4.3V. The power could instead connected directly to the FPGA 5V pin and discard the voltage regulator. The input and output of the voltage regulator is therefore shorted on the second PCB with a tin cord, see figure 4.15. The third PCB doesn't use the voltage regulator for the ADC, and the power is connected directly with a tin cord, see figure 4.16.

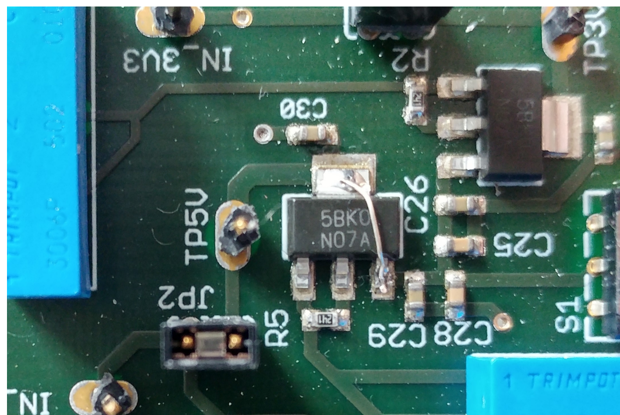


Figure 4.15: The shorted voltage regulator on the second PCB

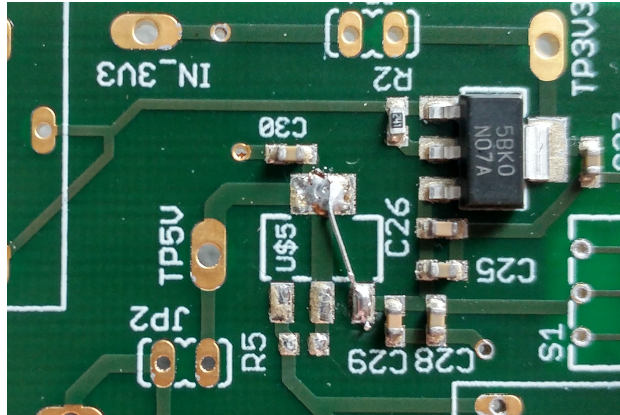
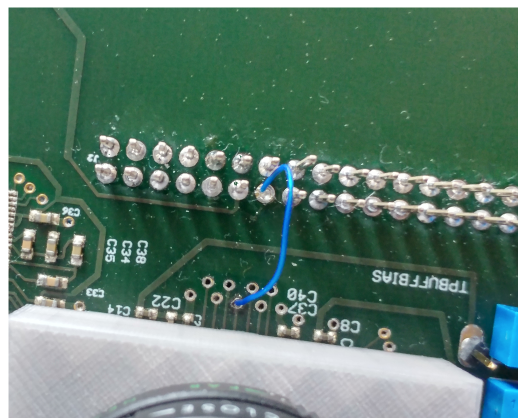
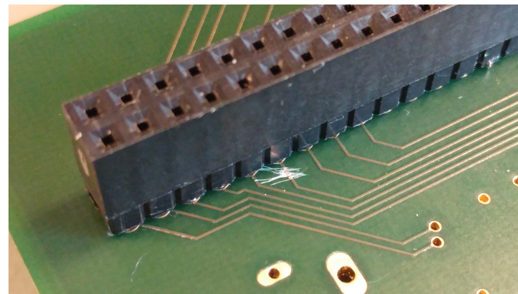


Figure 4.16: No voltage regulator used in the third PCB

4.2.4 Routing



(a) Top of the PCB with the copper tin



(b) Back of the PCB

Figure 4.17: Corrected route on the PCB

Before connecting the PCB to the FPGA, a mistake in routing is detected. Despite receiving documents of the I/O pins on the FPGA, column addressing bit 3 signal was routed to a reserved 3.3V pin. To correct this, the copper on the PCB needed to be manually scraped off. This signal is instead routed to pin 15 with a thin cord and solder tin, see

figures 4.17. This method should be sufficient because it's a digital signal and the path won't disturb the signal much. The melted solder filled the through hole completely, causing problems when trying to connect to the I/O pins. The second PCB has a thin cord without having its end cut off and is used to connect to the header by removing the original header pin.

4.2.5 Tx control

The potentiometers used for adjusting the voltage for the transistor Tx are connected directly to the 3.3V power plane and ground, but to further expand the voltage range, these should be connected directly to the 5V power instead. This suggestion is made by studying and testing the chip and considered the possibilities of voltage drop due to the parasitic resistance and capacitance in the chip.

Chapter 5

Test, Verification and Data Analysis

This chapter will provide the data extracted from the image sensor IC. The method for extraction, environment and results will be discussed.

5.1 Test Assembling

The developer board used, as mentioned earlier, in this project is Alteras low-end developer board FPGA DE0-Nano-SoC[1] kit. The kit contains Cyclone V SoC, combining FPGA and Hard Processor System(HPS), with ARM Cortex-A9 embedded cores. This section will give a brief explanation of how the program works, further details of the test system is not described and one must refer to Lillestøls paper[11].

5.1.1 FPGA

The FPGA is the image sensor control system and runs in VHDL code. This connects the C-program and PCB together by using HPS. The FPGA controls and sends the signals the image sensor chip requires in order to function, row, column, M1, Tx control and sample signals, and ensures that they are synchronized. The timing and functions are tested by simulating the code with a test file in ModelSim. The ADC is also controlled by the VHDL and the code connects the extracted value to the correct pixel address. The data is then stored in the On Chip Memory for further read out. This memory is designed strictly for writing from the ADC control system and toggles HPS to read when done to prevent overwriting or reading old frames together with the new. The VHDL code, besides the default values, is capable of receiving commands from the user interface through the C-program and enables different run mode along with different timing for exposure and Tx.

[1]System on Chip

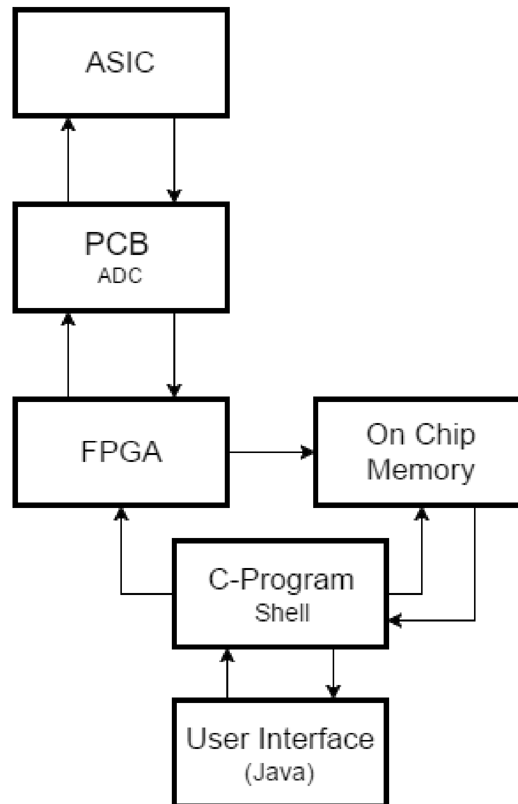


Figure 5.1: Simplified overview of the test system

5.1.2 C-Program

The embedded C-program is the link between the user interface and FPGA. This is done via Ethernet and the PIO system. The program receives and sends data to the user and acts as a shell, waiting for command when initialized. It also sends and receives data from the FPGA. The C-program can access the on chip memory, creates a frame with the stored data and sends it to the user.

5.1.3 GUI

The Graphical User Interface (GUI) is designed in Java and is only for simplicity use of controlling the timing in the image sensor. It consists of a terminal allowing the user to enter inputs for configuration. The program provides live frame streaming, histogram, a slider function to control the gain used during preview of the image, capture button to save the image in tiff format and subtract dark frame by capturing a photo in complete darkness and use it to remove FPN.

5.1.4 Connection Analysis

To verify everything, the PCB and FPGA are connected before inserting the chip, see Appendix C, D and E for images of the chip. All pin connections are measured and analysed with an oscilloscope. Power circuit are measured again to ensure the test system is flawless. The test pins are measured with an oscilloscope.

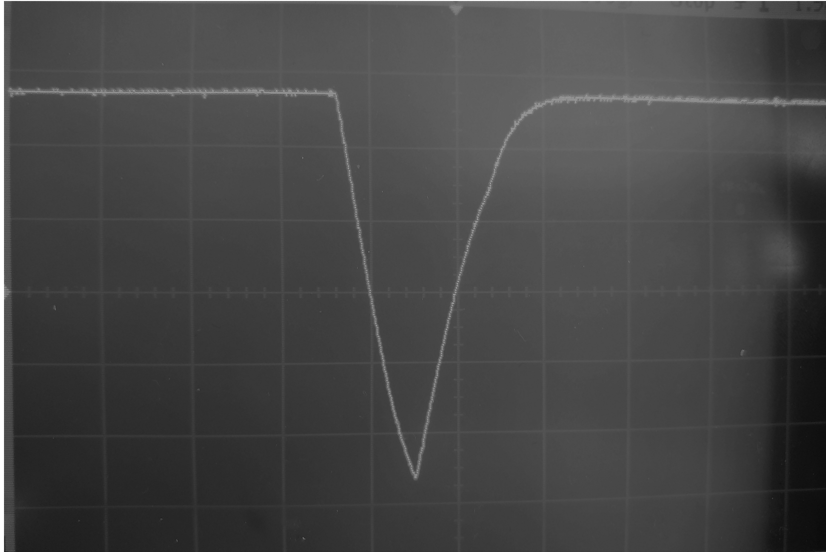


Figure 5.2: Column address number 16

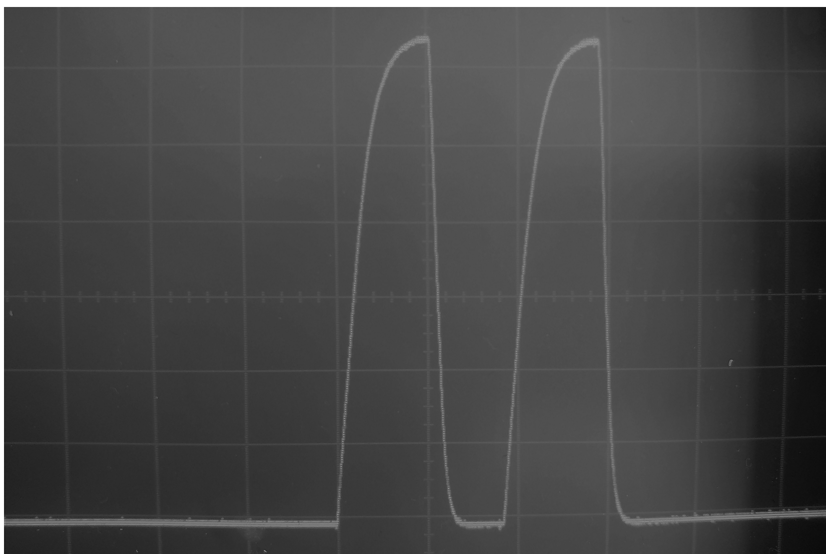


Figure 5.3: Row address number 0

The figure 5.2 and 5.3 are the measured value from the test pins connected directly to the image sensor chip. These signal are only used to verify they operate correctly according to the VHDL code.

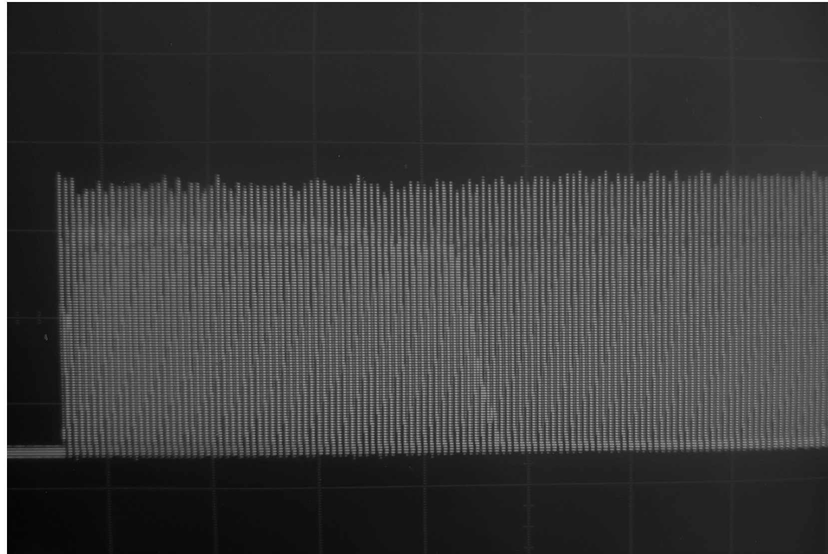


Figure 5.4: Output signal from the first column of pixels

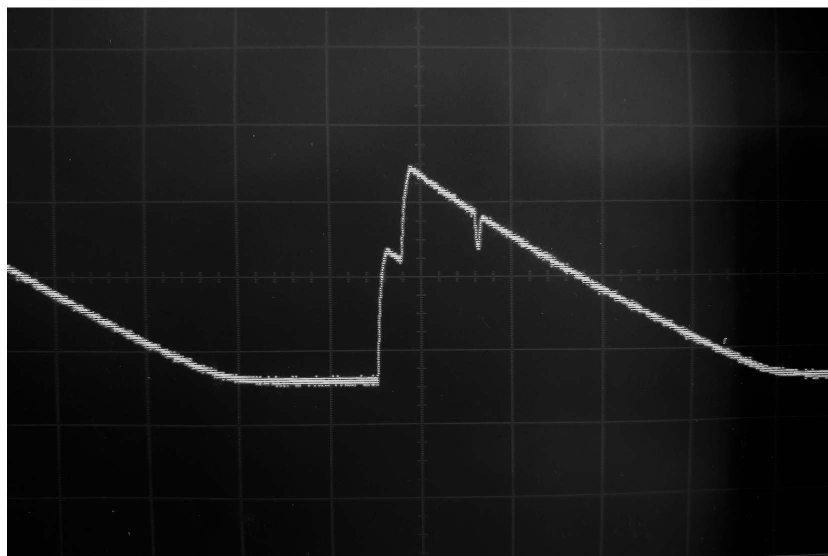


Figure 5.5: Output signal from the first column of pixel, zoomed in.

The figure 5.4 and 5.5 is the measured value from the first column of the pixel array. The close up figure shows the signal drop is sampled first and the reset is sampled afterwards. The measured values done in this phase has a slow rise and fall time and this is the cause of the probes used. The probes available in the lab has a capacitance of $15pF$ and $100M\Omega$.

5.2 Data Analysis

This section will provide the data extracted from the image sensor chip with the test system. Calculation and plot is done with the program

MATLAB. The values presented below is typically given in voltages versus exposure time. The voltage level are calculated by finding how fine the voltage quantization step is by using the specifications stated for the ADC. The equation 5.1 is used.

$$V = \frac{1.6V}{2^{14}} = 97.65\mu V \tag{5.1}$$

Since the exposure time parameter given by the user through the GUI is simply a multiplier for the actual exposure time, this need to be calculated correctly for the plot and equation 5.2 is used.

$$Exposuretime = 82 * 4096 * 20ns * input \tag{5.2}$$

5.2.1 Linearity

Measuring the linearity requires a uniform light. This is done by using a simple table lamp and cover the lens with a piece of paper to diffuse the light. Several images are captured by slowly increasing the exposure time. The captured images are then imported into MATLAB for further data extraction and only 10×10 pixels are used for calculating the average value and plotted in the figure 5.6.

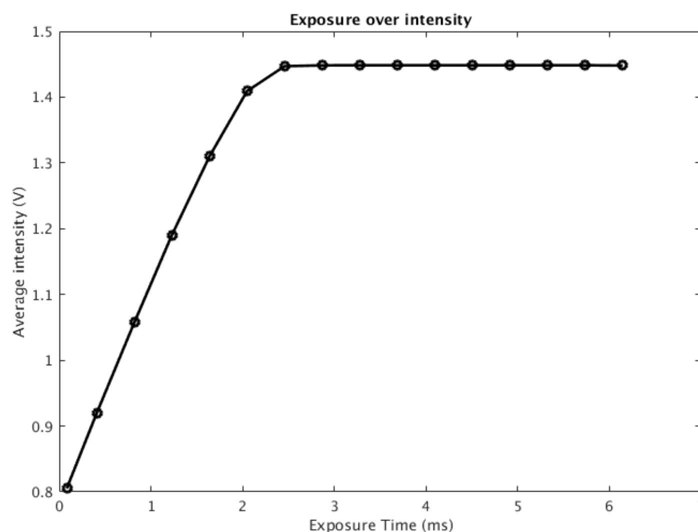


Figure 5.6: The linearity of the image sensor

The linearity of the image sensor is from 805mV to 1.4V with an exposure time between 0.8ms - 2.048ms[2] and the maximum output is 1.48V. The chip has an output range of 0.67V and the linear range of 0.595V. The linearity can be limited by the FD-node because of it's low capacitance

[2]this is with the the illumination source, table lamp

compared to the photodiode and saturates much faster. This assumption is made accordingly to the extracted value from Cadence and given it's a correct approximation.

5.2.1.1 Tx

The pixel has a transfer transistor, Tx, and finding it's ability to perform a complete transfer from the photodiode to the FD-node is necessary. The images used are taken in the same environment as the images used in the linearity plot, but instead of a varying exposure time, the pulse width of the Tx is swept. The exposure time is set to be constant and the time of the Tx pulse begins with a minimum pulse width and increases slowly. This method is capable of showing how much of charges Tx is capable of transferring based on the time and how long the pulse width needs to be in order to perform a complete charge transfer.

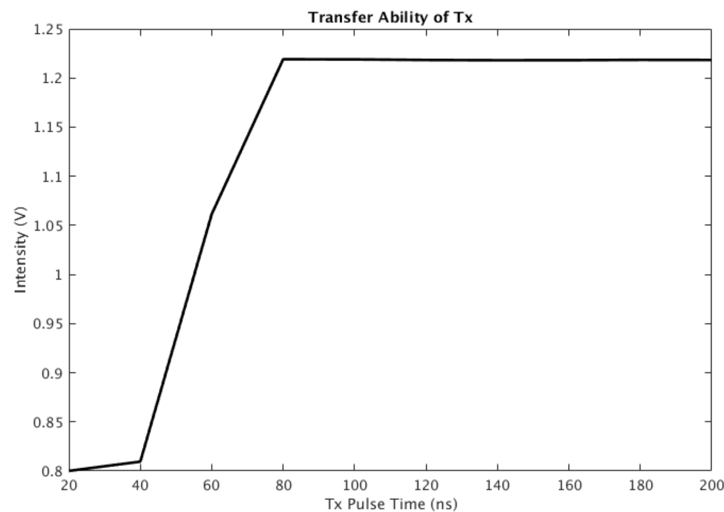


Figure 5.7: Transfer capability of Tx transistor

According to the plot, figure 5.7, the intensity settles quite early. This indicates that the Tx transistor has the ability to do a complete transfer within 80ns. The data extracted from these images is only an approximation and should be done by connecting test pins directly to the FD-node and photodiode to obtain a more accurate information. The plot may not be indicating a complete charge transfer, because this is usually difficult to obtain when using a regular photodiode and transistor, but instead how much charges the FD-node is capable of holding before reaching saturation and not all charges accumulated in the photodiode are fully transferred. By connecting the photodiode and the FD-node to test pins, this assumption can be analyzed.

5.2.2 Stray Light

Upon using a CMOS image sensor with a global shutter, measuring parasitic light sensitivity is necessary to find how much of this light contributes to the output signal. The test is taken with the transistor M1 on to prevent the photodiode from accumulating charges and keeping the Tx transistor off to analyze whether the FD-node collects any charges. The lens is completely open during the test with constant light illumination, a working lamp with tripod is used, diffused with a pieces of paper and the exposure time is swept by slowly increasing it.

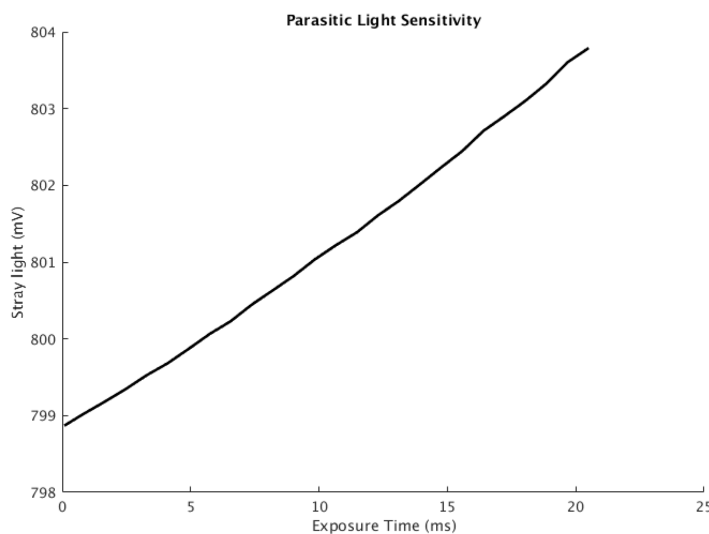
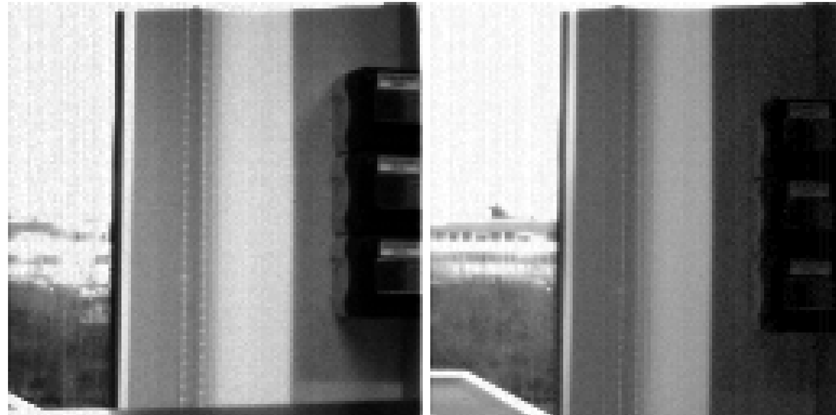


Figure 5.8: Parasitic light

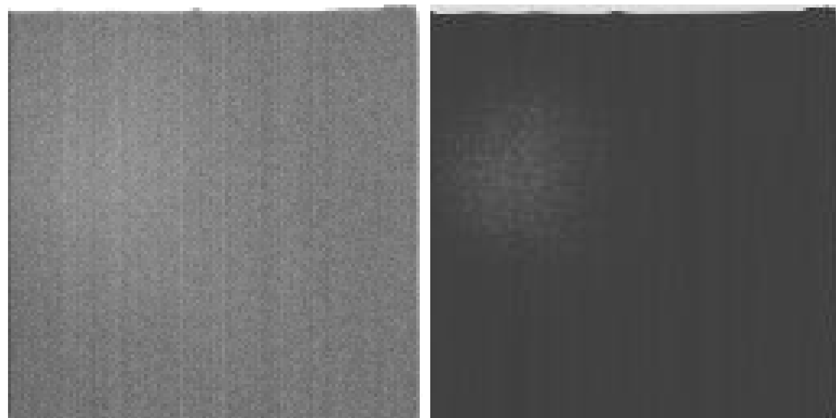
The plot in figure 5.8 shows the parasitic light detected. The lowest value plotted at an exposure time of 0.082ms is 799mV and highest value with an exposure time of 20.5ms is 804mV. Compared to the linearity plot, during the time from 0.082ms to 2.46ms the parasitic light contributes a total of $\frac{0.7993V - 0.7989V}{1.447V - 0.805V} \times 100 = 0.062\%$. The percentage calculated is simply an approximation and considering it's quite low, it's assumed that the parasitic light has a low contribution to the resulting image. This is the effect given by shielding the pixel array with MET4 and this contribution would've been higher without the shield.

Despite the parasitic light contribution is generally low, partial of the image still suffers from undesired light. This is apparent at the top and the right side of an image, see figures 5.9 and 5.10. The streak is caused by the top row of pixels being exposed to incoming light from the side due to the lack of dummy structure of metals under MET4 and hence no shielding wall is present. Studying the image even further, top right and in the middle is shielded properly and is noticeable due to the darker pixels around these areas. This is where the Tx control circuit, power routing



(a) Scene with an exposure time of 150ms (b) Scene with an exposure time of 100ms

Figure 5.9: Various image with undesired light



(a) Image taken with a long exposure time of 50ms(Edited) (b) Image taken with an exposure time of 10ms(Edited)

Figure 5.10: Images taken with the lens covered

path and M1 buffer are placed and these functions as a shield for the pixels because they consist of more metal layers and prevents unwanted light from infiltrating, see layout on figure 5.11 and 5.12.

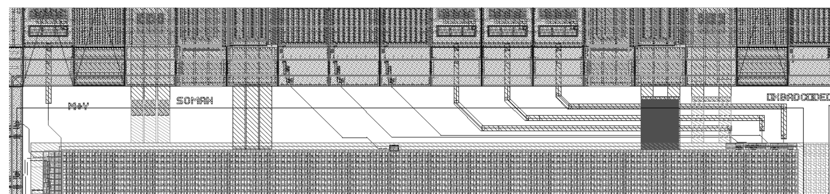


Figure 5.11: Top of the pixel array with M1 and Tx control circuit

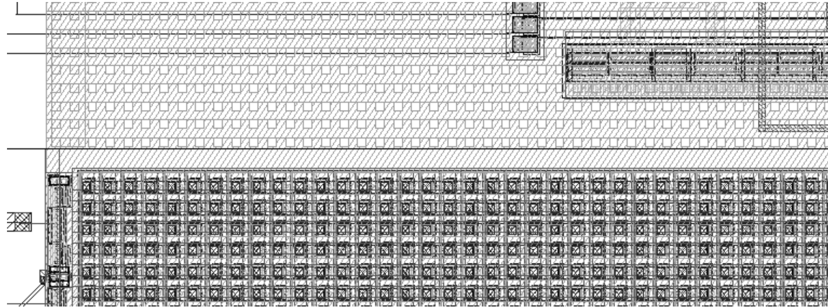


Figure 5.12: Rotated image of the right side of the pixel array

5.2.3 Temporal Noise

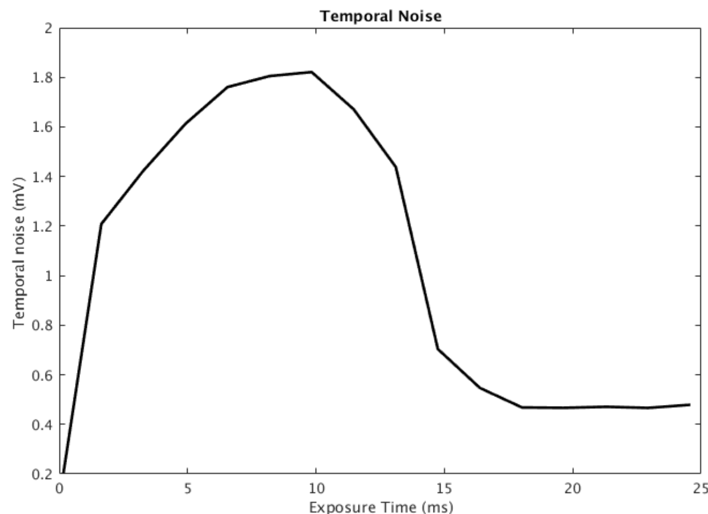


Figure 5.13: Plot of temporal noise over exposure time

In the literature review, temporal noise is mention. As described, this noise varies within time. To map this type of noise is difficult compared to FPN. For simplicity a scene with no movements and constant light illumination is captured twice with the exact same exposure time right after each other. For this plot, several images are taken by varying the exposure time. The two frames, taken at the same exposure time, are then subtracted to remove FPN noise and standard deviation is calculated with 100×100 pixels. As expected, temporal noise is relatively high during short exposure time and dominates, but decreases at longer exposure times. This is due the information acquired dominates the temporal noise.

5.2.4 FPN

FPN is calculated by finding the mean value along the row or column and take standard deviation of these values. The images used for this

calculation is the same images taken for linearity plot. The plot of both vertical and horizontal FPN is shown in figure 5.14.

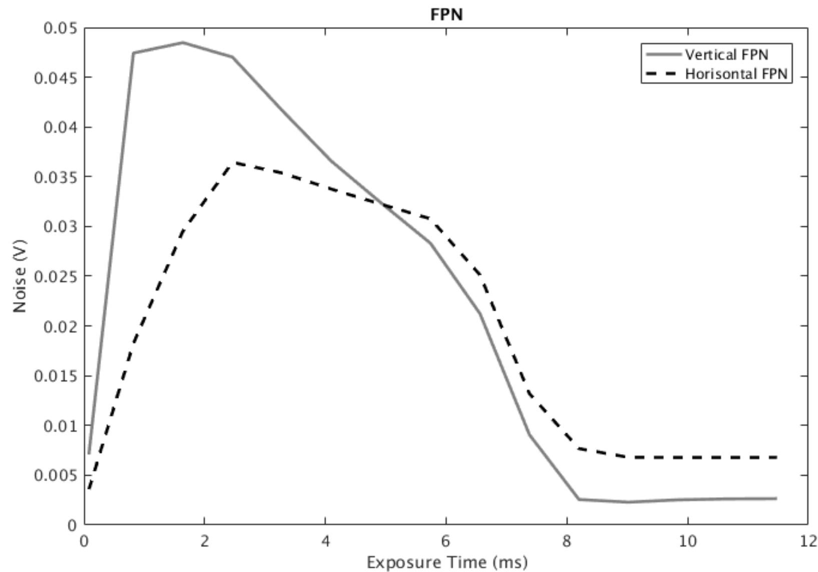
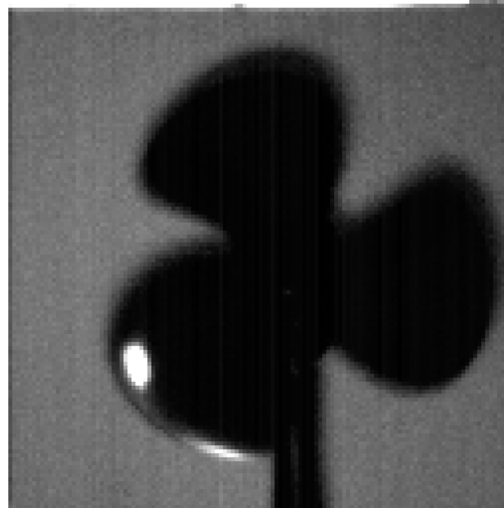


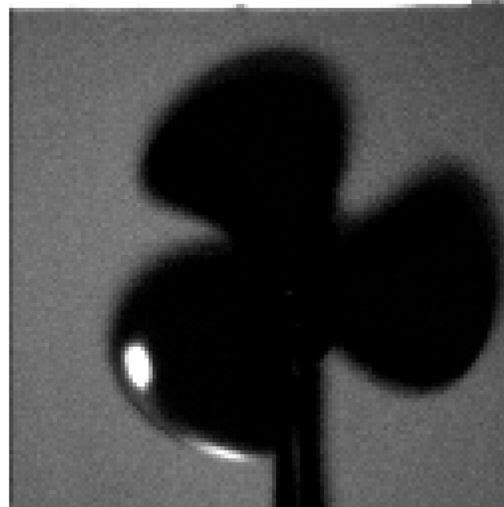
Figure 5.14: Fixed Pattern Noise

As expected, the horizontal FPN is much lower than vertical FPN due to the CDS technique used during sampling. If a DDS was included, the vertical FPN can be reduced as well, assuming most of it's noise contribution is due to the pMOS threshold offset in the CDS. It should be noted that the plot of the FPN is affected by the temporal noise as well, hence their graph are quite similar. To map the FPN noise as accurate as possible, multiple images should have be taken with the same exposure time and the average value for each row or column, for vertical or horizontal FPN respectively, should be taken with all the available images. This method will suppress the temporal noise and the graph would be more accurate.

FPN can be removed with digital processing by subtracting a dark image, which means an image captured with the lens completely closed and taken with the exact same exposure time. The images with and without FPN are shown in figure 5.15. The subtraction operation is done in MATLAB. The vertical streaks are apparent in the image with FPN, while the other one these streaks are suppressed. On the image sensor chip, the first column of the pixels output node is connected directly to a test pin and out for measurement. This connection causes a black vertical streak on the first column and is most noticeable in the images to the left.



(a) With FPN



(b) Wihtout FPN

Figure 5.15: Images with and without FPN (Edited)

5.3 Functionality Analysis

In this section, the method of testing of global shutter and HDR scheme will be described and results are presented.

5.3.1 Global Shutter

To confirm the image sensor has an electronic global shutter and it's functional, a simple rotating fan was used and a working light is present to brighten up the scene. The revolutions per minute is unknown, but the fan ran with the lowest speed. The first image taken, figure 5.16, is with a Samsung Galaxy S7 Edge cellphone. The cellphone uses an

Figure 5.16: Image taken with a rolling shutter (Device: Samsung)

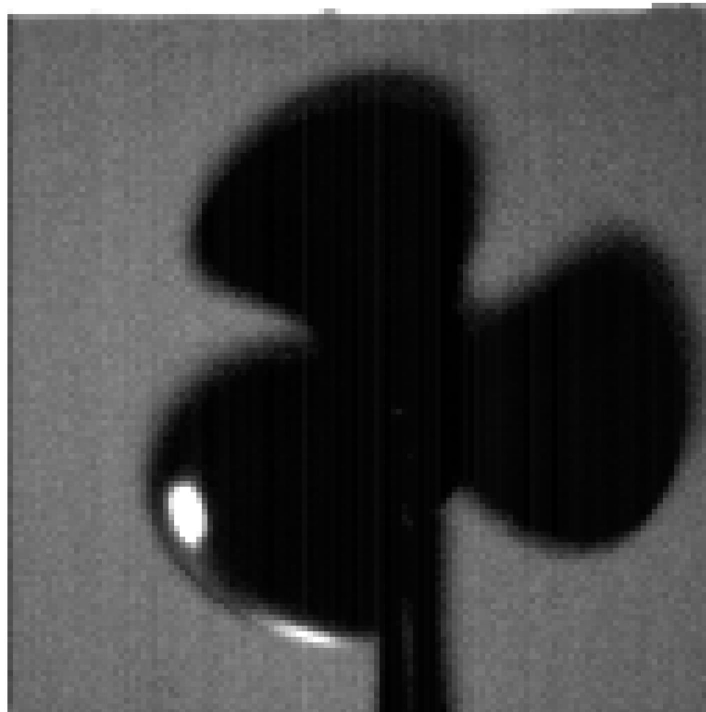


Figure 5.17: Image taken with the image sensor chip

image sensor with rolling shutter and the shutter speed is set at 1/700s to obtain motion artifacts. The chip is then set to have the same shutter time. The light sensitivity of the chip is weaker than Samsungs and, therefore the image taken with a rolling shutter is fairly bright and looks even saturated, whilst the image captured with the chip is much darker, see figure 5.16 and 5.17. As expected, the image of the rotating fan taken with a rolling shutter contains motion artifacts. The blades are bended

compared to the image taken with a global shutter. This confirm that the global shutter mechanism is functional and capable of capturing objects in motion without any artifacts.

5.3.2 High Dynamic Range

High Dynamic Range is one of main focuses of the image sensor chip. The main scheme used during the test phase is skimming. Various skimming methods were done and these will be presented and discussed in this section. The most optimal method will be used for further data extraction, analysis and compared to an image taken with no HDR scheme.

5.3.2.1 HDR Schemes

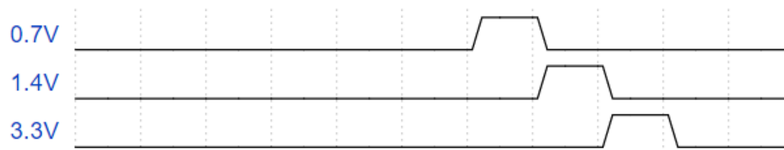


Figure 5.18: Timing diagram for the gate voltage levels for Tx

The Tx control diagram plotted in figure 5.18 is the first HDR scheme implemented. The method consist of pulsing Tx with an increasing voltage value for charge transfer and the pulse width of each is identical. The resulting image did not show any improvement due to the reset was never pulsed to reset the FD-node. The time between each pulsing Tx is minimal and the three pulses behaves as a large single pulse.

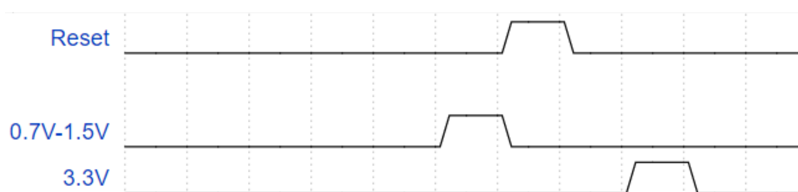


Figure 5.19: Timing diagram for the gate voltage levels for Tx

The second implementation done is to feed the Tx gate a voltage between 0.7V-1.5V and reset the FD-node before starting the charge transfer. This method is an improvement of the previous scheme. The saturates areas in a high contrast scene is reduced and has a lower value compared to a scene captured with no skimming. The problem this scheme encountered is that not only did the saturated areas been muted, but also the details. This scheme was incapable of acquiring any more information than a regular image with no HDR scheme. This means, the

scheme is capable of preventing the FD-node from going into saturation, but it's not capable of differentiating a saturated level from the possible non-saturated signal. This could be the combination of a non-multiple pulse used for skimming and the time between the reset and final charge transfer is too short, leaving the photodiode with insufficient time to accumulate more charges before the final pulse, see the timing diagram in figure 5.19.

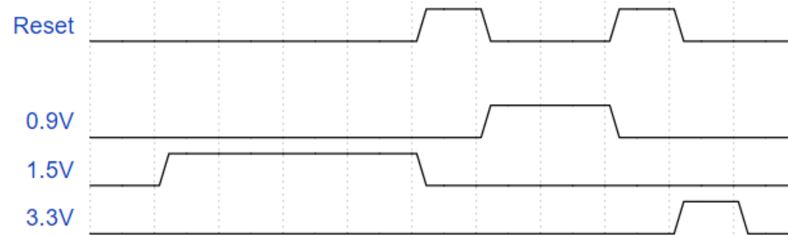
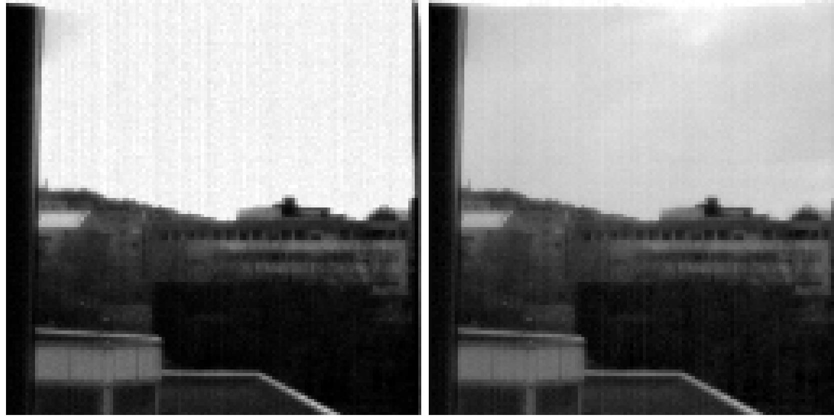


Figure 5.20: Timing diagram for the gate voltage levels for Tx

The final one, and the one the project opted for, is to pulse Tx with a medium high gate voltage, then with a small one and full transfer at the end with different pulse width, see figure 5.20. The idea of this method is to first remove saturated signals by transferring them over to the FD-node with a mid-high voltage with 4× the Tx minimum pulse width. After transferring these charges over, the node is reset to remove the transferred charges. After that, Tx receives a voltage level slightly above its threshold voltage only to remove the most saturated signals with a pulse width of 2× the Tx minimum pulse width. This allows the photodiode to accumulate just enough charges to differentiate the level from the highly saturated one. The charges that transferred with the low voltage level is removed once again with the reset. Lastly, the maximum voltage is applied for full charge transfer with the minimum pulse width. This is the signal read out from the pixel unit.

This scheme slows down the signal from entering the saturated region by removing excesses of charges. The second pulse along with its pulse width time allows the photodiode to accumulated just enough charges to differentiate the over saturated parts from the level which is slightly below it. By doing this, information between the two level is preserved and not lost. Figures 5.21 shows a scene captured with an exposure time of 30ms. The image 5.21a is captured without skimming and the sky is clearly saturated. The contrast level in this image is much higher and the shades of the clouds is nearly undetectable. By using the skimming method, image 5.21b, the contrast is decreased and some details of the shades are visible.

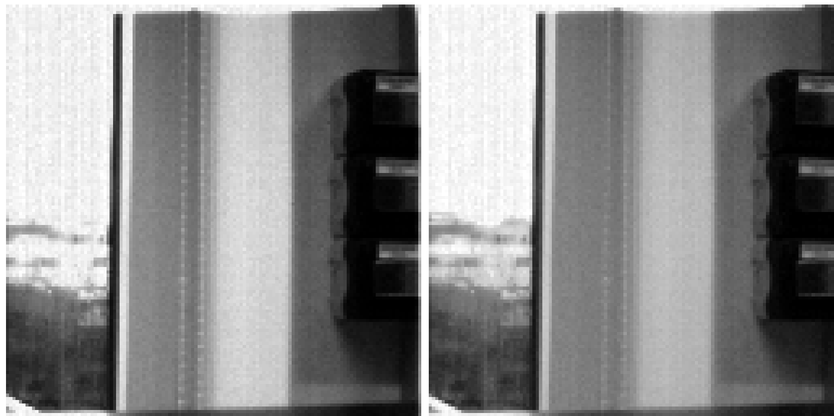
A second test done is by capturing a scene consisting of indoor button and outdoor scenery and both is taken with en exposure time of 150ms. The image taken with no skimming method, figure 5.22a, the buildings



(a) Scene captured with no skimming (b) Scene captured with skimming

Figure 5.21: Scene captured with global shutter with exposure time 2.45ms

outside are saturated and details are lost. By using the skimming method, the details on the building are preserved without losing any detail of the buttons in the wall, see figure 5.22b.

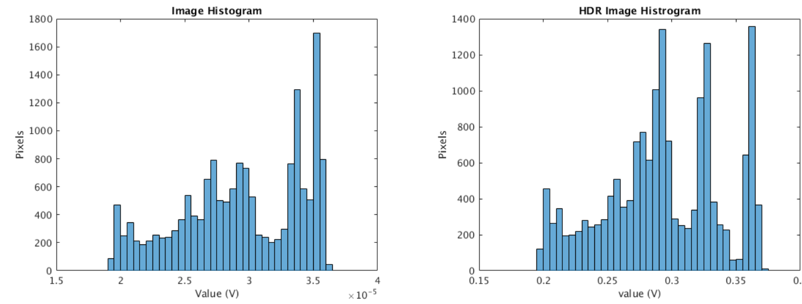


(a) Scene captured with no skimming (b) Scene captured with skimming

Figure 5.22: Scene captured with global shutter with exposure time 12ms

The histogram of the two images, figures 5.22, are plotted in figure 5.23. The histogram differentiates the two images captured with and without skimming by plotting quantities of pixels with their respectively value. The image taken with no skimming contains more pixels within the right part of range, which is the brighter scenes. The histogram of the image taken with skimming has distributed the pixels along the range and more pixels are found in the middle instead. The GUI used for capturing these images has a live stream with histogram of the image. The Tx voltage are adjusted accordingly by studying the histogram from the live stream to

find the optimal pixel distribution along the histogram, and the voltage values are 0.9V and 1.5V.



(a) Histogram of the original image

(b) Histrogram of the image with skimming

Figure 5.23: Histogram of the images

5.3.2.2 Linearity of method with HDR

The linearity of the image sensor with HDR scheme is plotted together with the one without.

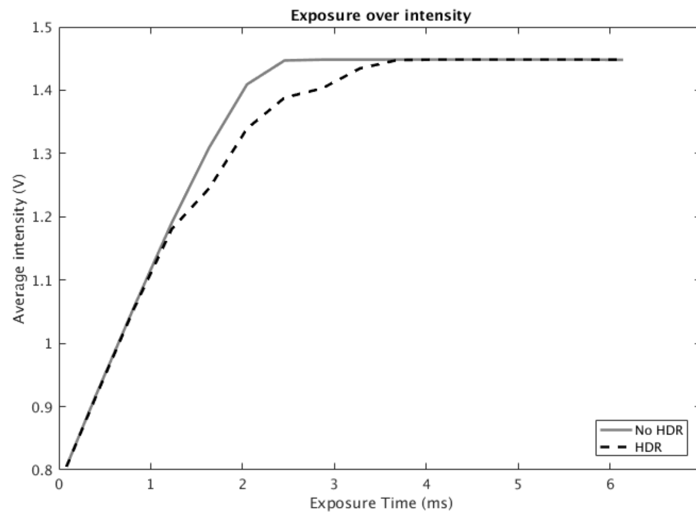


Figure 5.24: Linearity plot of images without skimming and one with

According to the plot, the HDR scheme increases the optical dynamic range by extending the exposure time range before the signal saturates. The skimming level is clearly visible in the plot as well, any value between 1.2-1.3V is skimmed with the mid level gate voltage while the values around 1.4V is skimmed with the low level gate voltage.

5.4 Future Work

In this section, possible configurations and improvements are discussed.

5.4.1 Pixel and pixel array

The pixel fill factor can be increased and charge transfer can be optimized by using a pinned photodiode or a costume made photodiode as Wilhelmsen[22] and Hjorteset [7] did in their project. The architecture can be modified to be a 6T-pixel for enabling true CDS scheme. The power supply connected to the FD-node and photodiode should be adjustable. This can be used to find the actual threshold voltage of each Tx and this information is useful for determining the gate voltage required for pulsing it.

The layout design can be improve by adding active dummy pixels around the core pixel. This is used to mirror the structure around the pixel array and creates a symmetry for the outermost pixels. This prevents any differences caused by the neighboring circuits. Optical black pixels should be included to measure dark current and use the information for noise reduction in the digital domain. Dummy structures or dummy pixels should frame the entire core to prevent undesired incoming light from the side. The guard ring used around the pixel array can be connected up to the power supply instead. This allows any free unwanted charges to be pulled up and out of the substrate. The FD-node can further be expanded with metal path or increase the size of the source follower to obtain a higher FWC.

If possible, an array of microlens should be implemented on the top to obtain an effective fill factor.

5.4.2 Tx

The output voltage versus gate voltage of the Tx should be plotted to study it's ability for charge transfer. This information can be used for determining the appropriate gate voltage level for HDR scheme.

5.4.3 CDS

nMOS transistor is used as a MOS capacitor in the CDS design. An nMOS needs a minimum of 700mV to create a channel between source and drain and this channel defines the capacitance of the MOS capacitor because the capacitance of the MOS capacitor varies based on the gate voltage. To establish a solid capacitance, the voltage needs to be higher than the threshold voltage. Since pMOS operates oppositely of an nMOS, which means it requires a voltage lower than the threshold voltage and it's approximately 2.6V, one can assume it might be a more preferable

option to use a pMOS. The output signal from the pixel is certainly not higher than 1.5V and with a range between 0V-1.5V the pMOS is capable is establishing a stable capacitance. If applicable, DDS circuit should be included to reduce vertical FPN.

The layout of the chip has swapped the sample signals. It didn't cause a major problem, but would've been nice to resolve it in the layout before taping out.

5.4.4 Decoders

Including additional buffers should be considered for the decoders. Currently, each decoder has a single buffer for each incoming addressing signal and routing from these buffers to the logic blocks is far and the path forked out is asymmetric. This may cause uneven delay. If DDS is implemented, a select signal for column decoder should be included as well for full control.

5.4.5 Analysis

Horizontal and vertical FPN should be recalculated by using more images with the same exposure time in order to reduce the noise contribution from temporal noise. Pixel wise FPN should be calculated with the acquired horizontal and vertical FPN by finding the total FPN noise with multiple images and subtract it with the horizontal and vertical FPN, see equation 5.3

$$FPN_{pixel} = \sqrt{FPN_{total}^2 - FPN_V^2 - FPN_H^2} \quad (5.3)$$

A platform allowing measuring and analysing conversion gain, quantum efficiency and image lag should be made.

5.4.5.1 Rolling Shutter

A configuration for running the image sensor chip with a rolling shutter mode should be implemented. The images taken with a global shutter and rolling shutter can then be compared to and the results can be discussed. Running with their own respectively operation can provide more information of the image sensor chip.

5.4.5.2 HDR

The skimming scheme should be tested with various voltage level and exposure time. New techniques should be applied for further HDR scheme study. Multiple frames with different exposure time should be taken and combined in the digital domain to obtain a HDR image.

5.4.5.3 PCB

The PCB should be redesigned and fabricated. The voltage regulator for the ADC can be discarded and re-routing the column addressing bit 3 to a correct pin should be done. The potentiometer can be switched out with controllable ones through the FPGA to obtain an accurate voltage biasing. The voltage biasing should have a voltage range of 0V-5V for further study of the Tx transistor. The ADC should receive a SENSE input voltage of 1V or connect it to ground to achieve a finer quantization step regarding differential voltages.

Chapter 6

Conclusion

An image sensor has been designed, fabricated and tested. The electronic global shutter with HDR support is realized. A camera system is created for capturing images, enabling live stream and configurations are available. The constructed system allows the user to gain a full control of the image sensor, understand how it functions and how the configurations affects the results.

The global shutter, compared to a rolling shutter, is capable of capturing moving objects without artifact and has a relatively decent shutter efficiency as the result of the shielding designed in the layout. The overall light sensitivity is low, but its the sacrifice done to achieve a good shutter efficiency, reducing the parasitic light sensitivity and preserving information stored in the FD-node. A non-true CDS is used resulting in a less efficient reduction in horizontal FPN. No DDS is implemented causing high vertical FPN. The frames taken are affected by incoming light from the side because of the lack of dummy structures of the metal layers.

HDR skimming scheme is capable of extending the optical dynamic range. This method successfully skimmed the FD-node with two specific values. The values are set to remove, first, nearly half of the accumulated charges and then a small fraction of charges. With the time between the first pulse and the last charge transfer, the photodiode is capable of accumulating enough charges to differentiate a brightness level from dark scene and over saturated scene. The results showed a better distribution in the histogram and the resulting images contains more details in the saturated areas.

The output resolution is low and could be improved if the SENSE input of the ADC was adjusted to a suitable range for the image sensor chip. This will provide a finer representation and fully utilize the available 14 bit. The current linearity can further be expanded by following the recommend future work for improvement.

The global shutter mechanism results were as expected, except for the stray light detected at the top of the pixel array. The HDR scheme performed much better than what was planned and gave relatively good

results.

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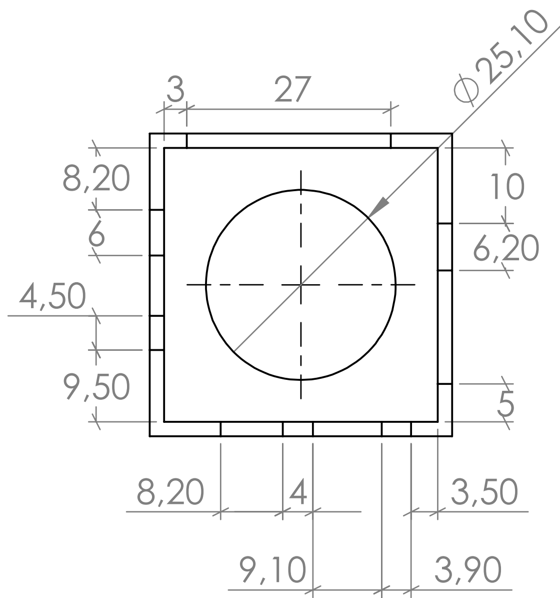
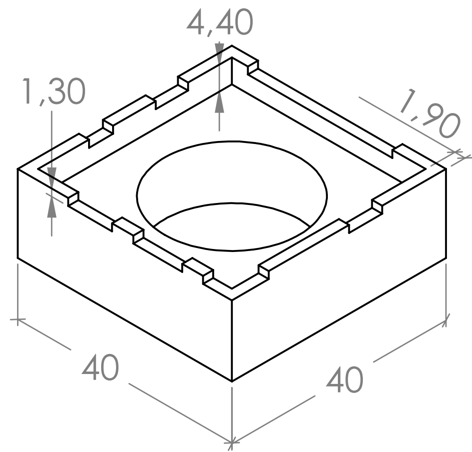
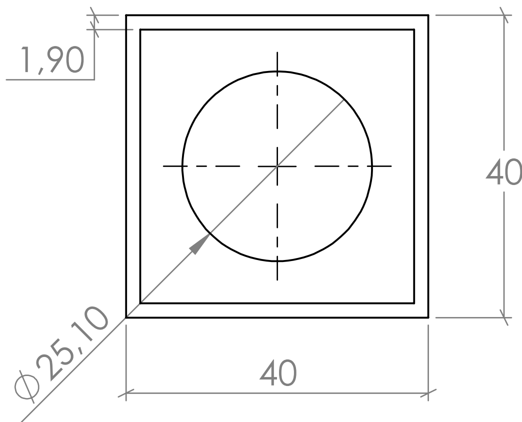
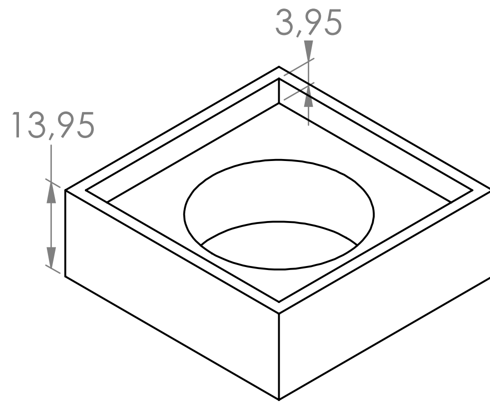
Appendix A

Lens Socket









SURFACE FINISH: TOLERANCES: LINEAR: ANGULAR:	DIMENSIONS: MILIMETERS	SCALE: 1:1	REVISION: 1.1

	NAME	SIGNATURE	DATE
DRAWN	Bård-Kristian Krohg		08.03.17
CHK'D			
APPV'D			
MFG			
Q.A			

TITLE: **Linse socket, med og uten ben**

MATERIAL: PLA

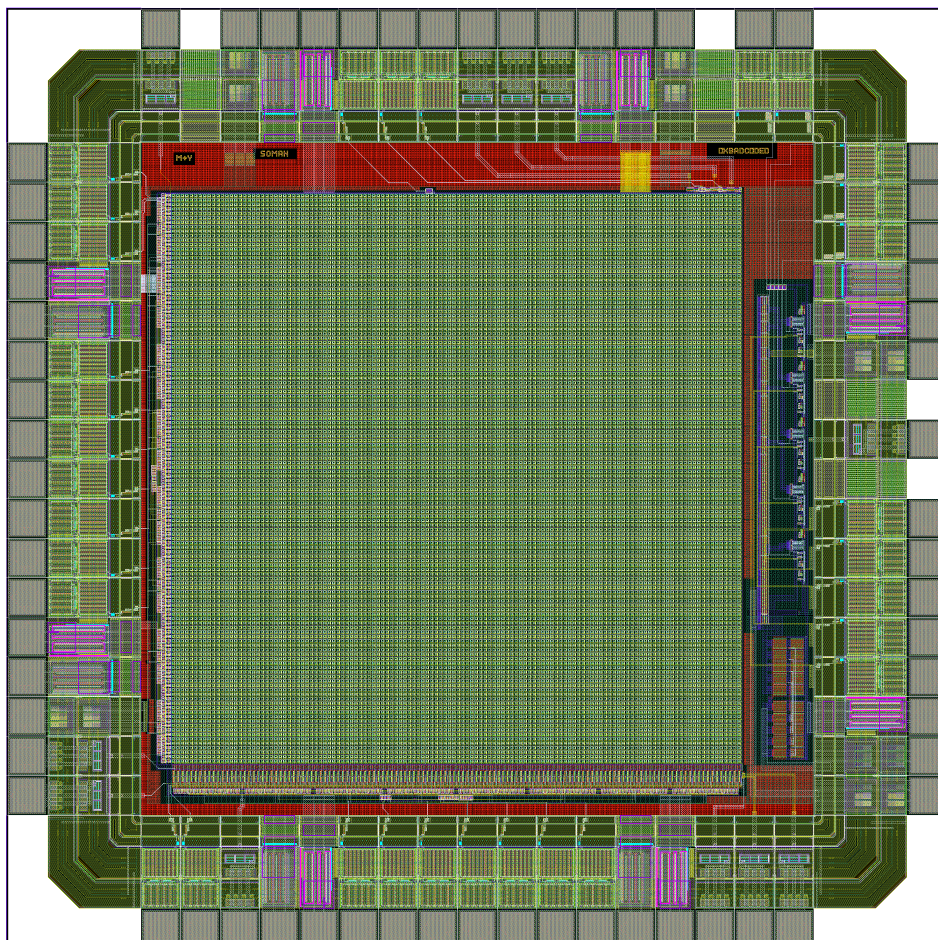
DWG NO. 1

A4

SHEET 1 OF 1

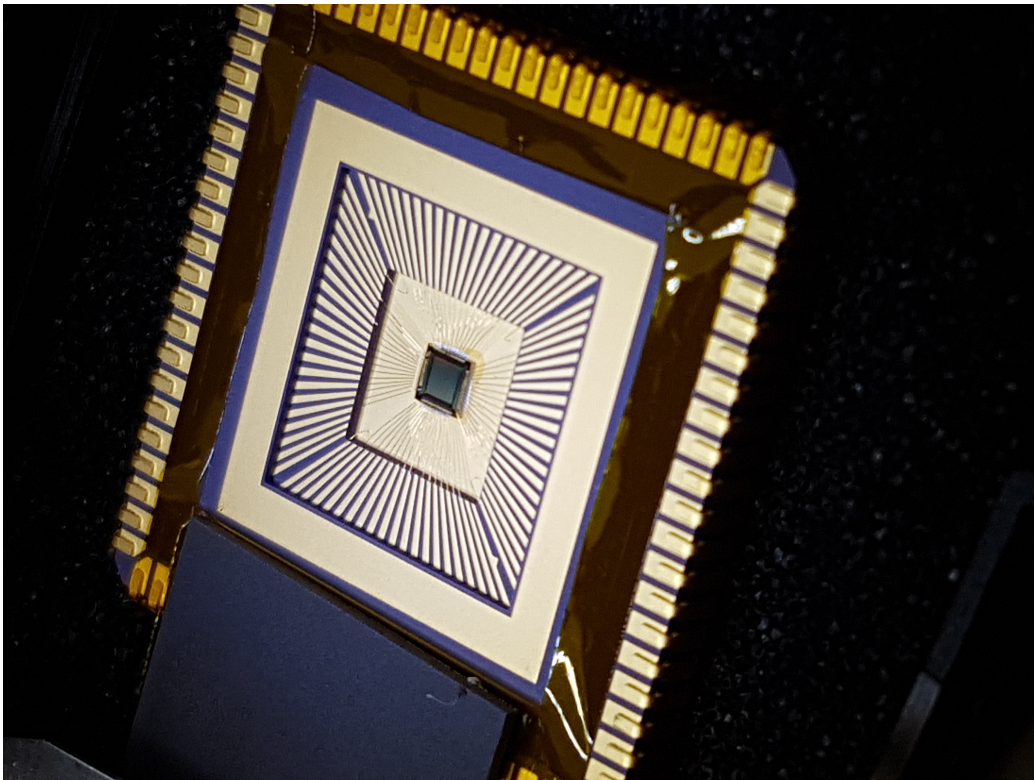
Appendix B

Layout of The Image Sensor



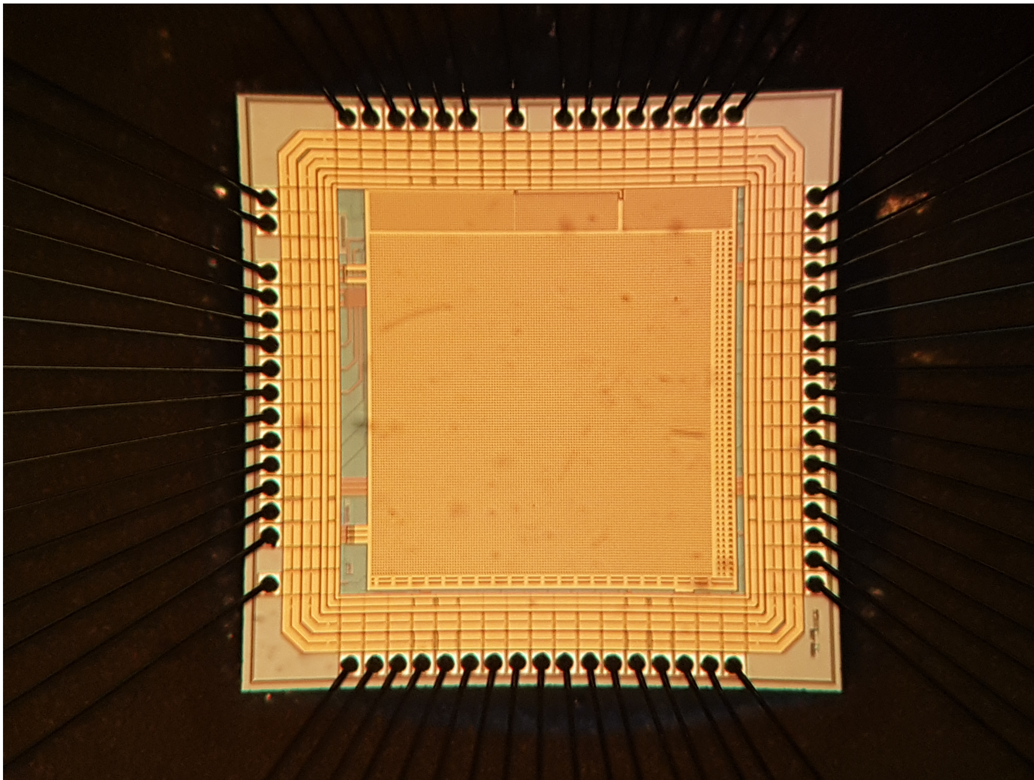
Appendix C

Chip



Appendix D

Chip though Microscope



Appendix E

Chip though Microscope (Close Ups)