UNIVERSITY OF OSLO
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Millimeter wave interconnect and slow wave transmission lines in CMOS

Master thesis

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Abstract

When heading into the millimeter wave frequency band, even wires on CMOS exhibit transmission line effects, this thesis therefore presents models, simulation and measurements for transmission lines on CMOS. The main goal is slow wave miniaturization, and models are explored for both a traditional CPW line above a silicon substrate and slow wave lines, emphasis is given on analytical over empirical formulations where loss is modeled by conductor skin effect, and conductive and dielectric polarization caused by the silicon substrate. Full 3D Electromagnetic simulation is used as a comparison, and to model more complex structures like a digitally tuned slow wave line. Models and simulations are compared to fabricated lines on a commercial CMOS process, where deembedding using the LL method is described in short. A new comb slow wave grounded coplanar waveguide (comb-S-GCPW) is presented, with an effective dielectric constant of 140 leading to a size reduction of $83\,\%$ compared to a traditional CPW. Applications of the published line is explored, with emphasis on filters.

Preface

This thesis is submitted as part of the degree Master of Science in Microelectronics, Electronics and Computer Technology at the Department of Physics, Faculty of Mathematics and Natural Sciences, University of Oslo (UiO). Most of the project was carried out at the Nanoelectronics group at the department of informatics (IFI), and parts at the Norwegian Defence Research Establishment (FFI). Work on this thesis began January 2012 and ended June 2013, the thesis is a "long" thesis giving 60 credits (one year).

I want to thank my supervisors Svein-Erik Hamran, Tor Sverre Lande (Bassen) and Kristian Gjertsen Kjelgård for accepting me as their student, your constant encouragement and scientific insight has been invaluable in the work towards this thesis. Especially Kristian for assistance with both software and measurements setup and not least for co-authoring a paper. In addition, for assistance with the chip and general guidance, the help of Olav Stanly Kyrvestad is acknowledged. Sverre Brovoll, Øyvind Aardal and others at FFI are thanked for interesting lunch breaks, stimulating discussions and making me quickly feel at home. Fellow master student at IFI are thanked for both a scientific and humorous lab environment.

In the end I would express appreciation to the entire open source community, tools/packages like LaTeX, amsmath, hyperref, booktabs, siunitx, latexmk, Inkscape, gerbv, Python, matplotlib, numpy, scikit-rf, mpmath and matrix2latex has been invaluable. In particular Geoffrey Poore for his work on PythonTeX and for accommodating my usage.

My whole hearted love and gratitude is extended to Ine, especially for your understanding when the hours ran late. I would also like to thank the rest of my family for their support, although you thought studying small wires sounded strange.

Contents

Nomenclature

"Explicit is better than implicit"

Z_{in}	Input impedance.	Ω
Z_0	Characteristic impedance.	Ω
ε	Dielectric constant, $\varepsilon_r\varepsilon_0$.	$\mathrm{F/m}$
ε_0	Physical constant, vacuum dielectric constant $\varepsilon_0 = 8.85 \times 10^{-12}$.	$\mathrm{F/m}$
ε_r	Material constant, relative dielectric constant.	
ε_{eff}	Wave constant, effective dielectric constant.	
l	Length.	m
l_{slot}	Length slot, see figure 3.13.	m
l_{finger}	Length finger, see figure 7.1.	m
W	Width.	m
W_s	Width signal, see figure 3.3.	m
W_g	Width ground, see figure 3.3.	m
W_{finger}	Width finger, see figure 7.1.	m
W_{slot}	Width slot, see figure 3.13.	m
h	Height (double subscript) and thickness (single subscript).	m
h_s	Thickness of signal, see figure 3.3.	m
h_g	Thickness of ground, see figure 3.3.	m
h_{slot}	Thickness of slot, see figure 7.1.	m
$h_{s\text{slot}}$	Distance between signal and slot, see figure 3.3.	m
h_{SiO_2}	Thickness of insulating (assumed silicond dioxide SiO_2) layer.	m
h_{Si}	Thickness of substrate (assumed silicon Si).	m

G	Gap	m
G_{sg}	Gap signal ground, see figure 3.3.	m
G_{vv}	Gap via, see figure 5.6.	m
V_c	Controll voltage, see figure 5.6.	V
d	Period.	m
G_{slot}	Gap slot, see figure 3.13.	m
$G_{\text{finger}x}$	Gap finger x, see figure 7.1.	m
$G_{\text{finger}y}$	Gap finger y, see figure 7.1.	m
σ_{Si}	Substrate conductivity (assumed silicon, Si).	$/\Omega\text{m}$
σ_{Cu}	Metal conductivity (assumed copper, Cu).	$/\Omega\text{m}$
δ	Skin depth.	m

CMOS	Complementary Metal-Oxide-Semiconductor
CPW	Coplanar Waveguide
CS	Coplanar Stripline
DRC	Design Rule Check
EM	ElectroMagnetic
FEM	Finite Element Method
FFI	Norwegian Defence Research Establishment
GSCPW	Grounded Slow wave Coplanar Waveguide
MoM	Method of moments
MS	Microstrip
NANO	Nanoelectronics
PCB	Printed Circuit Board
PEEC	Partial Element Equivalent Circuit
RF	Radio Frequency
SCPW	Slow wave Coplanar Waveguide
SMS	Slow wave Microstrip

SPI	Serial Peripheral Interface
TE	Transverse Electro
TEM	Transverse Electromagnetic
TM	Transverse Magnetic
VCO	Voltage Controlled Oscillator

Chapter 1

Introduction

With digital chips being everywhere, in computers, mobiles, cars and even washing machines, their underlying technology is rapidly progressing, leading to high performance and low mass production costs. This technology is called CMOS, and is based on the second most abounded resource on the planet, silicon. New applications are now emerging, with buzzwords like connected devices and internet of things. It is apparent that wireless communication between chips are becoming increasingly common.

Today, this communication usually relies on WLAN operating in the $2\,\mathrm{GHz}$ to $5\,\mathrm{GHz}$ frequency range. With the release of the unlicensed $57\,\mathrm{GHz}$ to $64\,\mathrm{GHz}$ band, data rates of over $3\,\mathrm{Gbit/s}$ is possible, leading to streaming high definition video. In addition, new applications emerge. Like short range radars, with uses in medical applications and cars. The $60\,\mathrm{GHz}$ frequency range is unlicensed mainly due to its high atmospheric attenuation (due to O_2 absorption), making it unsuitable for broadcasting or cellular applications. But this makes it ideal for short range (indoor) usage. For short range radar this means less interference from neighbouring radar systems, and in WLAN applications it leads to higher security and frequency reuse.

Handling signals at these frequencies is far from trivial, but commercial Complementary Metal-Oxide-Semiconductor (CMOS) process already provide transistors with an intrinsic frequency well over $100\,\mathrm{GHz}$. As a first baby step towards small, cheap and high performance radars and data links, we will in this thesis discuss *wires* on CMOS. As it turns out, in addition to the rather mundane usage of transporting a signal from point A to point B, which we will refer to as interconnect, wires carrying high frequency signals can perform useful functions, like delay lines, filters, matching networks, power combiners and many others.

Transmission lines has the potential to replace lumped capacitors and inductors, whose usage is prevalent at low frequencies. As all parasitics are naturally included in the modeling of a transmission line, they are easier to work with than lumped components which always has an upper frequency limit to their use. Transmission lines can however be rather large, leading to high cost. Novel techniques for reducing the physical length exists, these "slow wave" transmission lines can give substantial area saving when designing millimeter wave components. And will be one of the main objectives of this thesis.

Though mass production of CMOS devices is cheap, prototyping is very time consuming and costly. The chips fabricated for this thesis, used 4 months from final drawing to a physical device. This stresses the importance of a good model, where designs can be tested and optimized before fabrication. Trial and error is not an option for CMOS design.

Models can either be obtained from a mathematical description, where different levels of simplifications can lead to accurate; or less accurate models. If measurements are already available, empirical equations can be developed, leading to models that fit well with reality. These are however difficult to generalize to other geometries and manufacturers. A more accurate approach is the use of full wave simulation. Where the model is divided into smaller pieces and Maxwell's equations are solved for each block. This is however challenging and time consuming. The user must be proficient in both numerical techniques and ElectroMagnetic (EM) theory. Solution time and memory requirements scale quickly with growing problem size, so full system simulation is usually impossible. For reasonable simulation times, a number of simplifications must be made and we will discuss these in detail. Mathematical models should therefore be utilized for increased parameter insight and quick performance evaluation. While simulation provides an accurate check, before fabrication.

Transmission line theory is not a new field, in particular for Printed Circuit Board (PCB) designs, models, simulations and measurements are plentiful. In addition CMOS tool chains already extract wire models that are empirically determined by the manufacturer, leading to a high degree of accuracy. These models are however created for low frequency digital applications, leading to poor accuracy at millimeter wave frequencies ($30\,\mathrm{GHz}$ to $300\,\mathrm{GHz}$).

To support the high transistor density of modern CMOS processes, a staggering number of metal layers are available. The lowest layers are for local interconnect and are therefore made thin, while the higher layers are thicker and wider for reduced loss. For digital designs; this allows dense signal routing, and enables efficient power and clock distribution. The number of layers is only expected to increase in the future, paving the way for novel uses. In this thesis, usage of the 9 metal layers available in the utilized $90\,\mathrm{nm}$ process will be explored for low loss interconnect and slow wave lines, mainly by using the lower layers as shielding against the lossy semiconducting substrate.

Thesis goals are therefore as follows

- Investigate on-chip transmission lines with particular focus on slow wave miniaturization.
- Provide design guidelines and design on-chip slow wave transmission lines.
- Provide analytical models, that does not rely on measurements for empirical fitting.
- Compare models to EM simulation and on-chip measurements.
- Investigate potensial applications with focus on filters.

The thesis is divided in two parts, the first being a theoretical foundation and a literature review. Chapter 2 covers some fundamental wave and transmission line theory, in addition to advanced aspects of loss. The next chapter explore the literature of on chip CMOS transmission lines, highlighting some challenges and exploring slow wave realizations. Modeling is done in chapter 4, where mathematical models are presented in increasing complexity.

The second part is of a more practical aspects and cover simulation in chapter 5 and measurements in chapter 6. A new comb slow wave transmission line has been submitted for publication and is presented in chapter 7, with literature review, modeling, simulation and measurements. The thesis is ended with some simple applications, reviewed in chapter 8 and the conclusion is drawn in chapter 9.

Part I

Theoretical foundation

Chapter 2

Transmission lines

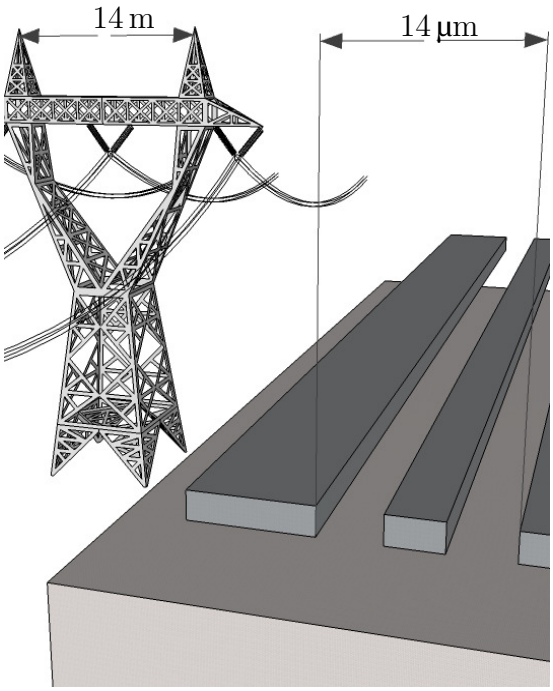


Figure 2.1: On chip and power transmission line.

This chapter explores basic transmission line theory, most of the material presented here, apply equally well on electrical power transmission lines and transmission lines fabricated on CMOS; see the illustration above. We will highlight the major transmission line effect, namely phase shift, loss and reflection. Except for section 2.3, where we do a deeper dive into loss, this is fairly textbook material.

2.1 A voltage wave

As in [LB09], we define a voltage wave

$$V(x,t) = \sin(\omega t - \beta x) \tag{2.1}$$
$$\text{where} \quad \beta = \frac{2\pi}{\lambda}$$
$$\text{and} \quad \omega = 2\pi f.$$

Where the wavelength λ is given in m and f is the frequency in Hz. We also introduce a phase velocity v_p with a period $T = 1/f$,

$$v_p = \frac{\lambda}{T} = \frac{\omega}{\beta}. \tag{2.2}$$

Assuming a wave in a uniform, non magnetic material, with a relative dielectric constant ε_r, we can also express the phase velocity in terms of the speed of light

$$v_p = c/\sqrt{\varepsilon}_r \tag{2.3}$$

Using (2.2) and (2.3), it is trivial to related, frequency, wavelength, phase velocity and derived quantities like angular wavenumber and angular frequency.

Equation (2.1) is a function of both time and space, to illustrate this we plot two periods of the wave at two different locations. Assuming the wave moves in an environment with $\varepsilon_r \approx 12$ (which corresponds to silicon) we get the waves in figure 2.2, which shows a $60\,\mathrm{GHz}$ signal at two locations $dx = 361\,\mu\mathrm{m}$ apart.

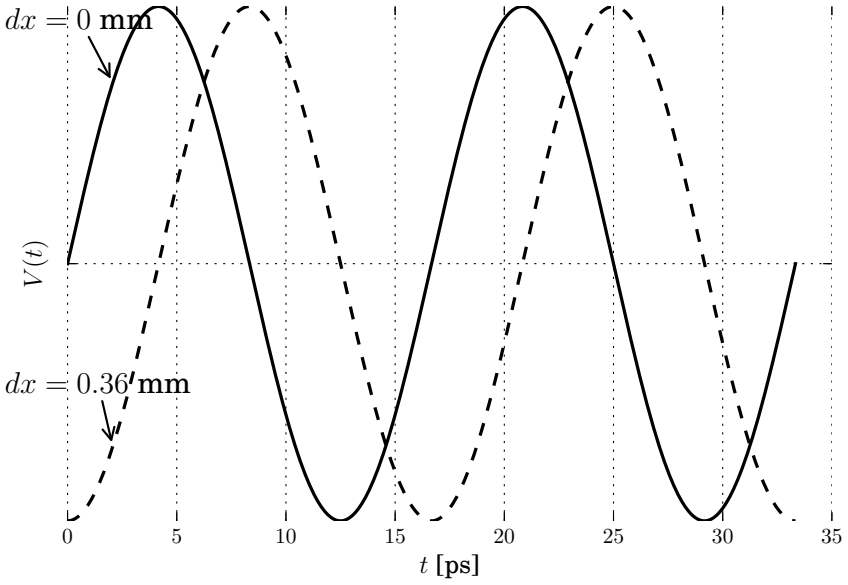


Figure 2.2: A sine wave on a lossless and infinite transmission line, measured at two locations.

The discussion above assumes the wave moves entirely in a single homogeneous environment being completely described by the relative dielectric constant ε_r. To generalize the discussion we introduce the effective dielectric constant ε_{eff}, which generalizes the discussion to a wider range of problems by including geometry of the transmission line and allows the wave to move in multiple materials. This replaces ε_r, which is a *material* constant, while ε_{eff} can be viewed as a *wave* constant. The reasoning and implications of this will be discussed later in section 2.3.2, for now it can simply be viewed as a scaling for the waves velocity.

Going back to figure 2.2, we can observe that if the distance dx is very small, then the phase shift is negligible and can be ignored. A common rule of thumb is that any distance shorter than

$\lambda/10$ can ignore transmission line effects. It is therefore useful to express the wavelength as

$$\lambda = \frac{v_p}{f} = \frac{c}{\sqrt{\varepsilon_{\text{eff}}} f}.$$

To give some numerical examples, table 2.1 gives the wavelength λ at different frequencies and material constants. To relate this to the power transmission line on the chapter page, if we assumed $f = 50\,\text{Hz}$ and $\varepsilon_r = 1$ (air) the wavelength is $5996\,\text{km}$.

Table 2.1: Wavelength λ for different effective dielectric constants and frequencies

f	$dx(\varepsilon_r = 1)$	$dx(\varepsilon_r = 4)$	$dx(\varepsilon_r = 12)$	$dx(\varepsilon_{\text{eff}} = 100)$
GHz			mm	
1	300	150	86.5	30.0
20	15.0	7.49	4.33	1.50
30	9.99	5.00	2.88	0.999
40	7.49	3.75	2.16	0.749
50	6.00	3.00	1.73	0.600
60	5.00	2.50	1.44	0.500
100	3.00	1.50	0.865	0.300

This thesis will mainly focus on the technology CMOS, which ruffly consists of silicon with $\varepsilon_r \approx 12$ and the insulator silicon dioxide $\varepsilon_r \approx 4$, more details will be given in chapter 3. To further reduce the waves velocity, there are a number of techniques under the name "Slow wave", discussed in detail in section 3.3, which can increase the effective dielectric constant to values as high as $\varepsilon_{\text{eff}} \approx 100$.

Since a typical CMOS chip is on the order of millimeter/centimeter in size, transmission lines are unsuited for low frequency ($< 1\,\text{GHz}$) applications; due to the long lengths required. However, at higher frequencies and utilizing slow wave techniques to increase ε_{eff}, transmission lines on CMOS is an attractive alternative.

In summary we can note that the phase shift caused by the finite speed of light can be ignored for low frequency signals (sub GHz) when working on CMOS. But to take advantage of the continuous transistor scaling, now reaching $f_{\text{max}} = 100\,\text{GHz}$, careful interconnect design becomes necessary.

2.2 Telegrapher's equations

One way to derive the wave equation for a transmission line is to use the equivalent circuit in figure 2.3. We can then apply Kirchhoff's laws to obtain

$$I(x)(R + j\omega L)\Delta x + V(x + \Delta x) = V(x),$$
$$V(x + \Delta x)(G + j\omega C)\Delta x + I(x + \Delta x) = I(x).$$

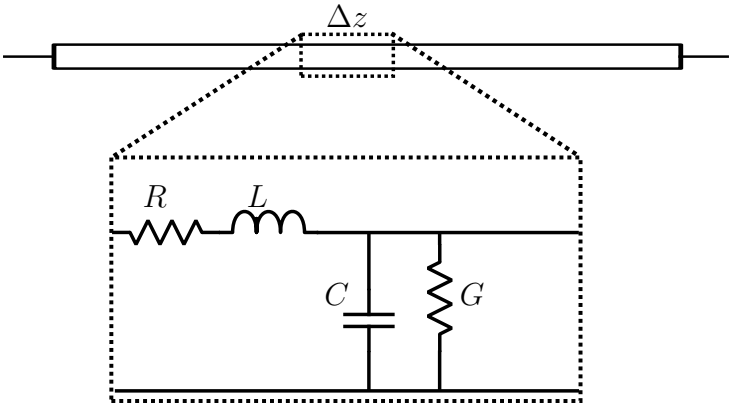


Figure 2.3: Basic RLCG model of a TL representing a short segment Δx

Letting $\Delta x \to 0$ this can be rewritten as a set of coupled differential equation,

$$\frac{dV(x)}{dx} = -I(x)(R + j\omega L),$$
$$\frac{dI(x)}{dx} = -V(x)(G + j\omega C).$$

Differentiating both sides we can write it as a set of second order equations

$$\frac{d^2V(x)}{dx^2} = V(x)(G + j\omega C)(R + j\omega L),$$
$$\frac{d^2I(x)}{dx^2} = -I(x)(R + j\omega L)(G + j\omega C).$$

With solutions

$$\begin{aligned} V(x) &= V^+e^{-\gamma x} + V^-e^{\gamma x}, \\ I(x) &= I^+e^{-\gamma x} + I^-e^{\gamma x} = \frac{V^+}{Z_0}e^{-\gamma x} + \frac{V^-}{Z_0}e^{\gamma x} \end{aligned} \tag{2.4}$$

Where I^+ is the wave traveling in the positive x direction and I^- is the wave traveling in the negative direction (caused by reflection). Note that a time dependence can be added by multiplying by $e^{j\omega t}$, when the line is exited by a steady sine wave.

In the above we have introduced the characteristic impedance

$$Z_0 = \sqrt{\frac{R + j\omega L}{G + j\omega C}} \tag{2.5}$$

and the propagation constant

$$\gamma \equiv \alpha + j\beta \equiv \sqrt{(R + j\omega L)(G + j\omega C)} \tag{2.6}$$

Some special cases can simplify these expressions, for the lossless ($R = G = 0$) and the low loss approximation ($R \ll \omega L$, $G \ll \omega C$) the characteristic impedance reduces to $Z_0 =$

$\sqrt{L/C}$. In addition to these approximation, the distortionless condition $L/R = C/G$ ensures a frequency independent characteristic impedance equal to $Z_0 = \sqrt{L/C} = \sqrt{R/G}$, which can be useful for lossy transmission lines. Under these conditions the propagation constant can be written as

$$\gamma = \begin{cases} j\omega\sqrt{LC} & \text{lossless } R = G = 0 \\ \frac{1}{2}\left(\frac{R}{Z_0} + GZ_0\right) + j\omega\sqrt{LC} & \text{low loss } R \ll \omega L,\ G \ll \omega C \\ \sqrt{RG} + j\omega\sqrt{LC} & \text{distortionless } L/R = C/G \end{cases} \tag{2.7}$$

2.3 Loss

We will now consider a non-ideal characteristic of a transmission line, namely "loss". This can be divided into different terms based on the underlying physical phenomena, [Hay97] suggests that the total loss for a transmission line on a conductive substrate (like silicon) can be expressed as

$$\alpha = \alpha_{\text{ohmic}} + \alpha_{\text{rad}} + \alpha_{\text{modes}} + \alpha_{\text{sub-pol}} + \alpha_{\text{sub-cond}}$$

where α is the attenuation constant in the propagation constant (2.7) with unit $\mathrm{Np/m}$. An example with $\alpha = 3\,\mathrm{dB/mm} = 0.345\,\mathrm{Np/mm}$ over a distance of 10 wavelengths is shown in figure 2.4. We see that after $1\,\mathrm{mm}$ the wave has attenuated by $e^{-0.345}$ or equivalently from the dB value, the signal has halved.

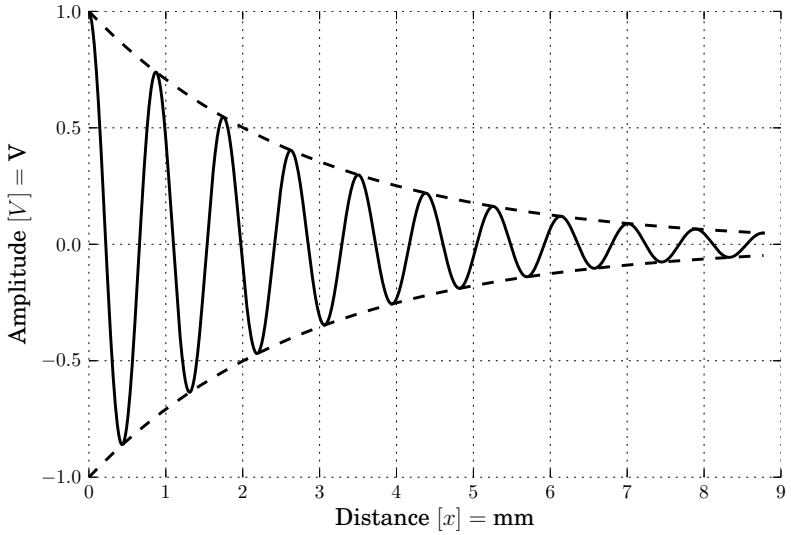


Figure 2.4: Voltage as function of distance with an attenuation loss $\alpha = 3\,\mathrm{dB/mm}$.

2.3.1 Displacement and substrate loss by Maxwell's equations

We start with some fundamental electromagnetic theory, for a more thorough introduction see a standard textbook, like *Foundations for Microwave Engineering [Col01]* or *University physics with modern physics [YFF08]*.

Maxwell's equations together with Lorentz force law form the basis for all electrical circuit theory. Force on a particle q with velocity $\vec{v}$ can be expressed in terms of the electric and magnetic field by the Lortenz force law

$$\vec{F} = q\Big(\vec{E} + \vec{v} \times \vec{B}\Big). \tag{2.8}$$

We can turn this equation around and state that a charge q experiencing a force $\vec{F}$ will radiate an electric field $\vec{E}$. If this charge is moving, it will also produce a magnetic field $\vec{B}$. The magnetic and electric field we have just introduced is not something that can be directly observed, is it rather an abstraction for the force a test charge q_0 will experience if it is placed in a particular position.[YFF08]

Gauss law relate a total charge Q and the electric field through $\vec{D} = \varepsilon_0\vec{E} + \vec{P}$. For a well behaving material (linear and isotropic), dielectric polarization can be expressed as a function of the electric field

$$\vec{P} = \varepsilon_0\chi_e\vec{E},$$

where the electric susceptibility $\chi_e = \varepsilon_r - 1$ is a measure of how easily a material polarizes (rotates or stretches when applying an electric field). We may now rewrite displacement to

$$\vec{D} = \varepsilon_0\vec{E} + \varepsilon_0(\varepsilon_r - 1)\vec{E} = \varepsilon_0\varepsilon_r\vec{E} \equiv \varepsilon\vec{E}. \tag{2.9}$$

We have here introduced a frequency dependent complex scaling factor $\varepsilon = \varepsilon' - j\varepsilon''$ (absolute dielectric constant). The complex frequency dependence can be intuitively explained by noting that the atom needs time to adjust to the applied field, if the applied field changes slowly (low frequency) the atom will reach a stable equilibrium, while at higher frequencies the atom may lag behind or oscillate like a spring–mass–dampening system (see [Col01] for details). Modeling the polarization of a crystal structure with free electrons (like silicon) requires quantum physics and is therefore outside the scope of this thesis.

Ampère's law gives a relation between the magnetic field and current density $\vec{J}$

$$\vec{\nabla} \times \vec{H} = \vec{J} + j\omega\vec{D}.$$

Inserting the current density $\vec{J} = \sigma\vec{E}$ and displacement from (2.9)

$$\begin{aligned}\vec{\nabla} \times \vec{H} &= \sigma\vec{E} + \varepsilon j\omega\vec{E} \\ &= \sigma\vec{E} + (\varepsilon' - j\varepsilon'')j\omega\vec{E} \\ &= [(\sigma + \omega\varepsilon'') + j\omega\varepsilon']\vec{E}\end{aligned}$$

Where we can define the loss tangent $\tan\delta$, where δ is the angle between the real (resistive) and imaginary (capacitive) part

$$\tan\delta \equiv \frac{\sigma + \omega\varepsilon''}{\omega\varepsilon'} = \underbrace{\frac{\sigma}{\omega\varepsilon'}}_{\text{extrinsic}} + \underbrace{\frac{\varepsilon''}{\varepsilon'}}_{\text{intrinsic}} \tag{2.10}$$

We have divided this into extrinsic and intrinsic loss. The intrinsic loss is from current going through the substrate and is a limitation of not having an insulating substrate ($\sigma_{\text{insulator}} = 0$) and the extrinsic loss is caused by polarization of the substrate and is loss due to the energy used to displace the atoms in the substrate. [RYCYYK$^+$06] The loss tangent is usually viewed as a material constant for a narrow frequency range, but it is important to remember that both ε' and ε'' are function of frequency which may cause $\tan\delta$ to change by orders of magnitude.

The per unit length model for this is an imperfect capacitor, so a resistor in parallel with C is used, see figure 2.5.

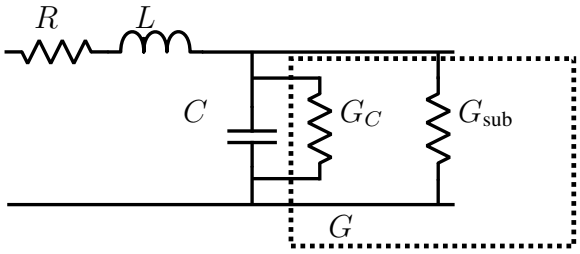


Figure 2.5: Accounting for an imperfect capacitor introduces G_C to the model in figure 2.3.

2.3.2 Mode coupling

An important assumption for transmission line design is Transverse Electromagnetic (TEM) propagation, where the magnetic and electric fields are orthogonal. This however only holds for a conductor in a homogeneous environment, like a coax. In this mode the wave travels with the same speed both above and below the conductor. When the line is created on top of a substrate the wave in the substrate will move slower than the wave above, at low frequencies this effect is not noticeable and the line behaves much like a true TEM line. For low frequencies this can be modeled by introducing an effective dielectric constant ε_{eff}. The mode is then often referred to as "Quasi TEM".[LB09]

Below we will investigate the loss caused by these non-TEM modes for a Coplanar Waveguide (CPW), in particular when the CPW is mounted on a substrate with a conductor backing (as in CMOS).

Based on Collier [Kwo91] we can express the "critical frequency" before the TEM mode starts to mix with Transverse Electro (TE) and Transverse Magnetic (TM) modes for a CPW on a silicon substrate of height h_{Si}

$$f_{TE} = \sqrt{\frac{2}{\varepsilon_{\text{Si}} - 1}} \frac{c}{2\pi \cdot h_{\text{Si}}} \left(\arctan 1 + \frac{\pi}{2}\right) = 137\,\text{GHz}$$

$$f_{TM} = \sqrt{\frac{2}{\varepsilon_{\text{Si}} - 1}} \frac{c}{2\pi \cdot h_{\text{Si}}} (\arctan \varepsilon_{\text{Si}}) = 86\,\text{GHz}$$

where both modes fall within the millimeter wave frequency spectrum. The frequencies was found by using typical CMOS parameters. What we observe is that the TM mode will start to interact with the TEM mode above $86\,\text{GHz}$, making CPWs less attractive above this frequency. Another observation is that the frequencies scale as $1/h_{\text{Si}}$, hence decreasing the substrate thickness will increase the critical frequencies.

Above the critical frequencies CPW transmission lines should be avoided, the solution is then to use TM or TE as the wavemodes, this can be achieved in waveguide structures and will not be further discussed in this thesis.

In [RMAF90] Riaziat et al. derive the following expression for loss due to coupling to the first TM mode

$$\alpha_{\text{mode}} = \frac{\pi^2}{2h_{\text{Si}}} \frac{Z_0}{\eta_d} \frac{(W_s + 2G_{sg})^2}{c^2} f^2 \varepsilon_{\text{Si}} \sqrt{1 - \varepsilon_{\text{eff}}/\varepsilon_{\text{Si}}}$$

where ε_{eff} is the effective dielectric constant of the CPW, $\varepsilon_{\text{Si}} = 11.7$ is the substrate's effective dielectric constant and $\eta_d = 377\,\Omega/\sqrt{\varepsilon_{\text{Si}}}$ is the wave impedance. In addition to the $1/h_{\text{Si}}$ seen above, the loss contains the geometric terms W_s (signal width) and G_{sg} (gap), but the most important term is the square root which goes to zero for $\varepsilon_{\text{eff}} = \varepsilon_{\text{Si}}$.

Figure 2.6 shows the loss for different values of the effective dielectric constant, as we approach the substrates dielectric constant the loss goes to zero. We also note that the maximum value of $\alpha_{\text{mode}} = 0.07\,\text{dB/mm}$ is very low.

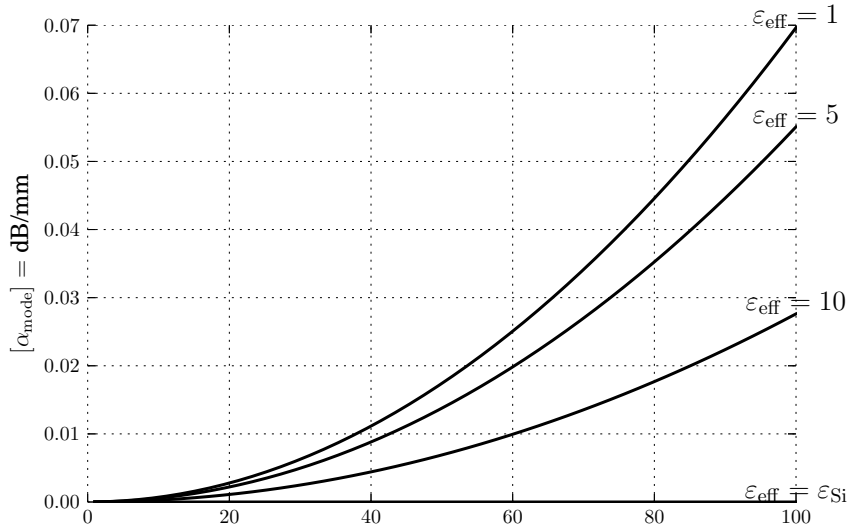


Figure 2.6: Loss due to non TEM mode.

2.3.3 Radiation

Any wire of significant length will act as an antenna, which can cause both noise (due to disturbance from other wires) and loss (due to the energy used to transmit). The received signal will typically be orders of magnitude lower than any signal we wish to transmit over the transmission line, especially if we shield our chip properly, unless of course the offending transmitter is close by (say on the same chip). Loss by radiation is decreased by having the return current flow close by the signal current, the emitted field is then decreased due to a TEM mode without a radiation mode. In addition, proper termination is important to avoid standing waves; this includes bends and other discontinuities. [KS88] Due to the complexity of transmission line radiation, EM simulation is usually required, as this will show any unwanted modes.

2.3.4 Summary

Turning back to our original expression

$$\alpha = \alpha_{\text{ohmic}} + \boldsymbol{\alpha}_{\text{rad}} + \boldsymbol{\alpha}_{\text{modes}} + \boldsymbol{\alpha}_{\text{sub-pol}} + \alpha_{\text{sub-cond}}$$

we have now covered substrate loss by polarization, mode coupling and radiation. These are the most obscure types of losses, and is often neglected. In the case of radiation and mode loss, their significance can be ignored if the transmission line is well designed. And substrate polarization is usually considered negligible, but we will later in the thesis highlight its importance for silicon designs.

Neglecting radiation and modes we can now develop a first order approximation to the total loss. The ohmic and conductive substrate loss can for the case of low loss be calculated from the definition of the propagation constant and the characteristic impedance, from (2.7) it is clear that the real part of the propagation constant ($\Re\gamma = \alpha$) can be expressed as $\alpha = \frac{1}{2}\frac{R}{Z_0} + \frac{1}{2}GZ_0$ Where the first part is the ohmic loss and the second contains both substrate conductivity and polarization. Since δ is the angle between the real and imaginary part we can write $\tan\delta = G/\omega C$, the above results in

$$\begin{aligned} \alpha_{\text{ohmic}} &= \frac{1}{2}\frac{R}{Z_0} \\ \alpha_{\text{sub-con}} + \alpha_{\text{sub-pol}} &= \frac{1}{2}GZ_0 = \frac{1}{2}\omega C Z_0 \tan\delta = \frac{1}{2}\frac{CZ_0}{\varepsilon'}(\sigma_{\text{Si}} + \omega\varepsilon'') . \end{aligned} \tag{2.11}$$

The conductive substrate loss is frequency independent, but the displacement loss is proportional to frequency and therefore cause problems at high frequencies. Equation (2.11) is a function of both line geometry (CZ_0/ε') and substrate material. Where the real part of the permittivity (ε') is the energy storage capacity. The loss factors are then the imaginary part (ε''), which is loss due to polarization, and conductivity (σ_{Si}) being the ohmic loss of the substrate (where $\sigma_{\text{Si}} \approx 0$ for a non-semiconductor substrate).

2.4 Reflection

Up until this point we have assumed a wave traveling down an infinitely long transmission line, with no start or end termination. We now add this effect by investigating the general setup in figure 2.7. The depicted setup can be viewed as a signal generator V_G with an output impedance of Z_G, connected via a transmission line Z_0 with phase shift and loss γ, to some load impedance Z_L we wish to characterize. But the discussion below is equally valid when the generator is a transistor and both Z_G and Z_L may contain a complex network including transmission line segments.

At any transmission line interface where the impedance changes we get reflection, some of the incident power will go back and the rest will continue. This can easily be proven by requiring $Z_L = I_L V_L$ and using the derived wave equation (2.4) at $x = 0$, the result is usually

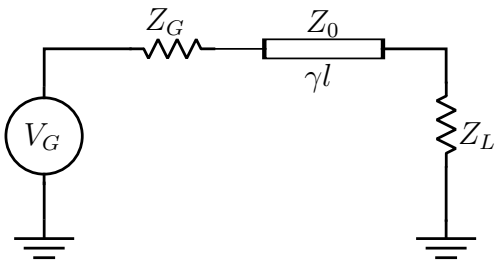


Figure 2.7: Transmission line characterized by Z_0 and γl, with generator (G) and load (L). Note that all quantities can be complex and frequency dependent.

called the reflection coefficient, here shown for the load

$$\frac{V^+}{V^-} \equiv \Gamma_L = \frac{Z_L - Z_0}{Z_L + Z_0}.$$

If Γ_i is 0 there is no reflection and if $|\Gamma_i|$ is 1 we have full reflection and all the incident power will be reflected back.

2.4.1 A time domain view

As an example, the transient response when V_G is a step function will be discussed, mostly following the example in [JG93]. At time $t = 0$ we have a voltage division between Z_G and Z_0, this is then delayed and attenuated by the transmission line. If the load impedance is different from the characteristic impedance of the line, the fraction Γ_L will reflect back towards the source. Depicted in the top part of figure 2.8 is the input (V_G) and V_{L0} which is the voltage over the load considering no further reflections.

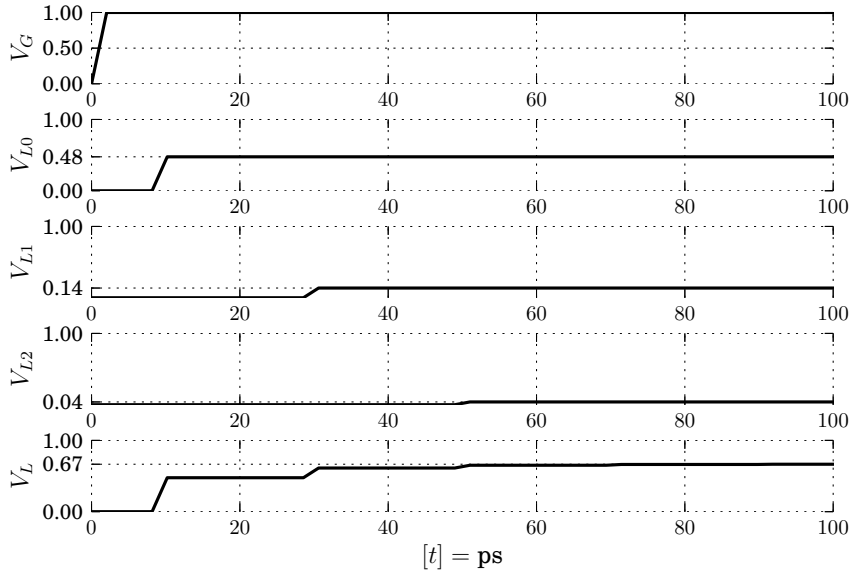


Figure 2.8: Reflection when $Z_G = 50$, $Z_0 = 20$ and $Z_L = 100$ (see figure 2.7). Showing the first intermediate voltages, the input V_G (top) and the output $V_L = \sum_i V_{Li}$ (bottom).

The reflected part will go back towards the source, reflect again by the fraction Γ_G then go towards the load and reflect by Γ_L, the result is V_{L1}. This continuous forever, but the magnitude

of the reflection falls off rapidly. In figure 2.8 the third step V_{L2} is included and at the bottom the output voltage $V_L = \sum_i V_{Li}$ is shown.

The time domain view is the most intuitive visualization, where a discontinuity will reflect part of the wave backwards. But a frequency view eases system design and gives a simpler mathematical foundation.

2.4.2 A frequency domain view

The time and frequency domain is linked by the fact that we can express most time domain waveforms as a weighted sum of $\sin(\omega_i t)$ terms. We are then focused on the *steady* state, and since we assume the transmission line is lossless, we can, in the steady state, ignore it completely. In the above example we can then conclude that the setup displayed in figure 2.8 will converge towards $1\,\mathrm{V} \cdot 100\,\Omega/(100\,\Omega + 50\,\Omega) = 0.67\,\mathrm{V}$, which is a lot easier to derive than drawing individual step functions, especially if the load is complex.

At higher frequencies the frequency domain view can be summarized concisely by the input impedance

$$Z_{\text{in}} = Z_0 \frac{Z_L + jZ_0 \tanh(\gamma l)}{Z_0 + jZ_L \tanh(\gamma l)}, \tag{2.12}$$

for which there are a number of neat special cases, depending on the load and wavelength for a *lossless* line ($\gamma = j\beta$) we write

$$Z_{\text{in}} = \begin{cases} jZ_0 \tan(\beta l) & \text{short } Z_L = 0 \\ -jZ_0/\tan(\beta l) & \text{open } Z_L = \infty \\ Z_0^2/Z_L & \text{quarter wave } l = \lambda/4 \\ Z_L & \text{DC } f = 0 \end{cases}. \tag{2.13}$$

The first two are particularly useful in filter synthesis, where a lumped filter consisting of inductors and capacitors can be realized by replacing inductors by shorted lines and capacitors by open lines. The quarter wave length can be used for low bandwidth matching networks and we used the last one above.

2.5 Summary

We have now covered the most central aspects of transmission line theory, first introducing waves and the transmission line equation, which forms the mathematical basis we work on. The discussion was quantified by a look at phase shift. A critical aspect of transmission line design on CMOS is loss, so a deep dive was done, dividing loss into ohmic, radition, mode and two kinds of substrate loss. We will quantify the discussion further in chapter 4, where ohmic and substrate loss is expressed in terms of geometry and material properties.

Maybe the biggest surprise for the low frequency engineer is reflection, where a badly designed circuit can cause some baffling behavior. Fortunately, reflection can be used as an advantage, and we will return the phenomena in chapter 8.

Chapter 3

Transmission lines in CMOS

This chapter serves as a literature review and explores different transmission lines in CMOS.

Figure 3.1 shows a simplified cross sectional view of the CMOS process used in this thesis. The vias between metal layers are not shown and the dielectric layers has been simplified, the process also has a single poly layer which is not shown. M10 is not available for routing and is made of aluminum, but is used for contacting measurement probes. The other metal layers are made of copper. Only top part of the substrate is shown, it actually extends to $z = -350\,\mu\mathrm{m}$.

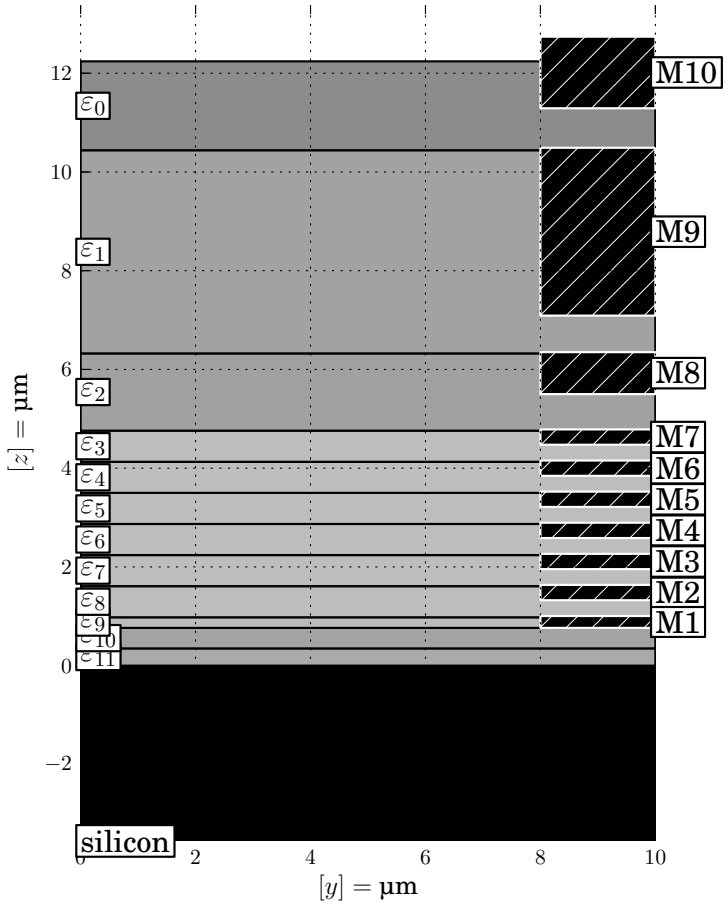


Figure 3.1: Layered structure of a typical CMOS chip, cross sectional view. Metal lines (white border) are submerged in multiple layers of dielectric material (shown simplified) on top of a silicon substrate. Brightness indicate the dielectric constant (silicon is black and air is white).

For most of the modeling part we will assume the dielectric layers are made of silicon dioxide (SiO_2), though mostly for notational convenience. This is however not true in a modern CMOS process, where more novel materials are used in addition to SiO_2. These materials usually have a lower ε_r to reduce capacative coupling between metal layers and is usually referred to as "low κ" materials. The exact material properties are confidential and the number of layers are staggering, so the illustrations used here shows multiple materials averaged together. We will return to the dielectric stack-up in the simulation chapter.

3.1 Limitations of CMOS for RF and millimeter wave design

3.1.1 Density rules

The silicon foundry for modern CMOS processes require that each metal layer has a certain percentage of metal. This is usually specified with both an upper and lower bound, meaning that every metal layer must have between say $30\,\%$ to $80\,\%$ metal fill. The exact numbers are generally kept confidential by the manufacturer. Density rules are checked by the Design Rule Check (DRC) and must be fulfilled in a sliding window of e.g. $100\,\mu\mathrm{m} \times 100\,\mu\mathrm{m}$.

Due to these density rules, additional metal must normally be added, these are usually left floating and perform no electrical function; these are therefore called metal-dummies. In a conventional (low frequency) design, these are automatically added by the design tool at a late stage. At higher frequencies (millimeter) these dummies can severely affect the circuit performance and should therefore be added at an early stage and included in the EM analysis. [SJPR09]

The density rules has two implications for designs

1. For sparse structures some form of metal filler must be added. This is typical for transmission lines where one generally only uses a couple of metal layers. One can for instance use the top layer for the signal line and bottom layer for shield, one then wants the space separating these to be free of metal to reduce capacitance and induced eddy currents. This configuration is however not allowed in a conventional CMOS process.

2. The upper bound prevents utilizing a solid ground shield. A solution by [SJPR09] is to use two layers in a complementary fashion, where the area not covered by one is covered by the other layer.

   One can also have a problems with very wide lines, the solution of "cheesing"[SJPR09] them will affect the wave propagation. To resolve this [OMHW10] suggests looking at the current distribution of the line. Due to the skin and proximity effect the current will crowd to the conductor edge and we can therefore remove the center. Doing this correctly resulting loss can be minimized and a slight decrease in velocity is observed (due to the increased self capacitance and inductance).

3.1.2 Substrate conductivity

As was discussed in section 2.3, substrate conductivity causes signal loss. Due to the high conductivity of silicon, CMOS has a major disadvantage compared to other technologies. It is

therefore vital to shield the line from the silicon substrate. Using alternative technologies, like Silicon On Insulator (SOI) or Gallium arsenid (GaAs) with order of magnitude lower conductivity, mitigate the problem but with the disadvantage of increased cost.

3.1.3 Characterization

Since CMOS is traditionally targeted towards digital applications, the manufacturers only supply transistor and interconnect models for low frequencies. At millimeter wave frequencies these models are simply no longer correct and modeling is then up to the designer. This becomes even more difficult due to the confidentiality of the process, where details of the manufacturing process which can be ignored at lower frequencies become dominant in the millimeter wave band.

As one example, I have been unable to find any information about the dielectric loss in either the substrate nor the dielectric layers. And the literature is of little help since people tend to avoid writing the manufacturers name (unless they are paid to do so), so that at least some confidential information can be included. It does not help that values for dielectric loss tangent range from 1×10^{-3} in [Hay97] and 0.05 in [RYCYYK+06], neither of which discusses CMOS. We will return to the loss tangent later in this chapter.

3.2 Common transmission line structures

We will now cover a few common transmission line structures before we dive into slow wave structures in the next section.

The most basic transmission line is the Microstrip (MS), depicted in figure 3.2, consisting of a signal line above a larger ground plane. The classical work by Hasegawa et al. [HFY71] analyses this structure when the ground plane is placed at the bottom of the substrate and is reviewed in section 3.3.1. Due to the coupling with the substrate this configuration is lossy and dispersive. This can be alleviated by creating a ground plane of the lower metal layers, as illustrated in figure 3.2 and studied on CMOS by Seo et al. [SJPR09] and [LP10].

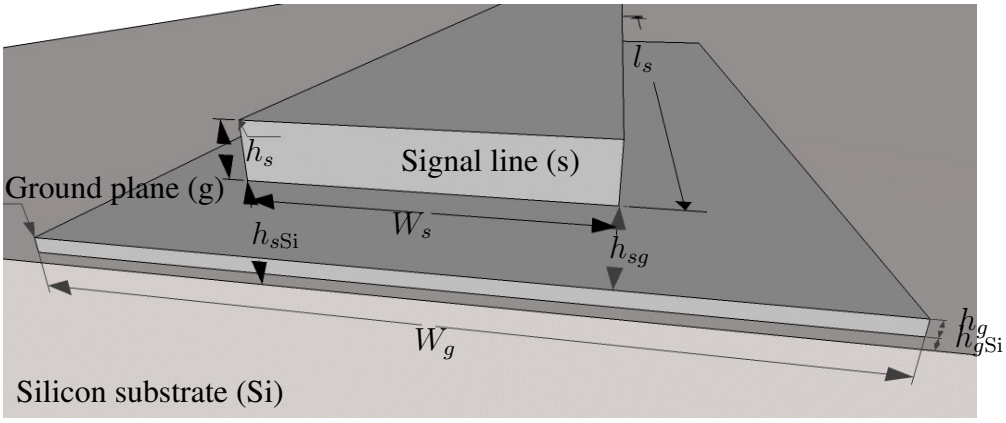


Figure 3.2: Microstrip (MS) transmission line, showing geometric symbols used in this thesis. Note that the ground line may be either on the lower metal layers (as illustrated here) or below the silicon substrate.

When designing for CMOS, it is the manufacturer who decides metal thickness and distances. As pointed out by Cheung and Long [CL06] and others; a microstrip line fabricated on CMOS can only use the signal width W_s as a design variable, as the rest is fixed by the manufacturer. This restriction leads to narrow and thereby lossy transmission line when designing for a characteristic impedance $Z_0 \geq 50\,\Omega$, since Z_0 is mainly influenced by the signal-ground height h_{sg} and W_s.

A more flexible transmission line configuration is the CPW depicted in figure 3.3, where Z_0 is instead influenced by the W_s to gap G_{sg} ratio. The characteristic impedance can then be tuned by varying G_{sg} without reducing W_s. The EM field is here concentrated between the signal line and the ground lines in the upper metal layer(s), reducing coupling to the substrate and other conductors. Because of these advantages the CPW is the most popular transmission line structure on CMOS and will be the main focus of this thesis.

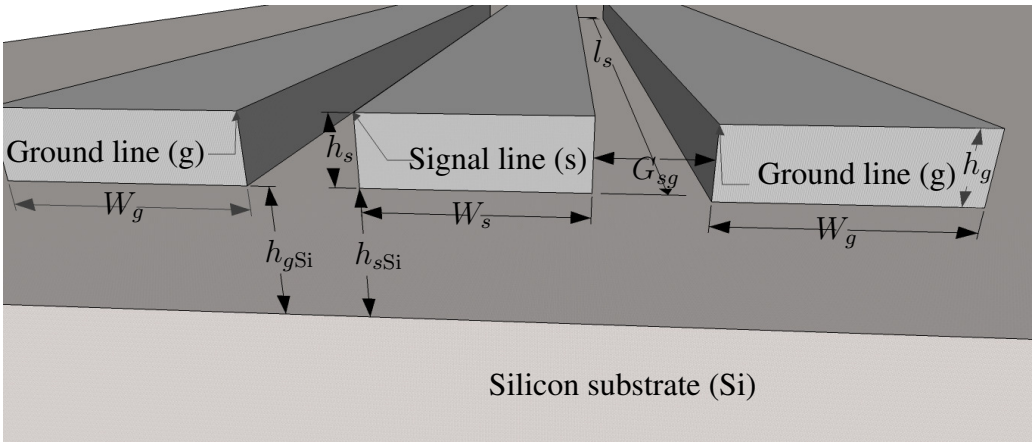


Figure 3.3: Coplanar Waveguide (CPW) transmission line, showing geometric symbols used in this thesis.

For differential signals there are a number of alternatives, one can either use a slot line (large metal sheet with a gap) or a simple extension of the CPW, the "Dual coplanar waveguide" presented recently by Long et al. in [LZW+12]. This is however outside the scope of this thesis.

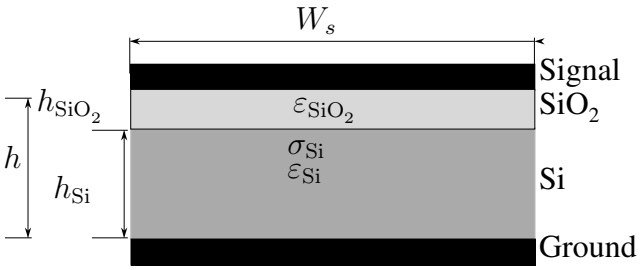
3.3 Slow wave

Remembering that a transmission line embedded in a material with a relative dielectric constant ε_r, moves at the speed $v_p = c/\sqrt{\varepsilon_r}$, an intuitively simple way of reducing v_p would be to use a high ε_r. For instance water ($\varepsilon_r \approx 50$) is a good candidate, but comes with a few practical problems.

The literature provides a number of alternatives for a "Slow wave" transmission line for bulk CMOS realization. The common characteristics is that by separating the electric and magnetic energy, the phase velocity is reduced without resorting to high ε_r materials. We will here briefly explore three of these phenomena, first the Maxwell-Wagner polarization which occurs at the conducting Si and insulating SiO_2 interface at low frequencies. Then in section 3.3.2 we

explore periodic low and high impedance segments and in section 3.3.3 we periodically load the transmission line with orthogonal slots.

3.3.1 Fundamental modes for SiO_2 on Si



(a) Geometry

Figure 3.4: Transmission line with insulator (SiO_2) and conducting substrate (Si).

A simplifying assumption is that electromagnetic waves on a transmission line satisfy TEM, where the electric and magnetic field is perpendicular to each other. With the geometry in figure 3.4, where a conducting substrate is sandwiched with an insulating layer this assumption is no longer valid. As investigated by Hasegawa et al. [HFY71] three different modes can be observed depending on the substrate conductivity and frequency.

Hasegawa et al. provides an equivalent circuit for each mode and an attempt has been made to implement the models and comparing them to simulation results. But I have failed to get a model that makes any sense, so more intuitive, but less mathematically rigorous, models will be presented.

1. Dielectric quasi TEM mode is valid above

$$\omega \gtrsim 1.5 \frac{\sigma_2}{\varepsilon_0 \varepsilon_{Si}}$$

and when the wavelength is longer than the thickness of the substrate and insulator. Higher order modes discussed in section 2.3.2 provides an upper bound.

An equivalent circuit is shown in figure 3.5, where the Y part of the equivalent circuit is modelled as a capacitor for the insulating material and a lossy capacitor (a G in parallel with an ideal C). The insulator is considered loss-less due to the assumed small thickness and much lower conductivity ($\sigma_{SiO_2} \approx 0$) of the insulating material. Resistance is included for both the signal line and ground line (R_s and R_g respectively) and the inductance is found as a function of distance to the ground plane.

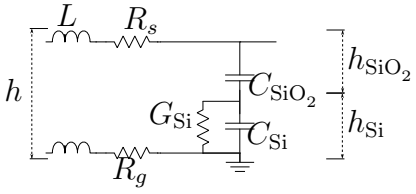


Figure 3.5: Equivalent circuit for the quasi TEM mode.

2. Substrate skin–effect mode: The wave penetrates only a distance

$$\delta_{\mathrm{Si}} = \sqrt{\frac{2}{\sigma_{\mathrm{Si}}\mu_0\omega}}$$

into the substrate and the substrate itself acts like a ground conductor due to the low resistivity. The series resistance is large and both inductance and resistance is a function of δ_{Si}. Capacitance is now dependent on the thinner SiO_2 insulating layer, but due to the increased inductance phase velocity is mostly unchanged. This is illustrated in figure 3.6, where R_g has been replaced by silicon R_{Si} and inductance is now reduced due to the reduced distance to the return current.

Energy loss is high since most of the return current now flow in the substrate.

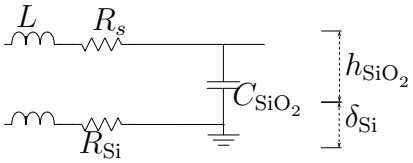


Figure 3.6: Equivalent circuit for the skin effect mode.

3. Slow-wave mode: When the height h is larger than δ_{Si} inductance is again only a function of distance to the ground plane, but free charges in the interface stops the electric field from penetrating the substrate. This creates a large capacitance combined with a large inductance, which slows down the propagating wave. The equivalent circuit is depicted in figure 3.7 where C_{Si} is removed from the quasi TEM model, substantially increasing the equivalent capacitance.

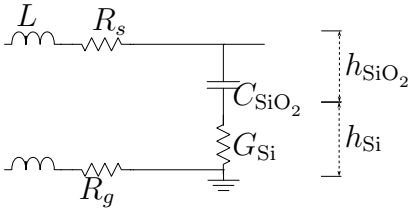
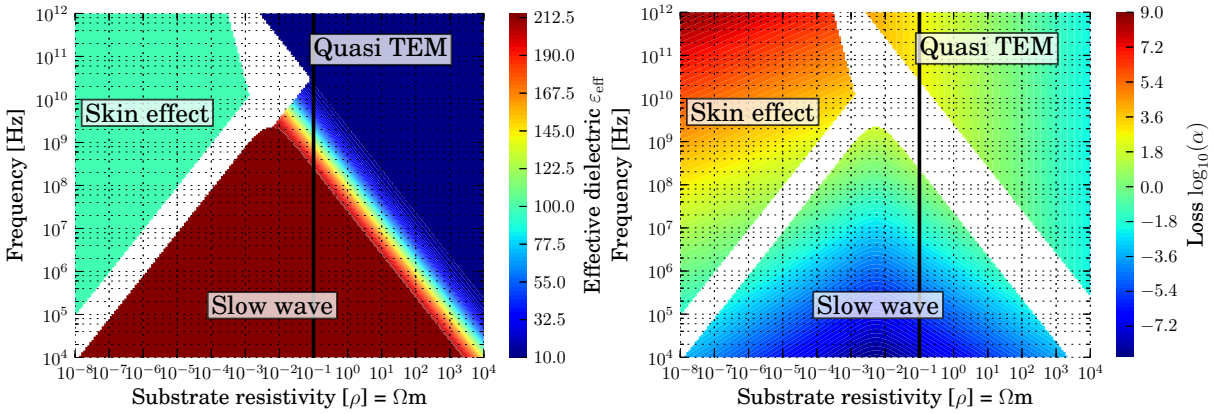


Figure 3.7: Equivalent circuit for the slow wave mode.

Figure 3.8 depict the frequency and resistivity values for the modes discussed above. In the figure CMOS resistivity is marked as a black line. Note that this value is very dependent on the purity and doping of Si, for instance [TPBQ08] report a resistivity of $\rho = 1/\sigma = 1 \times 10^{-4}\,\Omega\,\mathrm{m}$ for a heavily doped substrate. Leading to skin effect mode instead of a Quasi TEM mode at millimeter wave frequencies.

In figure 3.8(a) the colors indicate the effective dielectric constant. The related term "slow wave factor" can be defined as the wavelength in air (λ_0) divided by the actual wavelength (λ), in which case $\lambda_0/\lambda = \sqrt{\varepsilon_{\mathrm{eff}}}$. The figure shows that the slow wave mode has the highest slow wave factor, which is equivalent to a short wavelength, writing $v_p = \lambda f$ it is evident that this mode has the lowest phase velocity and hence the name "slow wave".

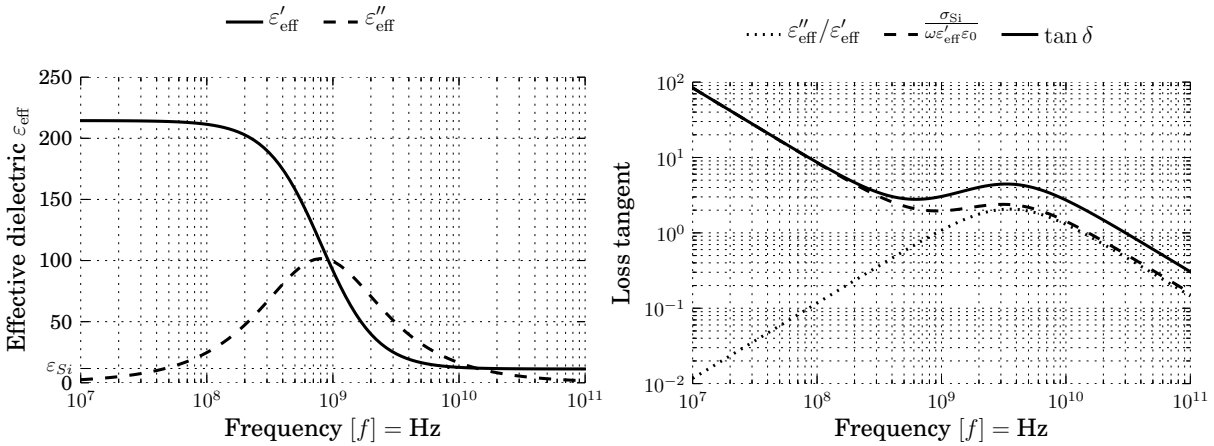


(a) Slow wave factor, only transition from slow wave to Quasi TEM is modelled.

(b) Loss, where α is in $\mathrm{Np/m}$.

Figure 3.8: "Resistivity-frequency domain chart"[HFY71] for $h_{\mathrm{SiO_2}}/h_{\mathrm{Si}} \approx 7\,\mu\mathrm{m}/350\,\mu\mathrm{m}$ showing slow wave factor and substrate loss. Black line at $\sigma = 10\,/\Omega\mathrm{m}$ indicated approximate bulk CMOS conductivity. Transitions in white are not modeled.

From the loss in figure 3.8(b) two general trends can be observed. First, as the frequency is increased so is loss and as the substrate resistivity is decreased (conductivity is increased) the loss increases. This makes the skin effect region the most lossy mode.



(a) Real and imaginary part of the effective dielectric constant, based on [HFY71].

(b) Loss by substrate conductivity and polarization.

Figure 3.9: Relative complex dielectric constant, accounting for polarization charge at the $\mathrm{Si/SiO_2}$ interface. Showing both relative dielectric constant and loss tangent divided into polarization and conductivity loss. Where $h_{\mathrm{SiO_2}}/h_{\mathrm{Si}} \approx 7\,\mu\mathrm{m}/350\,\mu\mathrm{m}$ and $\sigma_{\mathrm{Si}} = 10\,/\Omega\mathrm{m}$.

In figure 3.9 a 2D view is given, where the substrate conductivity is set to the black line in figure 3.8 to correspond to the CMOS process of interest. The effective dielectric constant is very high, but decreases quickly to the value of silicon in the millimeter frequency range. By decreasing the ratio $h_{\mathrm{SiO_2}}/h_{\mathrm{Si}}$, for instance by using lower metal layers, the effective dielectric constant increases but so does the cutoff frequency; making it even less attractive for high frequency applications. The assumed model is sometimes called a "Debye model", which seems to me as a fancy name for a first order (single pole) model.

Figure 3.9(b) shows a rather surprising result, by using the work by Hasegawa to estimate the real and imaginary part of the relative dielectric constant, combined with the conductivity of $10\,/\Omega\mathrm{m}$, we can by (2.10) calculate the components of the loss tangent $\tan\delta = \varepsilon''/\varepsilon' + \sigma_{\mathrm{Si}}/(\omega\varepsilon')$. First of all, $\tan\delta$ is far from constant, but this was also predicted when we introduced the loss tangent in section 2.3.1. Secondly, loss by conductivity is comparable to dielectric loss and the absolute value is much larger than previously reported. For instance [Hay97], gives typical values for $\varepsilon''/\varepsilon'$ as 10^{-4} to 10^{-3}. We will use the calculated $\tan\delta$ represented here in the modeling chapter, and will conclude that the model agrees well with measurements.

In the meantime, we still have two more slow wave realizations to cover.

3.3.2 Periodic high and low impedance

By cascading short low and high impedance transmission line segments periodicallly as depicted in figure 3.10 the wave can be slowed down.

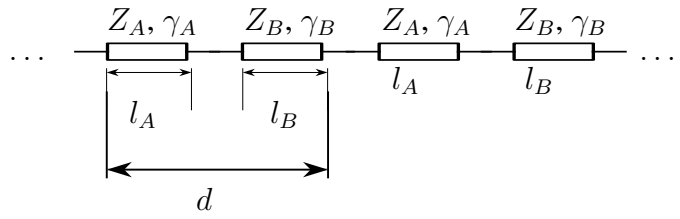


Figure 3.10: Periodically Cascading transmission lines with different impedances.

The phenomena can be explored by Floquet's theorem, which simply states that a periodic structure will have a periodic propagating field (Φ) [Col01]

$$\Phi(z+d) = \Phi(z)e^{-j\beta d} \tag{3.1}$$

where d is the period in meter and β is the fields propagation constant. This has been investigated by Seki and Hasegawa [SH81] and later in a more general form by Kwon [Kwo91]. Equation (3.1) is satisfied when both voltage and current is continuous at the boundaries, which we can express in terms of the $\mathbf{ABCD}$ network representation

$$\mathbf{ABCD}_{AB} = \begin{pmatrix} \cosh(\gamma_A l_A) & Z_A \sinh(\gamma_A l_A) \\ Z_A^{-1}\sinh(\gamma_A l_A) & \cosh(\gamma_A l_A) \end{pmatrix} \begin{pmatrix} \cosh(\gamma_B l_B) & Z_B \sinh(\gamma_B l_B) \\ Z_B^{-1}\sinh(\gamma_B l_B) & \cosh(\gamma_B l_B) \end{pmatrix}$$

Lumping this to an equivalent transmission line of length $d = l_B + l_A$ we must require that the above is equal to

$$\mathbf{ABCD} = \begin{pmatrix} \cosh(\gamma l) & Z\sinh(\gamma l) \\ Z^{-1}\sinh(\gamma l) & \cosh(\gamma l) \end{pmatrix}$$

The above can not be satisfied exactly since $\mathbf{ABCD}_{AB}$ is not symmetric (and $\mathbf{ABCD}$ is).

Based on the above, [Kwo91] derives the following relation for a slow wave line consisting

of alternating sections of low (A) and high (B) impedance

$$\cosh(\beta l) = \cosh(\beta_A l_A)\cosh(\beta_B l_B) + \frac{1}{2}\left(\frac{Z_A}{Z_B} + \frac{Z_B}{Z_A}\right)\sinh(\beta_A l_A)\sinh(\beta_B l_B). \tag{3.2}$$

The above is only valid when the lengths l_A and l_B is smaller than the wavelength and Z_B is much larger than Z_A (that is, $Z_A/Z_B \ll 1$).

Solving (3.2) for β and using one of the examples in [SH81] we get figure 3.11. The closed form solution in (3.2) is compared with a naive solution of multiplying ABCD representations of line A and B. Note that a large number of sections must be cascaded before the result converge. Also included is the line A and B alone, showing that the cascade has increased ε_{eff} from 9 to 153.

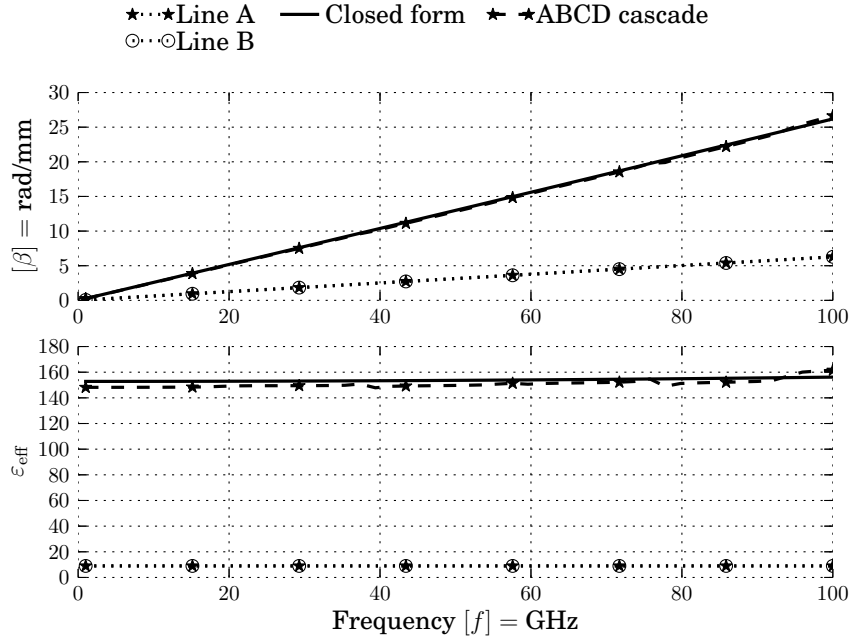


Figure 3.11: The closed form is from solving (3.2) with $Z_A/Z_B = 1/66$, $l_A = l_B = 10\,\mu\text{m}$ and $\beta_A = \beta_B = \omega/(1 \times 10^8)\text{rad/m}$. The ABCD cascade is found by cascading 64 ABCD sections of line A and line B.

3.3.3 Slow wave slots

We are now in a position to discuss the more conventional slow wave implementation in CMOS. This can be viewed as either a periodic structure, as seen in the previous section (3.3.2), or as separating the electric and magnetic field as in section 3.3.1. Figure 3.12 and figure 3.13 shows the microstrip and CPW implementation respectivly. We will also introduce some impressive abbreviations (GSCPW), so keep the nomenclature close by.

When comparing the slotted microstrip line in figure 3.12 to the conventional shielded line in figure 3.2 the location and direction of the return current is the deciding difference. For both structures the electric field will terminate on the ground layer, effectively loading the line with a large C. By moving the ground layer closer; C is increased and for the conventional design L is reduced, since the return current flows closer to the signal line. This keeps the phase velocity

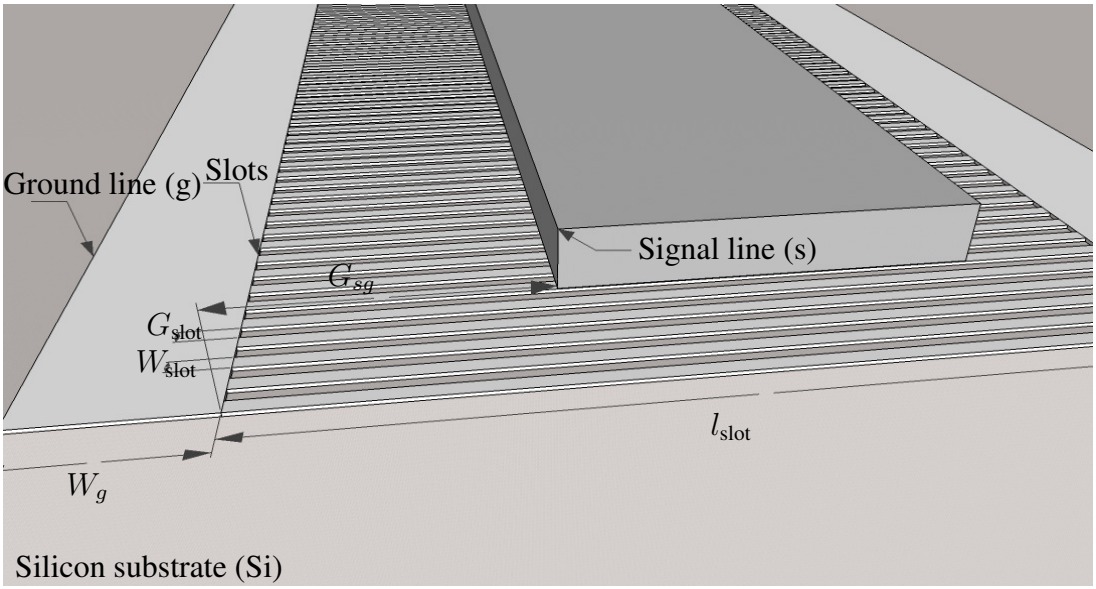


Figure 3.12: Slow wave microstrip line (SMS) transmission line, showing geometric symbols used in this thesis.

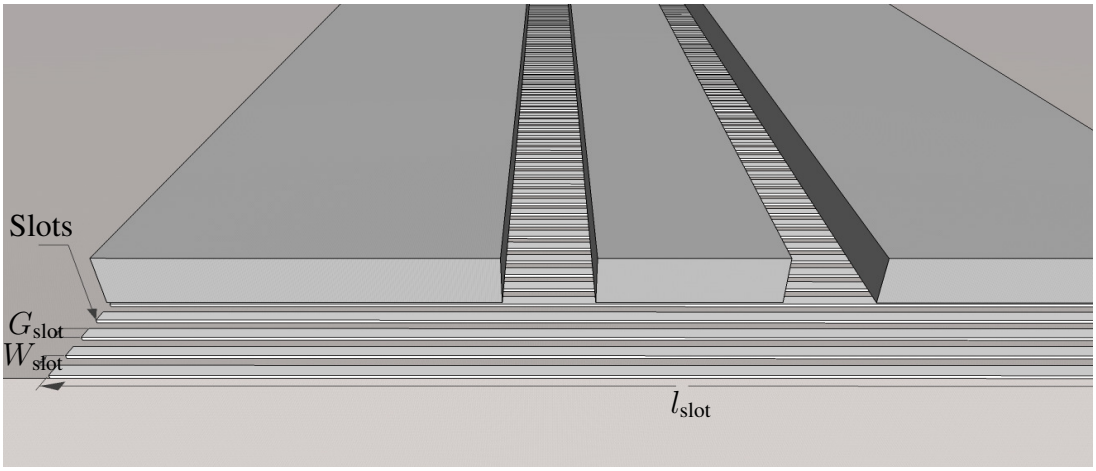
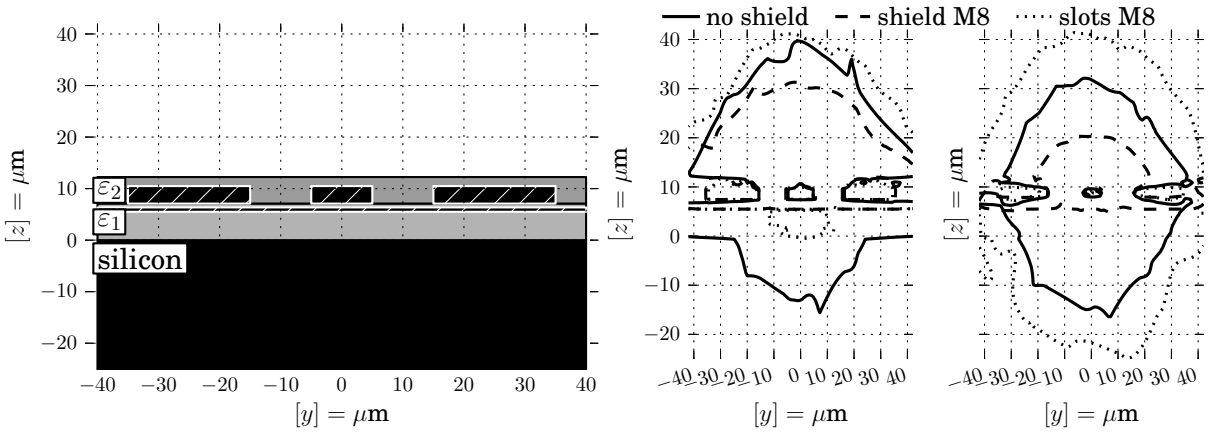


Figure 3.13: Slow wave Coplanar Waveguide (SCPW) transmission line, showing geometric symbols used in this thesis. If the slots are connected to the ground lines (for instance by vias) we have a Grounded SCPW (GSCPW).

constants, due to $v_p = 1/\sqrt{LC}$. In the slotted design the return current is forced away from the signal line and the inductance is therefore kept constant, leading to a reduced phase velocity. The slow wave microstrip line above can also be viewed as a special case of the Grounded Slow wave Coplanar Waveguide (GSCPW), where the signal line is elevated above the ground lines.

For the CPW line in figure 3.13 the slots can be viewed as shield against the conductive substrate. Had we used a whole shield, induced current in the thin lower metal layer would result in significant loss in addition to the increased L and C; which would reduce the characteristic impedance $Z_0 = \sqrt{L/C}$. In the same manner as above, the slots prevent current flowing orthogonal to the signal, thereby leaving inductance unchanged. If the shield is placed far enough away from the CPW (further away than the signal ground distance G_{sg}), the electric field is mostly confined between the signal and ground lines resulting in the shield not significantly increasing C leaving the characteristic impedance mostly unchanged by the added shield. A similar argument was given by Vecchi et al. [VRE+09a]. Further design guidelines are given below.



(a) Geometry.

(b) HFSS simulation constant E and H field.

Figure 3.14: Constant contour levels for CPW without shielding, floating shield in M8 and floating slotted shield in M8. Right: $E = 6 \times 10^3\,\mathrm{V/m}$, Left: $H = 50\,\mathrm{A/m}$.

We first investigate the field distribution of a conventional CPW line, a shielded line (continuous shield below the CPW) and a slotted shield line. This was simulated in the 3D simulator HFSS, the fields where extracted and a constant contour line for each line is shown in figure 3.14, together with the geometry. As expected, both E and H is confined when using a continuous shield, while for the slotted version only H is able to penetrate the substrate. Note the coordinate system used here, we will in this thesis assume that the signal is moving in the x direction (in/out of the paper), while z is pointing upwards and y is orthogonal to both x and z, making the z, y plane the cross sectional view.

3.3.4 Slow wave parameters

Based on the literature and experiments done in this thesis some design guidelines will be presented for slotted slow wave transmission lines. There is an extensive amount of papers on the subject where many focus on only a single aspect of the design, we will here try to give an overview and compare with my own experience from modeling, simulation and measurements.

A recent work by Franc et al. [FPGF12] investigates the slotted shield thickness t_{slot} and finds that it should be small to reduce induced eddy currents in the slots. It is interesting to note that authors like Franc contribute slot loss entirely to magnetically induced currents, while others consider only the electric coupling.

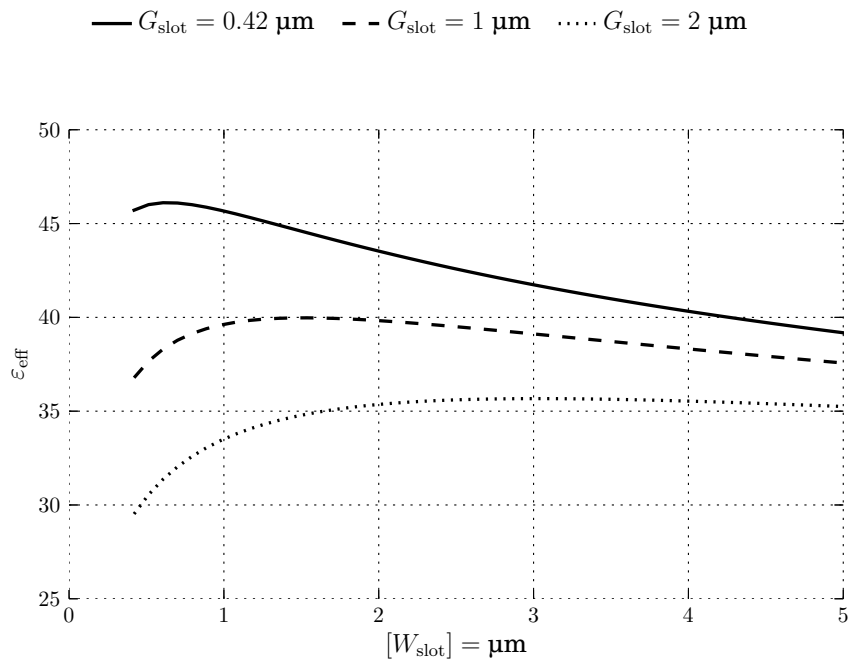


Figure 3.15: Effective dielectric constant for different width and slot gaps. Based on empirical work in [CYLW09].

The "slot ratio", $W_{\text{slot}}/(W_{\text{slot}} + G_{\text{slot}})$ is studied extensively by Aziz et al. for the Coplanar Stripline (CS) line, first by simulation in [AIK+09] and later with measurements in [AFE+12]. The discussion is lengthy, but can be summarized as follows: A smaller slot cross section (width and thickness) leads to reduced loss and the gap should be minimized (but not zero) for highest slow wave effect. The duty cycle of 0.5 (equal width and gap) with minimum dimensions therefore represent the best compromise between loss and size reduction. Although the study is done for a CS line, the field distribution resembles that of a CPW line and is therefore applicable. An empirical equation was derived in [CYLW09] for the CPW and is shown in figure 3.15. Although the absolute value does not coincide with any result in this work, the overall trend gives the same insight as above.

As is the case for a parallel plate capacitor, reducing the height between the signal line and the slots ($h_{s\text{slot}}$), increases capacitance per unit length. [SKXL09] investigates the slotline height $h_{s\text{slot}}$ and finds that the slow wave factor is inversely proportional to the distance $\varepsilon_{\text{eff}} \propto 1/h_{s\text{slot}}$. They also investigates having slots in multiple layers (as opposed to a single layer), but concludes this has little effect on the performance.

Extracting the data from [SKXL09] and including measurements and simulations carried out in this work, figure 3.16 is obtained. There is some discrepancy between simulation and measurements, but we will discuss that later in the thesis. It should be noted that an extensive study on slot distance was not carried out in this thesis, measurements was only done on two floating lines and a single grounded line. Therefore the straight line between two points should

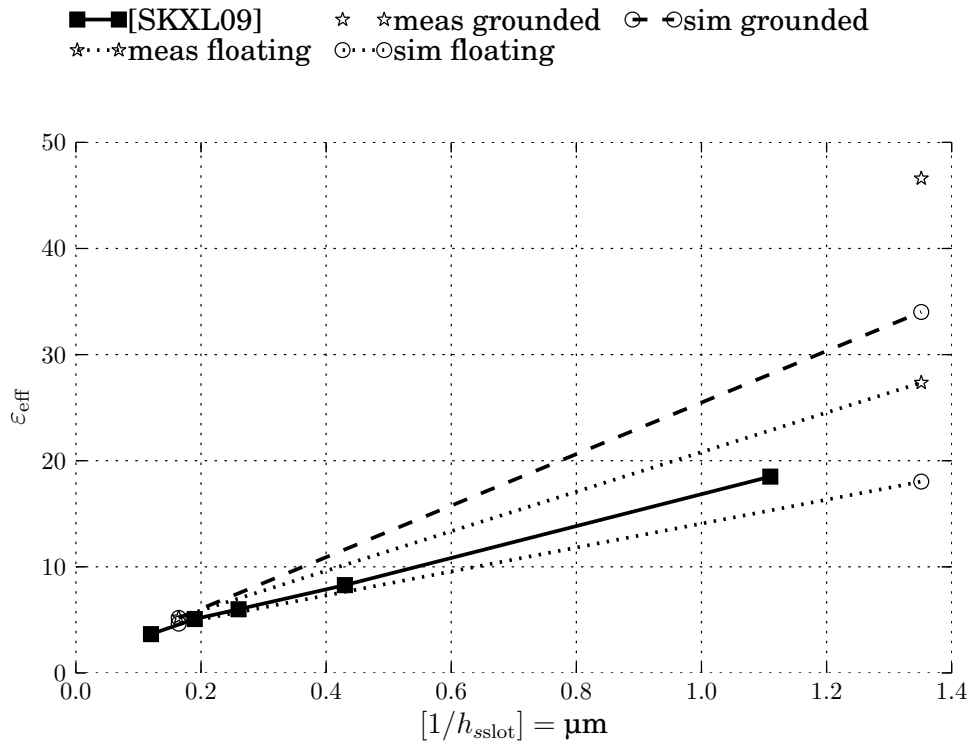


Figure 3.16: Effective dielectric constant for slow wave CPW as a function of reverse of height between slots and signal line. Supporting the data from [SKXL09] with measurements and simulation from this work.

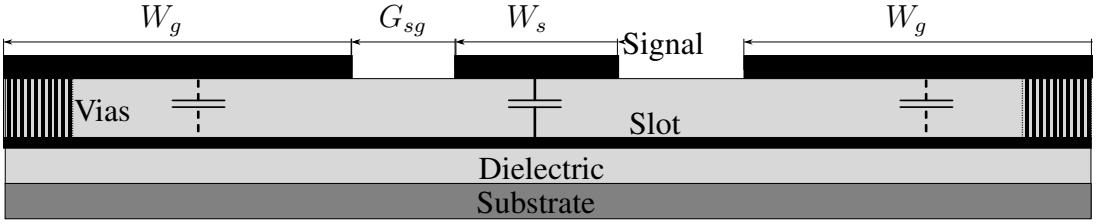


Figure 3.17: Showing capacitance for a floating and grounded (with vias) S-CPW transmission line. Dashed capacitances to ground will be shorted if the vias are used.

be viewed with some skepticism. The main point is that reducing the distance to the slots increases capacitance per unit length and therefore increases the effective dielectric constant.

Also shown in figure 3.16 is results for grounding the slots, these have a higher effective dielectric constant than their floating counterparts. This can be intuitively grasped by considering the equivalent circuit in figure 3.17. If the slots are connected to the ground lines (with vias), then the dashed capacitances will effectively be shorted. If the vias are not used, then the series combination of the signal capacitance and the ground capacitances results in an overall reduced capacitance.

Considering loss, Cheung and Long [CL06] shows that the slots should float to reduce loss at frequencies above $10\,\text{GHz}$. This is contradicted by [SRG09], who shows measurements that a grounded line has lower attenuation than a floating version, and argues that the silicon substrate used in their study ($\sigma_{\text{Si}} = 66.7\,\text{S/m}$) is too conductive for such a technique. This was therefore tested in this thesis and measurements seems to agree with Cheung and Long.

In [TFP+12], Ferrari and his team has done an extensive study on slot length (l_{slot}) for both

conductive and insulating substrate. The conclusion is that for conductive substrates the slots must extend to at least $W_s + 2(W_g + G_{sg})$ for adequate shielding and highest slow wave factor.

A few key points have, as far as I know, not been discussed in the literature in regards to slot dimensions. Firstly, as was implicitly assumed in the previous section, the slot period must be much smaller than the wavelength ($W_{\text{slot}} + G_{\text{slot}} \ll \lambda$), else the operation is limited by the "bragg frequency" and a low pass filter is created. Secondly, it would be reasonable to assume, that the slot thickness also plays a role in the shields effectiveness, as it does in a Faraday cage. This is something to keep in mind as future technologies downscale lower metal dimensions.

To summarize, the slow wave slots should be created in a thin layer with minimum width (to minimize loss) close to the signal line and with minimum gap (to maximize the slow wave factor). It should also be noted that the slow wave line is generally considered to improve the Q factor, but that due to the slow down, the loss per unit length α is not reduced; see for instance [SRG09].

3.3.5 State of the art

Table 3.1 shows some dimensions and performance characteristics of published transmission lines. Most of the entries can also be found in [LP10] and [FPGF12] but all data is based on reading the original source. Number of significant digits may not agree with standard practices, since 5×10^1 is harder to read than 50, if in doubt only a single significant digit should be assumed. Few authors include technology specific information like thickness of layers, height above substrate and substrate conductivity which can greatly impact performance characteristics. To my best knowledge all the transmission lines compared here are based on measurements on standard bulk CMOS.

Table 3.1: Physical size (where available) and performance (at $30\,\text{GHz}$) of published on chip slow wave transmission lines. Sorted by year of publication.

Type	Ref.	W_s	G_{sg}	W_g	$W_{\text{slot}}/G_{\text{slot}}$	Z_0	ϵ_{eff}	α	Q
				μm		Ω		dB/mm	
S-CPW	[CL06]	16	20	-	1.6	**50**	8	**0.4**	17
S-CPW finger	[LF07]	12	34	-	0.25	-	16	1	13
S-CPW	[VKKH08]	12	9	-	-	35	-	0.6	12
S-CPW	[KIF+09]	18	100	60	0.6	35	**47**	-	**40**
S-MS	[LP10]	4	40	-	0.6	45	25	**0.4**	32
S-CPW	[WZY+11]	10	10	45	0.1	**50**	6.0	**0.4**	17
S-CPS	[AFE+12]	**35**	**200**	-	0.6	45.2	-	0.6	27
S-CPW	[FPGF12]	5	50	10	0.16/0.64	35	25.6	**0.4**	35
S-CPW	[TFP+12]	17	20	15	0.1/0.55	28	30	**0.4**	30

Cheung et al. [CLV+03] is usually attributed as the first slow wave transmission line on CMOS, later explored in more details by Cheung and Long [CL06]. Mainly for density compliance, fingers are added in [LF07], an increase in effective dielectric constant is shown, but the impedance of the line is not discussed. High Q lines are presented in [KIF+09], where a large gap spacing and wide signal line are utilized. A "downscaling" of this line is presented in

[FPGF12], where the signal ground spacing is halved and the signal line is reduced to compensate, a comparable Q factor is achieved.

As can be seen, the highest available Q of 40 was created by a line of total width of

$$18\,\mu\mathrm{m} + 2 \cdot 100\,\mu\mathrm{m} + 2 \cdot 60\,\mu\mathrm{m} = 338\,\mu\mathrm{m}.$$

For comparison, in this thesis, lines with *lengths* down to $100\,\mu\mathrm{m}$ are fabricated to reduce cost and area on the small die.

3.4 Summary

We have now presented an in depth overview of slow wave teqniques, going from the work by Hasegawa et al. [HFY71] via periodic structures published by Kwon in 1991 to the more recent discussion on CMOS started by Cheung et al. [CLV+03]. Slow wave miniaturization is still an on-going research, the tradeoff between Q, ε_{eff}, α and Z_0 is far from trivial and most designs are based on simulation and guided by experience. To ease design, we will now investigate a mathematical model.

Chapter 4

Transmission line models

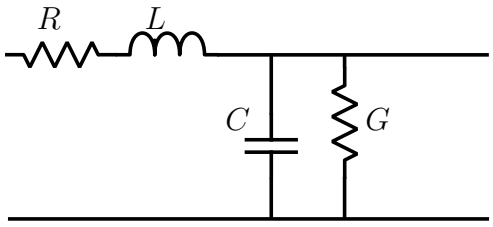


Figure 4.1: RLCG equivalent circuit for a short segment of a transmission line.

This chapter is devoted to different RLCG transmission line models. In this model R represent the resistance of the line, L the inductance, C the capacitance to surrounding media and G is leakage. Note that all these quantities are in units per meter; some authors distinguishes between lumped and per meter quantities by a R', but since we will almost exclusively deal with per meter quantities in this thesis the meaning should be clear from the context.

The literature provides a large number of RLCG models, which can be divided in two categories. The first category is based on *extraction*, either frequency dependent RLCG parameters are extracted directly from measurements (like in [EE92]) or a hypotheses is made by some least square error minimization.

We begin with a very simple model, where the main geometric dependencies are highlighted. We then improve the RL part by investigating different skin effect models in section 4.2, before we present a more advanced model. A quasi-empirical model is presented in the paper, given in chapter 7.

4.1 Parallel plate model

Below some physical intuition will be developed for the RLCG parameters, showing some simple qualitative formulas. The symbol $\propto$, which reads "proportional to" (not to be confused with the greek letter α), will be used to simplify the equations further highlighting the main geometric factors involved. The assumed geometry is shown in figure 4.2, where the metal is made of copper (conductivity of σ_{Cu}) and the substrate is slightly conductive. In the analysis edge effects are ignored, but the line is lossy (finite conductivity and thickness). The solution is given in most textbooks, so the mathematical details will be omitted (see for instance [LB09]).

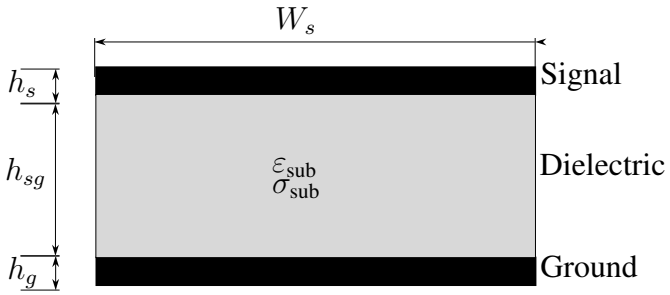


Figure 4.2: Assumed geometry for the parallel plate model. Two metal lines with conductivity σ_{Cu} are separated by a conductive substrate with relative dielectric constant ε_{sub} and conductivity σ_{sub}.

4.1.1 Resistance R

A copper wire with cross sectional area $A = Wh$, assuming uniform current density, will have a resistance inversely proportional to the width and thickness of the wire.

$$R_{dc} = \frac{1}{\sigma_{\text{Cu}} Wh} \propto \frac{1}{Wh} \tag{4.1}$$

with unit $[R] = \Omega/\text{m}$. Where copper conductivity $\sigma_{\text{Cu}} = 5.88 \times 10^7\,\text{S/m}$ [LB09, p. 60] is a material constant. If we assumed equal dimensions for ground and signal line, the total resistance is twice that of (4.1), but the ground line is usually made much larger than the signal and can therefore be neglected.

Manufacturing datasheets usually supply resistance value as sheet resistance in $\Omega/\square$, the corresponding conductivity can be found by multiplying the sheet resistance and the conductor thickness.

4.1.2 Inductance L

A time varying current will induce a magnetic field B, which in turn produces an opposing voltage. To model this, we define an inductance $IL \equiv \Phi$ with unit $[L] = \text{H/m}$. The magnetic field will behave differently inside and outside of the conductor, inside the field will be monotonically increasing due to the increase of enclosed current and on the outside the field will decrease. This lead to the inductance

$$\begin{aligned} L &= \Phi / I \\ &= \begin{cases} L_{\text{int}} = \frac{\mu_0}{8\pi} & \text{inside } h > h_s \\ L_{\text{ext}} = \frac{\mu_0 h_{sg}}{W_s} & \text{outside } h \leq h_s \end{cases} \end{aligned}$$

The total inductance is calculated as the sum of the internal and external inductance, but the internal inductance is usually much smaller in magnitude and is therefore usually neglected. It is included here since it is key to describe the skin effect in section 4.2. The above shows that inductance is proportional to the distance between the signal and the ground line. It should be noted that for other geometries, like two round wires, the inductance becomes $\propto \ln(h_{sg}/W_s)$.

In addition to this we need to account for any nearby conductors with time varying currents,

as these will induce a voltage on the wire of interest. This effect is modeled as a mutual inductance M. For two wires, mutual inductance on wire 2, caused by wire 1 is written as M_{12}. Whose sign is determined by the angle between current in wire 1 and wire 2, if the wires carry current in the same direction the mutual inductance is positive and if the current is opposite the inductance is negative. If however the current is perpendicular, the mutual inductance is 0, which was exploited in the previous chapter for the slow wave slots. In the same manner as Grover [Gro46], we can express the total inductance as

$$L_{\text{tot}} = L_{\text{int}} + L_{\text{ext}} + M_{+} - M_{-}$$

where M_{+} is the sum of all mutual inductances of same direction and M_{-} is the sum of any opposite currents. In transmission line applications the M_{-} term is mutual inductance caused by the return current and M_{+} is present if multiple parallel wires are used (for instance the ground return of a CPW line).

4.1.3 Capacitance C

The simplest formula for capacitance is for two parallel lines, the assumption being that the electric field is tangential to the plates.

$$C = \frac{\varepsilon W_s}{h_{sg}}$$

where the unit is $[C] = \mathrm{F/m}$.

4.1.4 Conductance G

Conductance G will contain any loss to the transmission line surroundings. While loss due to R will cause heating in the conductor itself, conductance will dissipate in the surrounding material. Though conductance will contain terms such as mode coupling and radiation (discussed in section 2.3.2 and section 2.3.3), the major term will be caused by the substrate. We have already seen that the loss tangent relate capacitance and conductance by $\tan\delta = G/(\omega C)$ so we can now write

$$G = \omega C \tan\delta = \frac{W_s}{h_{sg}}(\sigma_{\text{Si}} + \omega\varepsilon'') \approx \frac{\sigma_{\text{Si}} W_s}{h_{sg}}$$

where we ignore the polarization loss for now. Conductance has the unit of siemens, which is the inverse of ohm $[G] = /\Omega\mathrm{m} = \mathrm{S/m}$.

4.1.5 Summary

We are now in a position to discuss impedance and propagation constant in terms of fundamental geometric quantities, we simply insert our simple model into the equations given in section 2.2

and the rest is algebra. Starting with the characteristic impedance

$$Z_0 = \sqrt{\frac{R + j\omega L}{G + j\omega C}} \propto \frac{h_{sg}}{W_s}$$

This shows the difficulty discussed earlier when designing a high impedance microstrip line, where the signal width must be narrow for a given gap.

When doing the same for the propagation constant, a neat thing happens

$$\begin{aligned}\gamma = \alpha + j\beta &= \sqrt{(R + j\omega L)(G + j\omega C)} \\ &= \sqrt{\left(\frac{1}{\sigma_{\mathrm{Cu}}\cancel{W_s}h_s} + j\omega\frac{\mu_0 h_{sg}}{\cancel{W_s}}\right)\left(\frac{\sigma_{\mathrm{Si}}\cancel{W_s}}{h_{sg}} + j\omega\frac{\varepsilon\cancel{W_s}}{h_{sg}}\right)},\end{aligned}$$

and it is now independent of the signal width. One would assume that making the signal wider would reduce loss, but due to the linear increase in conductance the effect cancels out. In a "real" circuit things are not as neat, and we will return to a more realistic model at the end of this chapter. By simplifying further one can obtain

$$\propto \frac{\sqrt{\varepsilon_r}}{\sigma_{\mathrm{Cu}}h_s} + \frac{\sigma_{\mathrm{Si}}}{\varepsilon_r} + j\omega\sqrt{\varepsilon_r}$$

As expected, the phase constant β is proportional to the dielectric constant, while loss is inversely proportional to conductor conductivity and directly proportional to substrate conductivity. Of particular note is that the effective dielectric constant influences the loss per unit length, making α an inappropriate figure of merit for slow wave lines.

The major drawback of this model is the frequency response, where in real life R, L, C and G all vary with frequency. This represents a challenge for spice simulators, since they rarely allow passive elements to change value depending on frequency. Spice simulation is important for co-simulation and for delay and distortion estimation. Another reason for extending the RLCG model is that the underlying physics can become clearer. We will now extend the resistance and inductance model so that it includes skin effect, and also explore how the skin effect can be modeled with frequency independent components.

4.2 Skin effect

The assumption that the current is uniform is incorrect at frequencies comparable the conductor cross section, introducing the skin depth

$$\delta \equiv \sqrt{\frac{1}{\pi\mu\sigma f}},$$

results in the high frequency approximation [JG93]

$$R_{\mathrm{skin}} = \frac{1}{k_{\mathrm{skin}}(W + h)\sigma\delta} \propto \frac{1}{W + h}\sqrt{f} \tag{4.2}$$

where a frequency dependence of $\sqrt{f}$ is introduced. k_{skin} is an empirical constant having a value between 1 and 2. Note that (4.2) is only valid when $\delta \ll h$. To provide a wideband model we can either require $R_{\text{skin}} < R_{dc}$, which results in an asymptotic approximation. Johnson and Graham [JG93] suggests using the length:

$$R(f) = \sqrt{R_{DC}^2 + R_{\text{skin}}^2} \tag{4.3}$$

Comparing (4.3) (where $k_{\text{skin}} = 1.5$ was used) with the 2D field solver in Q3D for different values of W_s the relative error was found to be as high as $-20\,\%$ in the low to high frequency transition. For values $\delta \ll h$ and $\delta \gg h$ the error was less than $-7.5\,\%$. The error can be reduced by tuning k_{skin} for each line.

In figure 4.3 the resistance of a rectangular conductor with $W_s = 12\,\mu\text{m}$ and $h = 3.4\,\mu\text{m}$ is shown. Where it is clear that the skin effect is important for millimeter wave design.

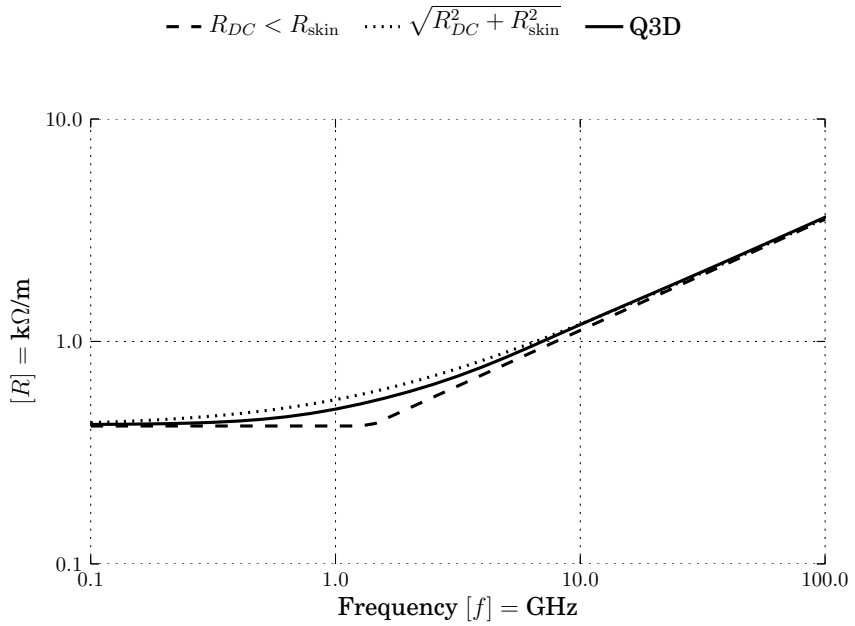


Figure 4.3: Comparing model with and without skin effect on resistance per meter. $W_s = 12\,\mu\text{m}$, $h = 3.4\,\mu\text{m}$.

Alternative formulations for the frequency dependent resistance uses either a field solver to determine empirical constants or the general Partial Element Equivalent Circuit (PEEC) method which, much like a field solver, discretizes the geometry and solves for each cell. To limit the scope of the thesis PEEC will not be considered in this thesis.

4.2.1 Skin effect by frequency independent components

The frequency dependent $R(f)$ models discussed above can not be directly inserted in a conventional spice simulator, the traditional solution is to use an RL ladder to "simulate" the current distribution as the frequency is increased. The model for this used by [WZY+11] and [PCCL06] is described by Kim and Neikirk [KN96] and applies to a circular conductor. The model promises to be both compact and accurate for a wide frequency spectrum.

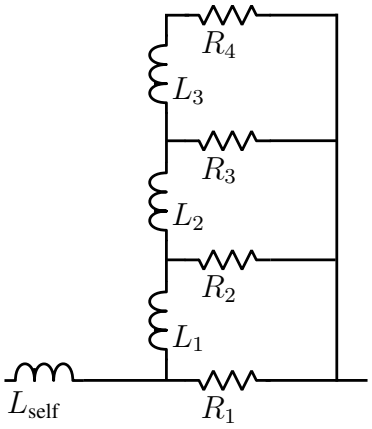


Figure 4.4: Four ladder skin effect model from [KN96]

The model is depicted in figure 4.4 for a four ladder case, if a wider frequency spectrum is wanted a larger number of "ladder steps" must be used. Using inductors we can steer the current through the different resistors based on frequency, at low frequencies the inductors will behave as shorts and the total resistance is the parallel connection of all of the resistors. As we increase the frequency large inductors will have a large impedance, blocking the current from entering a ladder. At sufficiently high frequency (f_{max}) all the current will go through the lowest ladder step (R_1).

The model components is found by $\frac{R_i}{R_{i+1}} = K_{RR}$ for $i = 1, 2, 3$ and

$$R_1 = K_R R_{\text{DC}}$$
$$K_R = 0.53\frac{R_{\text{skin}}}{R_{DC}}$$

Where R_{skin} is calculated at the highest frequency of interest f_{max}. The constant K_{RR} is found by solving the polynomial

$$K_{RR}^3 + K_{RR}^2 + K_{RR} + (1 - K_R) = 0 \tag{4.4}$$

which ensures that the resistance is equal to R_{DC} at DC. In a similar manner, the inductance can be found by $L_i/L_{i+1} = K_{LL}$ for $i = 1, 2$ and

$$L_1 = K_L L_{DC}$$
$$K_L = 0.315K_R.$$

To ensure L_{DC} at DC the constant K_{LL} must satisfy

$$K_{LL}^{-2} + \left(1 + K_{RR}^{-1}\right)^2 K_{LL}^{-1} + \left(K_{RR}^{-2} + K_{RR}^{-1} + 1\right)^2 - K_L\left(\left[1 + K_{RR}^{-1}\right]\left[K_{RR}^{-2} + 1\right]\right)^2 = 0 \tag{4.5}$$

The multiplication constant $0.315K_R$ have been found by the author to fit well for circular conductors. When using rectangular conductors [PCCL06] suggests using $0.2K_R$ instead. Note that the inductance is the *internal* inducance, in addition we need the *external* (self) inductance L_{self}. We must also supply the DC resistance R_{DC}, maximum resistance R_{skin}, low frequency

internal inductance L_{DC} and the maximum frequency.

As an example we consider a single wire with width $W_s = 12\,\mu\text{m}$, thickness $h = 3.4\,\mu\text{m}$ and $f_{\text{max}} = 100\,\text{GHz}$. For the DC and high frequency resistance we use (4.1) and (4.2) to obtain

$$\begin{aligned} & R_{DC} \approx 0.42\,\text{k}\Omega/\text{m} \\ \text{and} \quad & R_{\text{skin}} \approx 3.5\,\text{k}\Omega/\text{m}. \end{aligned}$$

The internal DC inductance is found from the empirical polynomial in [CF00] and self inductance is calculated by Grover [Gro46]

$$\begin{aligned} & L_{DC} \approx 0.044\,\mu\text{H}/\text{m} \\ & L_{\text{self}} = 0.2 \times 10^{-6}\left(\log\left(\frac{2l}{W+h}\right) + 0.50049 + \frac{W+h}{3l}\right) \approx 1.2\,\mu\text{H}/\text{m} \end{aligned} \tag{4.6}$$

we then obtain the ladder in figure 4.5 where $K_R = 8.51$, $K_L = 1.7$, $K_{RR} = 1.54$, $K_{LL} = 0.784$ and the skin depth at $100\,\text{GHz}$ is $t/\delta = 16$.

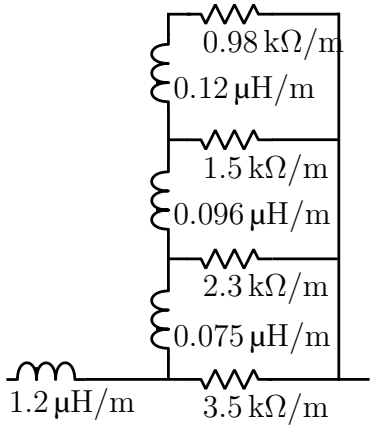


Figure 4.5: Four ladder skin effect model based on [KN96]

Resulting inductance and resistance of the ladder structure is shown in figure 4.6, where ladders with f_{max} equal to $25\,\text{GHz}$ and $50\,\text{GHz}$ is included for comparison. Also included is results from the 2D solver Q3D.

From the resistance graph we see that the ladder model is able to pass thought the supplied high and low frequency points. The maximum error when $f_{\text{max}} = 100\,\text{GHz}$ is as high as $-106\,\%$ and the resistance seems highly dependent on f_{max}. Only for f_{max} equal to $25\,\text{GHz}$ is the transition region accurately modeled for this case. Note that deviation for the $f_{\text{max}} = 25\,\text{GHz}$ model above $25\,\text{GHz}$ is expected, since the model only promises to be accurate between DC and f_{max}.

Inductance is dominated by the self inductance (which is orders of magnitude larger than the internal ladder inductance), so the accuracy of the inductance will be dominated by (4.6). But we can see good correlation between the frequency dependence of the Q3D simulation and the ladder model. For the $f_{\text{max}} = 100\,\text{GHz}$ case the inductance error is less than $-5\,\%$.

The model can be improved by tuning the empirical constants 0.53 and 0.2 or by tuning the inductance value. A general fitting procedure would then need the high frequency inductance;

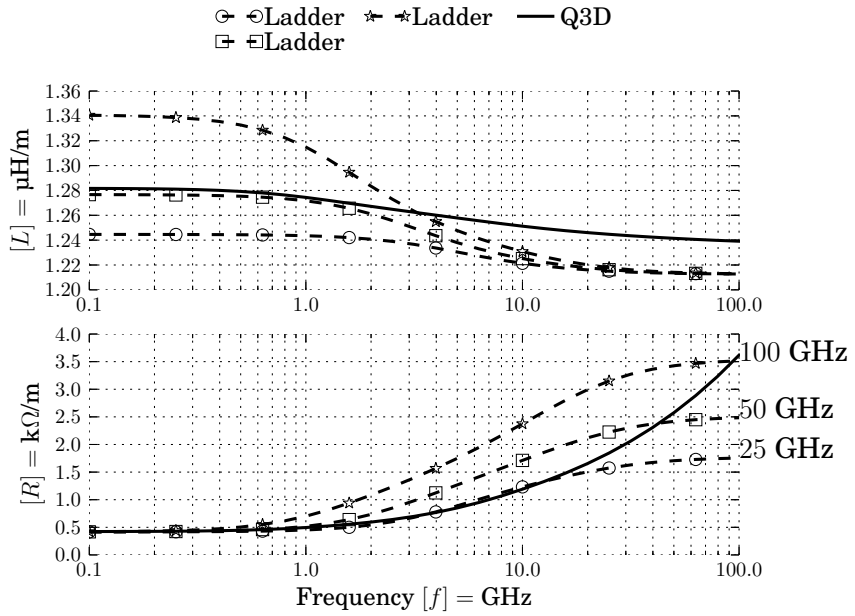


Figure 4.6: Modeling skin effect by 4 ladder network for different $f_{\max}$ values.

which is not trivial to compute analytically. This conclusion seems to agree with a similar comparison done by Mukherjee et al. [MWP04].

It should also be noted that the need for frequency independent components is decreasing due to the advancements in circuit simulators. Since most simulation environments, both commercial like Cadence and ADS and open source tools like Qucs, support using S-parameters directly as circuit blocks for both frequency and time domain analysis. Of course, this reduces physical insight and increases computational time due to the inherent inverse Fourier transform.

4.3 Analytic conformal mapping

An attempt was made to repeat the work of [WZY+11] as their results seemed promising, covering a large number of configurations. The work does however not seem adequately documented and a surprising amount of empirical relations are utilized; without adequate empirical evidence. Deriving empirical models for on chip transmission lines would require a very large set of transmission lines of different dimensions (width, gap, height and thickness), which is not feasible due to the large area such a test chip would need. In addition, since manufacturing processes differ, one would need chips from multiple process families. Since [WZY+11] is based on measurements from a $65\,\mathrm{nm}$ technology there is no way of knowing how the presented model fit with the technology in this thesis.

Instead the analytic model from Heinrich [Hei93] is used as a basis. The G and C part of the model is slightly improved in [BVM10], where the equivalent circuit now looks more like the one proposed by Hasegawa et al. [HFY71] for the quasi TEM mode.

The model is quite extensive, so a full description will not be given, my implementation is available[1] where the discussed model can be found between line 474 and 709. The geometry

[1] `www.ob.cakebox.net/masterThesis/src/tlModels.py`

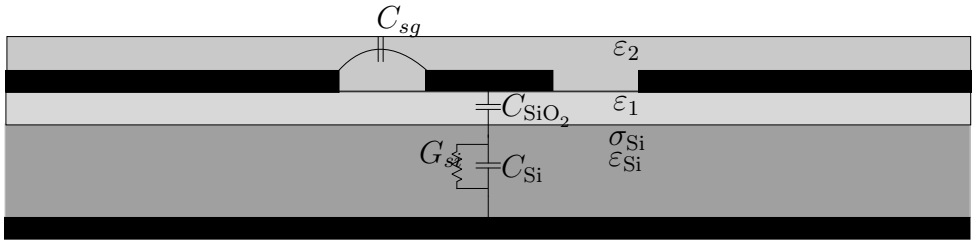


Figure 4.7: Geometry and equivalent circuit for the CPW model presented in [BVM10]. Not to scale.

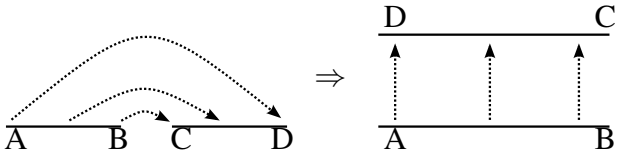


Figure 4.8: Example of conformal mapping, for the upper capacitance of two parallel lines. Adapted from [MKC+03].

is shown in figure 4.7 and consists of a CPW submerged in two layers of dielectric material, above a conductive silicon substrate.

The signal ground capacitance C_{sg} is found by conformal mapping. The conformal mapping technique is widely used to characterize capacitance of a coplanar line and can even be applied for multilayered substrates [GLK95]. The idea is shown in figure 4.8, where the leftmost geometry is transformed to the parallel plate version on the right. For a multilayered CPW, a similar set of transformations are used and this is applied for each layer, and the results are summed. G is found by the expression presented in chapter 2, namely (2.11), where $\varepsilon''/\varepsilon'$ was presented in section 3.3.1.

Resistance and inductance is modeled in three regions, DC, high frequency and a transition region as presented in [Hei93]. The proximity effect is modeled and the model is forced to have a continues derivative.

4.3.1 Results and comparison

Instead of focusing on the implementation the results will be presented and compared to both the simple model we started this chapter with, simulation results and measurements. Note that simulation and measurements are the topics for the next two chapters and will be described in more details there.

We start by varying the signal width W_s, with G_{sg} and W_g fixed at $10\,\mu\mathrm{m}$ and $54\,\mu\mathrm{m}$ respectivly. The resulting RLCG values are shown in figure 4.9. In accordance with our intuition, as the signal is made wider the resistance decreases and inductance increases. Due to the larger area, capacitance increases and there is a slight increase in G since we couple more to the substrate. The net effect of increased capacitance and decreased inductance is a decrease in characteristic impedance, being $65\,\Omega$, $54\,\Omega$ and $44\,\Omega$. In contrast to the MS line discussed earlier, conductance of the CPW shows a much smaller dependence on signal width. This is reasonable since the fields are confined in the signal ground gap; and as we will see next, increasing the gap has a large effect on G.

In figure 4.10, the signal width is fixed to $W_s = 12\,\mu\mathrm{m}$, and the signal ground gap G_{sg}

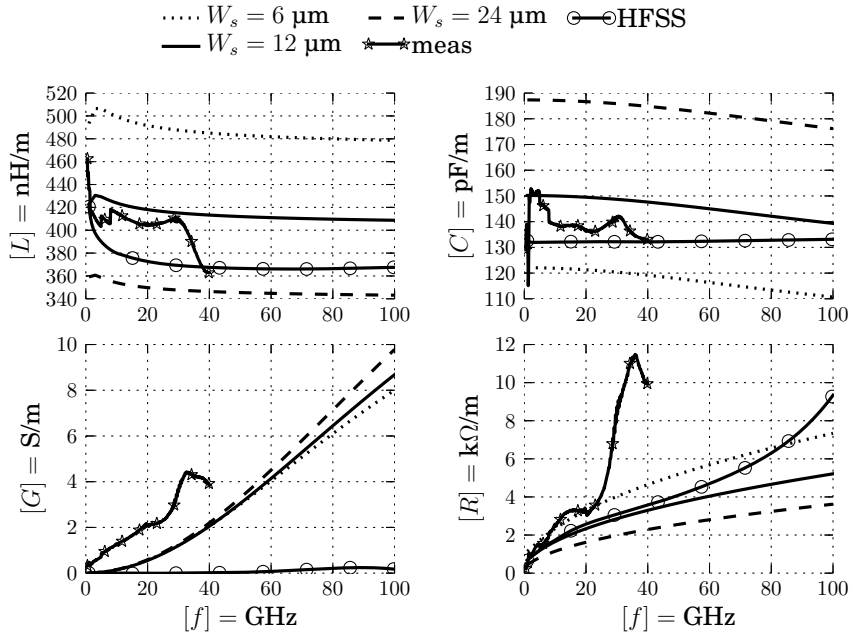


Figure 4.9: Modeled RLCG parameters for an unshielded CPW with varying signal width, simulation and measurements are for the $W_s = 12\,\mu\mathrm{m}$ line and the other parameters are $G_{sg} = 10\,\mu\mathrm{m}$ and $W_g = 54\,\mu\mathrm{m}$.

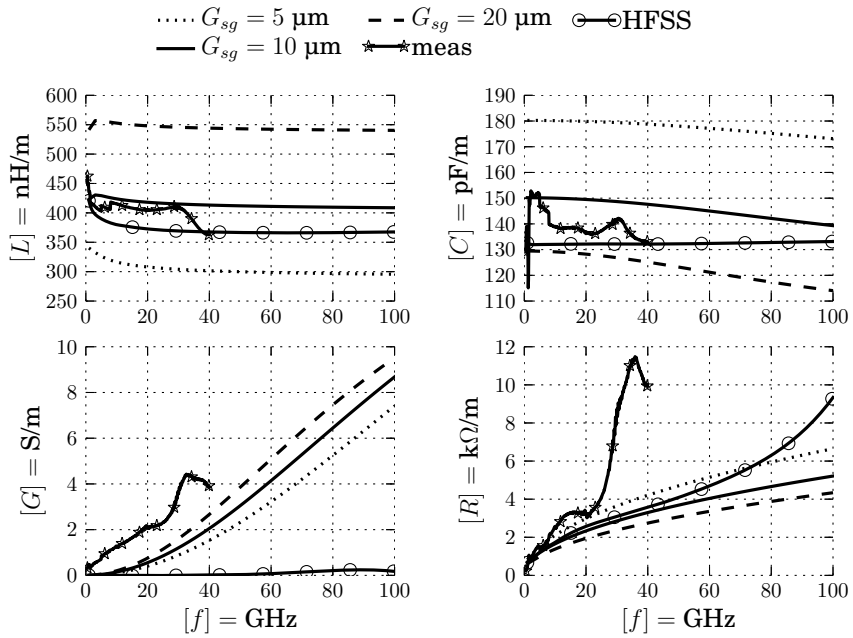


Figure 4.10: Modeled RLCG parameters for an unshielded CPW with varying signal ground gap, simulation and measurements are for the $G_{sg} = 10\,\mu\mathrm{m}$ line and the other parameters are $W_s = 12\,\mu\mathrm{m}$ and $W_g = 54\,\mu\mathrm{m}$.

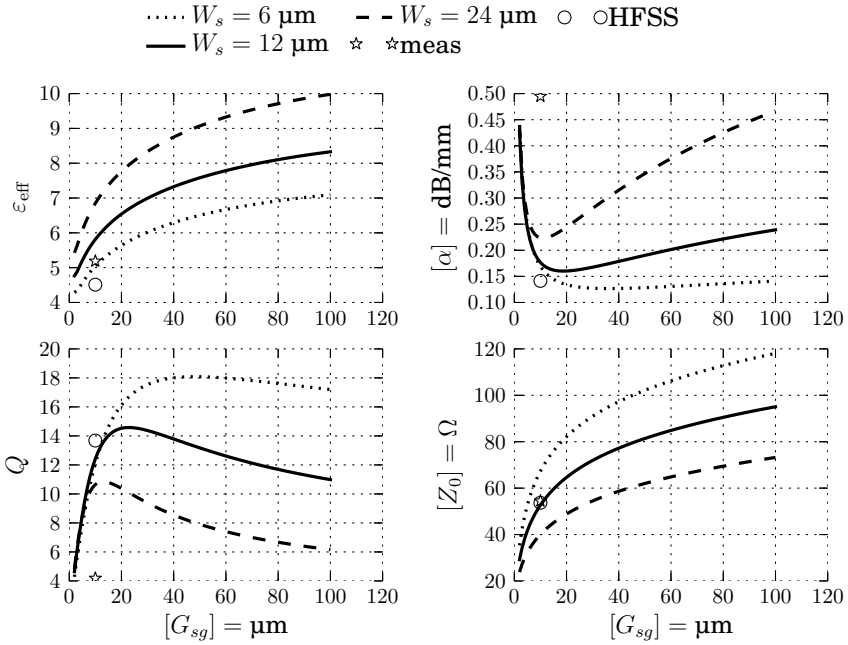


Figure 4.11: Performance characteristics as a function of gap spacing for different signal widths. Showing effective dielectric constant, loss per unit length, Q and Z_0 at $10\,\mathrm{GHz}$. Note: x-axis is *not* frequency.

is increased from $5\,\mu\mathrm{m}$ to $20\,\mu\mathrm{m}$. As the distance is increased inductance increases, and as in the parallel plate model capacitance decreases. This leads to an increase in characteristic impedance, being $41\,\Omega$, $54\,\Omega$ and $68\,\Omega$.

Sweeping both parameters, figure 4.11 is obtained at $10\,\mathrm{GHz}$. From the loss, the tradeoff between metal loss and substrate loss is apparent. For a larger gap spacing the total loss increases with increasing signal width and only slightly with gap, due to the large coupling to the substrate. With gap spacing below $10\,\mu\mathrm{m}$ the proximity effect forces more of the current to the sidewalls, thereby decreasing resistance rapidly with increasing gap. As a result of the large substrate loss at large gap spacings, the highest Q is obtained for the narrowest line.

4.4 Modeling slow wave lines

The above model assumes there is no shielding between the CPW and the silicon substrate, when adding a shield the only change is in the CG part. To model the change in capacitance per unit length, the signal to ground capacitance C_{sg} shown in figure 4.7 is kept, while the lower portion is replaced by either C_{slot} or $C_{\text{slot}} \parallel C_{\text{slot}}$ depending on whether the slots are floating or grounded respectively (see the discussion around figure 3.17, page 29). Formulation of C_{slot} is given in the publication as (7.4), and is just a weighted parallel plate formulation. As will be shown in the measurement chapter, very good agreement is obtained between model C and measurements when the slots are close to the signal line (relative to gap spacing).

For grounded slots conductance is modeled as capacitive coupling to resistive slots, that is

$$R_{\text{slot}} = \frac{R(W = W_{\text{slot}},\, h = h_{\text{slot}},\, l = l_{\text{slot}}/2,\, f)}{W_{\text{slot}} + G_{\text{slot}}}$$

where $R(\dots)$ is from (4.3). The series connection

$$Z_{\text{slot}} = R_{\text{slot}} + \frac{1}{j\omega C_{\text{slot}}}$$

can then be used to extract $G = \Re(1/Z_{\text{slot}})$. Unfortunately the above does not seem to agree with measured results, showing orders of magnitude lower conductance then measured values. A more realistic model must include

- Partial electric loss to the substrate due to incomplete shielding
- Magnetically induced eddy currents in the substrate.
- Eddy currents in the slots.

where it is believed that the last term is the most significant, see for instance [FPGF12].

We will do a proper comparison in chapter 6, where we will show that the capacitance and inductance is well modeled. Leading to accurate estimates for ε_{eff} and impedance Z_0.

4.5 Designing a slow wave transmission line on CMOS

We now have all the tools we need for setting up a simple design guide for slow wave transmission lines. The assumed task is to design a high Q line with a given characteristic impedance and electrical length (phase shift).

1. Start with the effective dielectric constant. First check if a floating slotted shield will meet the design criteria, remember that by moving the slots closer to the signal line you increase the effective dielectric constant. If the line is still to long, ground the slots, but remember that this might increase loss.

2. Use the width and gap to design the wanted characteristic impedance. This isn't trivial, since constraints on density and minimum feature sizes limit the options. In addition, by increasing the gap you increase the effects of the slots (not modeled above) and by decreasing the signal width or by making the gap too short you increase loss.

If the line is still too large, try the published comb structure in chapter 7. It may sound strange to not immediately use the highest possible slow wave factor, but keep in mind that by creating a large C, L must be compensated for a given Z_0. Since neither reducing W_s nor increasing G_{sg} (to achieve a higher Z_0) is desirable a decent value of ε_{eff} must be used. In addition, particularly when designing filters you may end up with lines that are physically very short, making them impractical and unreliable.

Part II

Practical aspects

Chapter 5

Simulation

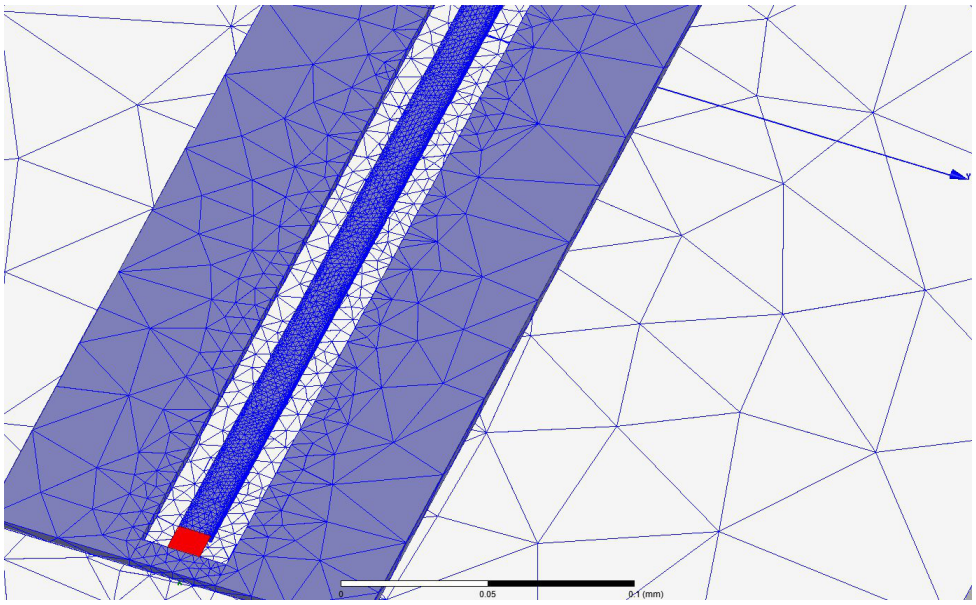


Figure 5.1: Example of adaptive meshing in HFSS. Red rectangle is a lumped gap port

We begin this chapter with some simulation theory and practical guidelines, in section 5.2 some necessary assumptions and simplifications are discussed and in section 5.3 selected simulation results are presented. Some concluding remarks are given in section 5.4.

5.1 Theory

Giving a detailed mathematical description of the utilized EM software is way outside the scope of this thesis, but some thoughts and motivation is given in this section.

Getting closed form solutions for complex EM problems can range from hard to impossible. But as any problems becomes easier when dividing into smaller pieces; so does solving Maxwell's equations. We have already applied this when developing models in chapter 4, where we first divided the problem into two independent parts, the RL and the CG section.

There are different ways of categorizing EM software, the most intuitive being the number of dimensions. There are 2D, 2.5D and 3D solvers available and the main trade-off should be obvious, more dimension increase computation time but also enable more complex geometries and effects. The 2D approach has usually been sufficient for transmission line design, where only the cross section is considered. In fact, most of the models in the previous chapter was

based on this assumption. But with the introduction of a periodic structure, like the slow wave slots, this method is no longer suitable.

By using a layered geometry, where the boundaries are either closed or "open" (infinitely far away), half a dimension is added. In this 2.5D method, current is restricted to two dimensions, while fields may extend in the third. This type of simulation is usually based on the Method of moments (MoM), and should be well suited for the layered CMOS stack or a PCB. On the other hand, [HK08] does not recommend MoM for tightly coupled conductors and problems with multiple modes, making it unsuitable for CPW simulation.

A full 3D method based on the Finite Element Method (FEM) is the most general tool (sledgehammer) for solving EM problems. Instead of meshing only the boundaries as in MoM, the entire volume is divided into tetrahedra and the fields are approximated to a low order polynomial inside each tetrahedron. In terms of memory usage, both MoM and FEM rely on storing the problem in memory as a matrix, the problem is then solved using techniques from linear algebra. According to [HK08], MoM solvers tend to create smaller but denser matrices than FEM which is capable of creating large but sparse matrices. An optimized FEM code can therefore outperform a MoM solver, but this is very application dependent.

The choice of tool is unfortunately limited to the tools available to me, which is ANSYS HFSS™ and Agilent ADS™, implementing FEM and MoM respectively. Some initial comparison was done and ADS came out as unstable and unreliable as a host of technical problems where encountered. The same layout, or slight variations, yielded different results that sometimes conflict with basic laws of physics; like the speed of light or conservation of energy (amplification though a passive device). It should be noted that a software update fixed some of these issues and that part of the problems was caused by a full home directory.

In addition, subjective factors like usability, documentation and graphical features are important when choosing software, my comparison is as follows:

- I know HFSS better and its better documented.
- Debugging a run away HFSS model is simpler, reported data about mesh and the number of options to tune are invaluable.
- Adaptive mesh in HFSS seems more reasonable than in ADS.
- HFSS's field and current visualizations (and export) options are essential for increased design insight.

The final choice of software and the superior results from HFSS has of course nothing to do with the fact that FFI (where I use HFSS) offers free coffe while IFI (where I use ADS) does not. A more objective comparison is done in the next section.

5.2 Simplifications and vertification

Ideally a simulator will reflect every aspect of the real world, this is of course not possible, so some simplifications must be applied. We will first explore the dielectric stack-up, as discussed in the introduction in chapter 3, a modern CMOS process has many thin layers of dielectric material and this presents a challenge to the simulator. Section 5.2.1 is therefore devoted to this

stack-up and also compares results from HFSS with ADS. In section 5.2.2 a novel approach to reduce a long transmission line into very short segment is explored.

5.2.1 Number of dielectric layers

A modern CMOS stack-up usually consists of a large number of dielectric layers situated between the various metal layers. These are added both as mechanical spacers and for electric isolation between different layers. Finite element methods are unsuited for this configuration as large thin layers requires a huge amount of mesh cells, resulting in long simulation time and large memory requirements.

To reduce the number of layers we can use the parallel plate formula to calculate an effective height and an effective dielectric constant.

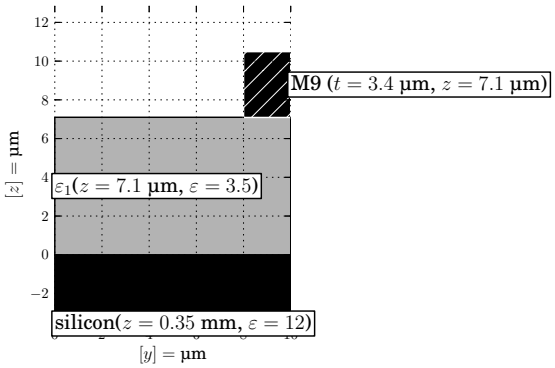
$$h_{\text{eff}} = \sum_i t_i$$
$$\varepsilon_{\text{eff}} = \frac{h_{\text{eff}}}{\sum_i (t_i/\varepsilon_i)}$$

Where the assumption is that the electric field is vertical, which is clearly not always the case, especially for a CPW.

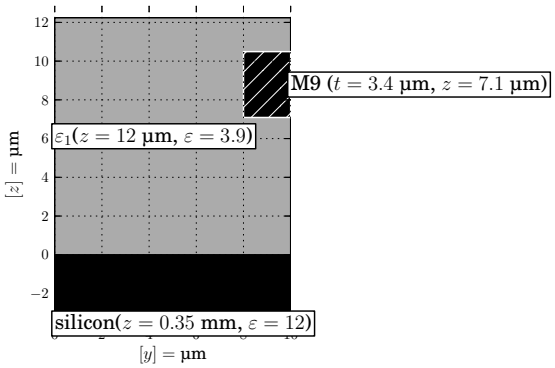
In figure 5.2 four different stack-ups are shown, consisting of silicon, different number of dielectric layers and the top metal layer. All are based on the $90\,\text{nm}$ process from TSMC. Figure 5.2a shows the typically assumed stack-up for some theoretical models where the metal is assumed to lie in air, this structure resembles conventional PCB design. A more realistic version is shown in figure 5.2b, where the transmission line is fully submerged in a uniform dielectric layer. This is likely to show less dispersion since the environment above and below the line is the same. The last two shows two and nine layers respectively, which are the ones we will focus on in this thesis.

Table 5.1: Different dielectric setups for HFSS (see figure 5.2) and waveport vs lumped port (lumped unless otherwise stated), compared to ADS and measurements. For a CPW without shield, showing maximum memory and computational time where available.

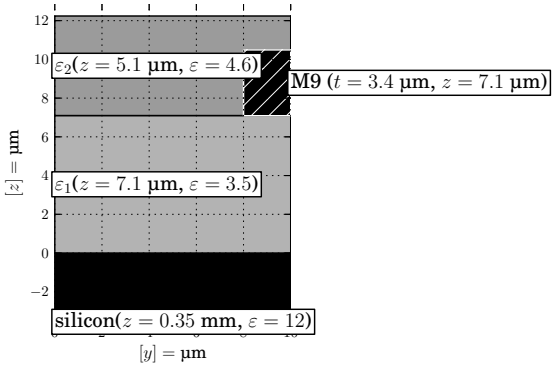
Name	Z_0 Ω	L nH/m	C pF/m	G S/m	R kΩ/m	CPU time h	Max mem. GiB
Meas.	52.2	363	133	3.86	9.92	-	-
D1-top	66.7	351	79.0	0.0201	3.54	0.121	0.468
D1	58.5	356	104	0.003 10	4.07	0.240	0.926
D2	58.4	375	110	−0.0274	3.74	7.42	12.8
Waveport D2	57.9	372	111	0.001 67	3.54	10.1	14.4
D9	52.7	368	132	0.0109	3.56	24.2	11.7
D9 ADS	58.4	367	108	0.442	0.966	-	-



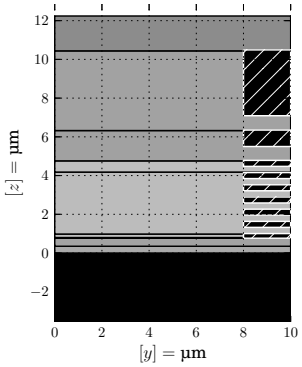
(a) Single layer, PCB style (D1-top).



(b) Metal submerged in single dielectric (D1).



(c) Two dielectric layers (D2).



(d) Nine dielectric layers and all metal layers, labels not shown (D9).

Figure 5.2: Simplified dielectric stack-up of a CMOS process, cross sectional view. Showing dielectric layers and some metal layers. Short names for each stack-up is shown in parenthesis.

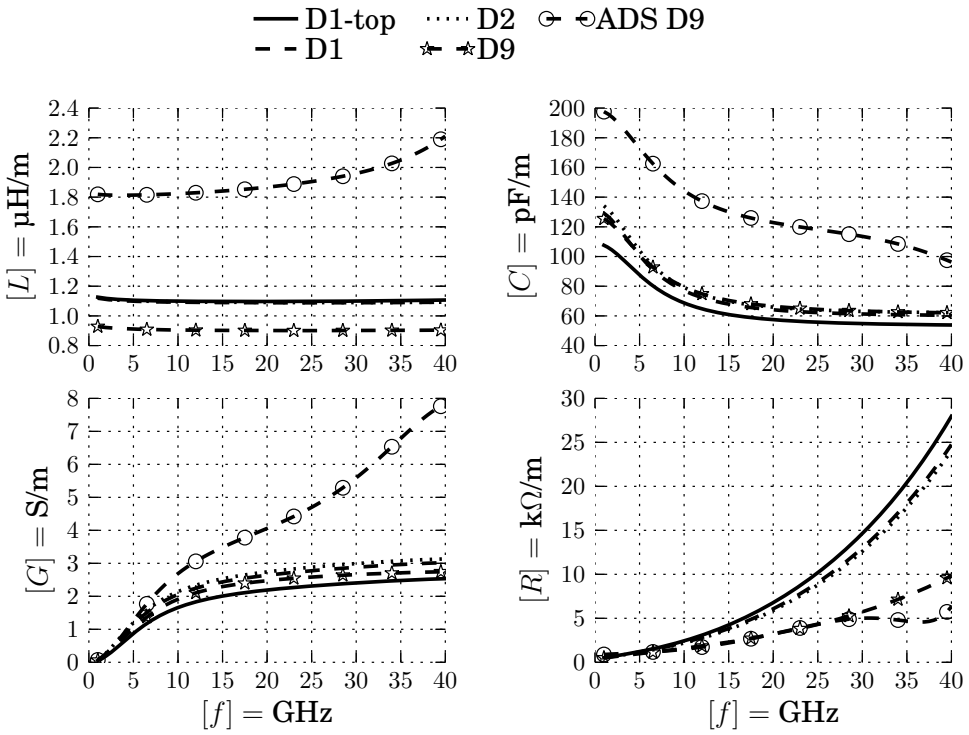


Figure 5.3: HFSS simulation of microstrip line with ground below the substrate and different dielectric configurations, ADS simulation with D9 is included for comparison.

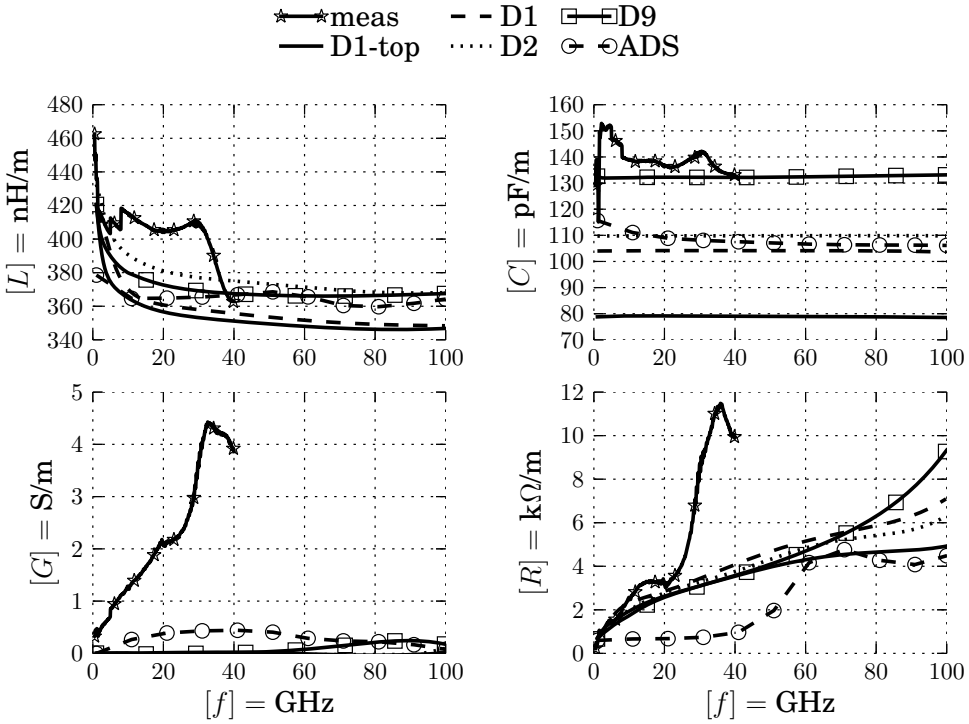


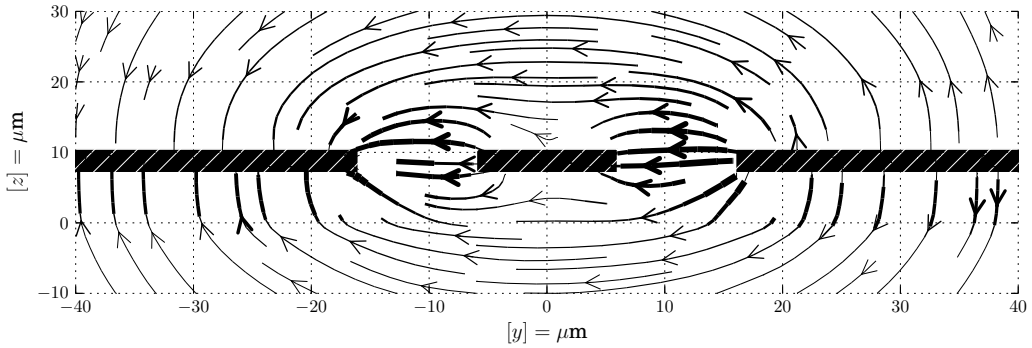
Figure 5.4: HFSS simulation of CPW with different dielectric configurations, ADS simulation with D9 and measurements are included for comparison.

The different stackups are compared for both a MS configuration with ground return in the lowest metal layer and a CPW without shield. The MS results are displayed in figure 5.3, the ADS results indicate an effective dielectric constant of 20, while HFSS lies around the more reasonable value of 5. Table 5.1 and figure 5.4 shows the CPW results, where consumed memory and CPU time is also included. The observant reader may find a CPU time of $24\,\mathrm{h}$ excessive, but due to the beauty of parallel processing the elapsed time is closer to $4\,\mathrm{h}$.

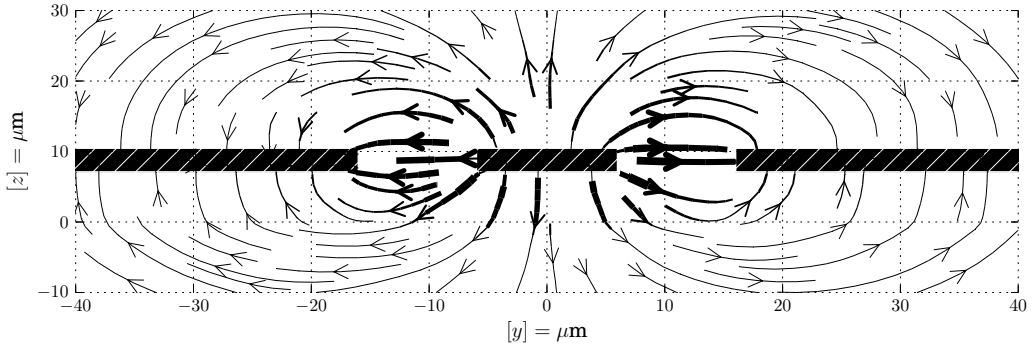
5.2.2 Unit cell

In [VRE+09b], Vecchi et al. presents a novel technique for simulating on chip transmission lines, instead of simulating an entire transmission line the inherent periodicity is exploited. The traditional way of simulating a transmission line in HFSS is to draw a long line, then excite the line by either a wave or a specified voltage difference (called wave port and lumped port respectively). The lumped version is shown as the chapter image in figure 5.1, where an arbitrary voltage of $1\,\mathrm{V}$ is applied between the ground and signal line. This is the intuitive circuit approach to the problem and is the one we will rely on in this thesis.

The method presented by Vecchi et al. instead relies on an eigenmode solution; where, as in linear algebra, the final solution is viewed as a weighted sum of eigenvectors (modes). One then draws a small unit cell (say $d = 1\,\mu\mathrm{m}$ in length) and then tells the solver that there should be a phase shift of $\theta = \omega\sqrt{\varepsilon_r}d/c$ between each end of the cell. No information is given to the solver about the applied voltage, and theirin lies the rub, because in most of my attempts



(a) 1st mode $(9.48 + 0.164\mathrm{i})\,\mathrm{GHz}$, $Q = 29$ and extracted impedance $(2500 + 560\mathrm{i})\,\Omega$.



(b) 2nd mode $(10.1 + 0.390\mathrm{i})\,\mathrm{GHz}$, $Q = 13$ and extracted impedance $(-63 + 5.6\mathrm{i})\,\Omega$.

Figure 5.5: Electric field lines for two modes when using the eigenmode solver in HFSS, thicker line correspond to greater field magnitude.

Listing 5.1: Pseudo code for solving the unit cell using HFSS eigenmode solver.

```
for each frequency f:
  ε_r = 4 # Inital guess
  while iteration is < max: # prevent ∞ loop
    θ = 2πf√(ε_r)d/c # Required phase shift
    f̂ = HFSS(θ) # Returns lowest mode

    ε̂_r = (θc/(2πf̂d))^2 # new value
    if |ε_r − ε̂_r|/ε_r < 1%: # if close to old one
      goto next frequency
    else: # try again
      f = f̂
      ε_r = ε̂_r
```

the solver gives a higher voltage on the ground lines than the signal line. This can be solved by simply swapping the sign of the calculated impedance (which comes out negative), but the tricky part, which is not discussed in [VRE+09b], is that HFSS gives you multiple modes, but not the weights.

Usually the lowest mode gives a mode which is reasonable, except for the sign mentioned above. But sometimes, some really strange modes appear, figure 5.5 shows the electric field from a "reasonable" mode in (a) and a "strange" mode in (b).

Another challenge with the discussed method is that as input, you must specify not only a frequency (which is natural), but also the effective dielectric constant. This defeats the purpose, since especially for slow wave lines, the effective dielectric constant is the main parameter of interest. With this in mind, and also noting that Vecchi et al. mentions "iterating", the algorithm in listing 5.1 was written. To automate the process, this was implemented in an IronPython HFSS script, which worked but with the major issue mentioned above. A typical iteration could for instance give the effective dielectric values of $[4, 4.2, 4.294, 1000, 1001, \ldots]$.

The critical piece to get listing 5.1 to work is the call $\hat{f}$ = **HFSS**(θ) to return the "reasonable" mode, instead of the lowest mode. One might think that the lowest mode is the correct one and that the problem lies with the drawn geometry[1], but what figure 5.5 doesn't show is where the current flows. In the bottom figure, currents flow *out* of the page in the middle (signal) line and *into* the page in the ground lines (as it should); but in the top figure the signal lines carries current both *into* and *out* of the page, which is clearly not what happens if we apply a voltage difference between the ground and signal line.

One odd observation is that the "reasonable" mode has, in all simulations that I have done, the lowest Q factor. This could be used as a reliable criteria for choosing the correct mode. But there remains some technical challenges as to how this can be automated. Some manual iterations where carried out, where the extracted characteristic impedance, loss and phase showed good agreement with other published work and simulations and measurements done in this thesis.

[1] or the dense master student

5.3 Results

This is not the best named section title, since we have already covered a lot of simulation results, but this section covers results for a tunable line in subsection 5.3.1 and shielded lines in subsection 5.3.2.

5.3.1 Tunable line, passive and active co-simulation

Presented here is the simulation setup for the tunable CPW transmission line. The line is made tunable by using MOS transistors to electrically tune the slow wave slots, this creates a "Digital controlled artificial dielectric" first published by Huang et al. [HHW+06] as part of a Voltage Controlled Oscillator (VCO). The proposed structure (see figure 5.6) is similar to [SXH+10], but uses a variable capacitor (varactor) structure instead of a variable resistor.

In [SXH+10] a tunability of $\varepsilon_{\text{eff}} = [13.2, 14]$ is reported for a CPW, while the coplanar stripline in [LTH+08] can be tuned from $\varepsilon_{\text{eff}}(60\,\text{GHz}) = [10.8, 79.9]$, where all values are at $60\,\text{GHz}$.

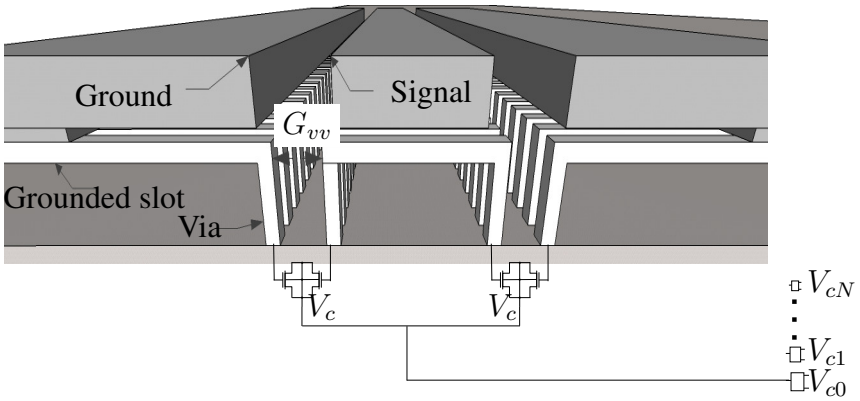


Figure 5.6: Varactor tuned CPW, cross section. Slots are placed on M8 and broken, all N slots are connected to individually controlled varactors.

To simulate transistors in HFSS, one possible option is to use the "lumped RLC" boundary condition to represent the varactor. We then need a frequency independent assembly of R, L and C which can be drawn as rectangles in HFSS with the appropriate boundary condition. After an initial transistor simulation the empirical RLC model in figure 5.7 was chosen.

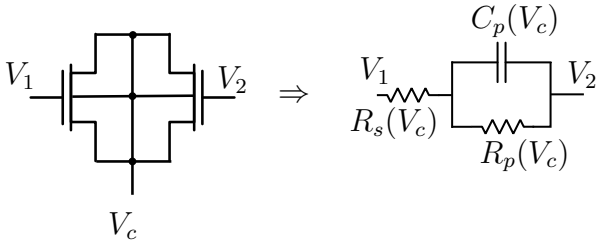


Figure 5.7: RLC model for varactor, C_p represents the tunable capacitor while R_s and R_p are parasitic components.

The Virtuoso simulation of the layout (after layout and parasitic extraction) of the varactor structure with width $120\,\text{nm} \times 5$ and length $500\,\text{nm}$ are shown in figure 5.8 together with the

extracted model. The resulting values are shown in figure 5.9, where the HFSS simulation was first run with all the varactors "on" and then all "off".

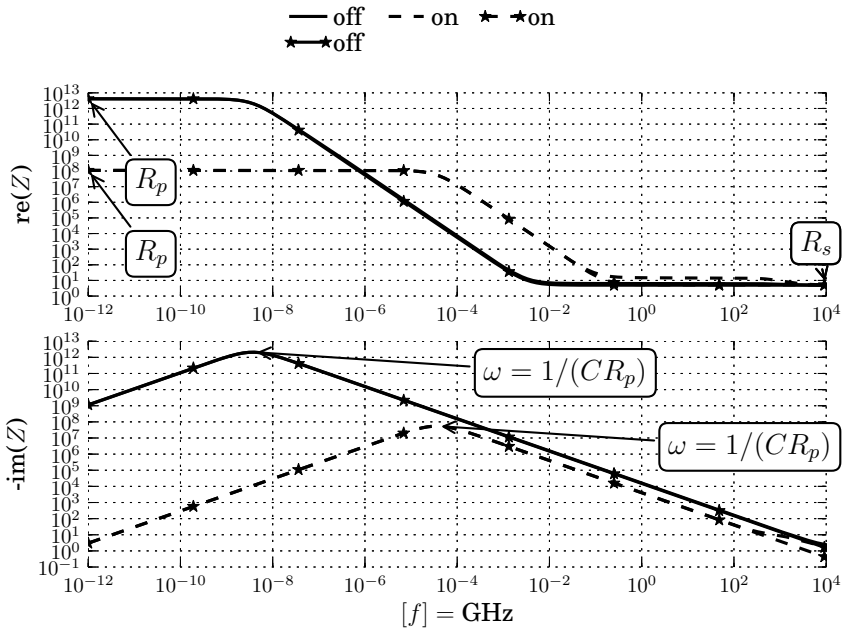
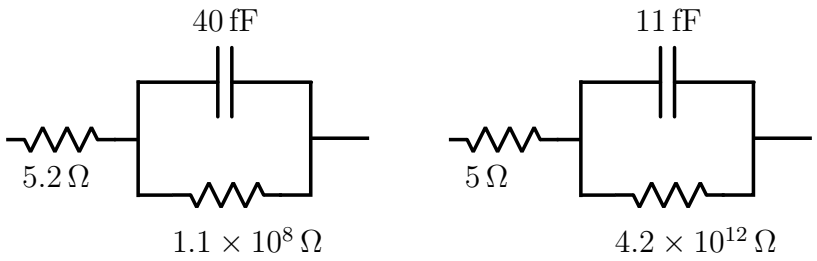


Figure 5.8: Impedance of varactor by Cadence simulation and extracted RLC model.



(a) On ($V_c = 1.2\,\mathrm{V}$) (b) Off ($V_c = 0\,\mathrm{V}$)

Figure 5.9: Extracted RLC values of simulated varactor.

Figure 5.10 shows the resulting ε_{eff}, where at $30\,\mathrm{GHz}$ simulation indicate a tunability of $[40.6, 39.1]$ while measurements show $[35.0, 34.8]$. It should be noted that an initial simulation using ideal open and short conditions (i.e. by either replacing the lumped impedances representing the transistors by a perfect conductor or removing them) a tunability of $[19.3, 10.9]$ was found, where the lower absolute values is due to a smaller gap spacing.

Further work is obviously needed, especially on the transistor modeling and design. The model presented above is clearly nonphysical, since no inductive term appears even above $100\,\mathrm{GHz}$ (not shown). It should also be noted that to date, the largest tunability published is for a CS line and not a CPW as attempted here.

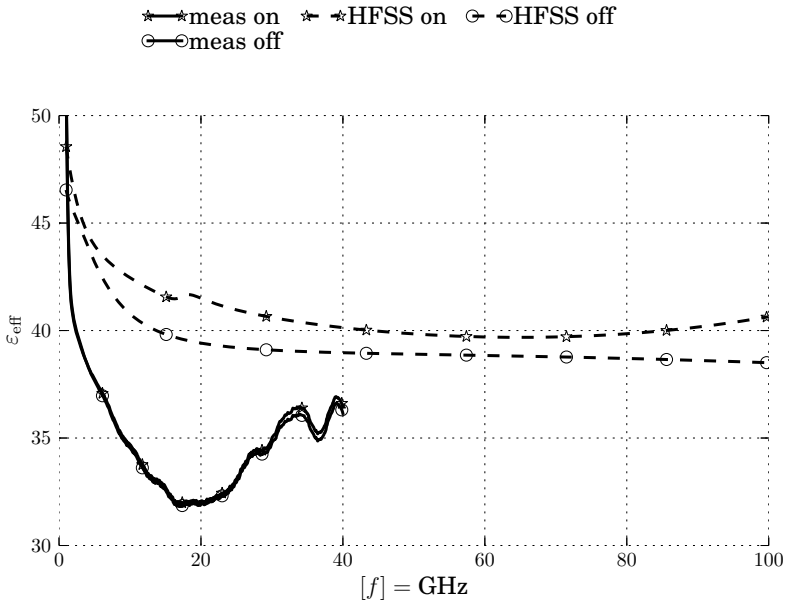


Figure 5.10: Effective dielectric constant of tunable CPW line, comparing measurements and simulation.

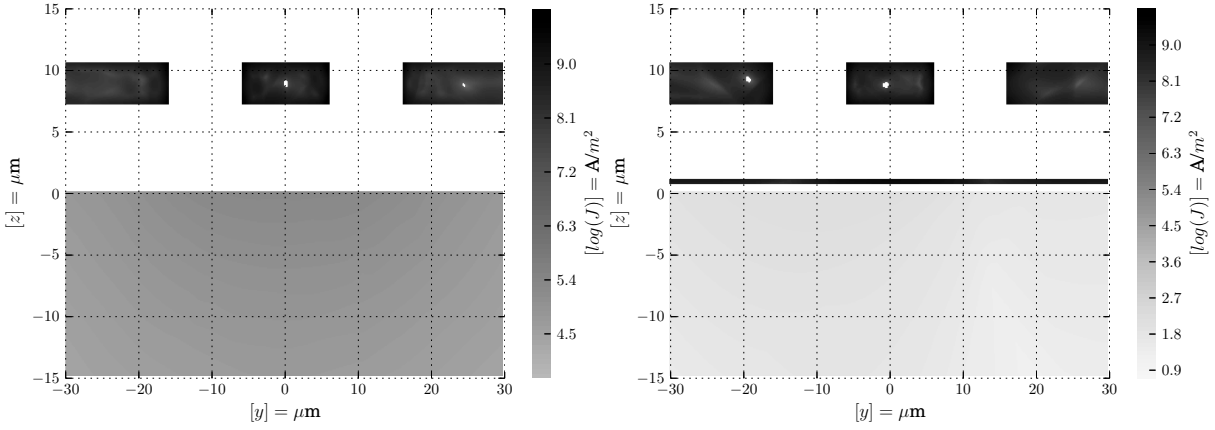
5.3.2 Shielding a CPW

By adding a continuous ground layer between the CPW and the lossy silicon substrate, loss is reduced as long as the metal loss from the shield does not exceed substrate loss. In this section we will explore a few different ways of shielding a CPW line from the substrate.

For low loss interconnect, [KJCH04] makes the observation that a grounded CPW has lower resistance due to the proximity effect pushing the current more evenly in the signal conductor. HFSS simulation of the structures proposed in [KJCH04] is shown in figure 5.11d), c) and f), where the current density on a cross section is shown. Also shown for comparison is a standard CPW without shield, and a floating shield in the lowest metal layers (M1) and M8. It should be noted that the unshielded line has a much higher current density in the substrate than the shielded lines. The white spots in the conductors is due to a current density of $< 10^{-15} \approx 0$, which the log function does not appreciate.

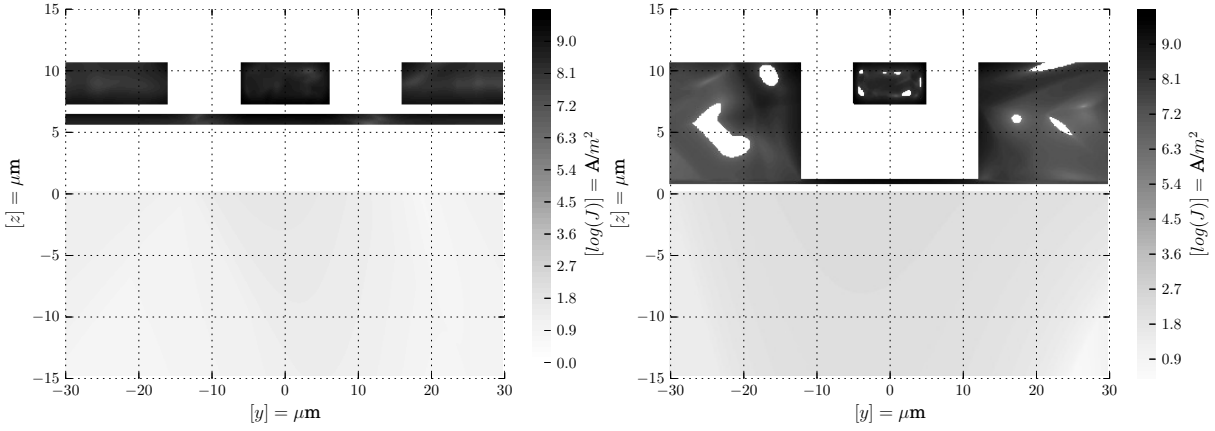
The extracted RLCG values for a $500\,\mu\text{m}$ long line (not deembedded) is shown in figure 5.12. As expected, the unshielded CPW shows the highest G and the lowest C. By adding a shield, C is increased and L is decreased.

The new structures, rectangular, circle and V shaped does not provide any reduction in loss compared to the simpler floating M1 shield. The only advantage is not investigated here, but it is reasonable to assume the new structures have lower coupling to neighboring circuits, as the fields are well confined. Note that the lines are not optimized, so performance might be improved by careful design, for instance the lowest metal layers is quite thin, so using multiple layers might help.



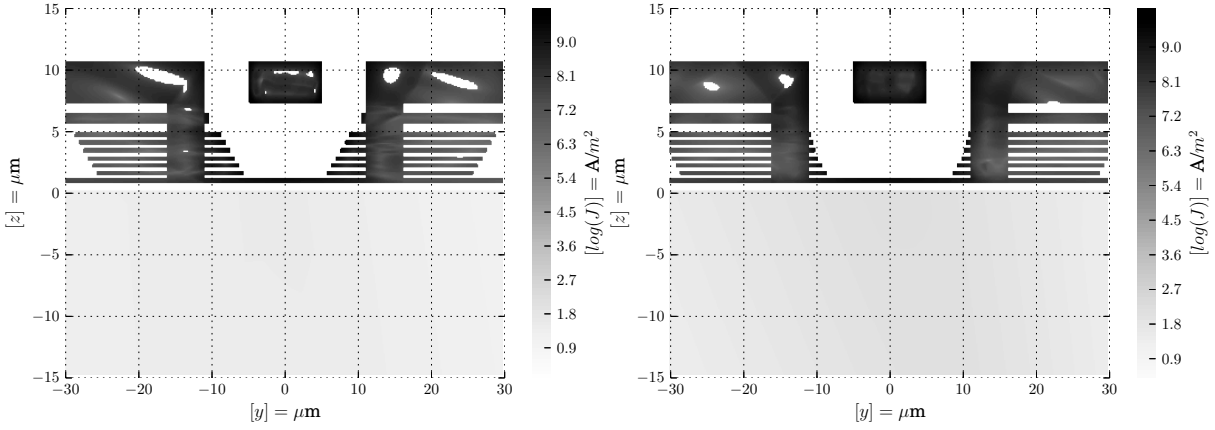
(a) CPW.

(b) CPW shield M1.



(c) CPW shield M8.

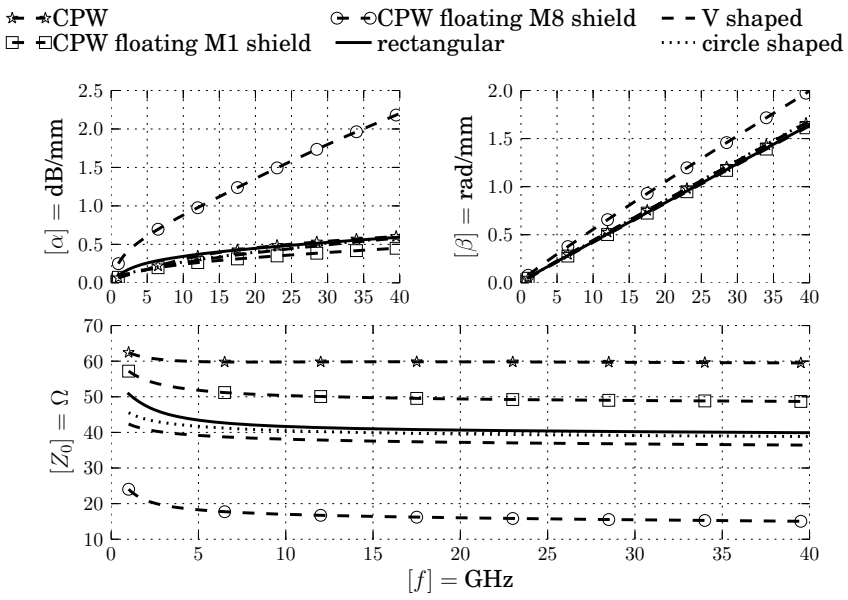
(d) GCPW rectangle.



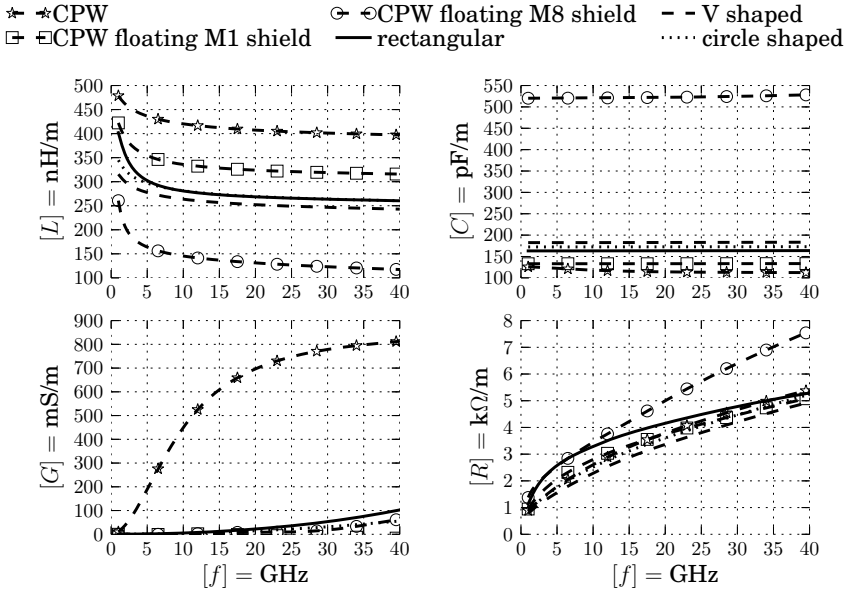
(e) GCPW V shaped.

(f) GCPW circular.

Figure 5.11: CPW shape comparison, showing current density in the cross section at $40\,\mathrm{GHz}$, grounded CPW with different shapes compared to simpler floating shields.



(a)



(b)

Figure 5.12: CPW shape comparison, showing extracted RLCG values, grounded CPW with different shapes compared to simpler floating shields. Geometry of the lines is shown in figure 5.11.

5.4 Other aspects

Another simplification that we have not mentioned is that the large aspect ratio between the signal lines and the slot lines is difficult to capture, requiring a huge amount of memory and exceeding the programs abilities. As was discussed when we explored slow wave parameters, the slot ratio is the most important aspect of the slots, so by keeping the ratio constant results should not be affected too much. Therefore all slots are simulated with $G_{\text{slot}} = W_{\text{slot}} = 1\,\mu\text{m}$ instead of the smaller values which where fabricated. When increasing the absolute size of the slots we would expect both a slight increase in loss, due to the wider slots, and a decrease in effective dielectric constant as the period is reduced. We will come back to this observation in the next chapter where we compare simulation and measurements for the slotted lines. In general, the major challenge for an EM simulator when simulating on chip devices is the large aspect ratios, where thin metal and dielectric layers are placed on a thick conductive substrate causes great headaches.

Discussed above is some of the more critical choices when performing an EM simulation for on chip applications, although the unit cell approach did not work out it has great potential for reduced simulation time and required memory. Not mentioned is some of the more "standard" challenges related to 3D simulation, like boundary conditions, sweep type, meshing and convergence criteria which is covered in manuals and quickly becomes more of an art-form.

In the end I would stress that doing a simulation is a lot like doing a measurement (except that, unless you are paid by the hour, it is a lot cheaper). One must first set up the measurement equipment, which is equivalent to drawing the model and assigning boundaries and excitations, this quickly becomes a habit and re-use is simple. One must then do the tedious task of confirming that the setup is indeed correct, preferably by simulating/measuring some simple well known structure, which was done by the microstrip and CPW lines presented. Now more novel approaches can be tested, and due to the wealth of data a simulator can pump out, the most time consuming part is analyzing the data and re-iterating and confirming the obtained data. This is where knowledge of the tools really come in, since it always becomes necessary to tune some parameters or setting up the model a bit differently.

Chapter 6

Chip and measurements

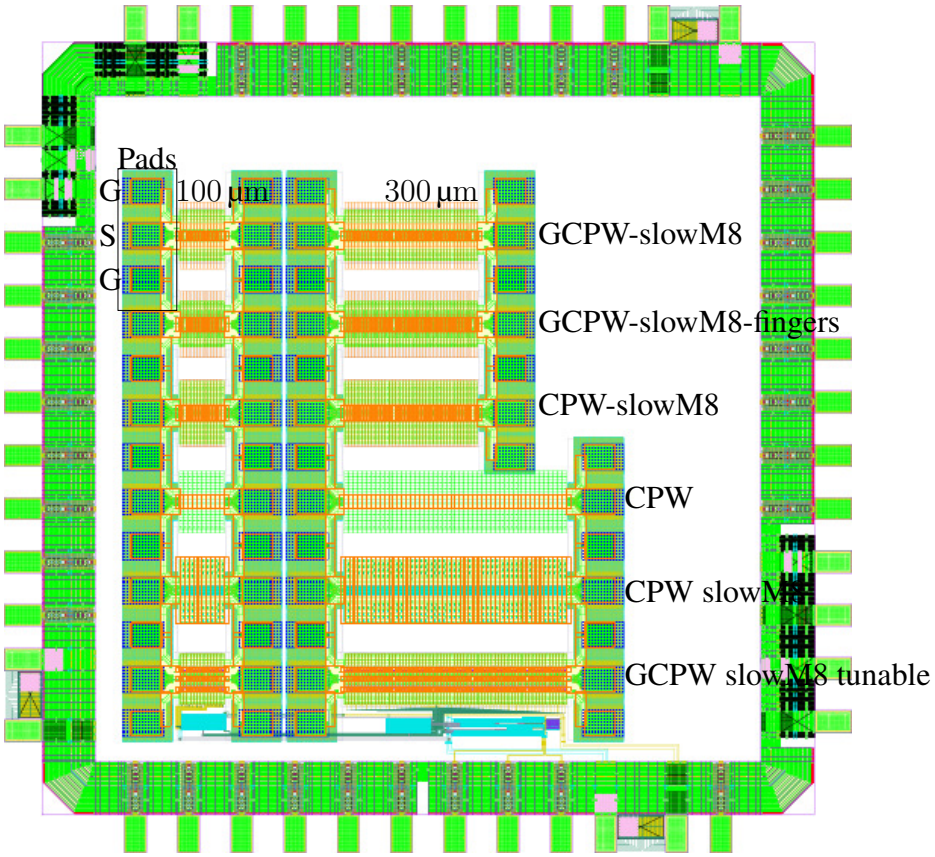


Figure 6.1: Chip before fabrication, dummies not shown.

In this chapter the fabricated chip will be presented, which is shown above. In addition the PCB and the measurement setup will be described in short. Emphasis is given to the deembedding procedure described in section 6.1.2 and the observed variation is explained in section 6.3. The chapter is ended with an extensive comparison between measurements, simulation and models given in section 6.4.

The chip was fabricated by TSMC on the $90\,\mathrm{nm}$ node with a thick top metal. The tunable line is shown at the bottom, together with a Serial Peripheral Interface (SPI) interface (layed out by Kristian Gjertsen Kjelgård, original designer Håkon A. Hjortland). The SPI control signals are connected to the encircling pad frame, which is connected to the PCB by wire bonding (not shown). For clarity, dummies are not shown, but dummy free zones are visible in orange. Note that the free area at the top right corner of the chip was used by another project. Transmission line dimensions are shown in table 6.1 and the chip measures $2\,\mathrm{mm} \times 2\,\mathrm{mm}$.

Table 6.1: Dimensions of fabricated transmission lines. In addition, each line has also has a $l = 100\,\mu\mathrm{m}$ duplicate for deembedding. The last on is published under the name comb-S-GCPW.

Name	W_s	W_g	G_{sg}	l µm	W_{slot}	G_{slot}	l_{slot}
CPW	12	54	10	500	-	-	-
CPW slow-M1	12	54	10	500	0.12	0.12	140
CPW slow-M8	12	54	10	300	0.42	0.42	140
GCPW slow-M8	12	25	25	300	0.42	0.42	114
GCPW slow-M8 tunable	12	25	25	500	0.42	0.42	114
GCPW slow-M8 fingers	12	20	25	300	0.42	0.42	100

Each line is probed with a Ground-Signal-Ground (GSG) pad, where ground pads are shared to reduce area. Pads are shielded from the substrate by a floating shield, which is created by strapping the two lowest metal layers together. As tested by Cheung and Long [CL06], the shield reduces the coupling to the substrate and should float to reduce signal-ground capacitance.

6.1 Calibration and deembedding

When doing measurements at microwave frequencies, measurement equipment and connecting cables will significantly influence the obtained data. In this thesis we are interested in extracting phase shift, loss and reflection from the fabricated transmission lines. Therefore it is important to remove effect like the phase shift of the connecting cables, reflection in the network analyzer and all joints and loss from both cables, analyzer and pads. The mathematical details of this have been relegated to the appendix, but the idea is to remove the unknown effects of the cables and analyzer by measuring "something" with known properties.

6.1.1 Calibration

The CS-5 alumina substrate from GGB Industries is used for this "something", fabricated on the substrate is a number of shorts, open, load ($50\,\Omega$) and through lines. With the substrate a floppy drive with a mathematical description of each standard is included, which is loaded into the network analyzer. We can now measure each of these standards and instruct the analyzer to remove the unwanted effects of the measurement setup. In theory one can measure all of the standards, but it is sufficient to measure standards such as short, open, load and through (SOLT) or through, reflect and match (TRM). The interested reader should consult a network analyzer manual for details, in this thesis multiple standards where used with similar results. Ideally this calibration step should place the reference plane at the probe tips, meaning that any subsequent measurement will have 0 phase at the probe tips. Figure 6.2 (page 63) shows the measurement setup, with network analyzer (VNA) and probing station.

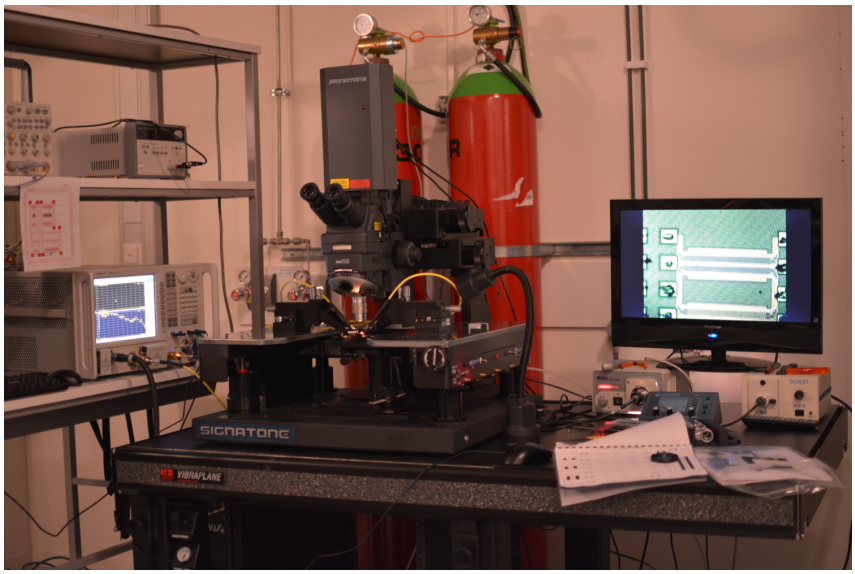


Figure 6.2: Measurement setup, from the left: 50 GHz network analyzer (Agilent™ N5245A), probing station with (Picoprobe™ 40A-GSG-100-DP) and microscope display.

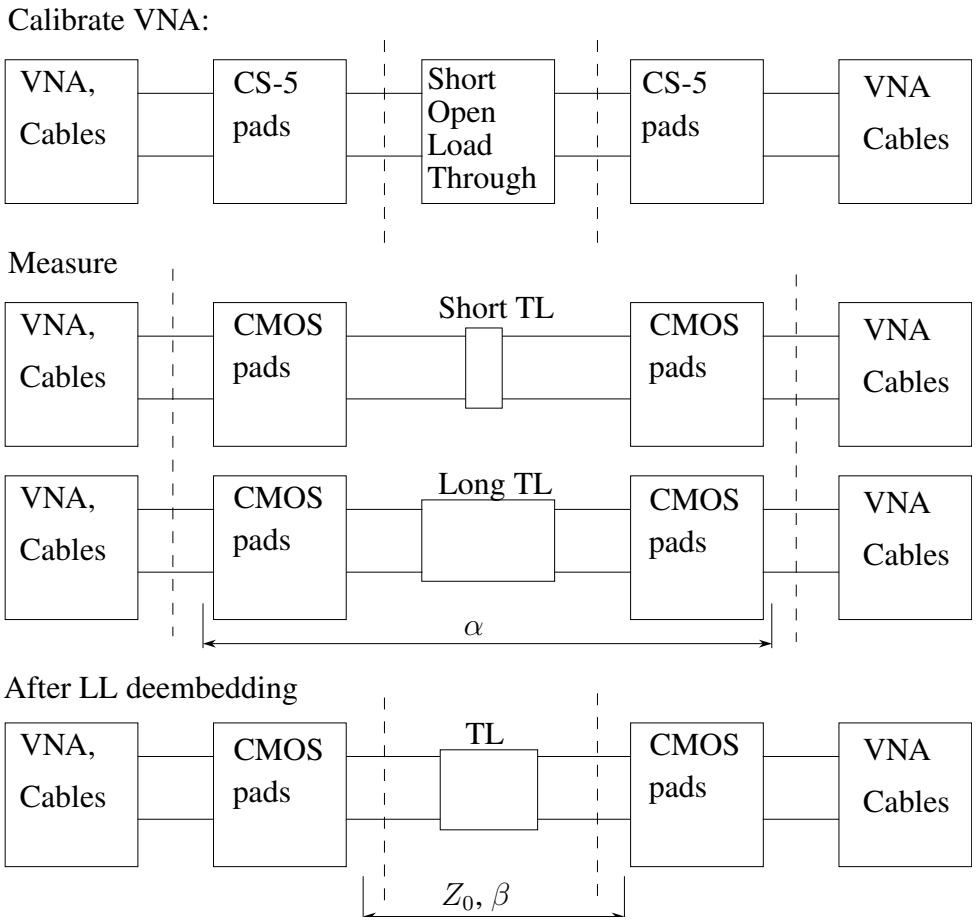


Figure 6.3: The deembedding process, first loss and phase associated with network analyzer (VNA) and connecting cables are removed by measuring known standards on the CS-5 substrate. The reference plane is now at the tip of the probes. Then the short and long transmission lines (TL) are measured and these measurements also include the CMOS pads.The conventional approach is to extract α, β and Z_0 after LL post-processing, but due to high variations in α it was chosen to extract α directly from the long TL, giving an upper bound.

6.1.2 Deembedding

We are now halfway there, since the probing pads on the CMOS chip are relatively large compared to the lines we want to measure, their effect must also be removed. These could have been removed with the steps described above, if accurate models for short, open, load and through structures was available for the CMOS substrate. Instead the LL method described in appendix A.2 was relied on for deembedding, where two lines of different lengths $l_2 > l_1$ give the characteristics of a new line of length $l_2 - l_1$. This method was first applied to simulation results and it was found that consistent results where obtained with $l_1 = 100\,\mu\mathrm{m}$ and l_2 at least $300\,\mu\mathrm{m}$ long.

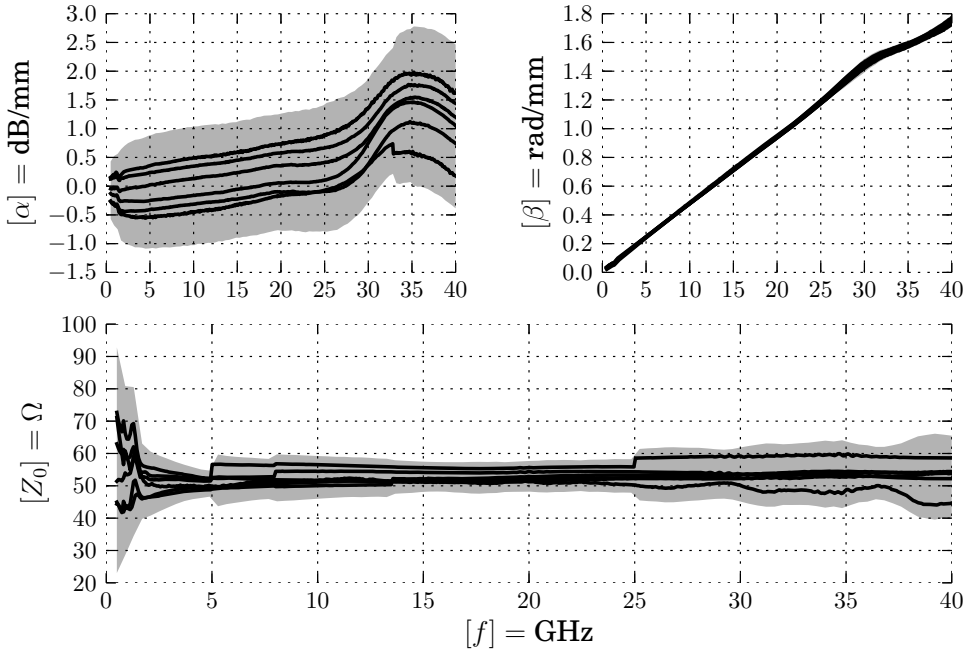
Unfortunately, fabricated lines with these lengths, did not give consistent results for line loss α. The effect is clearly visible in figure 6.4 a) (page 65), where repeated measurements shows large deviation in loss and even indicate gain through a passive structure. Though a Nobel Price for finding a new source of energy sounded tempting, I instead decided to extract loss using measurements for the long line. The transformation from S parameters to TL parameters are given in appendix A.1. The improvement is visible in figure 6.4 b). It should be noted that the proposed method gives an upper bound for the loss, as the loss now contains pad loss in addition to the line loss which we are interested in measuring. The proposed calibration and deembedding procedure is schematically illustrated in figure 6.3 and it is applied to both simulation and measurements results unless otherwise stated.

Table 6.2: Extracted pad parasitics for the CPW measurements, showing deviations at $40\,\mathrm{GHz}$.

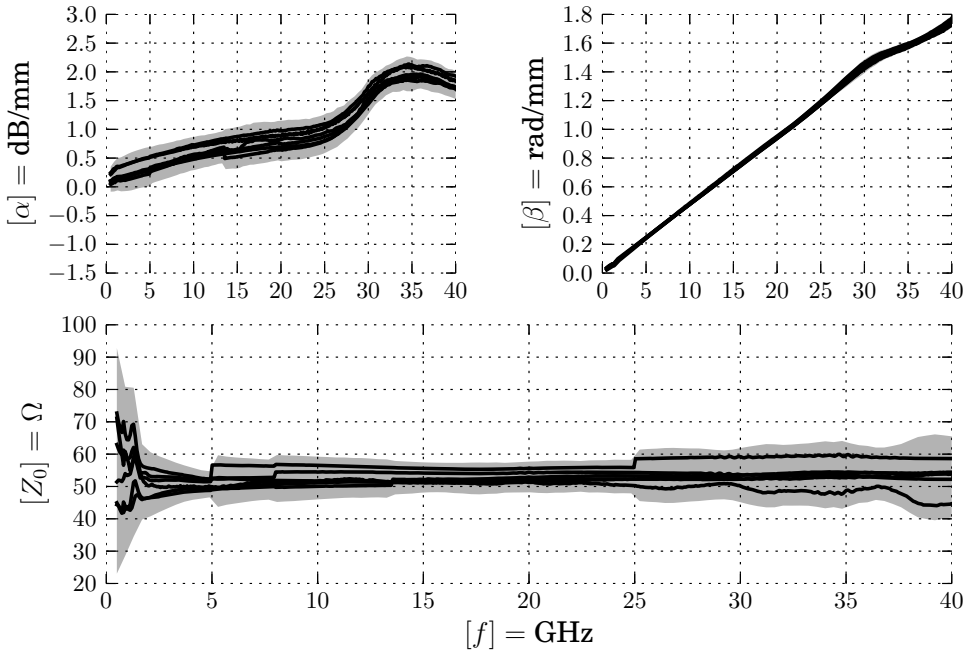
	R_{pad} Ω	L_{pad} pH	C_{pad} fF	G_{pad} mS
Mean	1.2	25	41	0.45
Standard deviation	0.69	9.9	12	0.38
Max	2.1	42	68	1.3
Min	0.18	14	33	0.20

The LL method above extracts a general "error box" which is difficult to analyze, a simpler but more physically intuitive deembedding method was also attempted. Based on the work by Tretiakov et al. [TVW$^+$04], an equivalent circuit for the pads can be extracted (based on measurements of two lines with length l and Nl). Running this on the same data as above, the shunt conductance and capacitance and the series resistance and inductance presented in table 6.2 was extracted. As we can see, the variation is quite larger and we can conclude that the variation is not caused by the deembedding method. For reference, the LL method described in the appendix shows a maximum standard deviation in extracted alpha as $0.48\,\mathrm{dB/mm}$, while the method from Tretiakov shows $0.65\,\mathrm{dB/mm}$ compared to the proposed solution with $0.12\,\mathrm{dB/mm}$.

Deembedding microwave frequency measurements on CMOS is discussed in great length in the literature and no consensus seems to have been reached. Since other methods generally require some addition deembedding structure to be fabricated on chip, other methods could not be applied. The LL method was relied on due to promising results when applied to simulation data and therefore no open, short or other structures where fabricated.



(a)



(b)

Figure 6.4: Individual measurements are shown as black lines and shaded region marks 3 standard deviations from the mean. (a) shows TL characteristics after conventional deembedding, and (b) the proposed solution of extracting α from the long TL. Maximum standard deviation for α goes from $0.48\,\mathrm{dB/mm}$ to $0.12\,\mathrm{dB/mm}$ and is now physical.

6.2 Removing outliers

Accurate probeing is difficult, creating large variations in measured data. In particular, when doing the calibration, a slight misplacement on one of the standards can lead to subsequent measurements being incorrect. In addition, since the deembedding relies on the two lines being measured the same way, slight discrepancies will lead to erroneous results. For some cases, incorrect calibration can be discovered immediate after the calibration is applied and it is always a good idea to re-measure some short, open, thru or loads structures to verify that the calibration went smoothly. Other, more subtle misplacements, are only discovered after the data has been processed and these errors are the subject of this section.

As an objective means of marking individual measurements as bad measurements (outliers), the IQR test was used as a guide. To simplify, the IQR test shows data-points which are far from the *mean*. In addition, the measured data was required to be both approximately continuous and symmetric. When applying this approach, for each of the lines, an interesting pattern emerged. About $85\,\%$ of the outliers, where "lumped together", and came from the same calibration (and VNA settings); which emphasizes the importance of a good calibration.

6.3 Explaining the variance by nudging

The deembedded loss can, at first order, be considered a subtraction of loss ($|S_{21}|$) from the long line minus loss from the short line. Since the calibration can not reliably and completely eliminate network analyzer, cable and probe loss and since probe placement is challenging, the resulting uncertainty becomes significant when trying to measure the small difference in loss between the two short transmission lines. To quantify the above hypothesis, we consider the original LL deembedding method described in the appendix (i.e. by considering loss from both lines).

By adding/subtracting a small constant (a random normal distributed value with variance of 0.02), lets call it nudging, to the S_{21} magnitude, to a single measurement of either the short or the long line; a similar behavior to that displayed in figure 6.4 is obtained. With 1000 samples the maximum (over frequency points) standard deviation becomes $0.46\,\mathrm{dB/mm}$, which is comparable to the measurements presented above. By nudging the other parameters, either the S_{21} phase or S_{11} the extracted β and Z_0 also becomes erratic and does not match the measured results. In addition, if both the short and long line is nudged with the same value, the variation remains low at $0.045\,\mathrm{dB/mm}$.

We can therefore conclude that the observed variation in deembedded loss is due to a difference in measured $|S_{21}|$ loss between the long and short line. By using longer lines, the absolute loss will increase and the measurements will be less sensitive to "nudging".

In addition to affecting loss, $|S_{21}|$ also has an effect on the deembedded Z_0, which variance we have yet to discuss. In the same manner as above, when considering all measurements presented in figure 6.4 we have a maximum standard deviation for Z_0 at $12\,\Omega$ while when nudging a single measurement a deviation of $5.7\,\Omega$ emerge, which doesn't account for all of the variation in Z_0 but covers some. When looking at figure 6.4 we note that the high measured deviation is from the low frequency (sub $2.5\,\mathrm{GHz}$) range, where on chip matching is of less importance and where we know the VNA is less precise.

6.4 Results and comparison

At this point we have actually seen most of the measurements, in figure 3.16 the extracted effective dielectric constant for the various slow wave lines where used to support the data from [SKXL09]; showing that the slow wave factor increases as $\propto 1/h_{\text{sslot}}$. It was also noted that the grounded slow wave lines had a higher capacitance then their floating counterparts.

Measurements for the CPW (without shield) is shown in multiple places to provide a common thread, in section 4.3 it was compared to the model from [Hei93, BVM10] and in figure 5.4 we used it to verify our simulation setup. In this chapter (figure 6.4) repeated measurements are displayed to show the high variation in loss when deembedding the pads.

The tunable line was entirely presented in section 5.3.1, with modeling, simulation and measurements. It turned out not to be tunable, so not much focus was given. Chapter 7 is entirely devoted to the GCPW slow-M8 finger line, showing the remarkable effective dielectric constant of 140. The GCPW slow-M8 line is also discussed in the publication for comparison.

6.4.1 Floating slots

We therefore present here (figure 6.5) a comparison of the CPW, CPW slow-M1 and CPW slow-M8 lines.

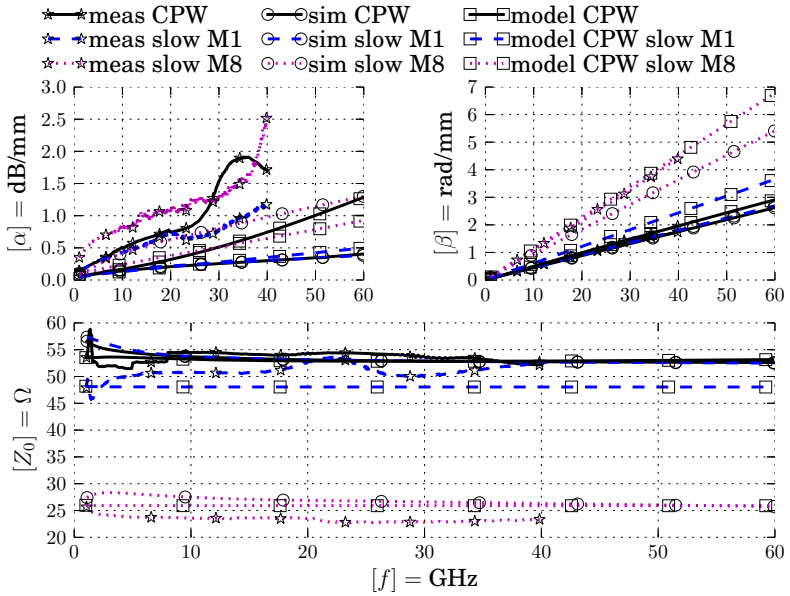
A couple of observations can be made, starting with the CPW-slow-M1 line we see that adding a slotted shield in the lowest metal layer has little effect on neither loss nor the effective dielectric constant, although a slight decrease and increase respectively can be observed. This can be explained by looking at the geometry, since the gap spacing is only $10\,\mu\text{m}$ (and the signal to slot distance is about $6\,\mu\text{m}$) the fields are mostly confined in the upper dielectric layers and what we do in the lower layers has little influence. The model does not account for this, since the model assumes the slot distance is much smaller than the gap distance, the predicted capacitance is larger than measured and simulated values.

The other extreme is the CPW-slow-M8 line, where the signal to slot distance is closer to $0.75\,\mu\text{m}$, here a substantial increase of capacitance is observed, effectively slowing down the wave. This increase does however not come for free, as measurements show a larger G (per unit length!) then the un-shielded line. As discussed at the end of the modeling chapter, [FPGF12] attributes this to induced eddy currents in the slots. Despite the increase in loss, the Q factor is improved, showing the merits of the slow wave transmission line. The reported Q is however far beneath (3 to 4 times lower) then previously reported values, but we attribute this to the deembedding problems outlined above.

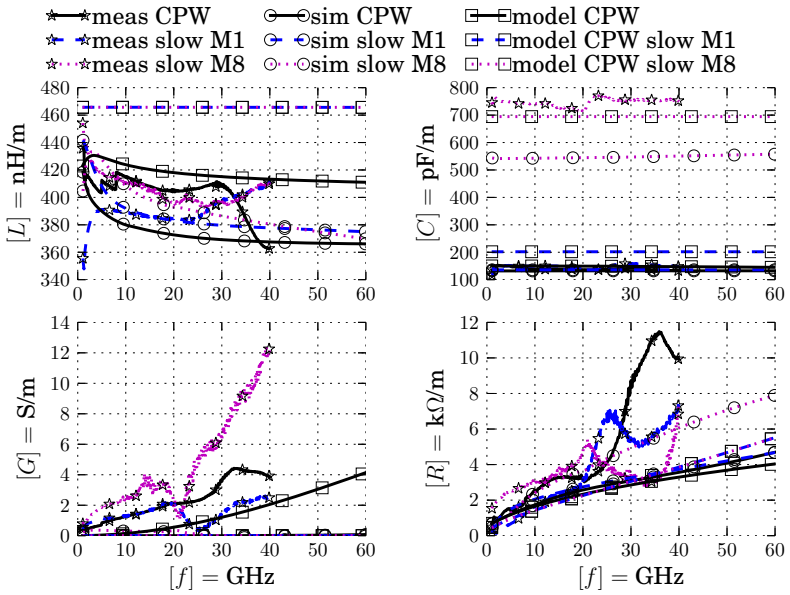
Since the simulation models the slots larger than the fabricated values, and due to the simplified dielectric stack-up used, simulation underestimates ε_{eff} for the CPW-M8 line, which also partly explains the lower simulated loss per unit length. We will come back to the difference between simulated and measured loss in the next section.

The modeled inductance for the slow wave lines is lower than measured values because we use a simple DC approximation.

Measurements of both R and G exhibit a distinct resonance. This is not caused by the transmission line, since the slow-M1 line has, at resonance, a wavelength of about $5.0\,\text{mm}$ while the CPW has $3.8\,\text{mm}$; since both are intentionally made short ($0.50\,\text{mm}$) there seems no relation between the wavelength and the physical length. In addition, this is not a deembedding



(a)



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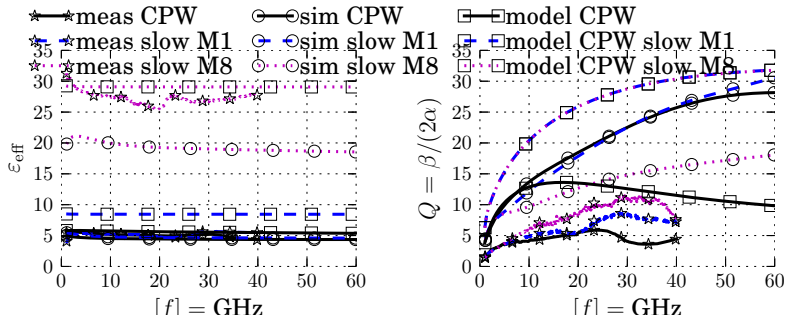


(c)

Figure 6.5: Model, simulation and measurement results for floating slow wave slots in M1 and M8 compared to conventional CPW.

problem, since the resonance is visible in the raw data (not included here), although the effect of the resonance becomes more profound as we post process the data.

I do believe the resonance is caused by the sharing of ground pads. At first, the problem was blamed on the measurement setup, so new cables where tested, then new probes and in the end even the network analyzer was switched; all in vain. An attempt was made at burning away the offending connections by using a laser, but the resulting data has not been included in this thesis since the results are inconclusive. The experiment did however show that the measured loss, and particularly the resonance, is sensitive to cutting away the extra ground line. Further experimentation is here needed, but the laser approach is not recommended since the thick top metal is not exactly designed to be burned away. In addition, though the line may be cut at DC, the cut must be large to prevent coupling at millimeter wave frequencies. Instead, the extra ground path could be simulated, or a new line could be fabricated.

6.4.2 All results

To ease comparison table 6.3 shows all performance characteristics of each line and compares measurements to simulation and models. For measurements, a "typical" value is given, which is the value extracted from the "meas1-day3" dataset, being a dataset with TLR calibration on the first chip. In addition, maximum and minimum measured value are included, note that, as with the rest of this thesis, clear outliers are removed. The "typical" approach might sound strange, but there is simply not enough data for a proper statistical analysis. In addition, by giving a single measurement, proper comparison between the linked parameters are obtained.

As already mentioned, the measured loss shows large variations, where the fingers structure is the most extreme with a minimum measured value of $2.8\,\mathrm{dB/mm}$ and a maximum of $8.2\,\mathrm{dB/mm}$. This results in a very uncertain G, which at it lowest is negative, where the simulation agrees with the negative result indicating that the RLCG model may not be the best way of describing the line. It should be noted that a negative G is not necessarily non-physical, as the total loss can still be positive (and is in all cases studied here).

The slow wave guidelines given in section 4.5 seems to hold, as the slotted shield is moved closer to the signal line the effective dielectric constant increases, by grounding the slots this increases even further and by adding fingers the maximum is reached. The best modeled aspect is the capacitance, which (except for the slow-M1 line, discussed above) shows less than $10\,\%$ deviation between measured and modeled value. This gives fair confidence in the modeled characteristic impedance, showing less than $15\,\%$ deviation for all the lines.

The geometry change between the CPW-slowM8 line created with $G_{sg} = 10\,\mu\mathrm{m}$ and the GCPW-slowM8 line with $G_{sg} = 25\,\mu\mathrm{m}$ was intentional, resulting in equal impedance for the two lines. This is generally considered to give a fairer comparison, because $\alpha = \frac{1}{2}\frac{R}{Z_0} + \frac{1}{2}GZ_0$; the impedance clearly influences loss. Though I am not completely convinced, since the change in geometry clearly also has an effect. However, if only an increase in gap is applied to the CPW-slowM8 line we would expect a decrease in capacitance, instead we observe the GCPW-slowM8 line has a higher capacitance, clearly showing the merits of grounding the slots.

In the next chapter we will have a closer look at the GCPW-slowM8-fingers structure, which I have decided to publish under the name comb slow wave grounded CPW.

Table 6.3: Measurements as "typical (max/min), # count", compared to simulation and models at 30 GHz.

Name	α dB/mm	β rad/mm	Z_0 Ω	L µH/m	C nF/m	G S/m	R kΩ/m	Q	ε_{eff}
CPW	1.5	1.4	54	0.41	0.14	3.6	8.0	4.1	5.20
(max/min), # 6	(1.8/1.4)	(1.5/1.4)	(59/50)	(0.45/0.38)	(0.15/0.13)	(4.5/3.6)	(11/6.0)	(4.4/3.5)	(5.43/5.09)
HFSS	0.25	1.3	53	0.37	0.13	−0.000 27	3	23	4.39
Model	0.51	1.5	53	0.42	0.15	1.2	2	13	5.55
CPW slow-M1	0.84	1.5	51	0.40	0.16	1.4	6.0	7.8	5.74
(max/min), # 10	(1.1/0.68)	(1.5/1.4)	(55/49)	(0.44/0.37)	(0.16/0.14)	(3.7/0.10)	(10/3.0)	(9.3/6.1)	(5.91/5.24)
HFSS	0.26	1.4	53	0.38	0.14	−0.029	3	23	4.64
Model	0.28	1.8	48	0.47	0.2	3.7×10^{-05}	3	29	8.45
CPW slow-M8	1.7	3.1	23	0.39	0.71	7.0	5.0	8.2	24.8
(max/min), # 6	(2.5/1.3)	(3.3/3.1)	(25/23)	(0.43/0.39)	(0.75/0.66)	(8.6/4.7)	(9.0/3.0)	(11/5.4)	(26.7/24.8)
HFSS	0.8	2.7	27	0.39	0.55	−0.019	4	15	19
Model	0.51	3.4	26	0.47	0.69	0.0025	3	29	29.1
GCPW slow-M8	2.9	4.2	24	0.54	0.94	14	8.0	6.3	45.4
(max/min), # 4	(4.8/2.9)	(4.2/4.1)	(27/24)	(0.59/0.53)	(0.94/0.79)	(22/12)	(13/8.0)	(6.3/3.7)	(45.4/41.6)
HFSS	0.67	3.6	27	0.52	0.72	3.1	1	24	33.5
Model	0.6	4.1	28	0.6	0.77	0.0047	3	29	41.9
GCPW slow-M8 tunable on	1.9	3.8	29	0.58	0.69	−4.4	16	8.5	36.6
(max/min), # 2	(1.9/0.57)	(3.8/3.7)	(29/28)	(0.58/0.55)	(0.69/0.66)	(−4.4/−29)	(27/16)	(28/8.5)	(36.6/35.0)
HFSS	1.3	4	29	0.63	0.72	0.91	8	13	40.6
GCPW slow-M8 tunable off	1.9	3.9	29	0.59	0.70	−6.5	18	8.6	37.8
(max/min), # 6	(2.2/0.59)	(3.9/3.6)	(32/28)	(0.61/0.55)	(0.70/0.60)	(7.4/−29)	(28/8.0)	(27/7.2)	(37.8/33.0)
HFSS	0.96	3.9	30	0.63	0.69	0.14	6	18	39.1
GCPW slow-M8 fingers	4.0	7.4	12	0.49	3.2	19	8.0	8.1	140
(max/min), # 4	(8.2/2.8)	(7.4/7.2)	(14/12)	(0.56/0.48)	(3.2/2.7)	(58/−4.8)	(16/8.0)	(11/3.9)	(140/130)
HFSS	2.6	6.6	14	0.49	2.5	−2.5	8	11	111
Model	1.2	7.7	15	0.6	2.8	0.0051	3	28	150

Chapter 7

A new comb slow wave CPW for on chip area reduction and its RLCG model

by Øystein Bjørndal and Kristian Gjertsen Kjelgård

Abstract– A compact low impedance transmission line in CMOS is presented. The new comb slow wave grounded coplanar waveguide (comb-S-GCPW) is modeled, simulated and fabricated. Model is a simple and analytic RLCG equivalent circuit. The model agrees well with simulation and measurements in $90\,\mathrm{nm}$ CMOS. Measurements show relative dielectric constant of 141 for a $12.3\,\Omega$ line, leading to a size reduction of $83\,\%$.

Keywords– **CMOS integrated circuits, Integrated circuit interconnections, Transmission lines, Millimeter wave integrated circuits** [1]

7.1 Introduction

In sub-$100\,\mathrm{nm}$ CMOS technology, transistors with an intrinsic frequency much higher than $100\,\mathrm{GHz}$ are available. Together with low production cost and on chip integration with digital circuitry, this technology is attractive for mass production of millimeter-wave integrated circuits (ICs). [LZW+12]

Transmission lines are a key component in millimeter wave ICs and can replace lumped capacitors and inductors in oscillators, filters, matching networks and distributed amplifiers, but suffer from high loss and large area consumption. Slow wave transmission lines show promising results, where significant area is saved by reducing the required physical length for a given phase shift. [FPGF12]

The literature provides a number of alternatives for slow wave transmission line in CMOS. The common characteristics is that by separating the electric and magnetic energy, the phase velocity is reduced. The first of these is the Maxwell-Wagner polarization, explored by Hasegawa et al. [HFY71] for the microstrip case, where the free charges of a conductive silicon substrate will at low frequencies create a virtual ground plane for the electric field. Magnetic energy is then distributed in the substrate while the electric energy is mostly confined to the insulating SiO_2 layer. Although the relative dielectric constant is high (theoretically[2] $\varepsilon_{\text{eff}} = 2 \times 10^3$), the slow wave mode has an upper frequency in the mega hertz range.

[1] Submitted as a conference paper, reformatted layout, fonts and notation to fit thesis, the text is otherwise identical. Acceptance status is at time of writing unknown.

[2] Based on $90\,\mathrm{nm}$ TSMC parameters for a microstrip using the lowest metal layer and equations from [HFY71]

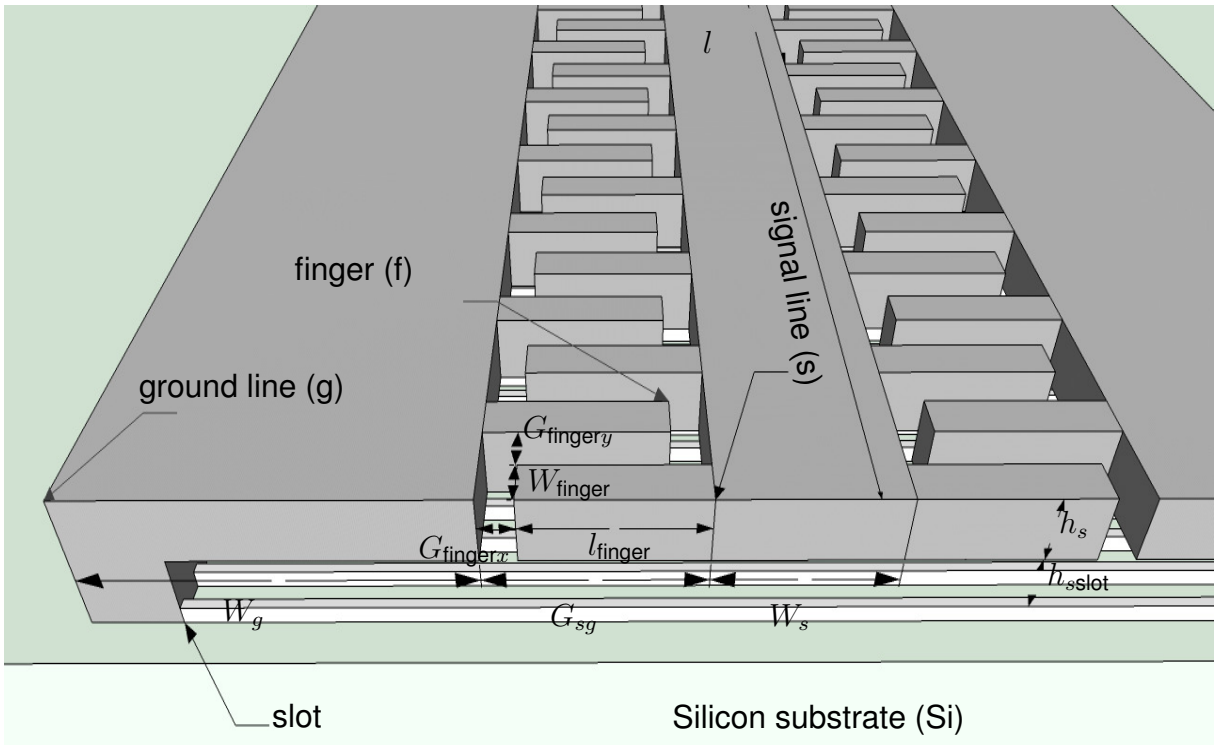


Figure 7.1: Geometry of the comb GCPW transmission line, not to scale. A CPW transmission line with fingers and underlying slots.

The next approach is similar in principle to the first, but uses metal lines orthogonal to the wave direction (slots) to screen the electric field so that it does not penetrate the substrate. The design can be explained by imagining that we create a solid ground plane, some of the return current will then flow in the lower shield, creating an opposing magnetic field which lowers inductance. By slotting the ground plane we prevent the longitudinal current but keep the electric field confined, thereby increasing capacitance without reducing inductance. This creates the same effect as the slow wave mode explored by Hasegawa et al., with an upper frequency range only limited by the slot period.

Previous work has focused on moderate impedance values between $30\,\Omega$ to $50\,\Omega$, but in some filter applications and matching networks, a wide selection of impedance values are required. Low impedance transmission lines can be useful in applications like matching networks for low impedance devices, or stepped impedance filters where the ratio between the lowest and highest attainable impedance must be high. The conventional way of achieving a low impedance CPW is to reduce the signal ground gap. To reduce loss by the proximity effect, Gillick and Robertson [GR93] introduces a low impedance CPW where the signal is extended beneath the ground lines. These methods are however unsuitable for area reduction techniques, since the fields are largely confined between the signal and ground lines.

In this thesis a new slow wave transmission line will be presented, inspired by the fixed comb capacitor. The structure is shown in figure 7.1 and compromises of a "standard" slow wave CPW line with "fingers" extending from both ground and signal lines to increase capacitive coupling. The signal and ground lines are created in the thicker top metal ($h_s = 3.4\,\mu\text{m}$) while the slow wave slots are placed in the next layer. The comb-S-GCPW was designed using the

RLCG model presented bellow and HFSS simulations, design was verified by measurements in the $90\,\mathrm{nm}$ TSMC process. To the authors knowledge, the new comb-S-GCPW has the highest reported size reduction in the literature.

7.2 RLCG Model

The RLCG model is largely based on the work of Kwon et al. [KHC87], who improves on the model from [HFY71]. The model is based on the quasi-TEM assumption

$$v_p = \frac{c}{\sqrt{\varepsilon_r}} = \frac{1}{\sqrt{LC}}, \tag{7.1}$$

where the dielectric layers are assumed non-magnetic ($\mu_r = 1$), L is per unit length inductance and C is per unit length capacitance. (7.1) can be solved for L when we set $\varepsilon_r = 1$ and C_{air} is found by conformal mapping (see [KHC87])

$$L = \frac{1}{c^2 C_{\text{air}}}. \tag{7.2}$$

Resistance is found by the simple skin effect model from [JG93], where the sum of the square of DC and skin effect resistance is for the signal line calculated as

$$R = \frac{1}{\sigma_{\text{Cu}}}\sqrt{\left(\frac{1}{W_s h_s}\right)^2 + \left(\frac{1}{1.5(W_s + h_s)\delta_{\text{metal}}}\right)^2}, \tag{7.3}$$

where $\delta_{\text{metal}} = 1/\sqrt{\pi\mu_0\sigma_{\text{Cu}} f}$ is the skin depth and 1.5 is empirically determined.

For high values of G_{sg} and slow wave mode, capacitance is mainly determined by capacitance beneath the signal line, creating an almost microstrip like mode. [KHC87] suggests the parallel plate equation $\varepsilon W_s/h_{s\text{slot}}$ multiplied with an empirical constant. [WZY+11] suggests using a fill factor which depends on the width and gap between slots (W_{slot} and G_{slot} respectively). Combining these articles we obtain

$$C(A) = \frac{\varepsilon A}{h_{s\text{slot}}}\left(\frac{W_{\text{slot}}}{W_{\text{slot}} + G_{\text{slot}}}\right)^{0.4} \tag{7.4}$$

where A is the overlap area.

Using fingers the capacitance is increased. To provide an upper bound the simple fringe model from [Lee03, p. 123] is used. Assuming the main contribution is from the finger sidewalls ($l_{\text{finger}} - G_{\text{finger}x}$)

$$\begin{aligned} C_{\text{sidewall}} &= \frac{\varepsilon(h_s + 1.5G_{\text{finger}y})((l_{\text{finger}} - G_{\text{finger}x}) + 1.5G_{\text{finger}y})}{G_{\text{finger}y}} \\ C_{\text{total}} &= C(W_s) + 2\frac{2C_{\text{sidewall}} + C(W_{\text{finger}} l_{\text{finger}})}{2W_{\text{finger}} + 2G_{\text{finger}x}}. \end{aligned} \tag{7.5}$$

Note that C_{sidewall} is in units of farad, so to get $\mathrm{F/m}$ we must divide by the period $2W_{\text{finger}} +$

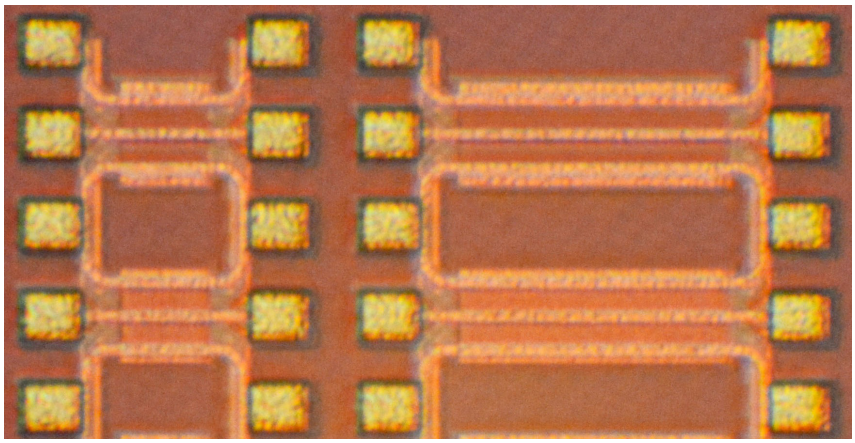


Figure 7.2: Chip micrograph, showing comb structure (bottom) and without fingers (top), for deembedding each line is $100\,\mu\mathrm{m}$ and $300\,\mu\mathrm{m}$ long. Probing GSG pads share a common ground pad to reduce area.

$2G_{\text{finger}x}$, after multiplying with the number of sidewalls 4. The additional term $C(W_{\text{finger}}l_{\text{finger}})$ comes from capacitance bellow the fingers to the underlying slots.

7.3 Measurements Results

Presented here are results for the structure shown in figure 7.1 and a version without the fingers, a chip micrograph of these structures are shown in figure 7.2. For both lines the signal line is $W_s = 12\,\mu\mathrm{m}$ wide and $h_s = 3.4\,\mu\mathrm{m}$ thick. The ground return path is placed at a distance $G_{sg} = 25\,\mu\mathrm{m}$ and is $W_g = 20\,\mu\mathrm{m}$ wide. The ground is connected to underlying slots with vias, where the slots are created with minimum width and gap $W_{\text{slot}} = G_{\text{slot}} \approx 0.4\,\mu\mathrm{m}$ and a thickness of $h_{\text{slot}} \approx 0.9\,\mu\mathrm{m}$. The fingers are created with a minimum gap in both x and y direction $G_{\text{finger}y} = G_{\text{finger}x} = 2\,\mu\mathrm{m}$, giving a finger length of $l_{\text{finger}} = 23\,\mu\mathrm{m}$.

To characterize the lines, the measurement setup (a Agilent N5245A) was deembedded using SOLT on a standard CS-5 alumina substrate and the probing pads was removed with the L-L deembedding method presented in [RH03, ZnJRHLYMS11, SGLYM$^+$12]. The L-L deembedding method allows us to extract transmission line parameters using two lines of different lengths, without the need of custom built open, short, through or load structures. The extracted characteristic impedance, calculated from [ZnJRHLYMS11, eq. (17)], is shown in figure 7.3.

Due to the short lines used in this study ($100\,\mu\mathrm{m}$ and $300\,\mu\mathrm{m}$), the conventional way of extracting $\gamma = \alpha + j\beta$ from [RH03] failed to give consistent results for loss α. Small deviations in probing placement gave large deviations in extracted loss, even resulting in gain through the extracted line. To obtain physically real results, it was therefore decided to extract α based on measurements on the long line [EE92]. The reported loss therefore represent an upper bound, as it contains pad loss.

Since loss per unit length is an inappropriate figure of merit for slow wave transmission lines, the Q factor $\beta/(2\alpha)$ is extracted. Measurements gives a Q of 8.3 for the comb structure and 5.4 without fingers; both at $20\,\mathrm{GHz}$. In addition, the effective dielectric constant is

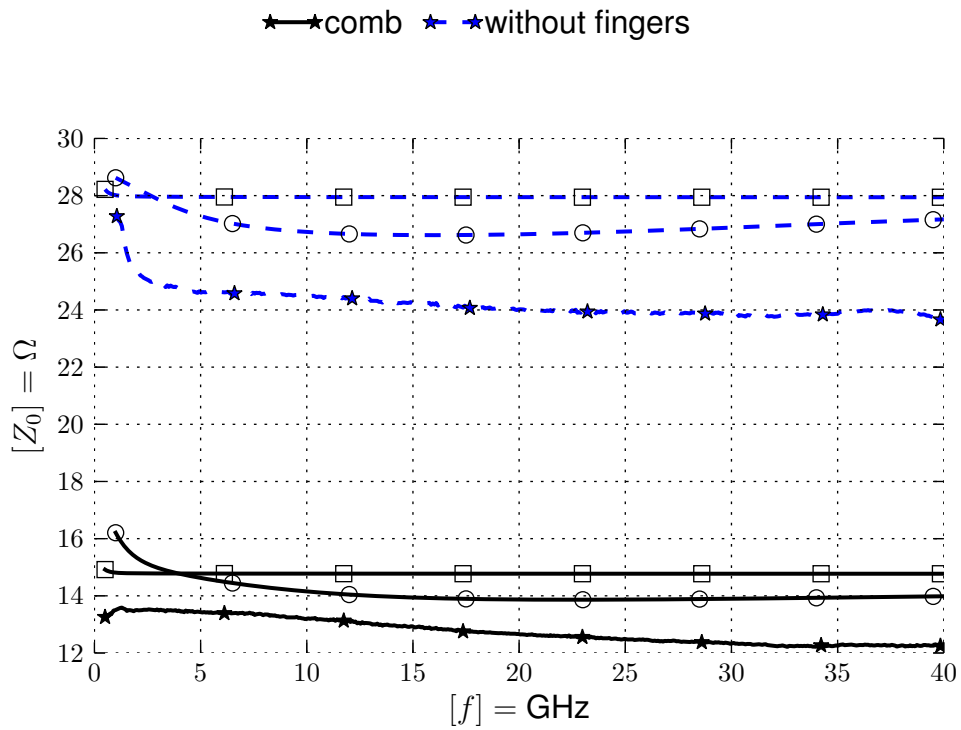


Figure 7.3: Comparing the real part of the characteristic impedance of presented model □ to simulation ◯ and measurements ★.

calculated as $(\beta c/(2\pi f))^2$ and is 141 for the comb structure at $40\,\text{GHz}$, which leads to a size reduction of $44\,\%$ compared to the slow wave structure without fingers ($\varepsilon_{\text{eff}} = 44.7$) and $83\,\%$ compared to a conventional CPW transmission line.

Phase related information like L, C, ε_{eff} and Z_0 seems to be accurately predicted by both model and simulation. But due to the difficulties in extracting loss, the measured loss is higher than predicted by simulation. This could have been improved by creating longer lines, but this was not possible due to the small chip used in this study.

To investigate the relative importance of loss by R and G we express α as

$$\alpha = \text{Real}\Big(\sqrt{(R + j\omega L)(G + j\omega C)}\Big).$$

We can then extract from measurements that $\alpha(G = 0) = 2.97\,\text{dB/mm}$ and $\alpha(R = 0) = 1.04\,\text{dB/mm}$, both at $30\,\text{GHz}$. Metal loss is therefore the major cause of loss ($\approx 75\,\%$), which can be reduced by increasing the signal thickness by using multiple metal layers. This would also further increase C, as the sidewall capacitance would increase. G could be decreased by using a thinner layer for the slots as investigated by [FPGF12], or by letting the slots float at the cost of reduced effective dielectric constant.

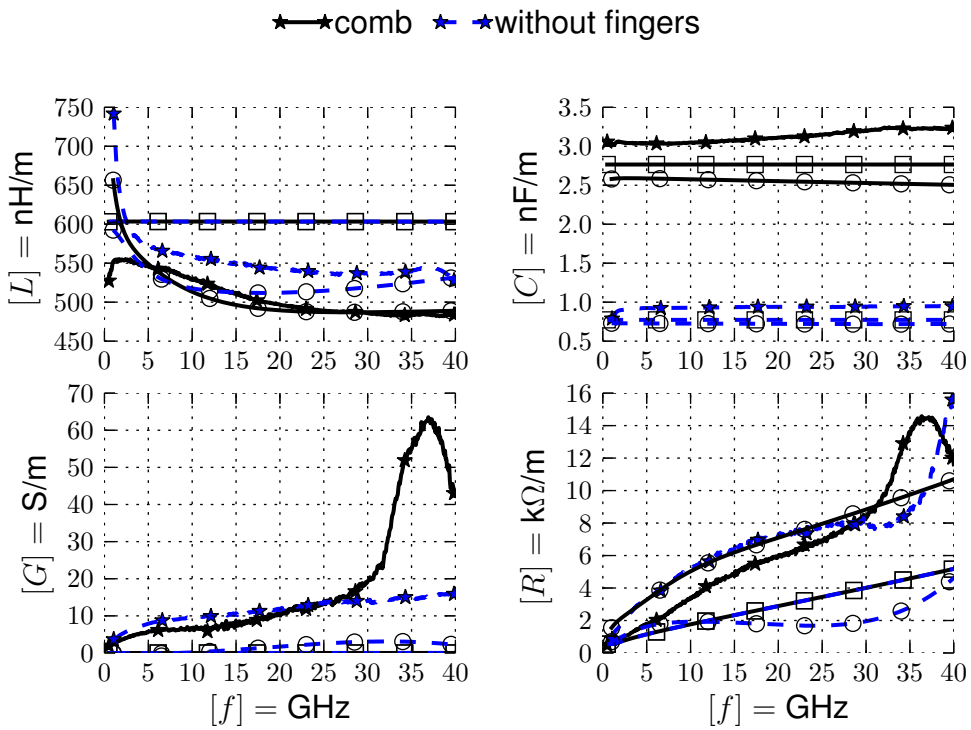


Figure 7.4: Comparing RLCG parameters of the presented model with measurements, where lines marked with ★ are measurements, □ is model and ◯ mark simulation (HFSS) .

7.4 Conclusion

A new slow wave structure providing large size reduction ($\varepsilon_{\mathrm{eff}} = 141$) and moderate Q value for low impedance applications ($Z_0 = 12\,\Omega$) has been presented. For design insight and ease of synthesis, a simple RLCG model was developed. The model is compared to full wave simulation in HFSS and measurements in commercial $90\,\mathrm{nm}$ CMOS. By using the comb-S-GCPW significant area reduction in millimeter-wave ICs are feasible.

Chapter 8

Applications

"Transmission lines are useful"

This chapter explores some applications of transmission lines and gives and overview of transmission line parameters. Transmission lines can be used for a variety of circuit functions, the most fundamental being interconnect which is briefly illustrated in section 8.2. We will focus on filters, and show two examples, a stepped impedance filter is presented in section 8.3, while a bandstop/bandpass filter is designed in section 8.4. Where the last one actually uses a transmission line for matching. Examples of other applications, which are not discussed here, are power combiners, baluns, distributed amplifiers, oscillator tanks, power dividers and attenuators. But we will first revisit transmission line parameters to give an overview over the essential features.

8.1 Choosing a line

Transmission lines can be fully characterized by different sets of parameters, here we will discuss S parameters, RLCG, wave properties, Q factor and slow wave performance parameters; and how these should be optimized for different applications.

8.1.1 S parameters

Scattering (S) parameters is the "black box" approach to RF circuit design. We assume the network (circuit) is connected with characteristic impedance Z_0 (usually $50\,\Omega$), for a general two port network we write

$$\begin{pmatrix} b_1 \\ b_2 \end{pmatrix} = \mathbf{S} \begin{pmatrix} a_1 \\ a_2 \end{pmatrix}$$

With a Z_0 reference impedance on both sides of the network we can simplify this to positive and negative waves

$$\begin{pmatrix} V_1^- \\ V_2^- \end{pmatrix} = \begin{pmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{pmatrix} \begin{pmatrix} V_1^+ \\ V_2^+ \end{pmatrix}.$$

If the network is symmetric, that is, if the input and outputs can be interchanged (which is the case for all transmission lines discussed in this thesis) the matrix is symmetric i.e. $S_{11} = S_{22}$ and $S_{12} = S_{21}$.

S_{11} is now a measure of reflection, or deviation from Z_0. If the goal is to design a transmission line of $50\,\Omega$, S_{11} should be minimized. If however a different impedance is desired the S parameters should either be renormalized or the line impedance should be extracted. Loss is characterized by S_{21} which is the related to the ratio between output to input power, a ratio of $1 = 0\,\mathrm{dB}$ signifies zero loss and is usually the goal. The S_{21} phase is related to the phase shift through the device, which should be maximized if miniaturization is a goal. It is important to keep in mind that transmission line S parameters are periodic, making S parameters unsuitable for transmission line comparison.

The S parameters can easily be converted to different network representations, see for instance [LB09, page 660]. Converting to RLCG or wave parameters is a slightly more complicated and is described in appendix A.1.

8.1.2 RLCG parameters

RLCG parameters are discussed in length in other parts of this thesis, in section 2.2 we introduce the RLCG parameters as solutions to the wave equation governing Quasi-TEM wave propagation. And in Chapter 4 different physical effects are mapped to either R, C, L or G.

Both R and G represent loss, where R is usually metal loss and G is mostly caused by the substrate, but any loss to ground gets lumped in G. For slow wave applications we want to increase both L and C, this keeps the characteristic impedance constant. G can often be neglected, but when utilizing CMOS technology we have a conductive and lossy substrate which must be accounted for. For the CPW structure total loss is often a compromise between metal loss and substrate loss, since a thin line with a short gap will have high resistance but low coupling to the substrate.

8.1.3 Wave parameters

We normally characterize transmission lines in terms of characteristics impedance Z_0 and propagation constant $\gamma = \alpha + j\beta$.

For interconnect design α, representing loss per unit length, should be minimized. For other (RF) applications we typically require some fixed "electrical length", so a loss per electrical length would be more suitable. Defining the Q factor as

$$Q = \frac{\beta}{2\alpha}$$

is consistent with the usual definition of energy storage divided by energy loss, assuming low dispersion[1]. A good slow wave line will have a large β and can therefore have higher loss (α) per unit length without reduction in Q factor. Another suitable slow wave figure of merit is the effective dielectric constant ε_{eff}, which is for a conventional design is slightly influenced by geometry but mostly defined by the surrounding material. Effective dielectric constant of ≈ 5

[1] see [GY63], we assume $v_p/v_g \approx 1$.

is not uncommon for a conventional design, the included paper discusses a transmission line with an effective dielectric constant of 140 which is the highest reported in the literature. Effective dielectric constant directly influences the physical length when realizing a fixed electrical length.

A related term is "slow wave factor" which is used sparingly in this thesis since the definition varies a little. In all cases the slow wave factor is defined as a ration between the wavelength of the slow wave line divided by some reference, where the reference might be a conventional design or that of a wave traveling with the speed of light.

We now move on to applications, we start with a time domain view before reviewing two filters.

8.2 Delay line

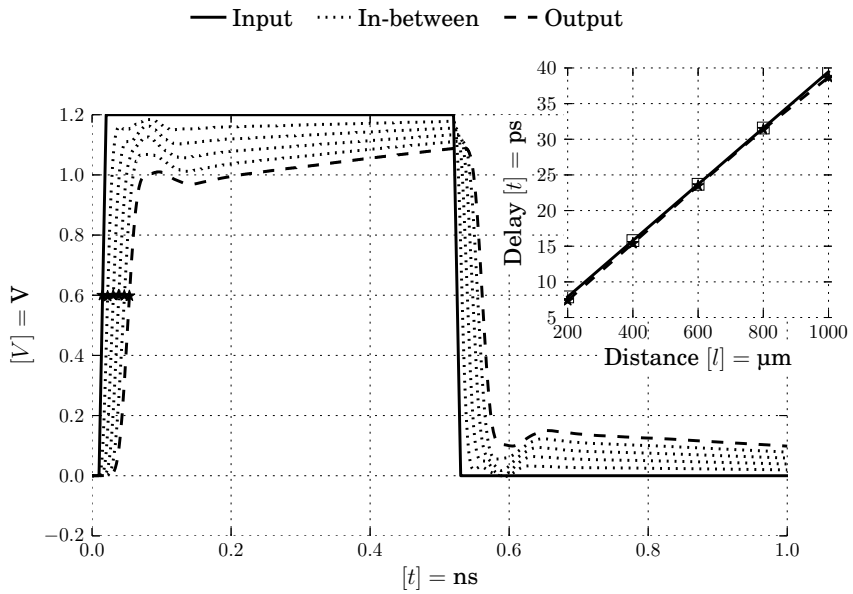


Figure 8.1: Pulse response of the GCPW-slowM8 fingers line, based on deembedded measurements down a $1\,\mathrm{mm}$ long line. Also shown is the voltage for each $200\,\mu\mathrm{m}$ down the line (marked as "In-between"). The inset shows delay (measured at $0.6\,\mathrm{V}$ and marked with ★), compared to $l\sqrt{\varepsilon_{\mathrm{eff}}}/c$ marked with □.

The simplest application of a transmission line is the delay line, by sending a signal down a transmission line we have accurate control over the delay. Shown in figure 8.1, an ideal pulse is sent down a cascade of 5 deembedded, $200\,\mu\mathrm{m}$ long S-parameter blocks in Cadence. As is shown in the inset, excellent agreement with the simple expression $l\sqrt{\varepsilon_{\mathrm{eff}}}/c$ is achieved. It should be noted that the simulation was done with the line terminated in its characteristic impedance ($12\,\Omega$) to minimize reflection.

The DC value is however a little strange, since the measured data does not include a good estimate for the low frequency loss. This can be remedied by relying on either simulation or modeled data at sub gigahertz frequencies.

8.3 Stepped impedance filter

A stepped impedance filter is a simple filter topology for realizing a low pass filter. Here a 5th order Chebyshev is used as an example, where the capacitors are approximated to low impedance transmission line segments and the inductors with high impedance segments. Using the published finger structure for the low impedance segments and the CPW slow-M1 line as the high impedance segment the corresponding deembedded S parameters where cascaded in ADS schematic. The structure is visualized in figure 8.2 where the values are calculated from the measured impedance and phase constants.

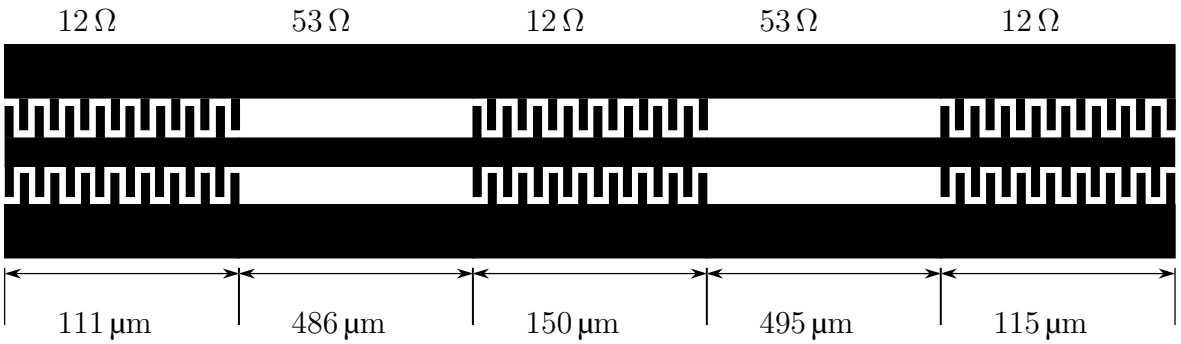


Figure 8.2: Stepped impedance filter consisting of low impedance GPCW slow-M8 lines cascaded with high impedance CPW slow-M1 lines. The figure is not to scale.

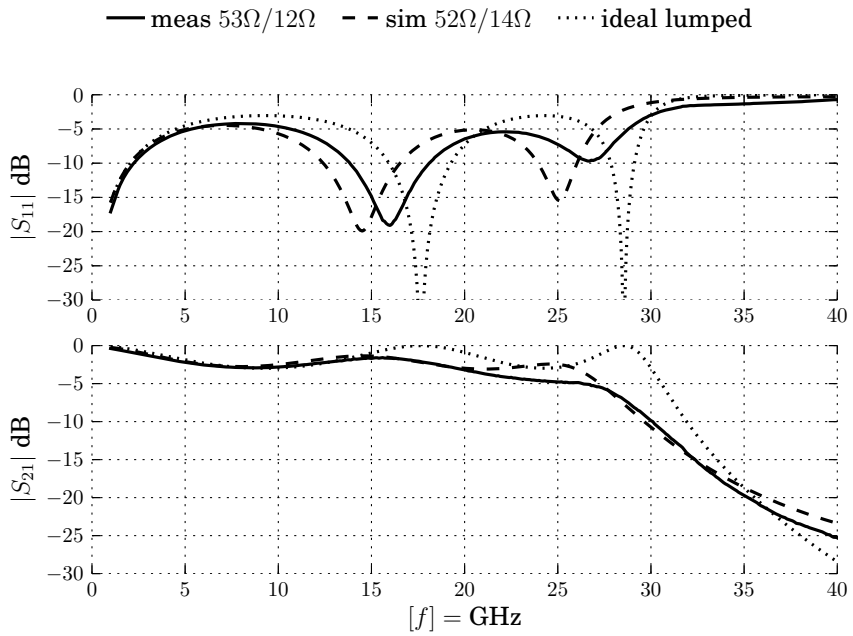


Figure 8.3: Simulated 5th order Chebyshev stepped impedance low pass filter, based on measurements and simulation of low and high impedance transmission lines. Compared to ideal lumped filter response.

Since measurements and simulation of these lines differ slightly, both where simulated and the resulting filter characteristic is shown in figure 8.3. Due to the high loss of the comb structure and that the simplifications when designing the filter require a very large ratio of low to

high impedance the filter response falls bellow the $-3\,\mathrm{dB}$ point well before the design goal of $30\,\mathrm{GHz}$. It should also be noted that the transmission line implementation exhibit a periodic behavior, and so the low pass filter will eventually transmit at higher frequencies (around $75\,\mathrm{GHz}$ with the presented design).

The presented filter can not be realized with standard CPW lines, using the model shown in figure 4.11 from [Hei93, BVM10], a $Z_0 = 12.5\,\Omega$ line needs something like $W_s = 152\,\mu\mathrm{m}$ and $G_{sg} = 1.2\,\mu\mathrm{m}$ which is not feasible. In addition, the entire filter would be over $3\,\mathrm{mm}$ long which is 3 times the proposed filter.

8.4 Bandstop and bandpass filter

I was asked to design a filter which could pick out the second harmonic of an oscillator working at $15\,\mathrm{GHz}$, traditionally this can be achieved by either a bandstop filter at $15\,\mathrm{GHz}$ or a bandpass filter at $30\,\mathrm{GHz}$. A straight forward approach was attempted, where a lumped bandstop filter was converted to shunt shorted stubs by following [LB09]. In addition to the wanted bandstop around $15\,\mathrm{GHz}$, the filter also showed a bandstop at $30\,\mathrm{GHz}$, completely defeating the purpose of the filter. Therefore the following approach was followed instead.

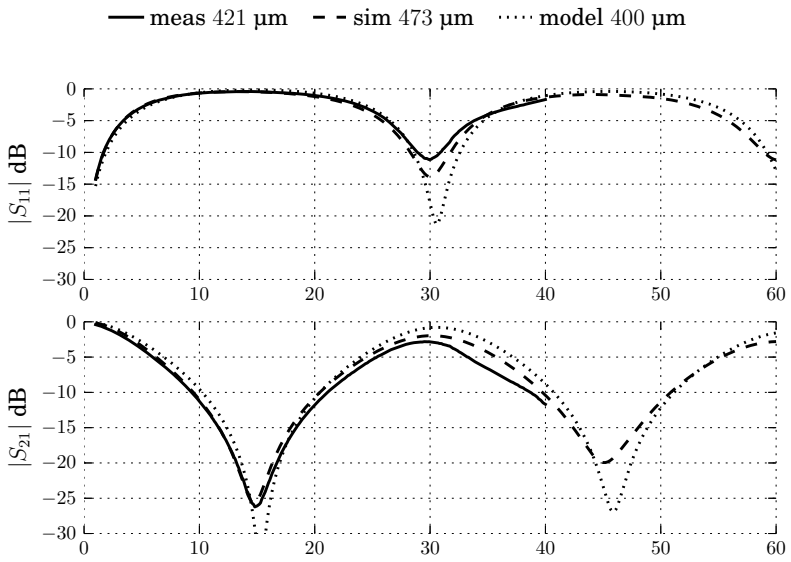


Figure 8.4: Single open shunt filter for suppressing $15\,\mathrm{GHz}$ and passing $30\,\mathrm{GHz}$. Filter response is based on deembeded measurements, simulation and model of the GCPW-slowM8 fingers which is ideally shunted.

We showed in (2.13) that an open transmission line has an input impedance of

$$Z_{\text{in}}(f) = -jZ_0/\tan\left(\frac{2\pi\sqrt{\varepsilon_{\text{eff}}}f}{c}l\right),$$

the tangent goes to ∞ at $\lambda/4$, so the input impedance will be zero at

$$f_0 = \frac{c}{4\sqrt{\varepsilon_{\text{eff}}}l}$$

while the impedance will "disappear" to ∞ at $2f_0$. Since the characteristic impedance is not critical to achieve the wanted response the published comb structure is utilized. The inital simulation is shown in figure 8.4, where the simulation using deembedded measurements shows an insertion loss ($20\log(S_{21})$) at $15\,\mathrm{GHz}$ of $-26.1\,\mathrm{dB}$ and $-2.84\,\mathrm{dB}$ in the passband ($30\,\mathrm{GHz}$).

As an example of matching, we can improve the matching at $30\,\mathrm{GHz}$ by utilizing a quarter wavelength transformer, the required impedance

$$Z_0 = \sqrt{Z_{\text{in}} \cdot Z_L} = \sqrt{28.2\,\Omega \cdot 50\,\Omega} = 37.5\,\Omega$$

is however not something we have fabricated so the models developed must be used. By using the CPW slow wave modeled outlined in the end of chapter 4, and designing for a high Q factor, an impedance of $37.5\,\Omega$ is achieved with $W_s = 8\,\mu\mathrm{m}$ and $G_{sg} = 25\,\mu\mathrm{m}$. The filter is sketched in figure 8.5 and the resulting idealized filter response in figure 8.6. Input impedance at $30\,\mathrm{GHz}$ is now $49.2\,\Omega$, or in terms of input return loss ($-20\log(S_{11})$), the return loss has gone from $11.1\,\mathrm{dB}$ to $34.1\,\mathrm{dB}$. In addition the matching now covers a larger bandwidth around $30\,\mathrm{GHz}$.

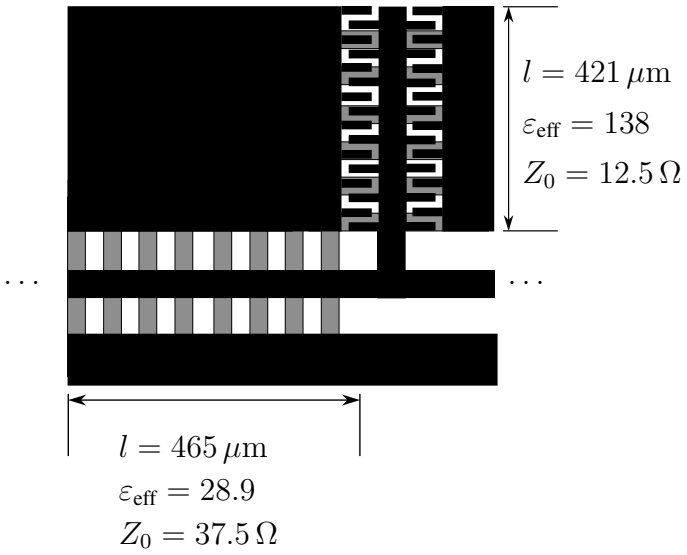


Figure 8.5: Sketch of harmonic filter with GCPW-slowM8-fingers as open shunt stub ($\lambda/4$ at $15\,\mathrm{GHz}$) and CPW-slowM8 as quarter wave transformer at $30\,\mathrm{GHz}$. Filter is assumed to lie in a $50\,\Omega$ environment. Slow wave slots shown exaggerated in grey, figure is in now way to scale.

The estimated area consumption of the proposed filter (if no bends are used) becomes $0.2\,\mathrm{mm}^2$. If we attempt the same filter with traditional CPW lines the shunt stub would be about $2.2\,\mathrm{mm}$ long, clearly showing the merits of the comb structure.

8.5 Discussion and improvements

In the above, we have done a number of simplifications. Firstly, I must stress that none of these circuits have neither been fabricated nor simulated, "meas" in the above refers to measurement data in the form of touchstone files, which are generated from deembedded measurements and "sim" is based on simulation of a single, isolated line. We will now discuss a few practical aspects that needs to be addressed before these circuits are ready for fabrication.

In the delay line, the transient simulation needs additional low frequency data points, these

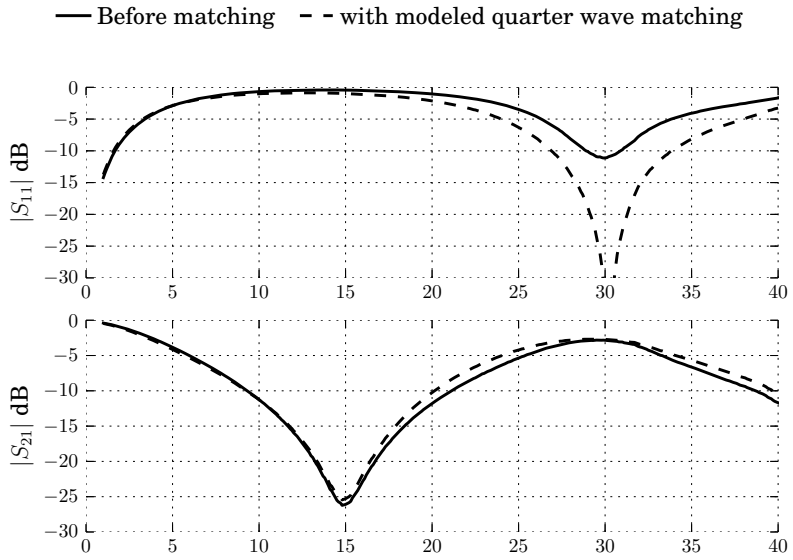


Figure 8.6: Open shunt filter with impedance matching for suppressing $15\,\mathrm{GHz}$ and passing $30\,\mathrm{GHz}$. Filter response is based on deembeded measurements and modeled CPW-slowM8 quarter wave transformer, which is ideally interconnected. Shunts are created with different lengths to obtain the same resonance frequencies.

could be gotten from simulation or models, but this would need some fitting to avoid un-physical effects at the transition. In addition, the driver and receiving circuits must be modeled as these will greatly affect the actual delay.

The stepped impedance filter of figure 8.2 is not actually as tidy as it looks, since the high impedance lines have a G_{sg} spacing of $10\,\mu\mathrm{m}$ while the low impedance finger structure has a spacing of $25\,\mu\mathrm{m}$, this creates discontinuities which we have not modeled. The filter can however be made without these discontinuities if the gap is made larger, and this will even improve performance. By increasing the gap *and* the finger length, the low impedance segments will show an even lower impedance, while the high impedance lines will have a higher impedance. A large low to high impedance ratio is vital for a stepped impedance filter and the filter will look more like the ideal response.

In the bandpass/bandstop filter of figure 8.5, the open line will show some capacitive loading which will offset the resonance, this can be remedied by adjusting the stubs length. The loading can be estimated by empirical expressions (which are plentifully) or by EM simulation. In the same design, the quarter wave line is based on our simple model and is likely to underestimate loss as discussed in chapter 6. The improvement in return loss should therefore be weighted against the added insertion loss. The design did not have any requirement on bandwidth, if such requirements are to be implemented the standard filter synthesis techniques should be re-visited.

In addition the T discontinuity of the bandpass/bandstop filter must be carefully simulated. However the conventional problem of air bridging is conveniently solved by grounding the slow wave slots.

It should also be kept in mind that due to the deembedding problems described earlier, the "meas" loss is always an upper bound, since they include pad loss. We have used the finger structure extensively, leading to quite low Q factors (filter selectivity), other lines like the CPW slow-M8 should be utilized if higher Q is required.

Chapter 9

The last chapter

"For the impatient"

9.1 Discussion and future work

"Real knowledge is to know the extent of one's ignorance" – Confucius

The focus of this thesis has not been to revolutionize the field of transmission lines on CMOS, the fabricated lines where not optimized before fabrication but rather created as a basis for comparison between design guidelines, mathematical modeling, simulation and measurements. Two novel approaches where however attempted, a tunable line and a finger structure. The tunable line did not work, and this is probably caused by the terrible varactor design.

I currently see three main points for improvements for the varactor design, firstly the nMOS based varactor should have a grounded body instead of being connected to the control voltage. Secondly, the floating terminal is difficult to model accurately and should be forced to a known potensial. Lastly, a better high frequency model for the transistors must be utilized, transistor modeling is not a new field and this should be doable. In my defence, the tunable line was designed in the hectic weeks before sending the chip to fabrication.

The finger structure shows an impressive size reduction of $83\,\%$, but this comes at a cost of very low impedance which may be undesirable (although we have shown some uses in the applications chapter). The only way of increasing the impedance, without impairing the size reducing, is to increase the inductance value. As discussed, this is done by moving the ground lines further away from the signal, and this could be achieved by lowering the ground lines to a lower metal layer, but keeping the fingers at the signal layer.

Mathematical modeling in this thesis is in large parts based on other work, a considerable amount of time was used (wasted?) wading through available models in the literature. If more time was spent on the theoretical background and methodologies, new models would not necessarily have emerged (due to the amount of work already available), but existing models could be understood in greater details and easily adapted to some of the odder geometries in this thesis.

Of particular interest is modeling of G, which seems to be difficult for both simulators and mathematical models. Or, the other way around, which seems to be difficult to measure. The literature seems to agree with the last assumption, although reported values for G are surprisingly sparse, both [SRG09] and [WZY+11] report G lower than $1\,\mathrm{S/m}$ for slow wave lines, whereas we have here measured values above $7\,\mathrm{S/m}$. We have also measured large negative values, further highlighting the difficulties. In large part this can be attributed to the deembed-

ding problems which forced the loss to be calculated from the long line, which raises the loss since the pads are included, and also makes the uniform RLCG model incorrect. In addition, we have indicated that sharing of ground pads can have unfortunate effects.

If on the other hand the measurements are correct, it should be noted that both mathematical modeling and simulation uses the same material constants, namely conductivity of both metal and silicon and loss tangent of silicon. This could indicate incorrect material specifications, as any model with crappy input will result in incorrect output, especially the dielectric layers, where little is known about the confidential materials used. Even simpler structures could be fabricated to extract the material properties, for instance waveguides and microstrip lines where the fields are well behaved.

We have attributed the deembedding problems to uncertainty in $|S_{21}|$ magnitude, but where this variation comes from needs further investigation, although probe placement is a likely candidate. The observed resonance in measured loss seems unrelated and has been attributed to the sharing of ground pads. Future work is therefore advised to do 1) proper modeling and design of pads, 2) not share ground pads with adjacent structures and 3) increase length of transmission lines for LL deembedding.

9.2 Perspective

To put this work in perspective; in a "local" scale, the investigation of high frequency on chip application is unique and significant progress have been made. Significant effort is being made at the nanoelectronics group in collaboration with FFI, in the millimeter frequency range and new equipment has been tested out in this thesis. Since interconnect is such a vital and fundamental part of any design it is hoped that the contribution of this work will help the group make a significant contribution to the field. On a "global" scale the work has resulted in a single conference paper with focus on transmission line miniaturization, which will hopefully inspire new and novel slow wave transmission lines.

9.3 Conclusion

Transmission lines are only useful when the wavelength approaches the physical length, or put another way, transmission line effects can be ignored if the wavelength is sufficiently long. We have pointed out when this happens and explored phase shift, loss and reflection. The importance of loss by dielectric polarization is pointed out, first from Maxwell's equations, then more quantitatively in terms of an intrinsic slow wave mode for the SiO_2 on Si stack-up and finally in a transmission line model compared to simulation and measurements.

Special considerations when designing on CMOS is highlighted and common transmission line structures are explored with an in-depth discussion on slow wave lines. Design guidelines for slow wave on-chip transmission lines are given and confirmed by models, simulation and measurements. Transmission line models are developed, from a very simple RLCG model to give a "feel" for the parameters, to a quasi-empirical model in the publication to explain the fingers and a frequency dependent analytical model was used for a more quantitative study.

Extensive EM simulation is carried out, where limitations and required simplifications are discussed. A novel simulation technique was attempted to reduce the significant memory and CPU time of full wave 3D simulation, here further investigation is required for automating the procedure. A tunable line is presented, which has an ideal simulated tunability of $\varepsilon_{\text{eff}} = [19, 11]$, but which turned out not to be tunable. Further work is needed, especially in regards to transistor modeling and varactor design.

The merits of grounding the slow wave slots was shown, resulting in a measured $\varepsilon_{\text{eff}} = 45$ and a simulated Q factor of 24. An even larger size reduction was obtained with the new low impedance finger structure, resulting in $\varepsilon_{\text{eff}} = 141$. Applications are explored and significant area reduction is obtained when utilizing the new structure for filter synthesis. Further investigation is required for accurate measurements of loss, but it should be noted that the challenges related to deembedding the loss, is in part due to the low loss of the lines compared to the measurement setup. Longer transmission lines with redesigned pads should be fabricated for proper evaluation of transmission line loss.

Slow wave on-chip transmission lines provide significant area reduction, and gives unique characteristics for applications like filters, which are essential parts of communication and radar systems.

Part III

Appendix

Appendix A

Characterization

A.1 From S parameters to RLCG

Since most simulators and measurement equipment export data as S parameters we need a way to convert this to transmission line properties (impedance and propagation constant) and frequency dependent R, L, C and G parameters. The standard file format for S parameters are touchstone files, to read these the python library `scikit-rf`[1] is utilized.

[DES+98, TPBQ08] gives a formula for converting from S parameters to impedance and propagation constant

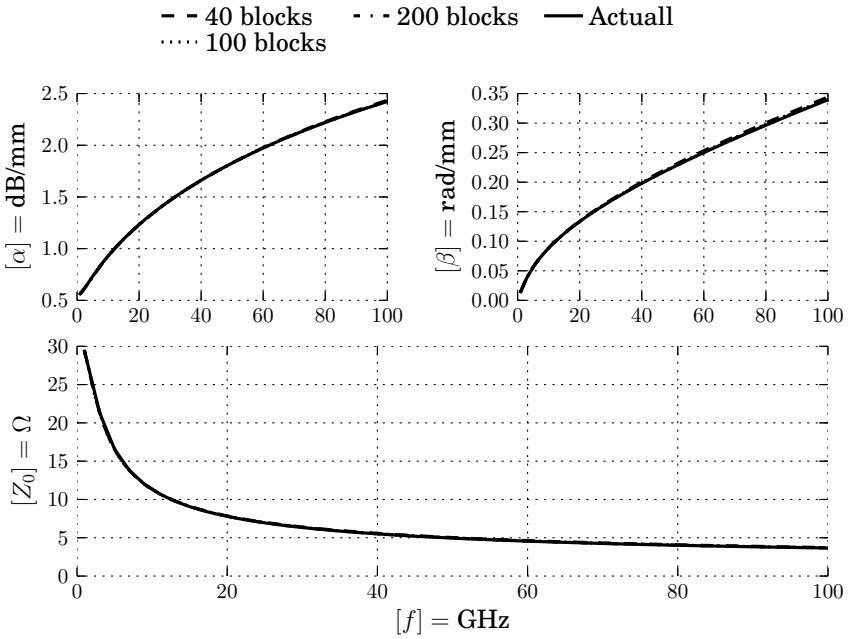
$$\gamma = \frac{2}{l} \operatorname{arctanh} \sqrt{\frac{(1 + S_{11} - S_{21})(1 - S_{11} - S_{12})}{(1 - S_{11} + S_{21})(1 + S_{11} + S_{21})}}$$
$$Z = Z_0 \sqrt{\frac{(1 + S_{11} + S_{21})(1 + S_{11} - S_{21})}{(1 - S_{11} - S_{21})(1 - S_{11} + S_{21})}}.$$

From the definition of R, L, C and G in (2.6), (2.5) we can now express

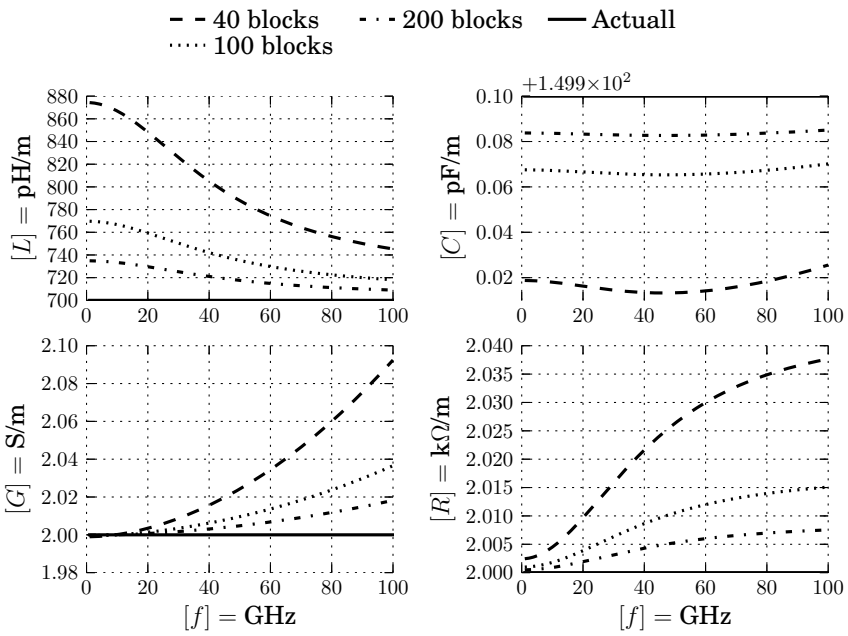
$$R = \Re(\gamma Z) \qquad L = \frac{\Im(\gamma Z)}{\omega}$$
$$G = \Re(\gamma / Z) \qquad C = \frac{\Im(\gamma / Z)}{\omega}$$

To test the above formulas and its implementation multiple RLCG circuit blocks are connected in series and simulated in ads schematic. The result is shown in figure A.1 for different number of blocks and compared to the specified parameters ($R = 2\,\mathrm{k\Omega/m}$, $L = 700\,\mathrm{pH/m}$, $C = 150\,\mathrm{pF/m}$ and $G = 2\,\mathrm{S/m}$). Where each block has a value of $R_i = R \cdot dx = R \cdot l/n$, with length $l = 1\,\mathrm{mm}$. As we can see, there is an inherent frequency dependent part in the conversion, which decreases as the number of blocks are increased.

[1] http://scikit-rf.org/



(a) TL.



(b) RLCG.

Figure A.1: Cascading frequency independent RLCG blocks.

A.2 Deembedding

Given measurements of two lines with $l_2 > l_1$ we get the S parameter matrices $[S]_{l_1}$ and $[S]_{l_2}$. These can be converted to ABCD, denoted as $[ABCD]_{l_1}$ and $[ABCD]_{l_2}$

$$[ABCD]_{l_1} = \begin{pmatrix} A_{l_1} & B_{l_1} \\ C_{l_1} & D_{l_1} \end{pmatrix} = \begin{pmatrix} \cosh(\gamma l_1) & Z\sinh(\gamma l_1) \\ \frac{1}{Z}\sinh(\gamma l_1) & \cosh(\gamma l_1) \end{pmatrix}$$
$$[ABCD]_{l_2} = \begin{pmatrix} A_{l_2} & B_{l_2} \\ C_{l_2} & D_{l_2} \end{pmatrix} = \begin{pmatrix} \cosh(\gamma l_2) & Z\sinh(\gamma l_2) \\ \frac{1}{Z}\sinh(\gamma l_2) & \cosh(\gamma l_2) \end{pmatrix}$$

From these we define [RH03, eq. (11)]

$$[T] = \begin{pmatrix} t_{11} & t_{12} \\ t_{12} & t_{22} \end{pmatrix} = [ABCD]_{l_1}[ABCD]_{l_2}^{-1}$$

We then solve the quadratic equation below for b_m and $\frac{a_m}{c_m}$ [RH03, eq. (18-19)]

$$t_{21}b_m^2 + (t_{22} - t_{11})b_m - t_{12} = 0$$
$$t_{21}\left(\frac{a_m}{c_m}\right)^2 + (t_{22} - t_{11})\frac{a_m}{c_m} - t_{12} = 0$$

This gives ambiguity in sign, which is solved in [EH79] by requiring

$$|b_m| < \left|\frac{a_m}{c_m}\right|.$$

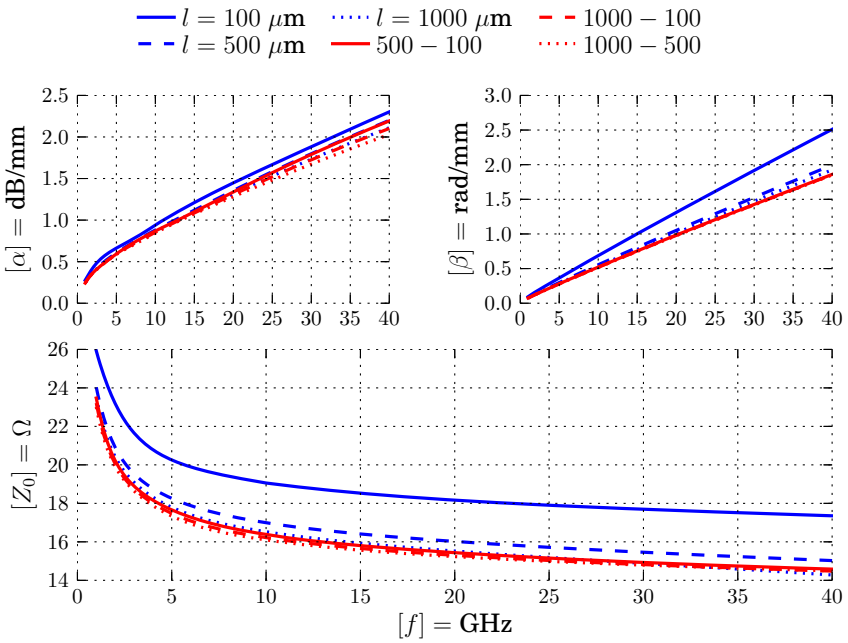
We can now determine the complex propagation constant by [RH03, eq. (17)]

$$\gamma = \frac{\ln(\lambda)}{l_2 - l_1}$$
$$\text{where} \qquad \lambda = \frac{\frac{a_m}{c_m} - b_m}{\frac{a_m}{c_m}t_{22} + b_m\frac{a_m}{c_m}t_{12} - b_m t_{11} - t_{12}}$$

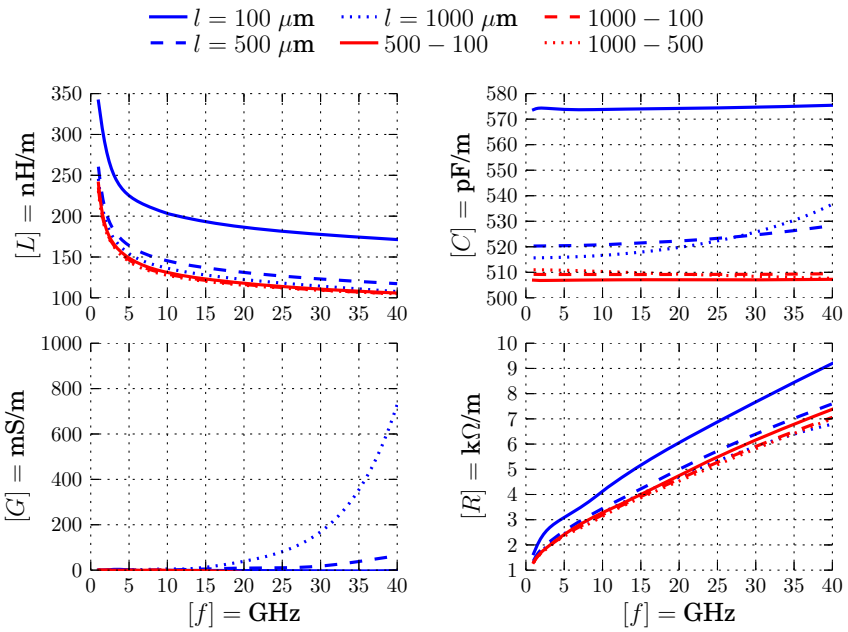
To determine Z we use the results from [ZnJRHLYMS11, eq. 30]

$$Z = \frac{B_{l_2}(\cosh(\gamma l_1) + A_{l_1}) - B_{l_1}(\cosh(\gamma l_2 + A_{l_2}))}{A_{l_1}\sinh(\gamma l_2) - A_{l_2}\sinh(\gamma l_1) - \sinh(\gamma l_2)\cosh(\gamma l_1) + \sinh(\gamma l_1)\cosh(\gamma l_2)}.$$

The above process has been tested on CMOS transmission lines by [SGLYM+12].



(a)



(b)

Figure A.2: Comparing deembedding for CPW.

Appendix B

PCB

To test the tunable line, the PCB shown in figure B.1 was created. From the top it consists of the chip, level converts ($1.2\,\mathrm{V}$ to $3.3\,\mathrm{V}$), bypass capacitors and connectors at the bottom. The leftmost connector is the $1.2\,\mathrm{V}$ power supply, while the larger connector was used for the SPI interface to a microcontroller which was controlled from a PC via USB. Microcontroller sofware was adapted from Håkon A. Hjortland, while Kristian Gjertsen Kjelgård helped with the fabrication and assembly of the PCB.

Some chips where also tested on a bare PCB with a continuous ground plane.

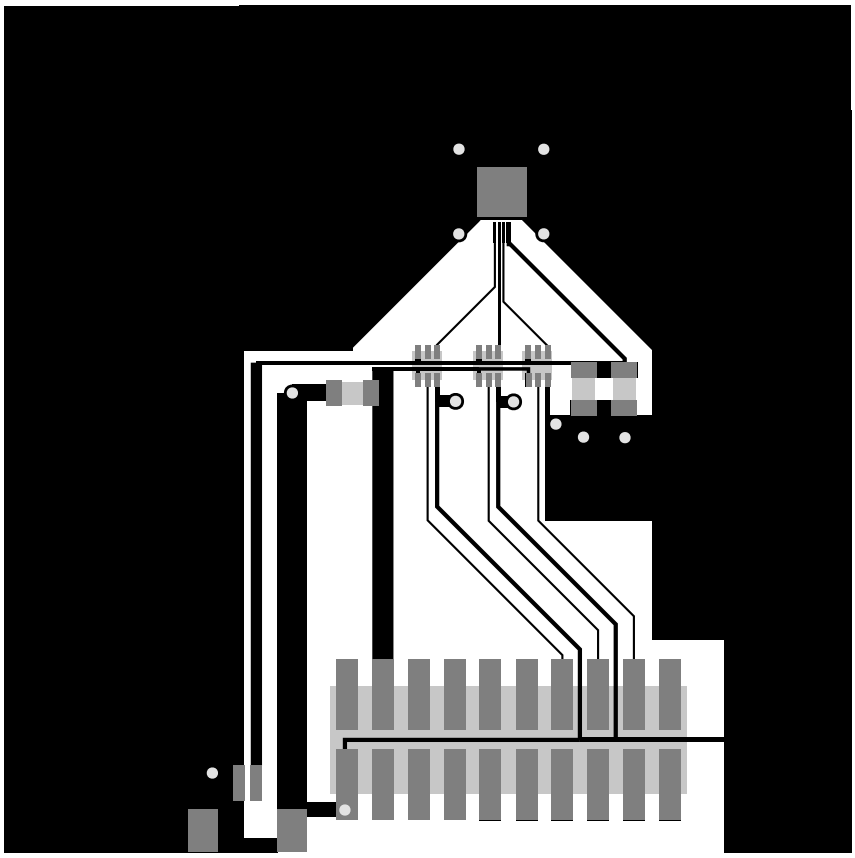


Figure B.1: Printed Circuit Board (PCB) to test the tunable transmission line.

Appendix C

Source Code and data

"Talk is cheap. Show me the code." – Linus Torvalds

During the work of this thesis, over 7000 lines of python code has been written (not counting comments and blank lines). Most of this is plotting related and not very exiting. But some pieces has been selected, a short description is given below:

- Utility files: `engineeringUnit.py`, `files.py` and `pythonPreamble.py`.
- `hfss-floque.py` implements the pseudo code in listing 5.1.
- `deembedding.py` implements the deembedding method presented in section A.2.
- `layers.py` is used to draw figures like figure 3.1, using matplotlibs bar function!
- `modes.py` contains implementation of formulas from Hasegawa et al. [HFY71].
- `slowWave.py` implements the periodic high and low impedance method presented in section 3.3.2.
- `networkRepr.py` and `networkSet.py` is an object oriented interface to a "Network", where subclasses "RLCG", "Z", "ABCD", "TL" and "S" provide some invaluable operations and conversions.
- `plotMeasurements_variation.py` uses the IQR test to help mark measurements as outliers.
- `tlModels.py` contains models from chapter 4 and `tlModels_designer.py` is a helper script for exploring the models.
- Some process specific constants are define in `KONF_myConstants.py`, which prevents me from sharing this file, a dummy file with confidential information removed is shared instead. (This file will raise syntax error)

In addition, the tex source code for both this and supporting documents are included. Since this thesis utilizes the PythonTEX package these files also contain lots of python code. Due to the confidentiality of the CMOS process, ADS, Q3D, HFSS and Cadence files can not be included, but resulting datafiles and measurements results are included. All of the above is available at

`www.ob.cakebox.net/masterThesis/`

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"Standing on the shoulders of giants"

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