High-k dielectric thin films: characterization and application in RF MEMS capacitive switches

Ph.D. Thesis

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ABSTRACT

This thesis presents the characterization of potentially high-κ (dielectric constant) materials for RF (Radio Frequency) Microelectromechanical Systems (MEMS) capacitive switches and the process development of RF MEMS capacitive switches with high-κ materials made of PZT/ZrO₂ thin films based on surface micromachining techniques for RF and microwave applications.

The primary focus of the thesis is the electrical characterization process, including the modeling, simulation, fabrication, measurement, and analysis of three different dielectric thin films (ZrO₂, PZT, and dual-layer PZT/ZrO₂) with high dielectric constants. In particular, the materials’ microwave properties up to 50 GHz are reported for the first time, specifically for the application of the RF MEMS capacitive switch as a dielectric layer, in addition to those for the application of RF tunable devices. Characterized dielectric constant of the PZT thin film deposited by chemical solution deposition (CSD) is 280–540 at 10 GHz depending upon the thickness. The dielectric constant of a 250 nm thick ZrO₂ thin film is ~25, and the loss tangent is less than 0.1 at 50 GHz. The dielectric constant of a dual layer of 420 nm thick PZT/280 nm thick ZrO₂ is ~130 at 50 GHz, and the loss tangent is less than 0.1 at 50 GHz. Our characterization reveals that both the ZrO₂ and the PZT thin films may be suitable for high-isolation RF MEMS capacitive switches due to their high dielectric constants at microwave frequencies and for tunable RF metal–insulator–metal (MIM) capacitors due to their high tunability.

This thesis also presents the microfabrication process development of the RF MEMS capacitive shunt switches, with the successfully characterized PZT and ZrO₂ thin films exhibiting excellent dielectric performances. Thus far, only two RF MEMS capacitive switches using the ferroelectric PZT thin film as a dielectric layer have been developed: by Thales R&D, France, and NIST, Japan. Here, we used ZrO₂ thin films as a seed layer for the PZT thin film and thus improved the dielectric properties of the PZT dielectric stacks for the RF MEMS switch. We report on the design, fabrication, and measurements of RF MEMS capacitive switches and discuss the process issues for obtaining reliable switches. Several experiments were performed using surface micromachining technologies, including thermal evaporation, electroplating, photolithography, wet etching, dry etching, and electrical characterizations, to develop the process steps for the RF MEMS switches.

Furthermore, this thesis also reports on a feasibility study of Cu/Sn SLID interconnects for RF applications. Two coplanar waveguides (CPWs) used for the die and substrate were modeled, simulated, and fabricated on a glass wafer, then they were flip-chip bonded together through Cu/Sn SLID interconnects. The 3D full electromagnetic (EM) simulation results show that the interconnects have a low loss (less than 0.5 dB at 20 GHz) compared to that of Au/Sn SLID interconnects. In addition, the RF performance can be improved by changing several parameters in the transition region of the interconnects: interconnect height, transition length, and bump radius.
This thesis is submitted in partial fulfillment of the requirement for the degree of Philosophiae Doctor at the University of Oslo, Norway. The thesis contains work done at Vestfold University College, Norway, and was made on the topic of RF MEMS capacitive switch with high dielectric constant materials, collaborated with SINTEF ICT. The work was funded by Vestfold University College, the Norwegian Research Council under Grant No. 181712/I30 "Microtechnological Research Platform, and NorFab (Norwegian Micro- and Nano-fabrication Facility).

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CHAPTER 1

1. INTRODUCTION

1.1 RF MEMS switch and high-κ dielectrics

Extensive development of RF MEMS switches has occurred over the last decade. Their excellent performance characteristics, such as extremely low power consumption, high linearity, low insertion loss, and high isolation make them key components for RF and microwave devices. These devices include phase shifters for phased array antennas and radars, switch matrices for telecommunications and satellite communication systems, and tunable capacitors for tunable filters and oscillators [1, 2]. RF MEMS switches offer substantial potential benefits, in terms of size and losses, over switch technologies that are currently employed in the microwave industry, such as mechanical switches (coaxial and waveguide) and semiconductor switches (FET and pin diodes) [3-5]. The fabrication process is compatible with integrated circuits (IC), rendering RF MEMS switches more attractive, especially due to their integration with complementary metal-oxide-semiconductor (CMOS) devices. Therefore, RF MEMS devices can easily be incorporated into RF systems at low costs [6]. Table 1.1 shows the comparison between different switch technologies.

Table 1.1 Performance comparison of FET switches, PIN diodes, and RF MEMS switches [7]

<table>
<thead>
<tr>
<th>Parameter</th>
<th>RF MEMS</th>
<th>PIN</th>
<th>FET</th>
</tr>
</thead>
<tbody>
<tr>
<td>Voltage (V)</td>
<td>20–80</td>
<td>3–5</td>
<td>3–5</td>
</tr>
<tr>
<td>Current (mA)</td>
<td>0</td>
<td>3–20</td>
<td>0</td>
</tr>
<tr>
<td>Power consumption (mW)</td>
<td>0.05–0.1</td>
<td>5–100</td>
<td>0.05–0.1</td>
</tr>
<tr>
<td>Switching Time</td>
<td>1-300 μS</td>
<td>1-100 nS</td>
<td>1-100 nS</td>
</tr>
<tr>
<td>Capacitance ratio</td>
<td>40–300</td>
<td>10</td>
<td>-</td>
</tr>
<tr>
<td>Cutoff frequency (THz)</td>
<td>20–80</td>
<td>1–4</td>
<td>0.5–2</td>
</tr>
<tr>
<td>Isolation (1–10 GHz)</td>
<td>Very high</td>
<td>High</td>
<td>Medium</td>
</tr>
<tr>
<td>Isolation (10–40 GHz)</td>
<td>Very high</td>
<td>High</td>
<td>Low</td>
</tr>
<tr>
<td>Isolation (60–100 GHz)</td>
<td>High</td>
<td>Medium</td>
<td>None</td>
</tr>
</tbody>
</table>
RF MEMS switches are devices that use mechanical movement to achieve a short circuit or an open circuit in an RF transmission line. The actuation force needed for the mechanical movement of the switch beam can be obtained from electrostatic, magnetostatic, piezoelectric, or thermal sources [8]. Among these, electrostatically actuated switches demonstrate high reliability (>10 billion cycles) and enable wafer-scale manufacturing techniques [9, 10].

Electrostatically actuated RF MEMS capacitive shunt switches basically consist of a metal bridge, a ground-signal-ground coplanar waveguide (CPW), and a dielectric layer placed on a pull-down electrode, which is part of the CPW signal line as seen in figure 1.1. The dielectric layer is used for preventing a short-circuit from forming between the top movable switch beam and the bottom pull-down electrode. In the up-state switch, the switch beam is suspended on the dielectric layer with an air gap, rendering the switch almost open as in a CPW line. However, when a DC bias voltage is applied to the pull-down electrode, the switch beam collapses on the dielectric layer due to the electrostatic force between the metal switch bridge and the bottom electrode. As a result, the switch is electrically short and closed.

<table>
<thead>
<tr>
<th>Insertion Loss (1–100 GHz)</th>
<th>0.05–0.2</th>
<th>0.3–1.2</th>
<th>0.4–2.5</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power handling (W)</td>
<td>&lt; 1</td>
<td>&lt; 10</td>
<td>&lt; 10</td>
</tr>
<tr>
<td>3rd order Intercept (dBm)</td>
<td>66–80</td>
<td>27–45</td>
<td>27–45</td>
</tr>
</tbody>
</table>

Figure 1.1 Principle of operation of a RF MEMS capacitive switch; (a) up-state and (b) down-state

RF MEMS capacitive switches in a shunt configuration need to have a high on/off capacitance ratio, an important figure of merit quantifying their RF performance, to achieve a high impedance ratio between the up- and down-states
of the switch, as well as achieve a high isolation. Up to the current date, various switch configurations have been presented to improve RF performance, including low spring-constant anchoring and inductive tuning. Increasing the down-state capacitance using high dielectric constant materials has also been demonstrated [10-12].

Three parameters can increase the down-state capacitance: (1) the overlapping area of the signal line and the moving bridge; (2) the thickness of the dielectric; and (3) the dielectric constant of the material. To obtain greater capacitance, the area of the actuation electrode can be increased. However, as the area increases, the up-state capacitance also increases, thus increasing the return loss of the switches. Decreasing the dielectric layer thickness is limited by pin hole and breakdown field strength. Inductive tuning can be performed to maximize isolation; however, the isolation frequency band is deep and narrow. On the other hand, an improvement in the switch performance and a high on/off capacitance ratio can be easily achieved using a material with a high dielectric constant [8, 12].

RF MEMS switches with a high dielectric constant were appealing early in the development of MEMS switches because it was easy to realize a high capacitance ratio, as silicon nitride or oxide, typically used as a dielectric layer in capacitive RF MEMS switches, have a relatively low down-state capacitance due to the low dielectric constant, which limits switch performance, especially in the low frequencies [13]. MEMS capacitive-shunt switches with Barium Strontium Titanate (BST) and Strontium Titanate (STO) were demonstrated by Liu and Park, respectively, with extremely high capacitance ratios [11, 12]. Thin film PZT was also demonstrated to have a high reliability as a dielectric layer in the MEMS capacitive-shunt switches [10]. PZT was used here as an insulator rather than as a piezoelectric actuator. All of the aforementioned materials have characteristics of ferroelectrics (permanent internal electric dipoles) and therefore a high dielectric constant [14].

Developments in thin film technology and materials deposition processes have contributed significantly to semiconductor applications and nanotechnology. Recently, metal oxide thin films such as TiO₂ (εᵣ = 20), HfO₂ (εᵣ = 22), ZrO₂ (εᵣ = 25), and Ta₂O₅ (εᵣ = 35) are being considered for the dielectric layer in the RF MEMS
capacitive switches [15-18]. Efforts to find new materials for MEMS switches, especially high dielectric constant materials, are expected to continue along with other emerging technologies.

1.2 Cu/Sn SLID Interconnects for RF Applications

In advanced RF MEMS as well as with conventional RF and microwave devices, the packaging approach is becoming more significant, particularly in terms of low-temperature packaging, integration methods, and cost efficiency. Flip-chip bonding for interconnections is a more promising technology for RF devices than conventional wire bonding, which has inherently higher signal loss. Flip-chip bonding is a cost-effective technique for realizing low interconnect resistance and inductance, and enables miniaturization and direct RF circuit integration. Solder bumping, Au/Sn eutectic bonding, and Au/Au thermo-compression bonding are primarily used in the flip-chip bonding of RF devices [19]. In this thesis, chip-scale Cu/Sn solid-liquid-inter-diffusion (SLID) flip-chip bonding was investigated and demonstrated. SLID is comparable to other flip-chip bonding methods in terms of cost efficiency and electrical performance.

Cu/Sn SLID interconnects have demonstrated low resistivity, high bonding rate, and high thermodynamic stability of up to 600°C (ε-Cu3Sn) [20]. Furthermore, Cu is a common back-end metal for CMOS devices, therefore, Cu/Sn SLID bonding is potentially compatible with CMOS for monolithic integration [21]. Second, the Cu/Sn SLID bonding process is economical as Cu and Sn can be electroplated. Electroplating is a low-temperature deposition process that offers a controllable metal-plating thickness. Almost any solder bump shape can be plated using photoresist molds and principally, it is cost-effective as compared to lift-off and other deposition methods.

SLID intermetallic compounds (IMCs) are created by reaction and diffusion between low- and high-melting point metals brought into contact with each other. When the temperature applied to the SLID interconnects is increased above the low-temperature melting point, an inter-diffusion process begins within the two metals. During annealing, reactions at the contacts transform the liquid phase into
solid IMCs [20]. Compared to a Au/Sn IMC, which is rather complex and consists of various phases, Cu/Sn SLID interconnects initially form two phases, $\eta$-$\text{Cu}_6\text{Sn}_5$ and $\varepsilon$-$\text{Cu}_3\text{Sn}$. Initially $\eta$-$\text{Cu}_6\text{Sn}_5$ is formed along the joint-axes between Cu and Sn. During continuous thermo-compression treatment, $\eta$ is dissolved into $\varepsilon$, resulting in only a $\varepsilon$-$\text{Cu}_3\text{Sn}$ IMC in the interconnect after all Sn is consumed [20].

A three-dimensional illustration of chip-scale flip-chip bonding of an RF MEMS switch is shown as an example in figure 1.2. Recently, various wafer-scale RF MEMS packaging methods have been reported, using Au/Au thermo-compression bonding [8, 20, 21], Au/Sn eutectic bonding [22], and Cu/Sn SLID bonding [19]. All use hermetic or near-hermetic metal seals to protect the movable structures, and all bonding methods share the common challenge of incorporating a feed-through that connects the device (flip-chip) to the external circuit outside the package. Buried feed-throughs [17, 21] and vias using Cu [22] appear to be the most promising approaches. Very recently, successful RF MEMS packaging techniques using silicon-on-insulator wafers with Au/Au thermo-compression bonding were demonstrated [4], with no diminishment of mechanical performance or decrease in RF switching time.

For this thesis, as a first step for realizing a low-cost Cu/Sn SLID RF MEMS packaging and direct-integration approach, the interconnect design was analyzed and various bonding tests were performed. High-performance RF feed-throughs and hermetic sealing will be introduced in future work. For simplicity, this study used a CPW flip-chip mounted onto a substrate in place of an active RF MEMS device. This allowed for detailed analysis and investigation of the manner in which a SLID interconnect influences the high-frequency performance of a direct package and integration approach.

![Figure 1.2 3D-schematic illustration of chip-scale flip-chip bonding structure](image)
1.3 Objectives of the work

This thesis endeavors to characterize dielectric thin films of ZrO$_2$ and dual layer PZT/ZrO$_2$ thin films for RF MEMS capacitive switches. The thesis also investigates the dielectric and acoustic properties of ferroelectric PZT thin films at frequencies in the gigahertz range. In this thesis, dual layer PZT/ZrO$_2$ thin films are suggested for use in RF MEMS capacitive switches and RF tunable capacitors. In addition, RF measurements characterizing both dielectric and acoustic properties of PZT thin films on the same measurement set-up are demonstrated using an metal-insulator-metal (MIM) capacitor with an annular ring slot.

Part of this thesis investigates the feasibility of Cu/Sn SLID interconnects for RF MEMS and RF/microwave devices. To determine the manner in which the electrical characteristics of IMC layers influence the high-frequency performance of RF devices and RF MEMS devices, 3D SLID interconnects comprising Cu and Sn are designed and simulated. An IMC created between Cu and Sn has low electrical resistivity, a high bonding rate, high thermodynamic stability, and their processing is economical (Cu and Sn can be electroplated) [20, 22]. It is also possible to calibrate and control the thickness of the electroplating quite well. The electrical resistivity of Cu$_3$Sn, an IMC in the interconnects, is lower than that of Sn. In addition, the melting point and Young’s modulus of Cu$_3$Sn is higher than that of Sn, a low melting-point material [44]. As a test vehicle, CPW structures are fabricated on the glass wafers, die, and substrate using a flip-chip bonder.

This thesis also covers the microfabrication process of RF MEMS capacitive switches, based upon surface micromachining techniques, wherein the release process is used to suspend membrane structures. Dual layer PZT/ZrO$_2$ thin films, verified in the characterization process, are employed for the dielectric layer. The processes were performed at the SINTEF MiNalab and HiVE clean room.
1.4 Thesis outline

Chapter 2: Experimental methods and characterization techniques for dielectric thin films
Experimental methods and characterization techniques for a thorough understanding of the dielectric properties of high-κ dielectric thin films, particularly at microwave frequencies where RF MEMS switches operate, are presented. The surface morphology was analyzed using atomic force microscopy (AFM), and the cross section of the films were investigated using focused ion beam (FIB) and scanning electron microscopy (SEM). The phase and crystalline analyses of the films were investigated using X-ray diffraction.

Chapter 3: Study on CuSn SLID Interconnects for RF Applications
The concept of flip-chip integration of RF MEMS devices using Cu/Sn SLID interconnects is presented. The feasibility of applying CuSn SLID interconnects for RF application is discussed. The chapter includes theory, design, simulation, and experiments.

Chapter 4: Microfabrication process of RF MEMS capacitive switches with PZT/ZrO₂ thin films
The RF MEMS switch process is presented with process flow and a discussion of the results. In addition, a MEMS capacitive switch with PZT/ZrO₂ thin films for achieving high capacitance ratio is demonstrated.
CHAPTER 2

2. EXPERIMENTAL METHODS AND CHARACTERIZATION TECHNIQUES

This chapter provides descriptions of dielectric thin film characterization techniques as well as experimental methods for investigating high-κ materials comprising PZT, ZrO₂, and PZT/ZrO₂ thin films. The ways in which the microwave dielectric properties of high-κ dielectric thin films can be effectively characterized are presented using conformal mapping methods and RF test devices such as CPW and MIM capacitors. Instrumental techniques for characterizing material properties are also introduced.

2.1 Microwave dielectric properties

High-κ dielectric thin films including ferroelectric thin films have been researched for many different RF applications such as constructing high density RF MIM capacitors, ferroelectric tunable phase shifters, and tunable capacitors for tunable filters and RF MEMS switches [15, 23-26]. The operating frequency range of RF devices is typically from MHz to GHz. Dielectric properties at high frequencies are generally different from those at low frequencies. Therefore, the characterization of dielectric properties over a wide range of frequencies plays an important role in estimating device and system performance.

Many different methods have been developed and employed for measuring dielectric constants and the loss of dielectric thin films at high frequencies. The high-Q resonator technique is frequently used for obtaining measurements at high frequencies[27]. However, the primary disadvantage of this method is that the measurements are applicable only over a narrow frequency band [28] and this method can only be applied to materials with very low losses. Other methods are widely accepted for characterizing dielectric thin films using the transmission and
reflection coefficient in RF devices such as coplanar waveguide (CPW) and metal-insulator-metal (MIM) capacitors. Using these methods, dielectric properties with low and high losses can be investigated over a wide range of frequencies, and have been successfully characterized over the past several decades [29, 30]. In the case of characterizing ferroelectric thin films, the use of two devices, CPW and MIM capacitors, becomes more important as they make it possible to investigate the effects of AC electrical field directions on their dielectric properties. Interdigital capacitors are also widely used to characterize dielectric thin films at high frequencies. However, the pattern feature obtained is generally very small between the arms ranging over ~2-4 μm [31]. When employed for test devices, processing cannot be carried out easily using standard photolithography. In addition, the frequency range for characterization is limited by quarter-wave length resonance, thereby resulting in a limited characterization frequency range [32]. In this thesis, two characterization methods that use CPW and MIM capacitors with annular ring slots were employed to investigate the dielectric properties of ZrO₂, PZT, and dual layer PZT/ZrO₂ thin films at microwave/millimeter wave frequencies.

2.1.1 Coplanar waveguides

A conventional CPW consists of a dielectric substrate and a conductor on a central strip separated by two narrow gaps arising from two ground planes on either side. Figure 2.1 shows a cross-sectional view (left) and top view (right) of a conventional CPW.

![Figure 2.1 Schematic cross-sectional view of a conventional CPW](image)
CPWs have been used in microwave monolithic integrated circuits (MMIC) such as millimeter-wave amplifiers, low-noise amplifiers, and harmonic mixers due to the ease of attaching to it both shunt and series circuit components [33, 34]. As transmission lines are placed in one plane on the substrate surface, via holes are not required. CPWs show low dispersion with little fringing field effect in air and their electric fields are mostly concentrated in the dielectric substrate due to the higher dielectric constant of the substrate. Recently, CPWs have been used to create RF MEMS capacitive shunt switches due to their coplanar configuration. Conventional CPWs do not have a conducting ground plane on the backside of the dielectric substrate and have low parasitic capacitances, making very small circuit layouts possible at high frequencies [35, 36].

In recent years, electrically tunable CPW phase shifters have been investigated using ferroelectrics such as BST and PZT thin films. This is due to the requirements of tuned circuits that are used in microwave devices such as tunable matching networks, tunable filers, and tunable phase shifters [24, 29, 37]. The phase shifter device also makes it possible to investigate dielectric properties over a very wide range of microwave frequencies [38]. Figure 2.2 shows a cross sectional view of a CPW phase shifter, in which conductor transmission lines are patterned on the ferroelectric thin film and dielectric substrate.

![Figure 2.2 Schematic cross-sectional view of a CPW phase shifter](image)

Microwave characterization techniques for dielectric thin films have been developed along with ferroelectric tunable phase shifters and conformal mapping (CM) [32, 39]. CM makes it possible to map complicated geometries into simpler ones and provides closed-form formulas for the effective dielectric constant of a
characterization device from which desired dielectric thin film properties can be obtained. The CM technique assumes a quasi-static transverse electromagnetic mode of propagation along the RF transmission line. The effective dielectric constant ($\varepsilon_{\text{eff}}$), characteristic impedance ($Z_0$), and attenuation ($\alpha$) of the CPW structure are determined by the size of the central signal line ($S$), the slot gap ($G$), the thickness, and the permittivity ($\varepsilon_r$) of the dielectric substrate. The relationship between $\varepsilon_{\text{eff}}$ and the geometrical parameters of the CPW structure is obtained from CM methods especially for CPWs as follows. A detailed explanation of how the equations are derived is found in appendix:

$$
\varepsilon_2 = \frac{\varepsilon_{\text{eff}} - \left( (1 + q_1(\varepsilon_1 - 1)) + q_2\varepsilon_1 \right)}{q_2}
$$

(2.1)

Here, $\varepsilon_{\text{eff}}$ is the effective dielectric constant of the CPW, and $q_1$ and $q_2$ are geometrical factors corresponding to the substrate and dielectric films, respectively, described in detail in the appendix A.1. $\varepsilon_1$ is the relative dielectric constant of the substrate.

The $\varepsilon_{\text{eff}}$ of a CPW with a dielectric layer placed on top of the substrate can be obtained from the phase of the transmission coefficient ($S_{21}$).

$$
\phi(\circ) = \frac{360\sqrt{\varepsilon_{\text{eff}}fL}}{c}
$$

(2.2)

Here, $c$ is the velocity of light in a vacuum, $l$ is the de-embedded transmission line length after calibration and $f$ is the frequency in hertz (Hz).

As long as the phase of a CPW line can be measured using a network analyzer, the dielectric constant of the dielectric films is easily obtained with high accuracy. On the other hand, as long as the dielectric substrate is an effective insulator with
high resistivity, the dielectric loss is obtained using a complex form of the effective dielectric constant as follows:

$$\varepsilon_{\text{eff}} = - \left( \frac{\alpha + j \beta_g}{\beta_o} \right)^2 \tag{2.3}$$

The complex propagation constant consisting of an attenuation constant ($\alpha$) and a phase constant ($\beta_g$) can be obtained using a multiline method, TRL calibration method, and ABCD parameter matrices based on measured scattering parameters [28, 32]. Here $\beta_o$ is the propagation constant of air.

One of the conditions to be satisfied when using CM properly is that the conductor of the CPW on any dielectric layer should not incur a loss [40]. However, the CPW metal does have a finite conductivity and experiences conductor loss that induces the slow wave effect at low frequencies [41]. Using high-temperature superconductor (HTS) films may solve this issue [28]. However, HTS materials show inhomogeneous nonlinear surface impedance, which is a crucial problem in applying HTS materials to microwave applications [42]. In order to remove the conductor loss contribution to the overall measured loss, a reference CPW line without any dielectric layers as seen in figure 2.1 can be used. This is what is termed the two-measurement method (TMM)[32]. By subtracting the measured effective dielectric constants of two CPWs, one with a dielectric layer (figure 2.2) and the other without a dielectric layer (figure 2.1), the complex dielectric constant of a dielectric layer can be obtained as follows:

$$\varepsilon_2 = \varepsilon_1 + \frac{1 + q_1 (\varepsilon_1 - 1)}{q_2} \frac{\varepsilon_{\text{eff}1} - \varepsilon_{\text{eff}2}}{\varepsilon_{\text{eff}2}} \tag{2.4}$$

Here, $\varepsilon_{\text{eff}1}$ and $\varepsilon_{\text{eff}2}$ are the effective dielectric constants of the CPW structure with and without dielectric thin films, respectively.
2.1.2 Metal-insulator-metal (MIM) capacitors

Metal-insulator-metal (MIM) capacitors are key components in RF and mixed signal integrated circuit (IC) applications [43]. They are applied in tuning filters and impedance matching networks as well as for DC filtering in RF IC and especially for dynamic random access memory devices [44, 45]. Recently, substantial effort has been put into increasing their capacitance density to reduce chip size and cost [15]. The use of high-κ dielectrics has been investigated, as reducing the dielectric thickness to increase the capacitance density will increase the undesirable leakage current [46]. Many different high-κ dielectrics as well as ferroelectric thin films such as ZrO₂, HfO₂, Al₂O₃, Ta₂O₅, SrTiO₃, PZT, and BST have been characterized using this device [15, 46-50]. Dielectric properties are frequency dependent, in that as the frequency increases they become lossy and dispersive. It is, therefore, important to investigate high-κ dielectric properties at high frequencies, especially for a wide range of applications. The low-frequency characterization of the dielectric thin films is easily achieved by performing C–V measurements. However, as the frequency increases and reaches the microwave/millimeter-wave range, the large reflection in signal yields results in unreliable measurements.

Several microwave measurement techniques have been suggested for the characterization of dielectric thin films using MIM capacitors [51, 52]. Among them, the technique proposed by Ma et al., [53] has been successfully employed for thin films with high and low dielectric constants, and continues to be improved upon [54]. The method is efficient in that sample preparation is simple and only the top metal layer must be patterned to complete the test devices without any processing of the dielectric layer. It is also suitable for the characterization of dielectric thin films in the broadband range at microwave frequencies with high accuracy [30, 55].

Figure 2.3 shows a top schematic view of two MIM capacitors with different sized annular ring slots that are used in the measurement technique proposed by Ma et al.[53]. The outer radius is the same, while the inner radius is different. In the case of only one RF measurement using one capacitor, the parasitic effect
induced by the outer ground electrode cannot be avoided. However, the effect can be effectively removed using two test structures with differently sized annular ring slots while maintaining the same outer radius for the top metal layer. Figure 2.4 shows a schematic cross-sectional view of an MIM capacitor and a CPW wafer probe on a metal-dielectric-metal layer deposited on the Si substrate. The MIM capacitor test structure makes it possible to measure the one-port reflection measurement of the device, and then the data input to (2.5) and (2.6) is converted to the impedance of the device. The PZT, ZrO₂, and PZT/ZrO₂ thin films characterized in this thesis are placed in the dielectric layer of the test structure. An equivalent model with an annular ring slot is seen in figure 2.5.

Figure 2.3 Schematic top view of an annular ring capacitor

Figure 2.4 Schematic cross-sectional view of a test wafer with an annular ring MIM capacitor and dielectric layer
The formulae for determining the complex dielectric constant of a dielectric thin film are described as follows [54]:

$$\tan \delta = \frac{\varepsilon_2}{\varepsilon_1} = \frac{(R_s/2\pi) \ln(a_2/a_1) - R_1 + R_2 + R_{c1} - R_{c2} + R_{tc1} - R_{tc2}}{X_1 - X_2 - \omega(L_{tc1} - L_{tc2})}$$  \hspace{1cm} (2.5)

$$\varepsilon_1 = \frac{t \left(1/a_2^2 - 1/a_1^2\right) \left(\left(X_1 - X_2\right) - \omega(L_{tc1} - L_{tc2})\right)}{\omega \pi \varepsilon_\infty} \left\{\left(\frac{1}{a_2^2} - 1\right) \left(\frac{1}{a_1^2} - 1\right) + \left(\frac{R_s}{2\pi} \ln(a_2/a_1) - R_1 + R_2 + R_{c1} - R_{c2} + R_{tc1} - R_{tc2}\right)^2 \left(\frac{R_{cs2} + R_{tc1} - R_{tc2}}{R_{cs2} + R_{tc1} - R_{tc2}}\right)\right\}$$  \hspace{1cm} (2.6)

Here, $a_1$ and $a_2$ are the different radii of the inner circle electrodes (figure 2.4), $R_s$ is the sheet resistance of the bottom electrode, $R_{tc}$ and $L_{tc}$ are the resistance and the inductance of the top circular electrode, respectively, and $R_{cs}$ is the resistance...
of the bottom electrode of the inner circular capacitor (C). The resistances $R_c$ and $R_{sc}$ and the inductance $L_c$ were calculated on the basis of a Bessel function of the first kind and zero order [53, 56].

Figure 2.6 (left) shows the top view of an MIM capacitor with an annular ring slot processed using a standard lithography process. The capacitor includes PZT and ZrO₂ thin films. A cross-sectional image of one of the test wafers milled by FIB and with an MIM capacitor structure for characterization is seen in Figure 2.6 (right). As seen above in (2.6), the dielectric constant varies with the dielectric film thickness. Therefore, it is important to determine the precise dielectric film thickness in order to obtain the correct dielectric constant. FIB milling and imaging provides accurate information about the thickness of PZT film and investigates the PZT nanostructure, therefore making it possible to analyze and characterize correctly both the test structure and PZT thin film. It was found that a PZT thickness of 340 nm exists between 720 nm Au and 220 nm Pt. Although Cr and Ti were deposited due to adhesion, they were so thin that the layers were not labeled on the figure. Carbon was deposited as a protective capping layer for cross sections and used to reduce charging on samples [57]. The top Au layer was patterned to have an annular ring structure as mentioned above to obtain the dielectric properties at high frequencies.
2.2 On-wafer RF measurements

S-parameter measurements of the test devices with dielectric layers that should be characterized were performed by using a vector network analyzer (Agilent E8364B, Rhode & Schwarz ZVM and HP 8510C) with RF probes, such as a GGB Picoprobe GSG-250 μm, a Cascade Microtech GSG-200 μm, and an infinity probe with a pitch of 200 μm. An on-wafer calibration routine using a calibration substrate provided by a probe manufacturer such as Picoprobe and Microtech was completed before performing the measurements. In order to investigate the DC electric field induced dielectric properties, a power supply system such as E5270 DC analyzer (Agilent Technologies) was connected to the network analyzer so that a DC bias could be applied to the test devices (MIM capacitor and CPW) through the RF probes.

2.3 Structural investigations

The crystalline material structures of PZT, ZrO₂, and PZT/ZrO₂ thin films were analyzed by grazing incidence X-ray diffraction with Cu K alpha radiation (GIXRD, Bruker D8 Discover). X-ray diffraction is a nondestructive technique that is used to
2.4 Thickness measurements

To accurately characterize the dielectric properties, it is necessary to know the dielectric film thickness. Film thicknesses of both conductors and dielectrics have been measured by a stylus profilometer from Detak 150 Veeco after patterning by wet etching. The device can take measurements within the range of a few nanometers to hundreds of micrometers with very high accuracy. On the other hand, metal layers and devices have also been characterized with a Wyko NT9100 optical profiler using white-light interferometry. The fringe pattern generated by interference that occurs between light reflected from a reference surface and from a target microbeam provides a three-dimensional profile. This is very useful in that the profiles of released MEMS switches can be measured without touching them. The thicknesses of nanosized thin films were measured using focused ion beam (FIB, SMI3050TB) and field emission scanning electron microscopy (SEM, JSM7500F). Figure 2.7 shows a test wafer for characterization with PZT/ZrO₂, which was milled by FIB and observed in detail by FESEM.
2.5 Electrical properties

The electrical properties of dielectric thin films have been investigated by making current-voltage (IV) measurements using a Keithley 6430 source meter. IV measurements are typically used to identify the electrical characteristics of semiconductor devices and are also essential for developing new materials and devices. They are also commonly performed to determine the resistance or conductance, leakage current, time dependent dielectric breakdown (TDBD) characteristics, and charging mechanisms of dielectric thin films. Figure 2.9 shows the picture of a ZrO$_2$ MIM capacitor where the probe tip is in contact with the bottom layer after patterning.

Figure 2.8 Picture of a ZrO$_2$ MIM capacitor
2.6 Dielectric properties of high-κ dielectric thin films

2.6.1 PZT thin films

Ferroelectric thin films have been researched for application in nonvolatile ferroelectric random access memories (FeRAMs), piezoelectric microsensors and microactuators, and tunable capacitors for RF devices and ultrasound transducers [58]. Materials that exhibit ferroelectricity show reversible spontaneous electric polarization and hysteresis loops at Curie temperatures. Ferroelectrics show nonzero electric polarization in the absence of an applied electric field and the direction of spontaneous electric polarization can be reversed by an applied field directed in the opposite direction. Above its Curie temperature, a ferroelectric crystal is no longer ferroelectric and shows only dielectric characteristics. Among many ferroelectrics, Pb(Zr,Ti)O₃ (PZT) films are most promising for meeting all of the applications noted above due to their superior properties including large remanent polarization and piezoelectric coefficient [59]. In addition, PZT thin films have large dielectric constants, and great efforts to apply PZT thin films to high density MIM capacitors for RF applications have been undertaken due to their large dielectric constants [60, 61].

Although PZT thin films have been considered as potential material for RF and microwave applications, large dielectric relaxation and losses at microwave frequencies prevents PZT from being applied to microwave devices due to the acoustic shear wave emission caused by movement of the domain walls [62]. The dielectric properties of PZT thin films depend upon the thickness of the films [5, 6]. Although the piezoelectric and dielectric properties of PZT thin films have been reported by many researchers [7, 8] in addition to their dependence on film thickness [9, 10], there remains a lack of data relating to the effect of film thickness on the dielectric properties in the gigahertz frequency range. Therefore, the investigation of PZT thin films is very appealing, particularly for high density MIM capacitors that are operated in the gigahertz range [63].
On the other hand, the thin film bulk acoustic resonator (FBAR) is now very promising and critical in wireless communication devices, such as a filter and duplexer, due to its small size and high performance, such as a high Q factor [64]. So far, various materials such as PZT, AlN and ZnO have been investigated for the FBAR applications. AlN is the most commonly used material for high frequency applications due to its lower acoustic losses. However, with respect to the realization of broadband filter applications, PZT thin films also have been extensively researched for their large electromechanical coupling coefficients and due to their matured deposition process technology [65]. Therefore, the effects of acoustic resonance responses induced by its DC electric field dependent piezoelectric and electrostrictive properties using a one dimensional (1-D) electro-acoustic model in a multilayer capacitor structure have also been investigated. Measurements and detailed analyses of the dielectric and acoustic properties of PZT thin films have been reported [63]. A large dielectric constant and moderate loss tangent ( < 0.1 at 4 GHz) were observed, suggesting that these CSD PZT thin films may be suitable for use in RF applications such as high density MIM capacitors. The thin films may also be applicable in RF tunable devices that require high tunability, ~34% at 280 kV/cm. Acoustic resonance analyses with DC bias voltages for the multilayer capacitor structure for PZT thin films showed the possibility of DC electric field dependent tuning of the films with a resonant frequency shift of ~15 MHz at 280 kV/cm.

2.6.2 ZrO₂ thin films

Zirconium dioxide (ZrO₂) ceramic is one of the most extensively studied materials in existence and has been used in many different areas such as oxygen sensors and medical applications [66, 67]. It is a ceramic with three different crystalline structures, monoclinic, tetragonal, and cubic, which are produced depending upon the processing temperature. The dielectric constant of each structural phase of ZrO₂ is different: the monoclinic phase is 19.7, the tetragonal phase is 36.8, and the cubic phase is 46.6 [68]. ZrO₂ thin films have recently
received much attention as a gate oxide material for CMOS devices due to the
excellent properties of ZrO₂ such as high dielectric constant, large breakdown
strength, and high thermodynamic stability at high temperatures [26, 68]. In
particular, the high dielectric constant of ZrO₂ is attractive for CMOS devices as
their dimensions using ZrO₂ can be greatly decreased due to its increased
capacitance density. Over time, the complexity of integrated circuits has been
continuously increasing, and thus efforts to develop thin films with high dielectric
constants will continue.

Attempts have been made to apply ZrO₂ thin films to RF MIM capacitors in
RF/mixed-signal integrated circuits, decoupling, filtering, oscillating, etc. [15, 43].
The current thesis work characterized the dielectric properties of ZrO₂ and
investigated the feasibility of using ZrO₂ as a dielectric layer for RF MEMS
capacitive switches. An improvement in the switch performance and high on-off
capacitance ratio can be achieved using a material with a high dielectric constant.
Although RF MEMS switches that possessed a ZrO₂ dielectric layer were
successfully demonstrated [69] and found to have a long switch lifetime, there
remains a lack of desirable dielectric properties (relaxation and loss tangent)
especially at microwave frequencies. RF measurements and characterizations for
ZrO₂ films were reported up to 5 GHz by Bertaud et al. [7]. However, the dielectric
properties at microwave frequencies, and particularly at frequencies where RF
MEMS switches operate, have not yet been reported. In addition, most of the
literature on ZrO₂ thin films have examined dielectric constants at very low
frequencies [70, 71]. Therefore, in the present thesis work, ZrO₂ thin films were
characterized up to 50 GHz using both metal–insulator–semiconductor (MIS)
structures and MIM capacitors. In addition, electrical properties using I-V
measurements were examined to find the leakage current and breakdown field
strength. Microwave characterization was performed on fabricated test wafers
with CPW and MIM capacitor devices. Figure 2.10 shows an SEM image of an MIM
capacitor structure with ZrO₂ thin films and figure 2.11 shows the X-ray diffraction
crystalline structure of ZrO₂, which details a tetragonal phase in the MIM capacitor.
The dielectric constant measured at 50 GHz indicated that ZrO₂ is promising due to
the high dielectric constant of ~25 in the MIM capacitor structure and ~22 in the CPW structure. The dielectric loss was measured to be lower than 0.1 at 50 GHz. In addition, the root mean square (RMS) surface roughness measured by AFM was 3 nm. Finally, the breakdown field strength was larger than 2.6 MV/cm. Discussions and analyses on the ZrO₂ thin films including the film deposition process and characterization methods and techniques were reported previously [26].

Figure 2.9 FE-SEM image of a test wafer with a patterned Au/Cr layer on a ZrO₂ thin film. Cr is not seen in this figure due to thin layer.

Figure 2.10 XRD pattern of a 250 nm ZrO₂ film on TiW/Au/TiW/Si substrates
2.6.3 PZT/ZrO₂ thin films

The use of a PZT thin film in RF MEMS capacitive switches is very promising due to large dielectric constants at GHz frequencies. However, as mentioned above related to PZT thin films, large relaxation and loss cannot be avoided. In addition, the breakdown field strength of a PZT thin film may be not large enough for typical actuation voltages of more than 30 V due to the typical dielectric thickness used in MEMS capacitive switches. Increasing the dielectric thickness increases the breakdown voltage. Therefore, more complex processes such as planarization need to be used with increasing process cost and concomitant decreases in down-state capacitance. Above all, the conductivity of Pt, which is a typical seed layer for growing PZT films, is lower than that for Au, which is typically used in MEMS switches. As a result, the insertion loss will increase. Therefore, in this thesis, in order to take advantage of the large dielectric constant of PZT, ZrO₂ thin film as a buffer layer that was already fully characterized as detailed above was proposed. ZrO₂ can serve as a buffer layer as well as a seed layer for PZT films. The ZrO₂ insulating buffer layer controls PZT film nucleation, orientation, and its growth rate [4]. Additionally, ZrO₂ thin films exhibit excellent dielectric properties including a large breakdown field strength. The electrical properties of PZT/ZrO₂ thin films have already been investigated by several authors, who observed large dielectric constants for dual layer PZT/ZrO₂ thin films with outstanding properties [72]. Furthermore, the dielectric loss of PZT thin films with a second dielectric material that has low dielectric loss may be decreased, especially at high frequencies [73]. There are a few reports on the dielectric properties of dual-layer thin films comprising a PZT thin film combined with a ZrO₂ buffer layer [4], however, only low frequencies measurements were conducted. Therefore, characterization of the microwave dielectric properties of PZT/ZrO₂ thin films is appealing for investigating the feasibility of their use in RF MEMS capacitive switches.

In order to characterize thin films, two test wafers with a CPW structure and an MIM capacitor with annular ring slots were fabricated including PZT/ZrO₂ thin
films so that the effects of the electromagnetic direction on the dielectric properties of a dual-layer could be investigated. Three different PZT thicknesses were designed to investigate the effects of thickness on the dielectric properties. Detail processes for the test wafers and characterization results with analyses were previously reported [74]. Figure 2.12 shows an SEM image of a test wafer with PZT/ZrO₂ thin films deposited on the bottom electrodes (TiW/Au/TiW) before top metal layers of Au and Cr were deposited. Following this, figure 2.13 shows an FIB image of a cross-sectional view of the CPW structure with PZT/ZrO₂ thin films deposited on the Si substrate. It was found that the dielectric loss of the dual-layer was significantly reduced compared to single the PZT film, which retained its large dielectric constant, and depended upon the PZT thickness and AC electric field direction. The dielectric constant measured for the CPW test structure was 80–130 at 50 GHz and the loss tangent was approximately 0.1 at 50 GHz. The experimental results for high dielectric constants (>50) and moderate loss tangent (<0.1) suggest that if a PZT thin film is combined with ZrO₂, then a dual-layer PZT/ZrO₂ stack may be used in microwave devices such as RF MEMS capacitive switches and tunable varactors. Figure 2.14 shows the top view of a CPW with PZT/ZrO₂ thin films deposited on a high resistivity Si wafer.

Figure 2.11 SEM image of a cross-sectional view of PZT/ZrO₂ thin films on metal layers
Figure 2.12 FIB image of a cross-sectional view of a CPW structure with PZT/ZrO₂ thin films

Figure 2.13 Top view of a CPW with PZT/ZrO₂ thin films; only part of the CPW near the taper is shown
2.7 Chapter summary

In this chapter, characterization methods and techniques for dielectric thin films with high dielectric constants are briefly presented. The test devices that were used for the characterizations are microfabrication compatible. Based on these characterization techniques, three different dielectric thin films of PZT, ZrO₂, and dual layer PZT/ZrO₂ were characterized using various measurements and analyses. Characterization results revealed that both PZT and PZT/ZrO₂ thin films have a tunability large enough for the application of RF tunable capacitors. Especially PZT/ZrO₂ thin films may be appropriate for wideband application. Furthermore, their large dielectric constant at microwave frequencies up to 50 GHz makes them potentially suitable for high-isolation RF MEMS capacitive switches. Especially, it was found that a PZT thin film generally not considered for microwave devices due to a high dielectric loss with increasing frequency might be applicable when it is formed as a dual-layer with a ZrO₂ thin film. It is also found that a ZrO₂ thin film, so far only being considered for semiconductor devices, can be employed for the RF MEMS switches. On the other hand, the dielectric loss of the thin films is relatively high, ~0.1 at 50 GHz. This may decrease the resonance depth magnitude of the RF isolation of MEMS capacitive switches. In addition, power dissipation in the down-state position of switches may be increased due to the high dielectric loss with increasing frequency. It requires careful switch design in terms of power handling and heat sink performance.
CHAPTER 3

3. **Cu/Sn SLID INTERCONNECTS FOR RF APPLICATIONS**

Design description Flip chip (FC), where integrated circuit (IC) chips and MEMS devices can be directly mounted onto a circuit board with bond pads in a “face-down” manner, is the most favored assembly technology for high-density RF applications, due to the short bump interconnects that reduce parasitic impedances and enhance broadband properties even in the mm-wave frequency range [75, 76]. As FC does not require wire bonds, the electrical loss can be reduced and the chip size can be considerably smaller. The electrical connection is achieved through conductive bumps placed between the dies and the substrates. The bumps also function as mechanical connections to the dies.

In order to make interconnects, for the thesis work, we have chosen solid-liquid inter-diffusion (SLID) bonding techniques instead of Au-Au thermocompression bonding that is typically considered for RF applications [76]. SLID makes low-temperature bonding with low pressure possible; this may be very helpful for sensitive MEMS devices. On the other hand, Au-Au thermocompression bonding requires high pressure with a high temperature of ~300°C [77]. Further, SLID enables 3D integration for IC and MEMS devices [22, 78]. A wide variety of material choices is another advantage of SLID bonding. SLID bonding using Cu and Sn in particular receives wide attention due to the nature of the intermetallic compound Cu₃Sn. This possesses a relatively low electrical resistivity of 8.93 μΩ/cm and a large Young’s modulus of 108.3 GPa [79]. The melting point of Sn is 235°C, which could lower the process temperature, whereas the melting point Cu₃Sn is ~670°C, which is considerably higher than the melting point of Sn. Above all, the process is cost effective due to the use of electroplating and the materials used are less expensive than Au. The details of Cu/Sn SLID bonding can be found in [22, 80]. Here, we investigate the feasibility of Cu/Sn SLID interconnects for RF
applications including RF MEMS devices. This chapter is based on the published paper [81] and presents the design and simulation of Cu/Sn SLID interconnects and various experiments on FC bonding using CPWs fabricated on a glass wafer.

3.1 Design description

Figure 3.1 shows the cross-sectional view of the flip-chip bonding test structure for RF applications. For both the die and the substrate, the CPW layout is designed to have a 30-μm gap and a 240-μm width corresponding to the characteristic impedance of 50 Ω. The areas of the flip-chip-mounted CPW and substrate are 17.64 mm² and 4 mm², respectively. In this design, the dielectric overlap length of the flip-chipped die is 100 μm and the transition length is 350 μm. A 70 μm-radius circular bump pad is selected for the interconnects. In order to fully consume any Sn present in the interconnect and to reach a stable ε-phase, a Cu to Sn ratio of 1:1.3 is needed. Therefore, the height of the Cu film is at least 2.5 μm for a Sn thickness of 1.5 μm.

Note that Sn is only electroplated on the die, not on the substrate, as the substrate is held at ~270°C during bonding (the melting point of Sn is 235°C). During the bonding process, the die establishes contact with the substrate, which is heated. Thus, any Sn would melt and diffuse into the Cu bumps before bonding if it had been located on the substrate.
The substrates are fabricated from Pyrex 7740 glass wafers with Au sputtered to a thickness of 500 μm. A 450-nm-thick nichrome (NiCr) layer is used as an adhesion layer for the Au. After photoresist patterning, using Shipley S1828 on the Au layer, Cu is electroplated, followed by Sn electroplated on the Cu. Photoresist can be chosen in terms of compatibility and thickness required for Cu and Sn. The overall process steps to fabricate the die (chip) and substrate are presented in figure 3.2.
Figure 3.2 Fabrication process for die and substrate. The metals used in the SLID interconnect are electroplated directly on Au transmission line

3.2 Electromagnetic simulation

Two different solder alloys, Cu/Sn and Au/Sn, are used in the electromagnetic simulations and compared to each other. The resistivity of ε-Cu₅Sn (8.9 μΩcm) is obtained from experimental results in [80]. In order to estimate the Au/Sn SLID IMC resistivity, the weighted average of Au and Sn resistivity is used. The weighted percentages of Au and Sn after Au/Sn SLID bonding are 37% and 63%, respectively, corresponding to the AuSn₂ IMC [82]. This yields a resistivity of 3.46 μΩcm.

<table>
<thead>
<tr>
<th>Metals</th>
<th>Resistivity (μΩcm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Au</td>
<td>3 [83]</td>
</tr>
<tr>
<td>Cu</td>
<td>1.7 [80]</td>
</tr>
<tr>
<td>Sn</td>
<td>11.5 [80]</td>
</tr>
<tr>
<td>AuSn₂</td>
<td>3.46</td>
</tr>
<tr>
<td>Cu₅Sn</td>
<td>8.9 [80]</td>
</tr>
</tbody>
</table>
Any decrease in bump height after bonding resulting from interdiffusion or compression of the interconnects is assumed to be negligible. The Ansoft HFSS 3D simulator, using a finite element method, is then used to evaluate the electrical characteristics of the interconnects. Two-port S-parameters representing signal loss characteristics for Au/Sn and Cu/Sn may be seen in Figure 3.3. All simulations in this work have been conducted in the 1–50 GHz range. The insertion losses are -0.39 dB and -0.92 dB at 30 GHz and 50 GHz for Au/Sn and Cu/Sn interconnects. The two bimetallic joints show close to unity in the transmission loss. Moreover, there is little difference in the return loss between the two interconnects. The relatively large electrical resistivity of NiCr, 150 μΩcm [84] beneath the Au layer, and any skin-depth effects, are factored into the CPW losses. The large dielectric overlap length (100 μm) in the die and transition length in the substrate (350 μm) also contribute to the losses. In addition, the detuning effect and the change in characteristic impedance of the interconnects adds to the losses [76].

Figure 3.3 Simulated insertion and return losses for Au/Sn and Cu/Sn interconnects. Inset: 3D structure of flip-chip-mounted CPW. Circle bump has a 70-μm radius and the height is 6.5 μm. Cu layer is 2.5 μm thick and Cu3Sn (new phase after bonding instead of Sn) is 1.5 μm.

The simulation for optimization according to bump height, transition length, and radius variation has been performed based on [76], and the results can be seen in figures 3.4 and 3.5 and table 3. Four different Cu-bump heights, 6.5 μm, 10 μm, 20 μm, and 30 μm, were selected to evaluate the effects of bump height. The height of
the Cu$_3$Sn IMC was set to 1.5 μm for all simulations. In figure 3.4, the simulated results show that when the bump height increases, the return loss improves to a point that is near a resonance, and the insertion losses are identical up to 32 GHz. Table 3.2 shows the worst-case insertion and return losses, in the frequency band up to 50 GHz, for different bump heights. The effect of bump height is related to the change in characteristic impedance in the interconnect region. Before the resonance of the return loss, the inductance, increased by the bump height, compensates the capacitance that exists between the die and substrate, resulting in an improvement in the return loss while the low resistivity of the interconnect maintains the insertion loss.

![Figure 3.4 Simulated insertion and return losses with different bump heights. Cu height is set to 6.5 μm, 10 μm, 20 μm, and 30 μm. Cu$_3$Sn is kept constant at 1.5 μm.](image)

<table>
<thead>
<tr>
<th>Bump height</th>
<th>Insertion loss (dB) at 50 GHz</th>
<th>Return loss (dB) at 16 GHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>6.5 μm</td>
<td>0.88</td>
<td>16.82</td>
</tr>
<tr>
<td>10 μm</td>
<td>1.08</td>
<td>18.01</td>
</tr>
<tr>
<td>20 μm</td>
<td>1.22</td>
<td>18.75</td>
</tr>
<tr>
<td>30 μm</td>
<td>1.31</td>
<td>18.93</td>
</tr>
</tbody>
</table>
To understand the effect of the interconnection area on the RF performance, four different lengths were used, 90 μm, 110 μm, 150 μm, and 210 μm, instead of the 350-μm transition length, as illustrated in figure 3.5. The bump height was set to 15 μm. It may be seen that the return losses increase as the transition length decreases and vice versa. Beyond 37 GHz, there are only small improvements in transmission.

Figure 3.5 Simulated insertion and return losses with different transition lengths. Height of Cu and Cu3Sn is 6.75 μm and 1.5 μm, respectively. Different transition lengths are 90 μm, 110 μm, 150 μm, and 210 μm.

The influence of different bump pad areas was observed by varying five different bump radii: 10 μm, 20 μm, 50 μm, 90 μm, and 110 μm. The results show that there are very small variations in insertion and return losses at large bump radius. However, significant improvements in insertion and return losses are observed as the bump radius decreases.

Table 3.3 Simulated losses over different bump radius

<table>
<thead>
<tr>
<th>Radius (μm)</th>
<th>Insertion loss (dB) at 50 GHz</th>
<th>Return loss (dB) at 16 GHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>10</td>
<td>-0.75</td>
<td>-18.6</td>
</tr>
<tr>
<td>20</td>
<td>-0.78</td>
<td>-18.1</td>
</tr>
<tr>
<td>50</td>
<td>-0.91</td>
<td>-17.5</td>
</tr>
<tr>
<td>90</td>
<td>-1.04</td>
<td>-16.8</td>
</tr>
<tr>
<td>110</td>
<td>-1.06</td>
<td>-16.5</td>
</tr>
</tbody>
</table>
Furthermore, for compensation, and to enhance the return loss, a high impedance line increasing the inductance before the transition region on the substrate can be included [76]. In addition, return and insertion losses can be further reduced by etching the substrate underneath the die and in the transition region of the interconnections, resulting in reduction of impedance mismatch caused by the small distance between the die and substrate [85, 86]. This method of etching a substrate would be an alternative to increasing the bump height. For the skin-depth effect, the losses are improved by increasing the thickness of CPW, such as by sputtering a thicker Au layer, or selectively electroplating a thicker CPW.

3.3 Experiments

In this section, some experimental results of Cu/Sn SLID bonding are presented. Figure 3.6 shows the measured bump profile of an electroplated 2.1-μm-tall Cu bump on the Au-layer using a DEKTAK 150 profilometer. Figure 3.7 illustrates the measured 1-μm Sn bump, which was then electroplated on top of the previously measured Cu bump. Figure 3.8 shows the image of bottom substrate (left) and the top die (right) with CPWs test structures fabricated on the glass wafer.

Figure 3.6 Measured surface profile of electroplated Cu bump on Au seed layer
Before FC bonding, some tests were performed. Figure 3.9 shows the SEM image of a cross-sectional view of the bonded test sample with Cu-Sn layers. Cu and Sn were electroplated on Au/TiW/Si substrates. The thickness of Cu on the bottom substrate and on the top die was ~10 μm and ~5-6 μm, respectively, and the thickness of Sn electroplated on the bottom substrate was ~3–4 μm. The chips were bonded at 300°C in a vacuum chamber for ten minutes. In this experiment, both IMCs of Cu$_3$Sn and Cu$_6$Sn$_5$ were observed and confirmed by EDX. It is expected that the phase of Cu$_6$Sn$_5$ will be changed to Cu$_3$Sn if there is an excess amount of Cu present. After test bonding, FC bonding using CPWs with Cu/Sn bumps was performed on the FC bonder (MAT 6400) at 270°C for five minutes with a pressure of ~8 MPa. The bonded structure is seen in figure 3.10.
After observing interconnects using the microscope (figure 3.11 (left)), it was found that during bonding, Sn overflowed onto the Au layer, which may be attributed to the misalignment between the die and substrate as seen in figure 3.11 (right). The Sn surface on the Cu bumps of the die was observed before bonding (figure 3.12 (left)), and after detaching the die from the substrate (figure 3.12 (right)). Figure 3.13 shows the bonding failure due to the low bonding pressure of ~4 MPa, calculated from total bonding area on each wafer. It may be seen that only some parts of the bumps were contacted during bonding. Another experiment was performed with new designs, including a smaller Sn bump dimension than the Cu, with a goal of solving the Sn overflow problem.
Figure 3.11 Image of bumps on the die (left) and image of misalignment (right)

Figure 3.12 Image of Sn surface on the bump before bonding (left) and after bonding (right)

Figure 3.13 Image of Sn surface on the bump before bonding (left) and after bonding (right)

The small slot gap between the bumps and the Au layer, which is part of the CPW, was also considered in the design, as seen in figure 3.14, considering the misalignment of the die and substrate. It was of interest to investigate how the slot
gap dimensions of A and B influence the Sn overflow onto the Au layer, and to find the optimized dimensions for A and B. Here, we have chosen NiCr, from other low conductivity materials, to be a bottom layer in order to distinguish the Au layer with high conductivity, and designed test structures for the experiments. Figure 3.15 shows the schematic cross-sectional view of the test structure with the NiCr sub-layer. The design included various distances for gap ‘A’, i.e., 0, 5, 10, 15, 20, 25, 30, 35, 40, 45, 50, 55, 60, and 65 μm, and for gap ‘B’, i.e., 30, 40, 50, 60, and 70 μm. The test structures were fabricated using standard photolithography and electroplating as seen in figure 3.16. One chip for the die has both Cu and Sn layers, whereas the other chip has only a Cu layer for the substrate. The test structure was designed to be diced along the diced line in the middle of the chip in order to have 14 different gaps. The cross section of the diced chips can be examined to find the quantity of Sn that overflowed, or did not overflow, after bonding on to the Au layer with different slot gaps. The preliminary results of experiments indicate that FC bonding with minimum misalignment is critical to investigate correctly cross sections of bonded samples. If the misalignment is large, Sn easily overflows out of the gap of “B,” resulting in incorrect measurement results. Therefore, it is advantageous to have a large gap of “B.” However, RF degradation due to an NiCr layer with large resistivity of 1μΩ·m should be taken into account as the gap increases. Design should be carefully considered with electromagnetic simulations in order to investigate the effect of the NiCr layer. On the other hand, as long as FC bonding misalignment is minimized, it was possible to determine much Sn overflowed onto the NiCr layer depending upon the gaps of “A” and “B,” providing implications as to how to determine the gap size. In addition, it is important to examine other materials than NiCr, due to its large resistivity.
Figure 3.14 Schematic top view of suggested bump areas to avoid Sn overflowing

Figure 3.15 Schematic cross-sectional view of the test structure to investigate Sn overflow; chip with Cu/Sn layer (left) and chip with only Cu layer (right)

Figure 3.16 Top view of fabricated test structure with interferometer measurement (right bottom)
3.4 Chapter summary

In this chapter, 3D SLID interconnects consisting of Cu/Sn bimetals have been studied in terms of electrical characteristics using a flip-chip-mounted CPW. A 3D electromagnetic simulation on Cu/Sn SLID interconnects has been performed, with analysis and discussion, by varying the geometry of the interconnect structure. The RF performance can be improved by changing several parameters in the transition region of the interconnects: the interconnect height, transition length, and bump radius. Test bonding was performed to verify intermetallic compounds. CPWs with electroplated Cu and Sn bumps were fabricated on a glass wafer and bonded to each other using FC bonder. Test structures to investigate the Sn overflow were designed and fabricated. Future work requires observation of the cross sections of test samples after bonding in order to determine the dimension of slot gaps and Sn bumps that will be acceptable.
CHAPTER 4

4. RF MEMS SWITCH WITH HIGH-\(k\) MATERIAL

4.1 Introduction

High RF isolation is always a requisite for improving RF performance. Lower isolation might cause unexpected intermodulation, which degrades the overall RF system performance [87]. High isolation over a broad band of frequencies is also an important feature for RF MEMS switches. Many different methods have been developed to ensure high isolation for switches so that they have a high capacitance ratio, including complicated switch geometries and different switching mechanisms that require complex processes; this, however, can increase the process cost [7, 16, 87].

Several researchers have successfully developed RF MEMS capacitive switches using high-\(k\) material over the past several decades. Park et al. were the first to fabricate an RF MEMS capacitive switch using SrTiO\(_3\) (\(\varepsilon_r \equiv 30-120, \tan\delta < 0.02\) at frequency lower than 20 GHz) [88]. They reported a large capacitance ratio of 600 and broadband isolation up to 20 GHz. Subsequently, capacitive series and capacitive shunt RF MEMS switches using barium strontium titanate (BST) were developed by Wang [57] and Liu et al. [12], respectively. The reported dielectric constant and loss tangent of BST thin film are approximately 200 and 0.05 at 20 GHz [29, 57]. By comparing their switches with Si\(_3\)N\(_4\) MEMS switches, these researchers clearly proved that high-\(k\) material capacitive switches have many advantages, especially large and broadband isolation. They also found that the size of RF MEMS switches could be significantly decreased due to the high dielectric constant, which can potentially heighten the interest in high-\(k\) material RF MEMS switches with the further development of microfabrication process technologies.
Recently, many other reports have been published on MEMS capacitive switches using metal oxides such as TiO₂[18], HfO₂Nₓ[16], ZrO₂[69], and Ta₂O₅[17]. All of the above materials have been used for years in applications such as dynamic random-access memory (DRAM) and RF MIM capacitors, due to their high dielectric constants and excellent dielectric properties. Their dielectric constants are relatively smaller than those of ferroelectric thin films. However, their dielectric constant is still at least three times that of typical dielectrics such as SiO₂ and Si₃N₄. In addition, metal oxides exhibit a larger breakdown field strength than ferroelectrics. Zhang et al. [16] reported an MEMS switch with hafnium oxynitride (HfO₂Nₓ) that had a dielectric constant of 19. Their modifications included dielectric stabilization to not subject the switch to crystallization of HfO₂, which resulted in a substantially increased breakdown field strength (> 9.5 MV/cm). In particular, the dielectric constant of tantalum pentoxide (Ta2O5) is 32, which is relatively higher than that of other metal oxides. An MEMS switch using Ta₂O₅ exhibited an excellent switch performance with wide band isolation up to 40 GHz and without failure over one million switching cycles. The breakdown field was higher than 4 MV/cm. To the best of the author's knowledge, dielectric loss of Ta₂O₅ thin films at microwave frequencies is not reported elsewhere.

Recently, Thales R&D developed MEMS capacitive switches using a ferroelectric PZT thin film for the dielectric layer [10]. The Thales switch exhibits a very long life cycle of more than 10¹⁰ cycles, although there is concern over charging resulting in switching failure of the switch. On the other hand, the breakdown field strength of the PZT thin film, which is typically less than 1 MV/cm [31], can be a problem for its use as a dielectric layer. The pull-in voltage of MEMS switches is 20–40 V. PZT switches with typical dielectric film thicknesses of 150–200 nm will easily fail due to the dielectric breakdown. In addition, dielectric loss of PZT thin film is typically larger than 0.1 at 3 GHz [63].

NIST also developed RF MEMS capacitive switches using a PZT thin film; in particular, they used HfO₂ as a sublayer of the PZT thin film [89]. However, the dielectric properties of a PZT film, especially on HfO₂ thin film, are different from typical ferroelectric properties. A PZT thin film always requires a seed layer to
exhibit ferroelectric properties with a high dielectric constant. In addition, NIST did not report the microwave dielectric properties of dielectric thin films, including PZT and HfO₂, but only showed the dielectric constant up to 1 MHz; this means the switch analysis may be incorrect.

This thesis addresses the process development of RF MEMS switches, where both PZT and ZrO₂ thin films are used as a dielectric layer for the first time. ZrO₂ can be a seed layer for PZT thin films and has a higher dielectric constant than HfO₂, which was used by NIST. Both PZT and ZrO₂ thin films were characterized at microwave frequencies to show large dielectric constants—larger than 120 at 50 GHz. The breakdown voltage of dielectric layers, including the PZT thin film, increased due to the addition of ZrO₂ thin films. In particular, this switch process used the Au CPW layer instead of the more conventional Pt as a seed layer for the PZT film and also a transmission line to improve insertion loss. Thus far, only Pt has been considered as a material for the PZT thin film [87]. We did not modify materials such as HfO₉Nₓ but rather combined the advantages of each material’s intrinsic properties. Table 4.1 compares the performances of some representative RF MEMS switches with high-κ materials.

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<tbody>
<tr>
<td>Pull-in voltage (V)</td>
<td>35</td>
<td>8</td>
<td>20</td>
<td>30</td>
<td>40</td>
</tr>
<tr>
<td>Dielectric constant</td>
<td>200</td>
<td>30-110</td>
<td>32</td>
<td>19</td>
<td>190</td>
</tr>
<tr>
<td>Loss tangent</td>
<td>0.05 at ~20 GHz [29]</td>
<td>0.02 at &lt;20 GHz [88]</td>
<td>0.02 at ~10 kHz [100]</td>
<td>-</td>
<td>0.1 at ~3 GHz [63]</td>
</tr>
<tr>
<td>Capacitance ratio</td>
<td>175</td>
<td>600</td>
<td>19</td>
<td>200</td>
<td>400</td>
</tr>
<tr>
<td>Isolation (dB)</td>
<td>-36 at 26 GHz</td>
<td>-42 at 5 GHz</td>
<td>-40 at 25 GHz</td>
<td>-27 at 25 GHz</td>
<td>-38 at 10 GHz</td>
</tr>
<tr>
<td>Insertion loss (dB)</td>
<td>-1.51 at 40 GHz</td>
<td>-0.08 at 10 GHz</td>
<td>-0.8 at 30 GHz</td>
<td>-0.8 at 26 GHz</td>
<td>-0.1 at 40 GHz</td>
</tr>
<tr>
<td>Life cycle</td>
<td>-</td>
<td>-</td>
<td>1 million</td>
<td>-</td>
<td>10 billion</td>
</tr>
<tr>
<td>Sacrificial layer</td>
<td>Photoresist</td>
<td>Photoresist</td>
<td>Photoresist</td>
<td>Photoresist</td>
<td>-</td>
</tr>
<tr>
<td>Bridge release</td>
<td>CPD</td>
<td>CPD</td>
<td>Oxygen plasma</td>
<td>Oxygen plasma</td>
<td>-</td>
</tr>
</tbody>
</table>
This chapter also discusses the investigation of the release methods for RF MEMS switches. MEMS switches are generally released by wet or dry etching [90]. Wet etching is typically performed with acetone and methanol and subsequent use of a critical point drier (CPD) to avoid stiction of the suspended membrane down to the dielectric layer [91]. The most commonly used sacrificial layer is photoresist. Photoresist is easily processed, and its thickness is easy to control. It can furthermore be removed with nontoxic acetone. Photoresist can also be released by oxygen plasma in dry etching. The release process is one of the most important steps in the overall process and is directly related to the switch reliability. Therefore, both the wet and dry release methods were used to release the switches, and the results are discussed here. We present the development of a microfabrication process for MEMS capacitive switches that uses surface micromachining techniques. Here, copper oxide (CuO) was used as a dielectric layer, as it is easy to process and has a low material cost and high dielectric constant [13].

4.2 Copper oxide MEMS switch

4.3.1 Design

Figure 4.1 (left) shows a schematic MEMS capacitive shunt switch with dimension parameters. Figure 4.1 (right) shows that the RF performance of the capacitive shunt switch can be precisely estimated with a series RLC electrical circuit. The capacitance in the up- and down-states can be accurately computed by using parallel plate formulas; only the knowledge of the electrode geometries and dielectric material is required for this purpose. The return loss ($S_{11}$) in the up-state switch is defined by (4.1). The R, L, and C parameters can also be derived by fitting the measured S-parameters of the switch.
Figure 4.1 (left) Schematic of MEMS capacitive switch with doubly clamped beam and (right) equivalent circuit model for the switch

\[ S_{11} = -\frac{j\omega C_u Z_o}{2 + j\omega C_u Z_o} \] (4.1)

Here, \( Z_o \) is the characteristic impedance and \( C_u \) is the up-state capacitance as defined by (4.5).

\[ C_u = \frac{\varepsilon_o w S}{g_o + \frac{t_d}{\varepsilon_r}} \] (4.2)

RF isolation in the down-state is estimated using the down-state capacitance \( (C_d) \):

\[ |S_{21}|^2 \approx \begin{cases} 
\frac{4}{\omega^2 C_d^2 Z_o^2}, & f \ll f_o \\
\frac{4R_s^2}{Z_o^2}, & f = f_o \\
\frac{4\omega^2 L^2}{Z_o^2}, & f \gg f_o 
\end{cases} \] (4.3)

where \( f_o \) is the down-state resonant frequency of the capacitive switch.

The down-state capacitance with an air gap \( (d_i) \) due to incomplete contact (surface roughness) of the switch beam to the bottom dielectric layer is defined as follows:
\[ C_d = \frac{\varepsilon_o A}{2} \left( \frac{1}{d_1 + \frac{t_d}{\varepsilon_r}} + \frac{\varepsilon_r}{d_2} \right) \] (4.4)

where \( d_1 \) is the surface roughness of the dielectric layer. \( \varepsilon_r \) and \( \varepsilon_o \) are the permittivities of the air and dielectric layer, respectively.

The capacitance ratio, which is one parameter to rate switch performance, is calculated as follows:

\[
\frac{C_{\text{down}}}{C_{\text{up}}} = \frac{A \varepsilon_p \varepsilon_r}{t_d} = \frac{\varepsilon_r g_o}{t_d} + 1
\] (4.5)

When the bridge is under tensile stress, the pull-in voltage, which depends upon the geometry and residual stress of the bridge and air gap between the top bridge and bottom dielectric layer, can be estimated by using the 1-D model and is defined as follows:

\[
V_p = \sqrt{\frac{8g_o^3}{27\varepsilon_o S}} \left( \frac{t}{L} \right)^3 \left( \frac{32E}{8} \left( \frac{x}{L} \right)^3 - 20 \left( \frac{x}{L} \right)^2 + 14 \left( \frac{x}{L} \right)^1 - 1 + \frac{8\sigma(1 - \nu)(t/L)}{3 - 2(x - L)} \right)
\] (4.6)

Here, \( \sigma \) is the residual stress of the bridge. \( x \) is \((S + L)/2\). \( t \) is the bridge thickness.

If the bridge is not a simple rectangular beam, 3D electromagnetic and electromechanical analysis tools such as HFSS Ansys and CoventorWare can be used to verify the switch performance. In order to enhance the dry release process and switching speed and reduce the residual stress, small holes were designed on the beams. Switches were designed to have a pull-in voltage in the range of 5–30 V, and five different masks were designed using L-Edit; some switches are shown in
Figure 4.2. The process steps were designed based on surface micromachining technology and a high-resistivity Si substrate considering compatibility with integration with CMOS; the steps are presented in figure 4.3.

Figure 4.2 Switch masks designed in L-Edit

Figure 4.3 Process flow of MEMS switches
4.3.2 Fabrication and measurements

The MEMS switches were processed as follows. An N-type high resistivity (~10 kΩ/cm) Si wafer was dry thermally oxidized at 1100°C for 1 hour in a tube furnace (Hitech Furnaces), and 130 nm thick SiO₂ was measured after wet etching with 7:1 BOE. In order to fabricate CPW, metal layers of 15 nm Cr, 120 nm Au, and 15 nm Cr were sequentially deposited onto an oxidized Si substrate using a thermal evaporator. Cr on top of Au was used as an adhesion layer between the dielectric layer and bottom Au layer. Evaporation started at 6·10⁻⁷ mBar, and the pressure maintained lower than 1·10⁻⁵ mBar during the evaporation process to produce high-quality metal layers. The deposition rates of Cr and Au were ~0.3 and ~1.5 Å/s, respectively. Next, a standard photolithography process was performed to make a wet etching mask for the metal layers of CPW. Shipley S1813 positive photoresist was spin-coated at a rotation speed of 3500 rpm. The wafer was then soft-baked on the hot plate at 110°C for 1 minute. A mask aligner (Karl Suss) with g-line UV radiation source was then used to expose the wafer. The exposure time was 22 seconds under a UV intensity of 16.6 mW/cm². Next, the wafer was developed for 25 seconds using a microposit MF-319 developer. Au and Cr films were etched using etchants: the Cr etchant was made up of diammonium hexanitratocerate (10%–15%), nitric acid (15%–20%), and water (60%–70%); and the Au etchant consisted of potassium iodide (10%–30%), iodine (1%–10%), and water (60%–80%) (Suncem AB). Cr and Au were etched at rates of approximately 2 and 20 nm/s, respectively. In order to make the dielectric layer, a copper pellet was thermally evaporated with a tungsten boat; the evaporated Cu thickness was 250 nm. All Cu evaporation process parameters were the same as those for the Au and Cr evaporation processes. The Cu layer was then patterned by the lithography process followed by wet etching. The etching rate of Cu was ~60 nm/s. The Cu thin film was oxidized during dry release with oxygen plasma. According to [92], the Cu thin film transforms to CuO upon reaction with oxygen plasma after 15 minutes with a power of 200 W, pressure of 250 mTorr, and O₂ flow rate of 10 sccm. The hot plate was also used to oxidize the Cu thin film; the
wafer was put on the hot plate for 20 minutes at 250°C. A sacrificial layer was made using S1813, following the same process as above, however, a spin speed of 2200 rpm was used to produce a ~2.5 μm thickness. The thickness was variable due to the non-uniform drying of the solvent during spin-coating. The wafer was hard-baked at 110°C for 3 minutes; this was sufficient to prevent reflow of the sacrificial layer during thermal evaporation of Au and to make a smooth slope at the anchor of the bridge. A 50 nm thick Au seed layer was deposited using a thermal evaporator on top of the wafer for Au electroplating to make the switch beam thick. The same process parameters presented above for CPW metal layers were used, except the vacuum pressure was 5·10⁻⁵ mBar when evaporation started. It was difficult to check the temperature inside the evaporator chamber, given that an early start of the evaporation process may have prevented the sacrificial layer on the wafer from quickly becoming hard, in contrast to the case of heating with long evaporation times. Au electroplating was performed at a plating rate of ~0.3 μm/min and a temperature of 60°C. The resulting switch beam thickness was ~600 nm. We used both wet and dry etching with oxygen plasma to release the MEMS switches. A combination of dry and wet release may be preferable for complete photoresist removal [93]. The flow rate and pressure of the oxygen gas were 48 sccm and 500 mTorr, respectively. The RF power and time were 350–400 W and 60–100 min, respectively. Figure 4.4 shows the SEM images of processed RF MEMS switches after release with wet etching followed by dry etching, which was carried out to remove any residual photoresist.
Dry etching was not successful due to the remaining photoresist, as shown in figure 4.5. Instead, the bridge buckled due to overheating as more time passed. The next images show the switches after bridges were removed to check the photoresist residues.
The measured and simulated S-parameters in the up- and down-state are seen in figures 4.6 and 4.7, respectively. The extracted lumped elements in the equivalent RLC circuit model are for the down state position: resistance was 0.04 Ω, inductance was 8 pH, and capacitance was 13.3 pF. For the up-state, capacitance was 65 fF and insertion loss was -0.4 dB at 20 GHz. The CuO thickness was estimated to be 75 nm by extracting the down-state capacitance. Copper oxide exits in two phases, cupric oxide (CuO) and cuprous oxide (Cu₂O) [92]. However, it was assumed that only CuO exists on the dielectric layer. No dielectric relaxation of CuO was observed up to 40 GHz. The low series resistance was because of the almost complete contact of the switch bridges with the dielectric layer. In this experiment, the bridge was purposely made to adhere to the dielectric layer to measure the ideal isolation characteristics. The surface profile of CuO measured using a stylus profilometer exhibited an approximate thickness of <4 nm. MEMS switches with a high capacitance ratio may operate over a wide frequency range with large isolation depth; using CuO here demonstrated that the switch could operate from the X-band to the Ka-band.

The variation of isolation in the down state switch was investigated by simulating with (4.4). Dielectric thickness was changed from 50 nm to 300 nm with an increment of every 50 nm. The same switch dimension and dielectric layer as seen in figure 4.7 were used. It is shown that as the dielectric thickness decreases, the isolation bandwidth becomes wide due to increased down-state capacitance and the resonance frequency becomes lower, enabling low frequency applications possible as well as high frequency applications.
Figure 4.6 Measured and modeled S-parameters for the up-state switch

Figure 4.7 Measured and modeled S-parameters for the down-state switch

Figure 4.8 S-parameters in the down-state with different dielectric thicknesses
4.2 Release methods

4.2.1 Wet release

The release process of MEMS switches that produces a free standing movable membrane is the most critical process in an RF MEMS. Many different materials have been employed for the sacrificial layer: Cu, a-Si, SiO₂, Al, photoresist, etc. Among them, photoresist is the most frequently used material due to its low cost and simple application techniques, as well as the fact that both wet and dry etching can be used to etch a photoresist sacrificial layer [94]. In this section, we present the results of testing the release process before fabricating MEMS switches. Therefore, test structures used in this case were fabricated with only switch bridges and sacrificial layer masks for the sake of simplicity, as shown in figure 4.9. S1813 photoresist was used as a sacrificial layer, and bridges consisted of evaporated and electroplated Au layers. Photoresist can be easily removed by acetone or a photoresist remover. However, a 2.5 μm thick photoresist, particularly that which is present underneath a membrane, cannot simply be removed while maintaining its up-state position without avoiding the stiction that occurs because of capillary forces during drying. Some methods, e.g., boiling methanol first and then rapidly heating the wafer, were introduced to prepare free-standing membranes [95, 96]. However, these methods were only useful for bridges with short lengths and limited the use of various dielectrics in MEMS capacitive switches. On the other hand, CPD allowed the effective elimination of surface tension through the use of carbon dioxide without causing stiction [91]. The bridges were successfully released with CPD (Tousimis 915B). The wafer pieces were soaked in acetone for 30 minutes, then soaked in isopropanol for 90 minutes, i.e., for 30 minutes each in three different beakers, and then soaked overnight. Next, the pieces were placed in the CPD chamber and left to dry. Figure 4.9 illustrates the procedure used to carry out the process in the case of the test wafers.
- Step 1: Thermally oxidized Si wafers were prepared with 400 nm Au and 15 nm TiW adhesive layers sputtered over the entire surface of the wafer.
- Step 2: A 2.5 μm thick photoresist S1813 was spin-coated and patterned using the photolithography process. The photoresist was hard-baked at 110°C for 2 minutes and 30 seconds to form a smooth profile near the edges and prohibit reflow during thermal evaporation.
- Step 3: A 40 nm thick Au layer was deposited using a thermal evaporator (Moorfield MiniLab 25 series). This was followed by Au electroplating with 1 μm thickness to thicken the switch bridge.
- Step 4: After Au was patterned with the photolithography process using S1813, the bridges were released using acetone and then dried with CPD.

![Figure 4.9 Process procedure for dry release experiments](image)

Figure 4.9 Process procedure for dry release experiments

Figure 4.10 shows the interferometer (Wyko NT9100) measurement of the 280 μm long and 80 μm wide bridges after the wet release process. The right side bridge contains holes, whereas the left side one does not. Both were successfully released without any stiction problems. The bridges were found to buckle to some extent at the center of the bridge, which could be attributable to the residual stress produced during thermal evaporation. The stress analysis has not been discussed
here, and instead, we focus on how switches can be released correctly and effectively.

![3D profile of the bridge from interferometry measurement: with holes (left), without holes (right)](image)

**Figure 4.10** 3D profile of the bridge from interferometry measurement: with holes (left), without holes (right)

![2D profile of the bridge with a beam length of 280 μm: (red curve) bridge with holes; (black curve) bridge without holes](image)

**Figure 4.11** 2D profile of the bridge with a beam length of 280 μm: (red curve) bridge with holes; (black curve) bridge without holes

It is important to check for photoresist residue on the back of the bridge. The bridge was turned over to check for residue by using a scalpel. Figure 4.12 shows microscopic images of the bridges that were removed using a probe to observe photoresist residues. No photoresist remained on the bottom Au layer or on the back of the bridges, in contrast to the dry release results, which are discussed later in the subsection.
4.2.2 Dry release

Dry etching uses oxygen plasma to remove the photoresist sacrificial layer that lies underneath a membrane. Oxygen gas (molecules) introduced into the chamber is partially ionized by the electromagnetic excitation emitted by an electrode located at the top of the chamber. The wafer is moved onto a grounded electrode. The pressure inside the chamber is in the range of a few to a few hundred milliTorr. The process depends upon parameters such as the pressure, gas flow, and RF power. Experiments were performed based on the parameters proposed by Yu et al. [97].

Figure 4.13(a–e) shows the process results of the dry release carried out using the PlasmaTherm SLR series. The bridges were removed using a probe in order to check for any residual photoresist underneath the bridges. The photoresist sacrificial layer was continuously removed as it was exposed to oxygen plasma; finally, it was successfully removed from under bridges with holes. However, bridges without holes buckled due to overheating. Table 4.2 lists the dry etching parameters employed during the removal of the sacrificial layer.

<table>
<thead>
<tr>
<th>Power</th>
<th>Pressure</th>
<th>Flow rate</th>
<th>Time</th>
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<tr>
<td>400</td>
<td>450 mTorr</td>
<td>48</td>
<td>60 min</td>
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The etching process was divided into four steps and was repeated every 15–20 minutes in order to prevent the overheating of bridges. After each step, the wafer was moved out of the chamber for approximately five minutes. The wafer piece was placed on the glass plate in order to minimize the heating of the wafer during the etching process. Figure 4.13(e) shows the result of the process when the glass plate was not used. Without the glass plate, the photoresist was easily hardened and could not be etched. It was possible to check whether the release was completed by using the probe test. If any photoresist remained underneath the bridge, the bridge could not be easily removed by a probe or scalpel, but some parts of the bridge could be removed, as shown in figure 4.13(c). However, as shown in figure 4.13(d), if the photoresist was removed completely, the bridge was easily removed when the probe was used to press the bridge.
Figure 4.13(e) Etching result after 50 min without the use of a glass plate

Figure 4.14 shows that some photoresist remained on the surface of the back of the bridge; in contrast, wet release resulted in clean removal, as discussed above. The photoresist was not completely removed even when a longer time was utilized; this was attributed to the presence of hardened photoresist. Lowering the power and using a time-consuming process with a good cooling system may improve the release process [90]. Therefore, based on the experimental results, wet release is believed to be more convenient and reliable than dry release.

Figure 4.14 Back of the switch beam with residual photoresist after 60 min
4.4 PZT/ZrO₂ MEMS switch

4.4.1 Design and fabrication

The microfabrication process of the MEMS capacitive shunt switch with PZT/ZrO₂ thin films is presented here. The MEMS switch process was defined based on surface micromachining technology as follows:

A 15 nm layer of TiW and 300 nm layer of Au were sputtered on a 500 nm thick thermally oxidized high resistivity Si wafer followed by CPW patterning using the photolithography process (figures 4.15(a, b)). Then, a multilayer of PZT/ZrO₂ (180/100 nm) was deposited over the entire surface by the chemical solution deposition (CSD) method for the dielectric layer (c). Details on the deposition
process are given in [26, 98]. A 15 nm thick layer of TiW was sputtered before the ZrO₂ film was deposited to improve adhesion. PZT/ZrO₂ thin films were patterned using 7:1 BHF:HCL:H₂O = 1:2:4. In order to accelerate the etch rate of the PZT film, the wafer was soaked in NiCr etchant at ~45°C for five minutes prior to BOE etching. The detailed etching process and related parameters were reported in [99]. Figure 4.16 shows an SEM image of the dielectric layer after wet etching. The dielectric residues were observed to remain on the CPW. Furthermore, undercutting of the dielectric layer was inevitable in order to remove the remaining photoresist on CPW. A TiO₂ adhesive layer was etched while the dielectric layers were patterned, and a SiO₂ layer was also etched to some extent owing to TiW layer etching.

Figure 4.16 SEM image of dielectric layer after wet etch

A 2.5 μm thick S1813 layer was deposited and patterned to make a sacrificial layer. An Ag metal layer for switch bridges that was approximately 200 nm thick was deposited over the entire surface of the wafer using a thermal evaporator and patterned using the photolithography process followed by wet etching with Cr etchant. The sacrificial photoresist was successfully removed by soaking in acetone for 30 minutes at room temperature, rinsing with isopropanol, and drying with CPD. On the other hand, dry release was not successful due to the oxidation of the Ag bridges during dry etching of the sacrificial layer, as shown in figure 4.17 (left).
4.4.2 Experimental results

Figure 4.18(a) shows the interferometer measurement of the switch after wet release. The bridge buckled to a large extent, which may be attributable to the residual stress during thermal evaporation. There was ~1.2 μm bending at the center of the bridge.
Figure 4.19 shows the interferometer measurement of the up-state switch before (left) and after actuation (right); the switch was destroyed because of a high pull-in voltage. Pull-in voltages were in the range of 30–80 V depending upon switch geometries with different lengths. The pull-in voltage of the switch in figure 4.19 (left) was estimated to be 15 V calculated using (4.6) with residual stress of 30 MPa and a thin metal membrane bridge of approximately 200 nm, but it is measured to be 75 V, primarily attributed to the large residual stress. It should be noticed that all the switches were designed to have pull-in voltage less than 30 V. Although the air gap decreased considerably after wet release owing to the residual stress, the pull-in voltage did not decrease and actually increased considerably. Other switches also showed almost identical damage due to dielectric breakdown. This made accurately measuring the isolation impossible in the down-state.

Figure 4.19 (left) Up-state switch and (right) dielectric breakdown due to a high pull-in voltage of 75 V

Figure 4.20 (up) shows the measured and simulated S-parameters in the up state. The fitted up-state capacitance was 53 fF. Figure 4.20 (down) shows the isolation in the down-state after actuation; there was a small capacitance of 0.8 pF corresponding to the air dielectric constant due to dielectric breakdown. The large inductance was due to the damage caused to the bridges. The theoretical value of the capacitance ratio (C_r) of PZT/ZrO_2 RF MEMS capacitive switches is approximately 800; 40 pF down-state capacitance and 50 fF up-state capacitance. Down-state capacitance is estimated using the characterized dielectric constant. However, the down-state capacitance of the switch can be largely decreased due to
the roughness of the dielectric surface. When the surface roughness of PZT film is 10 nm [101], the down-state capacitance decreases approximately 50% corresponding to $C_r$ of 400. It is found that the calculated $C_r$ of PZT/ZrO$_2$ switch is larger than other high-$\kappa$ material switches, BST switch with $C_r$ 175 [11], Ta$_2$O$_5$ switch with $C_r$ 19 [17], HfO$_2$N$_x$ with $C_r$ 540 [16].

Figure 4.20 Measured and fitted S-parameters of the PZT/ZrO$_2$ MEMS switch at the up-state (up) and down-state position (down)
4.5 Chapter summary

This chapter presented the release methods used for RF MEMS switches. The wet release process with CPD drying successfully removed photoresist sacrificial layers, whereas the use of oxygen plasma did not achieve the same result due to overheating. A microfabrication process was developed for MEMS capacitive switches using the CuO dielectric layer. High capacitance ratio MEMS switches were found to potentially provide a high RF performance of more than -20 dB over broadband ranges covering up to 40 GHz. The insertion loss was -0.4 dB at 10 GHz. In order to demonstrate high-isolation RF MEMS capacitive switches, MEMS switches were processed using PZT/ZrO₂ thin films. However, due to the large residual stress induced by thermal heating during evaporation, the isolation performance could not be properly characterized. In a future work, the deposition process of the bridge metal layers will be optimized in order to produce a low residual stress that can reduce the pull-in voltage. Furthermore, residual stress analyses will be performed using other test structures, such as Guckel rings and cantilever beams, to investigate the stress gradient in such cases.
CHAPTER 5

5. SUMMARY OF APPENDED PAPERS

This section presents a brief summary of the published papers.

Paper 1: Microwave properties of PZT/ZrO$_2$ thin films for RF MEMS capacitive shunt switches


† Dielectric properties of the PZT/ZrO$_2$ films were extracted in order to determine the feasibility of using these dielectric thin films as a dielectric layer for RF MEMS capacitive switches, and using propagation time delay directly measured from the vector network analyzer together with a conformal mapping model (CMM)-based coplanar waveguide model.

Paper 2: Microwave characterization of PZT/ZrO$_2$ thin films


† In this paper, we present the microwave dielectric properties of PZT/ZrO$_2$ thin films characterized by the use of CPW. Due to an additional microwave loss induced by the depletion layer at the zirconium oxide/Si semiconductor interface, the dielectric loss could not be correctly measured. Therefore, MIM capacitors with annular ring slots were processed in order to correctly measure the dielectric loss.
Paper 3: Dielectric properties of thin film ZrO2 up to 50 GHz for RF MEMS switches


† This paper presents dielectric properties and analyzes the measurement results of ZrO2 thin films for RF MEMS capacitive switches. Material properties, including crystal structures and electrical properties, were measured and analyzed. In order to investigate dielectric properties at microwave frequencies, two different measurement techniques using MIM and CPW devices were employed.

Paper 4: Characterization of dielectric and acoustic properties of CSD PZT thin films at high frequencies


† Dielectric and acoustic properties of PZT thin film with different film thicknesses were characterized for application in RF tunable capacitor and FBAR devices using the same measurement setup and analyzed. The thickness dependency of the dielectric constant and tunability were investigated and simulated.
Paper 5: The microwave dielectric properties of dual-layer PZT/ZrO2 thin films deposited by chemical solution deposition


† Dual layer PZT/ZrO2 thin films were investigated for their application to RF MEMS capacitive switches. Microwave dielectric properties and electrical properties were characterized to up to 50 GHz using both MIM and CPW devices combined with conformal mapping methods. Material properties, including crystal structures and electrical properties, were also measured and analyzed.

Paper 6: Study on Cu/Sn SLID Interconnects for RF Applications


† 3D Solid-Liquid Inter Diffusion (SLID) interconnects consisting of Cu/Sn are designed and simulated to investigate how the electrical characteristics of the intermetallic compound (IMC) layers influence the high frequency performance. As test vehicles, co-planar waveguide (CPW) structures fabricated on glass substrates are bonded together using Cu/Sn and Au/Sn SLID interconnects.
Paper 7: Enhanced wet etching process of PZT/ZRO2 thin films for RF MEMS capacitive switches


† This paper presents a wet etching process of CSD PZT/ZrO₂ thin films. PZT thin film is typically etched using BHF and HCL. However, it was found that the etching rate of PZT is low. Therefore, we proposed an additional process with NiCr etchant consisting of diammonium hexanitratocerate, nitric acid, and water prior to the use of BHF and HCL, and observed that dielectric thin films were etched faster than the one without using NiCr etchant.

• Author contributions

The first author was primarily responsible for the design, modeling, measurements, analyses, and writing. SINTEF ICT and SINTEF M&C contributed by providing the materials—PZT and ZrO₂ thin films with test wafers—for the characterization and microfabrication process of RF MEMS switches.
CONCLUSION

This thesis focused on characterizing and investigating potentially influential high-κ materials for RF MEMS capacitive switches and RF tunable devices. Three different dielectrics—ZrO₂, PZT, and dual-layer PZT/ZrO₂ thin films—were chosen for evaluation. SINTEF ICT and M&C provided the PZT and ZrO₂ thin film deposition technology for the characterization and microfabrication of RF MEMS capacitive switches. Measurement results revealed that the characterized ZrO₂ deposited using chemical solution had a high dielectric constant of ~25 at 50 GHz without large relaxation. Dielectric loss was relatively low, and the loss tangent was less than 0.1 at 50 GHz. Further, the breakdown field strength was greater than 2.6 MV/cm. Although ZrO₂ thin films have long received attention for various applications, these new results at high frequencies make ZrO₂ a good candidate for the dielectric layer in RF MEMS capacitive switches as well as competitive against conventional dielectrics such as silicon nitride and silicon dioxide. PZT thin films have been considerably researched for ferroelectric and piezoelectric applications. However, PZT is also a potentially important material for RF applications due to its high dielectric constant and high tunability. Test wafers with PZT thin films were processed and characterized to investigate the dielectric and acoustic properties of the RF MIM tunable capacitor and FBAR devices. The results showed that CSD PZT has a high tunability (~34% at 280 kV/cm) and large dielectric constant of more than 350 at 10 GHz for a 420 nm PZT thin film. This suggests that it is good candidate material for high-density RF MIM capacitors. The PZT thin film showed the possibility of DC electric field dependent tuning of films with a resonant frequency shift of ~15 MHz at 280 kV/cm. A PZT film and ZrO₂ thin film were stacked together to make dual layers of PZT/ZrO₂ and investigated as a dielectric layer for RF MEMS switches. Both electrical and dielectric properties were measured and analyzed by a MIM capacitor and CPW test structures. The dual layer PZT/ZrO₂ was measured by a CPW transmission line and shown to have a large dielectric constant, in the range of ~80–130 at 50 GHz depending on the PZT
Conclusion

thickness. The dielectric loss was ~0.1 at 50 GHz, which is a significant improvement at microwave frequencies compared with typical PZT thin films grown on Pt. The measured values indicated that PZT/ZrO₂ thin films may be suitable for use as dielectric layers in RF MEMS capacitive switches.

This thesis also focused on the development of a microfabrication process for RF MEMS capacitive switches with high-κ materials using surface micromachining technologies. Two dielectrics—CuO and PZT/ZrO₂ thin films—were employed as a dielectric layer. Switches were successfully released using wet etching and dried with a critical point dryer. The results showed that wet release using acetone and CPD is more effective than dry release. On the other hand, due to the large residual stress, the pull-in voltage of the switches was much larger than that the dielectric layer can tolerate, which deteriorated the switch performance. Optimizing the process parameters for the switch bridges may be required to operate MEMS switches correctly, particularly to control the pull-in voltage. Wideband large isolation RF MEMS switches with CuO dielectric layer were demonstrated to show potentially high RF performance over broadband ranges with the use of high-κ materials. Further development of RF MEMS switches is expected to continue with advances in micromachining and nanotechnology, and high-κ materials such as ZrO₂ and PZT will play an important role in improving switch performance. Their material properties are also expected to be improved with further developments in materials science and technology.

As part of this thesis, 3D SLID interconnects consisting of Cu/Sn bimetals were investigated for their RF applications. Two flip chip mounted CPW structures were designed, simulated, and fabricated. Electromagnetic simulations revealed the possibility of improving RF performance by changing the transition region of the interconnects. Test bonding was performed to check intermetallic compounds. In addition, test structures to investigate the Sn overflow were designed and fabricated.
Conclusion

Outlook

Although all of the characterized materials (PZT, ZrO₂, and PZT/ZrO₂) in the thesis works are very promising in terms of high dielectric constant and relatively low loss at microwave frequencies, reliability investigation will be needed in the future, in addition to a study on the charging and discharging mechanism in the dielectric thin films to completely apply to the RF MEMS switches.

Further microfabrication process developments for RF MEMS switches are required to obtain switch bridges with low residual stress and to simultaneously control residual stress. Despite difficulties in obtaining positive results of the release process with dry release using oxygen plasma, such is still very attractive due to the simple process and vacuum environment. It is expected that optimization of the dry etching parameters will take a long time. However, as long as the dry etching parameters are optimized, dry release will be promising for RF MEMS switches.

Further research on Cu/Sn SLID interconnects for RF devices requires careful design near bumps for interconnects to improve insertion loss, and requires the right selection of materials for CPW and minimized misalignment of flip chip bonding in order to prevent the Sn-overflow issue. Cu/Sn IMC has excellent properties, including low resistivity and 3D stacking capability, therefore, the Cu/Sn SLID packaging technology for RF applications is expected to receive a great deal of attention in the near future with further process developments in fabrication processes.
REFERENCES


Reference


Reference


# ACRONYMS

<table>
<thead>
<tr>
<th>Acronym</th>
<th>Description</th>
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<tbody>
<tr>
<td>RF</td>
<td>Radio Frequency</td>
</tr>
<tr>
<td>MEMS</td>
<td>Microelectromechanical Systems</td>
</tr>
<tr>
<td>ZrO₂</td>
<td>Zirconium Dioxide</td>
</tr>
<tr>
<td>PZT</td>
<td>Lead Zirconate Titanate</td>
</tr>
<tr>
<td>CPW</td>
<td>Coplanar Waveguide</td>
</tr>
<tr>
<td>MIM</td>
<td>Metal-Insulator-Metal</td>
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<tr>
<td>SLID</td>
<td>Solid Liquid Interdiffusion</td>
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<tr>
<td>EM</td>
<td>Electromagnetic</td>
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<tr>
<td>FET</td>
<td>Field Effect Transistor</td>
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<tr>
<td>CMOS</td>
<td>Complementary Metal-Oxide-Semiconductor</td>
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<tr>
<td>BST</td>
<td>Barium Strontium Titanate</td>
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<tr>
<td>STO</td>
<td>Strontium Titanate</td>
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<tr>
<td>HfO</td>
<td>Hafnium Oxide</td>
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<tr>
<td>Ta₂O₅</td>
<td>Tantalum Pentoxide</td>
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<tr>
<td>IMC</td>
<td>Intermetallic Compounds</td>
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<tr>
<td>AFM</td>
<td>Atomic Force Microscopy</td>
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<tr>
<td>FIB</td>
<td>Focused Ion Beam</td>
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<tr>
<td>SEM</td>
<td>Scanning Electron Microscopy</td>
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<tr>
<td>MMIC</td>
<td>Microwave Monolithic Integrated Circuits</td>
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<tr>
<td>CM</td>
<td>Conformal Mapping</td>
</tr>
<tr>
<td>HTS</td>
<td>High Temperature Superconductor</td>
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<tr>
<td>TMM</td>
<td>Two Measurement Method</td>
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<tr>
<td>IC</td>
<td>integrated circuit</td>
</tr>
<tr>
<td>TDDB</td>
<td>Time Dependent Dielectric Breakdown</td>
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<td>FERAM</td>
<td>Ferroelectric Random Access Memories</td>
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<tr>
<td>FBAR</td>
<td>Film Bulk Acoustic Resonator</td>
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<tr>
<td>RMS</td>
<td>Root Mean Square</td>
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<tr>
<td>CuO</td>
<td>Copper Oxide</td>
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<tr>
<td>CPD</td>
<td>Critical Point Drier</td>
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<tr>
<td>CuO</td>
<td>Cuprous Oxide</td>
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<tr>
<td>RIE</td>
<td>Reactive Ion Etching</td>
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APPENDIX

A.1 Conformal mapping formulae for CPW

This section describes how the dielectric constant is extracted with conventional CPW and with calculated partial capacitance of CPW combined with the conformal mapping method. Assuming that CPW has a transmission line with perfect conductivity and zero thickness and a dielectric substrate with a relative dielectric constant, CPW can be divided into several partial regions with static capacitance, as seen in figure 1. Figure 1 shows the schematic CPW device with top and bottom metal covers on dielectric substrates with an air gap.

![Figure 1 Schematic of a CPW with top and bottom metal cover on a double-layered dielectric substrate](image)

The total capacitance consists of the partial capacitances $C_1$, $C_2$, $C_{air}$: $C_1$ and $C_2$ correspond to the first and second dielectric layers, respectively, and $C_{air}$ corresponds to the air spaces outside the dielectric layers, that is, the upper and lower air layers between the metal and dielectric layers. The configuration for the partial capacitance $C_1$ is described as follows [39, 40].

$$C_1 = 2\varepsilon_0(\varepsilon_1 - 1) \frac{K(k_1)}{K(k'_1)}$$  \(1\)
\[ k_1 = \frac{\sinh \left[ \frac{\pi S}{4h_1} \right]}{\sinh \left[ \frac{\pi(S + 2W)}{4h_1} \right]} \]  

(2)

\[ k'_1 = \sqrt{1 - k_1^2} \]  

(3)

\[ K'(x) \equiv K(\sqrt{1 - x^2}) \]  

(4)

Here, \( K \) is the complete elliptic integral of the first kind, and \( k \) is the modulus.

Figure 2 Schematic CPW for calculating the first partial capacitance

Partial capacitance \( C_2 \) is described as follows:

\[ C_2 = 2\varepsilon_0 (\varepsilon_2 - \varepsilon_1) \frac{K(k_2)}{K(k'_2)} \]  

(5)

\[ k_2 = \frac{\sinh \left[ \frac{\pi S}{4h_2} \right]}{\sinh \left[ \frac{\pi(S + 2W)}{4h_2} \right]} \]  

(6)

\[ k'_2 = \sqrt{1 - k_2^2} \]  

(7)
Figure 3 Schematic CPW for calculating the second partial capacitance

The partial capacitance $C_{air}$, which is due to the upper and lower air layers between the metal and dielectric layers, is described as

$$C_{air} = 2\varepsilon_0 \frac{K(k_3)}{K(k_3')} + 2\varepsilon_0 \frac{K(k_4)}{K(k_4')}$$

(9)

Here,

$$k_3 = \frac{\tanh \left[ \frac{\pi S}{4h_3} \right]}{\tanh \left[ \frac{\pi(S + 2W)}{4h_3} \right]}$$

(10)

$$K(k_3') = K\left(\sqrt{1 - k_3^2}\right)$$

(11)

$$k_4 = \frac{\tanh \left[ \frac{\pi S}{4h_4} \right]}{\tanh \left[ \frac{\pi(S + 2W)}{4h_4} \right]}$$

(12)

$$K(k_4') = K\left(\sqrt{1 - k_4^2}\right)$$

(13)

Figure 4 Schematic CPW for calculating the partial capacitance $C_{air}$
In practice, there are no metal covers on the CPW structure. Thus, we assume that \( h_3 \) and \( h_4 \) are infinitely large; then,

\[
h_3 = h_4 = \infty \quad \rightarrow \quad k_3 = k_4 = k_o = \frac{S}{S + 2W}
\]

\[
C_{air} = 4\varepsilon_o \frac{K(k_o)}{K(k_o')}
\]

Subsequently, the capacitances \( C_1, C_2, \) and \( C_{air} \) are summed, and (15) is used to relate the effective dielectric constant and capacitances.

\[
\varepsilon_{eff} = \frac{C_{cpw}}{C_{air}}
\]

\[
\varepsilon_{eff} = \frac{C_{cpw}}{C_{air}} = \frac{(C_1 + C_2 + C_{air})}{C_{air}}
\]

Finally, the next simple form related to the effective dielectric constant and dielectric constant of the substrate and dielectric layer can be obtained by the geometrical factor \( q \).

\[
\varepsilon_{eff} = 1 + q_1(\varepsilon_1 - 1) + q_2(\varepsilon_2 - \varepsilon_1)
\]

\[
q_i = \frac{1}{2} \frac{K(k_i)}{K'(k_i)} \frac{K'(k_o)}{K(k_o)} , \quad i = 1, 2
\]
Appendix

\[ Z_o = \frac{1}{C_{CPW} v_{ph}} = \frac{30\pi}{\varepsilon_{eff}} K(k_o) \]  

(19)

A.2 List of appended papers


