Physical model for charge accumulation and technology development for robust RF MEMS switches

Dissertation for the degree of Philosophiae Doctor

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December 2012

Abstract

Radio frequency (RF) micro-electromechanical system (MEMS) capacitive switches are expected to be a very promising technology for many microwave and wireless applications since they can provide low loss, low-power consumption, high linearity and quality factor. However, the reliability problem is still one of the important limitation factors which present a research challenge for the commercialization. The lifetime of these switches is believed to be strongly influenced by dielectric charging. In spite of huge effort has been made from many research groups worldwide for more than a decade to develop robust RF MEMS switches, little information is available in the literature providing a fundamental solution to this problem. The key challenge is to understand the principle of charge injection when the field across the dielectric layers.

In this thesis, we employed a metal-insulator-semiconductor (MIS) capacitor structure to investigate the dielectric charging and discharging for high reliable capacitive RF MEMS switches. The dielectric charging and discharging kinetics were qualitatively and quantitatively characterized by comparing the measured capacitance-voltage (C-V) curves on MIS structure before and after charge injection.

We firstly investigated the charging and discharging properties in Si_3N_4 and SiO_2 single dielectric layers, respectively, e.g., the dependence of charge injection and relaxation on the stress time, magnitude, polarity of applied voltage. To explain the observed experimental results, we have proposed a generalized charge injection model and a relaxation model by taking into account the roles of holes and electrons. From the investigation of charging and

discharging properties in Si_3N_4 and SiO_2, we concluded that there are two basic approaches for mitigating charge accumulation: (1) reducing charge injection level when high stess voltage is applied and (2) accelerating charge relaxation process after the high voltage is removed. Based on the first approach, we have investigated how charge accumulates in multi-layer dielectric stacks, e.g., double- and triple-layer dielectrics. The experimental results suggest that it is possible to balance the number of charges injected from the top and bottom electrodes by optimizing the thickness ratio of Si_3N_4 to SiO_2 in Si_3N_4/SiO_2 double dielectric layers. Based on the second approach, we have investigated the charge accumulation in doping dielectrics, e.g., doping phosphorus or boron ions into SiN_x dielectric films and doping silicon nanocrystals into silicon oxide, the experimental results indicate that it is possible to create 'combination center' in the dielectric for short relaxation mechanisms by doping technology.

Keywords: RF MEMS switch, Dielectric charging, discharging, MIS capacitor

Publication list

Journal papers

(1) **Gang Li** and Xuyuan Chen, "Modified Fowler-Nordheim tunnelling for modelling charge injection in Si_3N_4 of MIS structure", Appl. Phys. A, Vol.109, 2012.

(2) **Gang Li,** Haisheng San, Xuyuan Chen, "Charging and discharging in ion implanted dielectric films used for capacitive RF MEMS switch ", J. Appl. Phys105, 124503 (2009).

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(4) **Gang Li,** Ulrik Hanke and Xuyuan Chen, "Effect of SiO2 thickness on charge accumulation in double-layer dielectric for high reliable Capacitive RF MEMS Switch", submitted to J. Appl. Phys.

(5) **Gang Li** and Xuyuan Chen, "Investigation of Charge injection and relaxation in multi-dielectric stacks for Capacitive RF MEMS switch application", IEEE Transactions on electron devices, in process.

(6) Haisheng San, Zhiqiang Deng, Yuxi Yu, **Gang Li,** and Xuyuan Chen, "Study on dielectric charging in low-stress silicon nitride with the MIS structure for reliable MEMS applications", J. Micromech. Microeng. 21, 125019 (2011).

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(1) **Gang Li**, Ulrik Hanke, Zaijun Cheng, Deokki Min, Haisheng San and Xuyuan Chen, "Si_3N_4/SiO_2 dielectric stacks for high reliable Capacitive RF MEMS Switch", IEEE NANO 2011, Aug. 2011, Oregon, USA.

(2) **Gang Li,** Ulrik Hanke, Deokki Min and Xuyuan Chen, "Comparison of charge injection in SiO_2 and Si_3N_4 for Capacitive RF MEMS switches", 2011 International conference on electronic packaging technology and high density package, Aug. 2011, Shanghai, China.

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(6) **Gang Li,** Linxian Zhan, Haisheng San, Peng Xu, Xuyuan Chen, "Influence of Ion Implantation on dielectric charging in Capacitive RF MEMS switches". SPIE Photonics Asia 2007, Nov. 2007, Beijing, China.

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Contents

Chapter 1
Introduction

1.1 Why RF MEMS switch?

  Micro-Electro-Mechanical Systems (MEMS) technology plays an important role in today's society. The integration of MEMS into traditional Radio Frequency (RF) circuits, which will result in great progress with miniaturization, superior performance and lower manufacturing costs. These superior performance enable them to be used in a wide array of commercial, aerospace, and defense application areas, including satellite communications systems, wireless communications systems, instrumentation, and radar systems [1]. As an example of RF MEMS technology, RF MEMS Switch has the potential of replacing many of the mechanical and semiconductor switches used in mobile and satellite communication systems [2]. Fig 1.1 shows an example of RF MEMS capacitive switch [3].
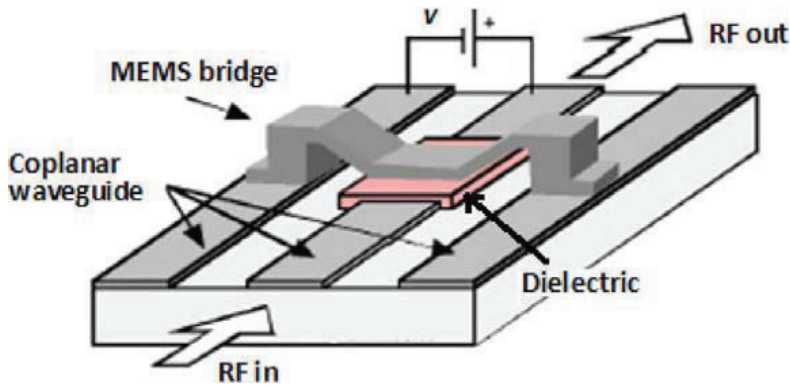
Figure1.1An example of RF MEMS capacitive switch.

  In many cases, such switches would not only reduce substantially the size and power consumption, but also promise superior performance. In comparison to semiconductor switches (FET-Field Effect Transistor and PIN-diodes), RF capacitive MEMS switches have displayed excellent RF characteristics, including lower insertion loss, higher isolation, zero power consumption, small size and weight and very low intermodulation distortion, and long battery life. Table 1.1 provides a general overview of the performance comparison related to RF MEMS, PIN diode, and FET switches [4].

Table 1.1Performance comparison of FET, PIN diode and RF MEMS switches.

PARAMETER	RF MEMS	PIN-DIODE	FET
Voltage(V)	20 – 80	± 3 – 5	3 – 5
Current (mA)	0	0 – 20	0
Power Consumption (mW)	0.5 – 1	5 – 100	-.5 – 0.1
Switching	1 – 300 μs	1 – 100 ns	1 – 100 ns
C_{up} (series) (fF)	1 – 6	40 – 80	70 – 140
R_s (series) (Ω)	0.5 – 2	2 – 4	4 – 6
Capacitance Ratio	40 – 500	10	n/a
Cutoff Freq. (THz)	20 – 80	1 – 4	0.5 – 2
Isolation (1–10 GHz)	Very high	High	Medium
Isolation (10–40 GHz)	Very high	Medium	Low
Isolation (60–10 GHz)	High	Medium	None
Loss (1–100 GHz) (dB)	0.05 – 0.2	0.3 – 1.2	0.4 – 2.5
Power Handling (W)	<1	<10	<10
3rd order Int. (dBm)	+66 – 80	+27 – 45	+27 - 45

1.2 RF MEMS Switches Classification and Application

As already mentioned, RF MEMS switches are used in a wide array of commercial, aerospace, and defense application areas, including satellite communications systems, wireless communications systems, instrumentation, and radar systems. There are many kinds of RF MEMS switches, which can be classified in terms of actuation method (electrostatic, electrothermal, magnetic, piezoelectric), axis of deflection (laterally, vertically), circuit configuration (series, shunt), clamp configuration (cantilever, fixed-fixed beam) and contact interface (capacitive, ohmic). As for the electrical part, a MEMS switch can be placed in either series or shunt configurations and can be a metal-to-metal contact or a capacitive contact switch [4]. In order to choose an appropriate RF MEMS switch, one must first consider the required performance specifications, such as frequency bandwidth, linearity, power handling, power consumption, switching speed, signal level, and allowable losses.
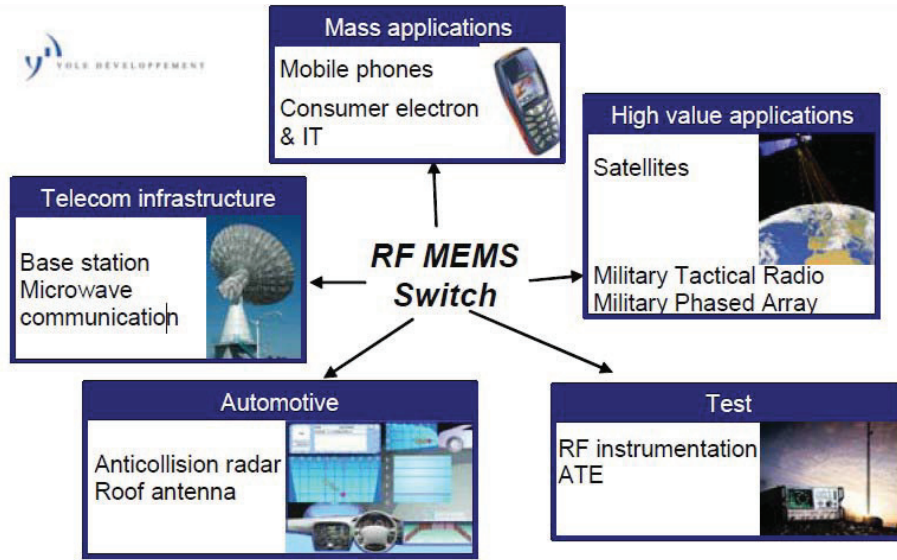
Figure 1.2 Examples of RF MEMS applications areas

Capacitive RF MEMS switches are usually designed for frequencies above 1GHz and small bandwidths. Especially when targeting wireless equipment, low power consumption and small size are required. As shown in Fig1.2, specific application of these switches can be found in phase shifters, tunable band filters/matching networks and reconfigurable phased arrays antennas [5].

1.3 RF MEMS Capacitive Switches Reliability

1.3.1 Common reliability issues in MEMS

An important challenge in achieving successful commercial MEMS products is associated with MEMS reliability. Many of the MEMS failure mechanisms are not well understood. MEMS reliability requires a broad understanding of physics and mechanics in order to handle the challenges during research, development, and productization. Since in general MEMS behavior is governed by multiple physical domains, MEMS reliability is also governed by many different degradation mechanisms. An overview of reliability issues in MEMS devices can be found in a publication of NASA and JPL [6]. In table 1.2 the most common reliability issues in MEMS structures are shown.

Table 1.2Reliability issues in MEMS structures [6].

Failure mode	Underlying causes/ Examples
Mechanical fracture and creep	Mechanical stress above Yield strength
	Fatigue (prolonged cycling)
	Intrinsic mechanical stress
	Thermal fatigue
Degradation of dielectrics	Dielectric charging
	Break down
	Leakage
Stiction	Capillary forces
Wear	Adhesion
	Abrasion
	Corrosion
Delamination	Loss of adhesion between material interfaces
Environmentally induced	Vibration
	Shock
	Humidity effects
	Radiation
	Temperature changes
	Electrostatic discharge

The reliability of MEMS switches is of major concern for long-term applications and is currently an important subject of an intense research effort, as shown in Table 1.2, many physical mechanisms can alter the lifetime of MEMS devices: mechanical creep effect, electro migration due to high current density, stiction through capillarity forces. For ohmic contact MEMS switches, the main reliability issues, such as failure due to stiction, contact welding and contact resistance degradation, have been observed to be the key failure modes. Stiction is the unintentional adhesion of the movable and fixed parts in MEMS devices caused by surface adhesion forces [7].

Failure due to stiction is frequently encountered in electrostatically actuated type MEMS relays for the case when the beam is in contact with the dielectric that coats the bottom electrode. Typically, stiction of the metal bridge to the dielectric layer is a major failure mode

in capacitive MEMS switches. Mechanical degradation of MEMS capacitive switches is generally seen as less of an issue than dielectric charging [4]. This is due to fact that a carefully designedswitch operated under the right circumstances can operate for billions of cycles [8, 9].

1.3.2 RF MEMS capacitive switch operation and failure mode

A typical example of a capacitive RF MEMS switch is shown in Figure 1.3, it consists of a freestanding plate suspended by beams above a coplanar waveguide (CPW). Under this 'bridge', a high-ε_r dielectric is present. When a dc voltage is applied between the CPW central conductorand the surrounding ground plane, the bridge is attracted electrostatically, and when the dc actuation voltage is high enough, it collapses and lands on top of the dielectric.
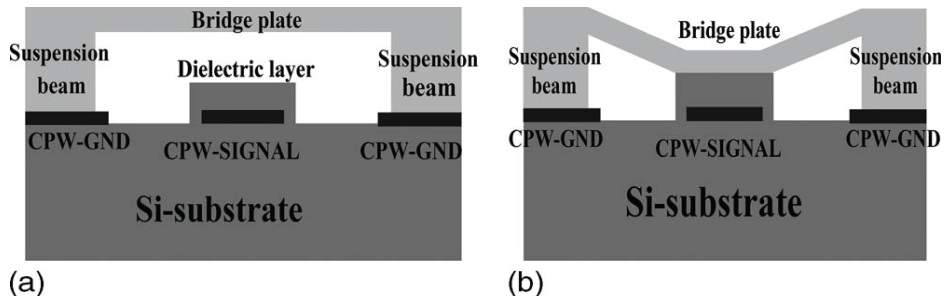
Figure 1.3.(a) Schematic structure of rf MEMS capacitive switch. (b). Downstate of rf MEMS capacitive switch.

When the dielectric film contact the metal bridge, a high electrical field will be produced across the layer so that it is possible for charges to be injected and further to be trapped in the dielectric film. The screening voltage resulted from accumulated charge in the dielectric layer detracts the actuation voltage until there is no more enough electrostatic force pulling on the membrane to cause it to actuate, or when the actuation voltage is removed, the accumulated charges provide enough electrostatic force to keep the membrane down. That is the main failure mechanism for the stiction of the RF MEMS switches.

1.4 Literature review for the solution of dielectric charging

To improve reliability of these switches, charge accumulation in the dielectric must be reduced. On the way to mitigating charge accumulation in the switch dielectric, significant

attempts have been made from many research groups worldwide for more than a decade. Designing switches with lower actuation and hold-down voltages was firstly taken into consideration [10–13]. Innovative dielectric materials [14–15], no dielectric layer structures [13], doping the dielectric materials[14] and multi-waveform actuation voltages [16–18] were also attempted to increase switch reliability. Other efforts, in terms of reducing the amount of dielectric material present in capacitive switches, at the expense of capacitance ratio have been proposed [19]. Alternatively, making the switches smaller, using patterned dielectric posts, or no dielectric whatsoever has resulted in improved lifetimes [19-21]. Application of a leaky dielectric material with non-zero DC conductivity is also an approach for decreasing the recombination time of these trapped charges [22, 23]. Recently, a smart discharging mechanism employed to the dielectric was proposed by Pillans et.al., where they designed and processed a Schottky barrier contact-based RF MEMS switch [10]. One of the more recent efforts has been made in terms of optimizing the stoichiometry (N/Si) of silicon nitride to reduce charge accumulation [11].

In spite of the huge efforts, as mentioned above, have been made, the charge injection and relaxation process in the dielectric is not thoroughly understood yet. Therefore, current approaches of controlling charge accumulation still cannot solve the problem. The key challenge is to understand the principle of charge injection when the field across the dielectric layers.

1.5 Research objective

To solve the switch reliability issue caused by dielectric charging, a large amount of work is still ahead of us. A major goal of this thesis was to increase the understanding of charge accumulation in the dielectric layer and to learn how to design innovative and robust RF MEMS switches that are fabricated by using silicon surface and bulk micromachining and with a capacitive structure. Charge accumulation in dielectric will be thoroughly investigated in order to understanding mechanisms of ionization, charge injection, positive and negative charges formation, and charge trapping and recombination solution to eliminate or reduce charge accumulation for high reliable capacitive RF MEMS switches.

The control of the charging/discharging processes is a key factor to allow a fast recovering of the dielectric after charging. The main works are detailed as the following:

1) How to characterize charge injection and relaxation behaviors in the dielectric.

2) Investigation of charge injection behaviors in the dielectric under high bias voltage.

3) Investigation of Charge relaxation behaviors in the dielectric after high bias voltage.

4) Comparison of charge accumulation behaviors between different dielectric materials, e.g., Si_3N_4 and SiO_2.

5) Charge injection and relaxation process in multi-layer dielectric, e.g., double- and triple-layer dielectric.

6) Effects of SiO_2 thickness on charge accumulation in Si_3N_4/ SiO_2 dielectric stacks.

7) Charge injection and relaxation investigation in ion implanted dielectrics, e.g., P and B ions implanted dielectrics.

8) Charge injection and relaxation in SiO_2 films containing silicon nanocrystals.

1.6 Outline of the thesis

The thesis is organized based on the published and submitted journal and conference articles. The first chapter gives an overview about state of the art technologies, the motivation and the scope of the research. In Chapter 2, the novel characterization methodology has been proposed after discussing the traditional characterization methodology. In Chapter 3, charge injection and relaxation behaviors have been clearly presented by collecting two journal papers and one conference paper. In chapter 4, the investigation of charge accumulation in multi-layer dielectrics has been presented by combining one submitted journal paper and one book chapter. In chapter 5, the investigation of charge accumulation in doing dielectrics have been presented based on one journal paper and one conference paper. In Chapter 6, the investigations are summarized and the contribution of this work to science is concluded. The last chapter gives some comments for the further investigation.

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Chapter 2
Characterization Methodology

2.1 Traditional Characterization Methodology

The stiction failure mode for capacitive MEMS switches is due to dielectric charging, keeping the switch in a permanently closed state. In order to understand the dielectric charging and discharging in RF MEMS switches, one must be able to measure and quantify the trapped charge in the dielectric. Considerable effort has been devoted to both the experimental characterization of dielectric charging and the developmentof models that can be used to predict the impact ofdielectric charging on electro-mechanical behavior of a capacitive switch. So far, several attempts have been made to model the effect of stiction and screening caused by charge accumulation; however there still remains a lot of work to fully characterize, understand and solve this challenge.

2.1.1Lifetime Characterization

The first experimental characterization of dielectric charging in capacitive RF MEMS switch, implemented by Goldsmith et al., is to characterize switch lifetime [1]. In this method switch lifetime depends exponentially on the applied voltage (as shown in Figure 2.1), it was argued that charge accumulation was attributed to Frenkel–Poole conduction [2], which depends exponentially on voltage. As shown in Fig 2.1, it can be seen that the switch lifetime shortens as the drive signal amplitude increases. But switch lifetime only gives a qualitative measure of dielectric charging.
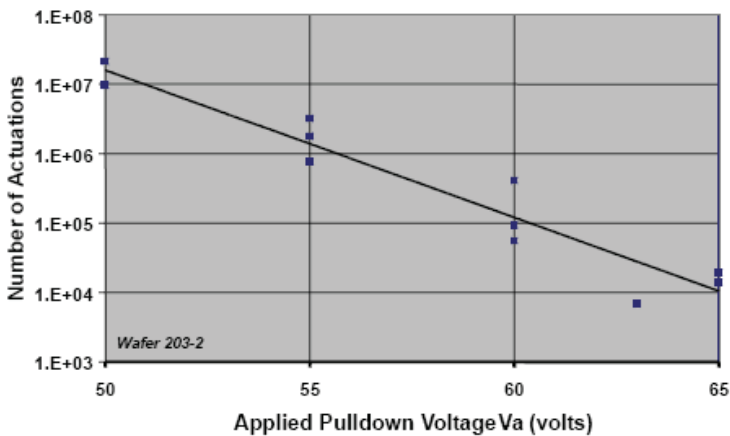
Figure 2.1. MEMS lifetime characterization [1].

2.1.2 Capacitance - Voltage (C-V) shift Characterization

The most popular method to measure charge build-up in the dielectric involves analyzing a capacitance voltage (CV) curve. A capacitance meter is used to obtain the capacitance values atvarious voltages [3, 4, 5]. From the *CV* curve, one can observe how the capacitance of the shunt switch changes with applied voltage. First, an initial CV measurement between the silicon substrate and the capacitive bridge was performed with no DC offset, as the magnitude of the applied DC offset voltage increases, the CV measurements are taken periodically until the bridge is pulled-in. The difference between the final and initial CV values is proportional to the sheet charge trapped in the dielectric layer. Figure 2.2 shows the C-V curve before and after a switch has been stressed.
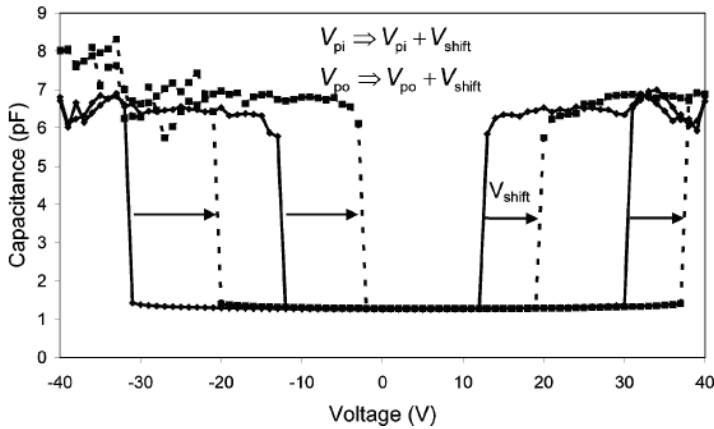
Figure 2.2. C-V curve before (black) and after (grey) a switch has been stressed at 65 volts for 727 seconds [6].

2.1.3 Charging and discharging current Characterization

Recently, it was reported that because dielectric charging caused by charge injection, another approach [7] through the experimental investigation of charging and discharging current transients a charging model was developed and used in for the quantitative description of dielectric charging. Charging and discharging currents of traps were measured on permanently down RF MEMS capacitive switches [8] or a MIM capacitor [9]. In this method, as shown in Figure 2.3(a), they found that charging and discharging time constants are relatively independent of control voltage, and as shown in Figure 2.3(b), steady-state charge densities increase exponentially with control voltage.
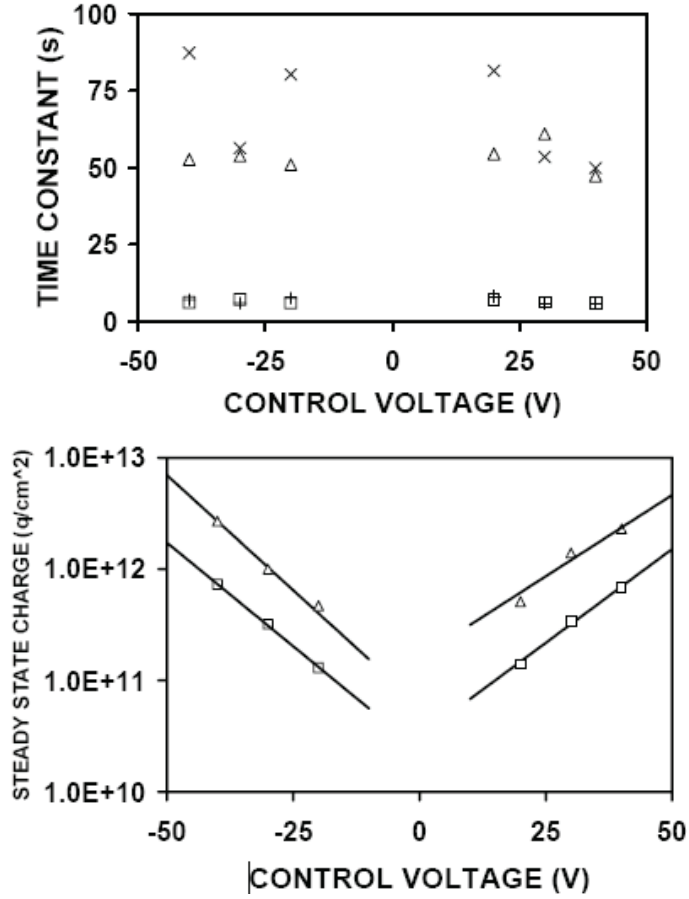
Fig 2.3. (a) Trap 1 (□) charging and (+) discharging and trap 2 (Δ) charging and (x) discharging time constants and (b) (symbols) extracted and (lines) fitted steady-state charge density for (□) trap 1and (Δ) trap 2 under -40, -30, -20, 20, 30 and 40 V.

2.2 Characterization Methodology in this thesis

These characterization methods as mentioned above, which have been used to investigate the dielectric charging, arecomplicated and time consuming for evaluating the switch dielectrics because fabrication of actual RF MEMS switches is required, or the quantification of the trapped charges and their relaxation process cannot be easily performed by using both MIM structure and MEMS switches.

According to the schematic structure of the switch shown in Fig. 2.4, a model was established for stiction modeling. When the suspended metal bridge of the capacitive RF

MEMS switch is electrostatically actuated to contact the surface of dielectric [Fig. 2.4(a)], the switch can be modeled as a metal-insulator-metal (MIM) structure [Fig. 2.4(b)]. In Fig. 2.4(b), the simple, parallel plate model is used, which consists of a metal plate with anarea of A suspended by a linear spring with stiffness of k and a dielectric layer with thickness of t above the central conductor of the coplanar waveguide (CPW). When the bridge contacts with the dielectric layer, the bridge deflection is indicated with the displacement d. The charges in the dielectric layer include the top surface parasitic charges $Q_{surface}$, bulk charges Q_{bulk}, and bottom interface charges $Q_{interface}$. It is also important to note that the bottom interface charges donot have any influence on the metal bridge because the image charges generated in the CPW conductor cancel the bottom interface charges exactly. When the stiction happens, the electrostatic force F can be expressed as

$$F = \frac{1}{2}Q_{indu} \cdot E = \frac{1}{2}Q_{indu} \cdot \frac{AQ_{indu}}{\varepsilon_o \varepsilon_r} = \frac{1}{2}\frac{AQ_{indu}^2}{\varepsilon_o \varepsilon_r} = -kd \tag{2.1}$$

where Q_{indu} is the induced charges at the metal bridge, E theelectric field, ε_0 the permittivity of free space, and ε_r the relative dielectric permittivity. Therefore, the critical charges that result in stiction can be expressed as [10]

$$Q_{critical} = -\left[Q_{surf} + \frac{A}{t}\int_0^t x\rho(x)dx\right]_{critical} = -\sqrt{\frac{2kd\varepsilon_o \varepsilon_r}{A}} \tag{2.2}$$

Where $\rho(x)$ is the sheet charge density at position x that relatives to the coordinate in which origin of coordinate is set at the interface between the CPW metal layer and the dielectric layer.
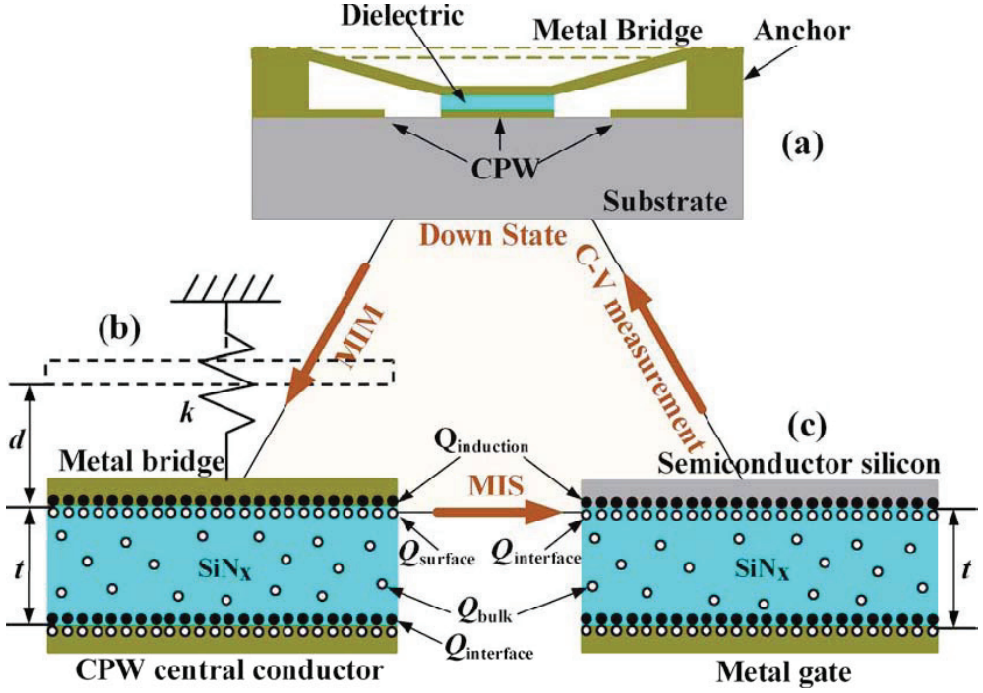
Figure 2.4. (Color online) Analytical model of RF MEMS capacitive switch. (a) Schematic structure of RF MEMS capacitive switch, (b) MIM model, and (c) MIS model.

Since high frequency C-V measurements on MIS devicesare generally used to study trapped charges in dielectric, we propose a method to study dielectrics charging in RF MEMS switches by measuring the C-V characteristics of MIS structures. It can be found by comparing Fig. 2.4(b) with Fig. 2.4(c) that $Q_{interface}$ and Q_{bulk} in the MIS structure are equivalent to $Q_{surface}$ and Q_{bulk} in the MIM structure. The trapped charges in the MIS structure will shift the C-V curve from an ideal (no trapped charges) site, while the bottom interface charges have much less influence on the flatband voltage. The flatband voltage V_{fb} of the MIS structure can be expressed as[11]

$$V_{fb} = -\Phi_{ms} - \frac{1}{C_o}\left[Q_{int} + \frac{A}{t}\int_0^t x\phi(x)dx \right] \tag{2.3}$$

where C_0 is the capacitance of the MIS structure, Φ_{ms} is the work function difference between the metal and semiconductor,and the sheet charge density at position x is expressed as$\Phi(x)$. Therefore, the flatband trapped charges can be given by

$$Q_{fb} = -\left[Q_{int} + \frac{A}{t}\int_0^t x\phi(x)dx\right] = C_o\left(V_{fb} + \Phi_{ms}\right) \tag{2.4}$$

To compare Eq. (2.2) with Eq. (2.4), it can be found that the effective trapped charges in the two models have same expression form. Therefore, the charging behavior in the RF MEMS switch can be analyzed by using the MIS structure. However, the metal-dielectric contact surface in the switch is different from the dielectric-semiconductor interface in the MIS structure. Therefore, it is difficult to establish a quantitative relation between Eqs. (2.2) and (2.4). However, the change of the trapped charges in the dielectric can be observed by the flatland offset of the MIS devices.

According to above modeling, the effects of different levels of the electrical stresses on C-V characteristics of the MIS devices were investigated for simulating the chargingbehavior of an actual switch under actuation voltage. In our experiments, the electrical stress was performed by applying dc voltage to the gate electrode of the MIS (Al/Insulator/Si) device.

2.3C-V measurements and tool setup

2.3.1C-V measurements and dc stress

The charge accumulation in the silicon nitride films can be evaluated by C-V measurement, which is the most widely used method for characterizing charge within dielectric layer of MIS, MOS and MOS-like structures. It has been reported that the amount of charge accumulated in a certain dielectric layer depends on the magnitude and time of applied electric field [12]. The DC pulse, simulating the actuation voltage, is used to electrically stress the MIS structure in this work. After the DC pulse stress, *C-V* measurements are carried out by applying a DC gate voltage with a superimposed small AC signal of varying frequency. The DC gate voltage changes slowly to obtain a continuous curve showing regions of accumulation, depletion, and inversion for the conduction layer in the substrate semiconductor (as shown in Fig.2.5).
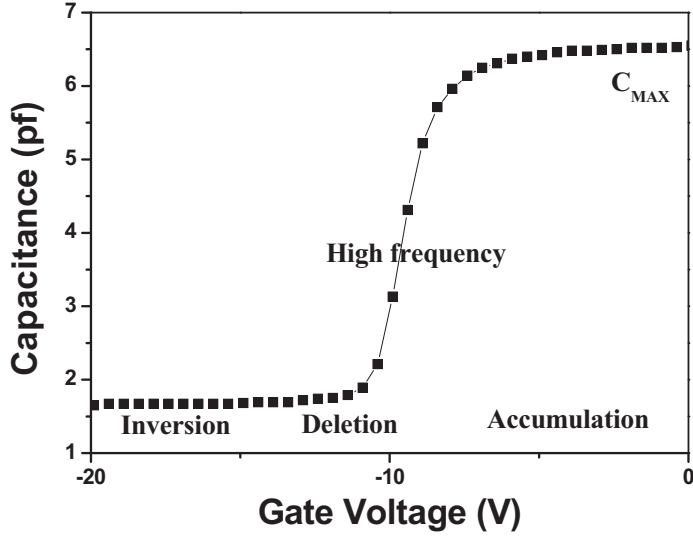
Figure 2.5An example of CV curve measured at high frequency

C_{max} can be obtained from the C-V curve in Figure 2.5, or it can be calculated by

$$C_{max} = \frac{\varepsilon_{die}}{t}$$

(2.5)

Where $C_{max} = C_{die}$ is the dielectric capacitance (F/cm^2), ε_{die} is the permittivity of the dielectric, and t is the thickness of the dielectric. If there is more than one dielectric film, C_{max} is a series combination of capacitances made of individual dielectric layers, as following:

$$C_{max} = \frac{c_1 c_2}{c_1 + c_2}$$

(2.6)

Where C_1 and C_2, respectively, represent the two different dielectric capacitances. However, C_{min} is the series combination of C_{max} and C_{dep} capacitances

$$C_{min} = \frac{C_{max} C_{dep}}{C_{max} + C_{dep}}$$

(2.7)

where C_{dep} is the depletion capacitance in the semiconductor, which in turn is defined as:

$$C_{dep} = \frac{\varepsilon_s}{W_{dep}}$$

(2.8)

18

where ε_s is the permittivity of the substrate, while W_{dep} is the substrate depletion width,which can be calculated using Eq. 2.9. Eq. 2.9 represents the maximum depletion width for any given doping concentration N_x.

$$W_{dep} = \sqrt{\frac{\varepsilon_s |\Phi_f|}{qN_x}}$$ (2.9)

In the above equation Φ_f is the Fermi potential of the substrate.

The charge variation due to the AC signal gives rise to a measurablecapacitance which can be given by:

$$C = -\frac{dQ}{dV}$$ (2.10)

Where Q represents the total charge in the conduction layer of the substrate semiconductor, V represents the gate voltage, and C represents the capacitance.

Flat band voltage (V_{FB}) which is a negative voltage applied between the metal and semiconductor to achieve the flat band, as a function of the time of the DC stress or the total amount of the injected charges, provides information on how many charges are trapped in the insulator in the MIS structure, so the amount of charges accumulated in the dielectric layer can be obtained by measuring the V_{FB} shift in the C-V curves. The shifts of C-V curves towards the left or right indicate that the net positive or negative charges injected intothe dielectric.In the experiments, the samples were first biased with DC stress, so that charges can be injected into the dielectric films.The dynamic process of charging and discharging can be analyzed by comparing the C-V curves measured before and after charge injection.

In order to determine the flat band voltage, we must calculate the flat band capacitance (C_{FB}), the voltage corresponding to which is V_{FB}, the $C_{FB}$is given by [13]

$$\frac{C_{FB}}{C_0} = 1/[1+\frac{\varepsilon_{ro}}{\varepsilon_{rs}}(\frac{\varepsilon_{rs}\varepsilon_o k_o T}{q^2 N_A d_0})^{\frac{1}{2}}]$$ (2.11)

where C_0 is the capacitance which is corresponding to the biggest capacitance shown in the C-V curve, ε_0 the permittivity of free space, ε_{ro} the relative permittivity of the dielectric, ε_{rs} the relative permittivity of the semiconductor, k_o the Boltzman constant, T the temperature,

the measurement was performed at room temperature, q the elementary charge, N_A the dopant concentration, and d_0 the thickness of the insulator.

V_{FB} can be extracted from the C-V data according to C_{FB}. In order to simplify the process of calculation, we can assume that all the trapped charges are located at the silicon-insulator interface although the trapped charges can be generated not only at the silicon-insulator interface, but also in the bulk. The trapped charge, ΔN_t, can be calculated by:

$$\Delta N_t = -\frac{C_0}{q}\Delta V_{FB} \tag{2.12}$$

Where ΔV_{FB} caused by the trapped charge is the magnitude of measured V_{FB} shift.

Trapped charge calculated from the change in flat band voltage is an approximation of the charge located in the insulator structure. By measuring the C-V curve shift along the voltage axis as a function of DC stress to determine the charge accumulation; this measurement technique has the advantage of being simple and direct.

2.3.2 Tool setup for CV measurement

Fig. 2.6 shows the schematic diagram of our measurement setup for C-V measurement, this system consists of 590 CV Analyzer, which is a sophisticated instrument designed as a complete solution for individuals requiring capacitance and conductance versus voltage measurements in semiconductor testing. The 590/100k/1M can test devices at either 100 kHz or 1 MHz, depending on installed modules. Test voltage for both frequencies is 15 mV RMS; 4200-SCSSemiconductorCharacterization System, which allow users to conduct simultaneous high frequency (HF) and quasistatic (QS) C-V (Capacitance-Voltage) measurements on wafer devices with a single voltage sweep and improves C-V measurement accuracy by reducing the voltage stress on the devices under test and eliminating the need for the use of theoretical curves and doping, in electronics: see semiconductor; Prober station which is used to connect the device-under-test (DUT) to testing instrument, the prober station should be placed inside of a shielded boxin order to avoid the effect of electromagnetic field and illumination on measurement. Agilent 33250A Function/Arbitrary Waveform Generator and Power Amplifier-

TREK model 630, in order to avoid the effect of the illumination and electrical noise from environment on the measurement results, the prober station was placed inside of a shielded box.

The voltage stress was conducted by biasing the MIS capacitor with a high voltage which was generated by Agilent 33250A Function /Arbitrary Waveform Generator and amplified by TREK Model 630 Voltage Amplifier. The bias is applied to the metal gate. The bottom of silicon substrate is held at the prober station chuck. All measurements were made at room temperature in air ambient.
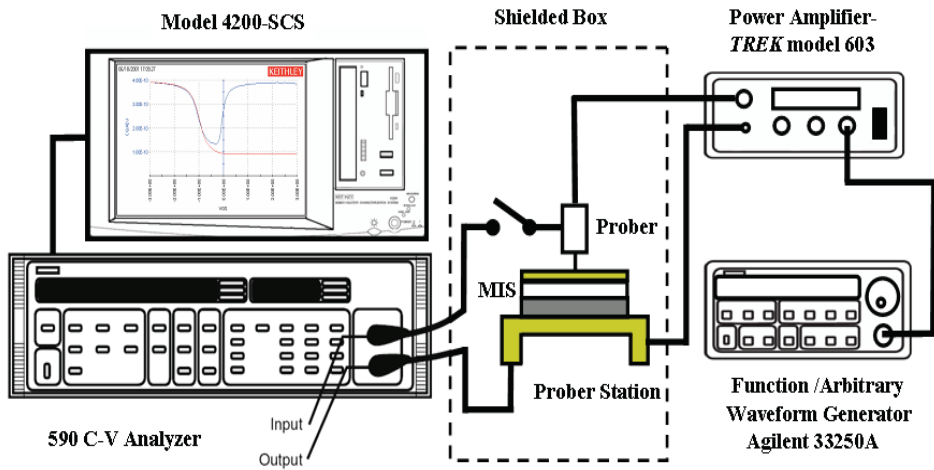
Figure 2.6. Schematicstructureof our C-V measurement systems

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Chapter 3

Charge Accumulation Theory

Chapter 4

Multi-layer Dielectrics for Low Charge

Accumulation

Chapter 5

Doping Dielectrics for low Charge Accumulation

Charging and discharging in ion implanted dielectric films used for capacitive radio frequency microelectromechanical systems switch

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In this work, metal-insulator-semiconductor (MIS) capacitor structure was used to investigate the dielectric charging and discharging in the capacitive radio frequency microelectromechanical switches. The insulator in MIS structure is silicon nitride films (SiN), which were deposited by either low pressure chemical vapor deposition (LPCVD) or plasma enhanced chemical vapor deposition (PECVD) processes. Phosphorus or boron ions were implanted into dielectric layer in order to introduce impurity energy levels into the band gap of SiN. The relaxation processes of the injected charges in SiN were changed due to the ion implantation, which led to the change in relaxation time of the trapped charges. In our experiments, the space charges were introduced by stressing the sample electrically with dc biasing. The effects of implantation process on charge accumulation and dissipation in the dielectric are studied by capacitance-voltage (*C-V*) measurement qualitatively and quantitatively. The experimental results show that the charging and discharging behavior of the ion implanted silicon nitride films deposited by LPCVD is quite different from the one deposited by PECVD. The charge accumulation in the dielectric film can be reduced by ion implantation with proper dielectric deposition method. © *2009 American Institute of Physics.* [DOI: 10.1063/1.3147862]

I. INTRODUCTION

rf microelectromechanical systems (MEMS) is currently gathering an increased interest from academic and industrial community working on microwave and antennas applications for defense or space technology.[1] A rf MEMS switch is one of the basic building blocks in the rf communication systems.[2] However, their commercialization is currently hindered by their poor reliability. The accumulation of charge in the dielectric layer of capacitive rf MEMS switches has been identified as a primary source of switch failure.[3,4] The development of reliable switches requires a good understanding of the charging and discharging mechanism in the dielectric films, which were deposited using different processes.[5] In order to eliminate or minimize dielectric charging, one must be able to understand and quantify the charging in the dielectric.

In rf MEMS switches, the exact mechanisms for the charge accumulation in the dielectric layers are not well known. However, charge accumulation can be measured by several methods that have already been reported. One method to measure dielectric charging, implemented by Goldsmith *et al.*,[3] is to characterize switch lifetime. Reid and Webster[6] investigated dielectric charging in capacitive shunt switches by measuring a shift in bias voltage after continuously switching on and off the switches. It has been confirmed that the injected charge in the dielectric can cause *C-V* curve of the switch to shift by an amount directly pro-

portional to the magnitude and polarity of the charge.[7,8] After an initial *C-V* measurement between the silicon substrate and the capacitive bridge with no dc offset is made from the difference which the initial *C-V* measurement is subtracted from all subsequent *C-V* measurements with specific dc offsets, the quantity of the trapped charges can be calculated quantitatively.[9]

In this paper, we modified the distribution of the energy states in the dielectric films experimentally by ion implantation technology. By measuring and analyzing the *C-V* curves of metal-insulator-semiconductor (MIS) structures, the relaxation process of injected charges in the dielectric layer after dc bias stress was characterized qualitatively and quantitatively.

II. THEORETICAL ANALYSIS

A. MIS structure for studying charge accumulation and relaxation in dielectric films in rf capacitive MEMS switches

A schematic structure of rf MEMS capacitive switch is shown in Fig. 1(a). It consists of a freestanding bridge plate above a coplanar waveguide (CPW) transmission line. Under this "bridge," a dielectric with high permittivity is present. When a dc voltage is applied between the CPW central conductor and the surrounding ground plane, the bridge is attracted electrostatically, and it collapses and lands on top of the dielectric when the dc actuation voltage is high enough [as shown in Fig. 1(b)].

When the dielectric film contact the metal bridge, a high electrical field will be produced across the layer so that it is

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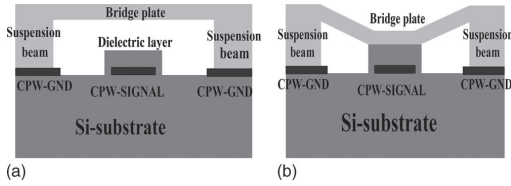
FIG. 1. (a) Schematic structure of rf MEMS capacitive switch. (b). Down states of rf MEMS capacitive switch.

possible for charges to be injected and further to be trapped in the dielectric film. The screening voltage resulted from accumulated charge in the dielectric layer detracts the actuation voltage until there is no more enough electrostatic force pulling on the membrane to cause it to actuate, or when the actuation voltage is removed, the accumulated charges provide enough electrostatic force to keep the membrane down.[3,10] That is the main failure mechanism for the stiction of the rf MEMS switches.

According to the schematic structure of the switch shown in Fig. 1(b), metal-insulator-metal structure (MIM) can be used to model the charge injection and trapping process for rf MEMS switches. However, the quantification of the trapped charges and their relaxation process cannot be easily performed by using MIM structure. Fortunately, we are more interested in the trapped charges and their relaxation process in the dielectric layer, so we can use MIS structure shown in Fig. 2 to model the rf MEMS switch after the charge injection although the charge injection mechanisms may not be the same as in the real rf MEMS switches. It will be efficient to characterize the charges accumulated in the dielectric and to study relaxation process of the trapped charges by performing C-V measurement on the MIS structures. In Ref. 11, we have demonstrated that the effective trapped charges in MIM and MIS have same expression form, an analogous analysis for switch model can be realized by means of the C-V characteristics of MIS structure.

B. dc stress and *C-V* measurements

It has been reported that the amount of charge accumulated in a certain dielectric layer depends on the magnitude and time of applied electric field.[12] The dc pulse, simulating the actuation voltage, is used to electrically stress the MIS structure in this work. After the dc pulse stress, C-V measurements are carried out by applying a dc gate voltage with
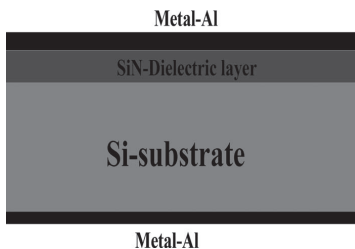

FIG. 2. MIS capacitor structure.

a superimposed small ac signal of varying frequency. The dc gate voltage changes slowly to obtain a continuous curve showing regions of accumulation, depletion, and inversion for the conduction layer in the substrate semiconductor. The charge variation due to the ac signal gives rise to a measurable capacitance which can be given by

$$C = -\frac{dQ}{dV}, \tag{1}$$

where Q represents the total charge in the conduction layer of the substrate semiconductor, V represents the gate voltage, and C represents the capacitance.

Flat band voltage (V_{FB}), which is a negative voltage applied between the metal and semiconductor to achieve the flat band, as a function of the time of the dc stress or the total amount of the injected charges, provides information on how many charges are trapped in the insulator in the MIS structure, so the amount of charges accumulated in the dielectric layer can be obtained by measuring the V_{FB} shift in the C-V curves. The shifts of C-V curves toward the left or right indicate that the net positive or negative charges injected into the dielectric. In the experiments, the samples were first biased with dc stress, so that charges can be injected into the dielectric films. The dynamic process of charging and discharging can be analyzed by comparing the C-V curves measured before and after charge injection.

In order to determine the flat band voltage, we must calculate the flat band capacitance (C_{FB}), the voltage corresponding to which is V_{FB}, the C_{FB} is given by[13]

$$\frac{C_{FB}}{C_0} = 1 / \left[1 + \frac{\varepsilon_{ro}}{\varepsilon_{rs}} \left(\frac{\varepsilon_{rs}\varepsilon_o k_o T}{q^2 N_A d_0} \right)^{1/2} \right], \tag{2}$$

where C_0 is the capacitance, which is corresponding to the biggest capacitance shown in the C-V curve, ε_0 is the permittivity of free space, ε_{ro} is the relative permittivity of the dielectric, ε_{rs} is the relative permittivity of the semiconductor, k_o is the Boltzman constant, T is the temperature, the measurement was performed at room temperature, q is the elementary charge, N_A is the dopant concentration, and d_0 is the thickness of the insulator.

V_{FB} can be extracted from the C-V data according to C_{FB}. In order to simplify the process of calculation, we can assume that all the trapped charges are located at the silicon-insulator interface although the trapped charges can be generated not only at the silicon-insulator interface, but also in the bulk. The trapped charge, ΔN_t, can be calculated by

$$\Delta N_t = -\frac{C_0}{q} \Delta V_{FB}, \tag{3}$$

where ΔV_{FB} caused by the trapped charge is the magnitude of measured V_{FB} shift.

Trapped charge calculated from the change in flat band voltage is an approximation of the charge located in the insulator structure. By measuring the C-V curve shift along the voltage axis as a function of dc stress to determine the charge accumulation, this measurement technique has the advantage of being simple and direct.

TABLE I. The parameters of the deposition process.

Sample	1	2
Deposition method	PECVD	LPCVD
Temperature (°C)	250	780
Pressure (Pa)	8	30
Flow ratio (SCCM:SCCM)	$SiH_4:NH_3$ (38:11)	$SiH_2Cl_2:NH_3$ (150:10)
Thickness (Å)	2000	3000

III. EXPERIMENT

A. Preparation of silicon nitride films

It is well known that SiO_2 and Si3N4 thin films contain high density of traps associated with dangling bonds. The space charges can be built up by the trapping processes. Due to the absence of convenient conducting paths in SiO_2 or Si_3N_4, the lasting time for trapped charge dissipation can be of the order of seconds to days.[1,3]

In this work, we select Si_3N_4 as the insulator layer in the MIS structure. For reference purposes, eight same Si wafers were prepared, four of them deposited with low pressure chemical vapor deposition (LPCVD) silicon nitride films, the others deposited with LPCVD silicon nitride films. The resistivity and doping level of the Si wafer are about 0.5 Ω cm and 1.5×10^{16} cm^{-3}, respectively. Hydrogen is built into the deposited layer during the films preparation. For plasma enhanced chemical vapor deposition (PECVD) silicon nitrides the hydrogen content can reach 40% while in LPCVD silicon nitrides the concentrations as small as 3% was observed. H atom is bonded mostly to nitrogen in the deposited layer.[14] The deposition parameters are shown in Table I.

B. Ion implantation

By employing ion implantation, impurity energy levels are introduced into the forbidden band of the dielectric layer. Ion implanted samples will have different charging/discharging properties from the virginal samples (samples before the ion implantation). Either P or B ions were implanted into both PECVD and LPCVD silicon nitride films. Table II lists the parameters for the ion implantation process.

After ion implantation, two unimplanted samples, which were selected from LPCVD and PECVD samples, respectively, together with all implanted samples were rapidly thermal annealed at 900 °C for 30 min to reduce the defects caused by the ion implantation. Then Al was sputtered onto the top surface as the gate electrode (150×150 μm^2), and on the backside of the silicon substrate to form a better con-

TABLE II. The parameters of the ion implantation process.

Parameter	Thickness (nm)			
	200	300	200	300
Doping Ions	B		P	
Implantation energy (KeV)	30	40	80	105
Implantation Depth (nm)	150	175	150	180
Implantation concentration (cm^{-3})	2×10^{12}	2×10^{12}	2×10^{12}	2×10^{12}

TABLE III. The information of the eight different samples.

	LPCVD	
1	Virginal sample	
2	Annealed sample	Annealing
3	P ions implanted sample	Annealing, P ion implantation
4	P ions implanted sample	Annealing, B ion implantation
	PECVD	
5	Virginal sample	
6	Annealed sample	Annealing
7	P ions implanted sample	Annealing, P ion implantation
8	P ions implanted sample	Annealing, B ion implantation

tact between the sample and chuck plate for getting ideal C-V curves. Table III lists the information of the eight different samples.

IV. EXPERIMENTAL RESULTS AND DISCUSSION

A. Results for samples without electrical stress

The C-V curves had been measured on all samples by performing a voltage sweep from −20 to 20 V with frequency of 100 kHz. As shown in Figs. 3(a) and 3(b), the V_{FB} obtained from the C-V curves of different samples are different. For the LPCVD samples shown in Fig. 3(a), the V_{FB} obtained from the C-V curve of the virginal sample is −11.47 V, which is the maximum observed one. The V_{FB}

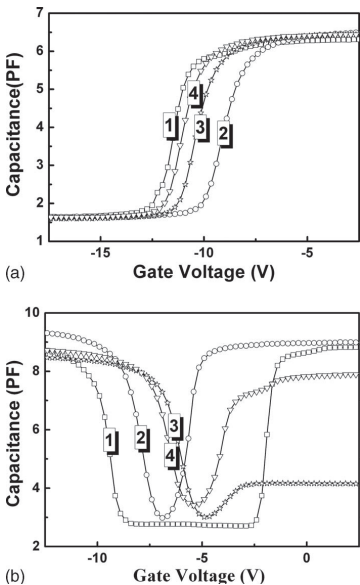FIG. 3. (a) C-V curves measured on four different MIS samples prepared with LPCVD process before charge injection. (b) C-V curves measured on four different MIS samples prepared with PECVD process before charge injection. (In the two figures, 1 is the C-V curve measured from the original sample, 2 is for the annealed original sample, 3 is for the annealed B ion implanted sample, and 4 is for the annealed P ion implanted sample.)

obtained from the *C-V* curve of the annealed sample is -9.01 V, which is the minimum observed one. For P and B implanted samples, the values of V_{FB} are -10.95 and -10.37 V, respectively, which are between the value of the V_{FB} for the virginal sample and the annealed sample.

The distributions of positive space charges are observed in all four LPCVD samples, which can be shown in Fig. 3(a). Because the greater absolute value of V_{FB}, the more space charges in the sample, among the four samples the virginal sample contains the largest number of the space charges, followed by the ion implanted samples, while the annealed sample contains the lowest number of space charges.

Based on the virginal sample, changes in the quantity of space charges in other samples can be calculated by using Eq. (3). Compared with the virginal sample, the quantity of the positive space charges in the annealed sample can be reduced about 9.84×10^7 due to the annealing process. However, compared with the annealed sample, the positive space charges have been introduced into the ion implanted samples. We found that B ion implantation can reduce 2.32×10^7 more space charges in the dielectric layer than P ion implantation does. The above results can be explained as the following.

Under the high temperature of the annealing, outgas of hydrogen will occur because that Si–H and N–H bond will break due to its low bonding energy in the silicon nitride films. Apparently, the annealing process would lead to the increase in N and Si dangling bonds, which are shown as positive charges. However, all N and Si dangling bonds would likely recombine during the annealing process. Furthermore, high temperature can also repair the structural defects in the film. So the dangling bonds shown as positive charges in the dielectric can be significantly reduced as the annealing result.

As the positive charges (implanted impurity ions) would be introduced into the dielectric films by ion implantation, more space charges would exist in the ion implanted samples in comparison with the virginal sample. Because the P ion has a higher chemical valence than B ion, thus, P ion implantation can introduce more positive charge than B ion implantation.

For PECVD nitride silicon films, our experimental results presented in Fig. 3(b) show different distributions of the space charges from LPCVD samples. The V_{FB} obtained from the *C-V* curve of the virginal sample is -9.43 V, which is the maximum observed one, while -6.36 and -5.86 V are the V_{FB} obtained from the *C-V* curve of P and B ions implanted samples, respectively. Both of them are less than the V_{FB} of -7.76 V obtained from the *C-V* curve of the annealed sample.

During annealing, the PECVD silicon nitride films will go through similar crystal reparation process as LPCVD deposited films do. In addition, for the PECVD silicon nitride films, the implanted ions have great chance to recombine some N and Si dangling bonds, which appear because of bad quality of the PECVD nitride silicon films. Therefore, compared with the annealed sample, the ion implanted samples contain the lowest number of space charges although the positive charges are simultaneously introduced into the di-
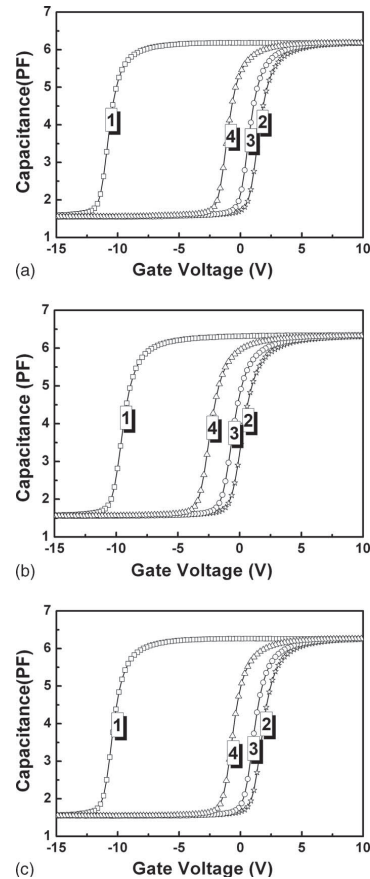

FIG. 4. (a) *C-V* curves measured on the annealed sample before and after the charge injection. (b) *C-V* curves measured on the P implanted sample before and after the charge injection. (c) *C-V* curves measured on the B ion implanted sample before and after the charge injection. (In the three figures, 1 is the *C-V* curve measured before charge injection. 2 is the *C-V* curve measured 0 min after charge injection. 3 is the *C-V* curve measured one minute after charge injection. 4 is the *C-V* curve measured fifty minutes after charge injection.)

electric films by ion implantation, and the annealed samples contain less but not the lowest number of positive space charges.

As shown in Fig. 3(b), comparing the virginal sample with the annealed sample, the quantity of the space charges can be reduced about 9.84×10^7 by annealing. Compared with the virginal and annealed samples, the *C-V* curves measured from P and B ion implanted samples both shift to the right side. Obviously the positive space charges can be reduced by ion implantation. We can also find that B ion implantation can reduce 2.8×10^7 more space charges in the dielectric film than P ion implantation does.

B. Results for LPCVD samples after electrical stress

After making the *C-V* measurements without electrical stress, all samples were electrically stressed by biased with
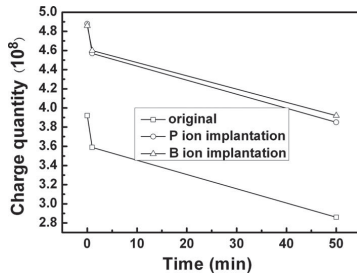
FIG. 5. The quantity of trapped charges vs time after dc stress for the three LPCVD samples.

dc (80 V) for 30 s, while the gate electrode was connected to the positive polarization. Then, the *C-V* measurements were performed immediately (0 min), 1 and 50 min after the stress (charge injection), respectively. For the LPCVD silicon nitride samples, Figs. 4(a)–4(c) present the *C-V* curves measured before and after dc stress for the annealed sample and the ion implanted samples. For the annealed sample, the ΔV_{FB} of 9.82 V is obtained by the measurement instantaneously (0 min) after the charge injection, while, for the P and B ion implanted samples, we obtained the ΔV_{FB} as 12.22 and 12.12 V, respectively. Clearly, after the same electrical stress, there are more charges injected into the ion implanted samples in comparison with the annealed samples.

The discharging processes of the trapped charges in the dielectric layer can be analyzed by the measurement results presented in Fig. 5. After the charge injection, the *C-V* curves measured from both the implanted sample and the annealed sample shift to left side along the voltage axis, while the magnitude of the shift (ΔV_{FB}) depends on the waiting time before the *C-V* measurements. Following Eq. (3), the values of ΔN_t can be obtained for the different measurements. From the measurement, which was made after discharging for 0 min, 1 and 50 min after the charge injection, the ΔN_t values were found to equal 3.92×10^8, 3.59×10^8, and 2.86×10^8, respectively, for the annealed sample, 4.88×10^8, 4.57×10^8, and 3.58×10^8, respectively, for the P ions implanted sample, and 4.86×10^8, 4.60×10^8, and 3.92×10^8, respectively, for the B ions implanted sample.

As a brief summary, the discharging processes in all three different type of samples, e.g., the annealed samples, and the P and B ion implanted samples, have similar behavior. However, quantitatively, the number of the injected charges finally remained in the annealed sample is the lowest, and the discharging speed of the injected charges in the annealed sample is the fastest. We can conclude that the trap centers introduced into the silicon nitride layer by the P and B ion implantation enhance the charge accumulation in the dielectric layer.

C. Results for PECVD samples after electrical stress

In Fig. 6(a)–6(c), the *C-V* curves were measured from the PECVD samples before and after the dc stress (80 V for 30 s). For the annealed sample, the ΔV_{FB} of 17.15 V is obtained from the measurement instantaneously after the
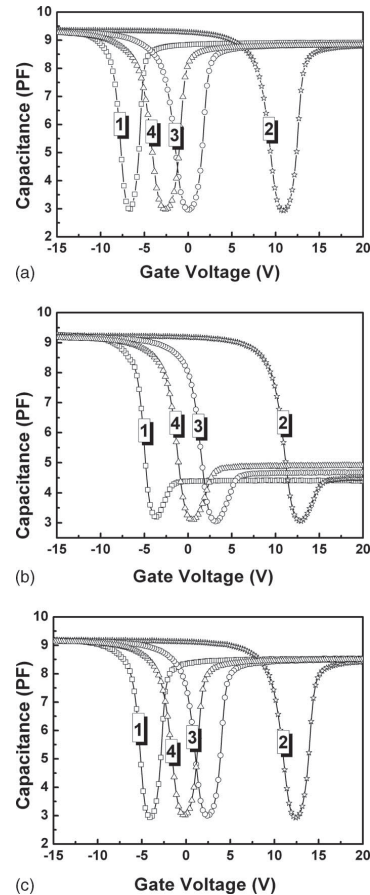

FIG. 6. (a) *C-V* curves measured on the annealed sample before and after the charge injection. (b) *C-V* curves measured on the P ion implanted sample before and after the charge injection. (c) *C-V* curves measured on the B ion implanted sample before and after the charge injection. (In the three figures, 1 is the *C-V* curve measured before injection. 2 is the *C-V* curve measured 0 min after charge injection. 3 is the *C-V* curve measured one minute after charge injection. 4 is the *C-V* curve measured fifty minutes after charge injection.)

charge injection. For P and B ion implanted samples, such ΔV_{FB} are found to equal 16.16 and 15.98 V, respectively. Unlike LPCVD samples, we found that for the PECVD samples the electrical stress results in a smaller right shift of *C-V* curves of the implanted samples than that of the annealed samples. Thus, there are more space charges injected into the annealed sample.

The relaxation processes in silicon nitride layer deposited by PECVD can be analyzed by the results presented in Fig. 7. The ΔN_t values were also obtained from the measurements, which were made after discharging for 0, 1, and 50 min, respectively, after the charge injection. For the annealed sample, the ΔN_t equals 10.06×10^8, 3.68×10^8, and 2.13×10^8, respectively. For the P ions implanted sample, the ΔN_t equals 9.48×10^8, 3.67×10^8, and 2.08×10^8, respectively.
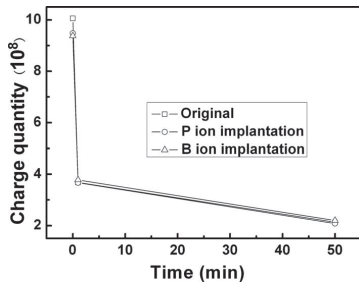
FIG. 7. The quantity of trapped charges vs discharing time after dc stress for the three PECVD samples.

For the B ions implanted sample, the ΔN_t equals 9.38×10^8 to 3.78×10^8 and 2.20×10^8, respectively. Those data exhibit the different results from the LPCVD deposited samples, e.g., the discharging process happened much quicker in the PECVD samples than that in the LPCVD samples.

In order to analyze the effect of ion implantation on the charging and discharging processes in the PECVD samples, the results presented in Figs. 5 and 7 can be compared in detail. We can see that there are more negative space charges injected into the annealed sample than into the ion implanted samples. After discharging for 50 mins, the quantity of injected charges finally remained in the P ions implanted sample is the lowest among all the PECVD samples. It shows that the implanted ions can act as recombination centers in the dielectric layer, and P ion implantation can alleviate the charge accumulation more efficiently than B implantation.

We also found that the effect of ion implantation on the charging and discharging in PECVD samples differ from that in LPCVD samples. The implantation effect is not more obvious in PECVD samples than in LPCVD samples, possibly because of higher density of defects in PECVD samples than in LPCVD samples. Our reasoning is that more defects will screen the influence of the implantation to the charging and discharging processes.

V. CONCLUSIONS

In this work, the charging/discharging behaviors of the dielectric used in rf capacitive MEMS switch have been investigated by the C-V measurement on a MIS structure. The results show that:

(1) Independent of the deposition methods (here LPCVD and PECVD), positive charges were observed in all samples before the electrical stress, e.g., annealed samples (annealing after deposition) and implanted samples (ion implantation and then annealing after the deposition).

(2) Compared with the annealed sample, both P and B ion implantation processes add more positive charges into the implanted samples, which were deposited by LPCVD, on the contrary, the implantation processes reduce some positive charges in the implanted samples, which were deposited by PECVD.

(3) Electrical stress with dc bias (80 V, 30 s) injects negative charges in all samples used in this work. After removal of the bias voltage, some of the injected charges in the dielectric layer will disappear quickly, and some of the injected charges will remain in the dielectric layer for a relative long period. Thus, both fast and slow states exist in the samples.

(4) At the same electrical stress, charges are much more easily injected into the samples deposited by PECVD than by LPCVD. We find that the discharging process happened much quicker in the PECVD samples than in the LPCVD samples.

Above experimental results and analysis offer some useful information for understanding the doping effect on the charge injection and discharging in the dielectric layer. Ion implantation and deposition methods will play a very important role to cause or delay the stiction failure of capacitive rf MEMS switch due to the charge accumulation in the dielectric layer. In order to improve the lifetime and reliability of the rf MEMS switch, fast states have to be created in the dielectric layer to accelerate the relaxation processes with proper ion implantation and deposition methods, and ion implantation, which forms trap centers in the dielectric layer, must be avoided.

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Chapter 6
Conclusions

The development of reliable switches requires a good understanding of the dielectric charging and discharging characteristics. The ultimate goal of this research is to fully investigateand understand dielectric charging and discharging properties, and find the effective way to migrate charge accumulation in the dielectric for high reliable RF MEMS switch.

6.1 Charge accumulation in silicon nitride

6.1.1Charge injection in silicon nitride

The behaviors of charge injection in the silicon nitride of an Al/Si_3N_4/n-Si metal–insulator–semiconductor (MIS) device are systematically studied before and after applying different high constant DC bias conditions with the aim of controlling charge accumulation in the dielectric when a high actuation voltage is applied. We found that both polarity and magnitude of charge accumulation in silicon nitride depend on the biasing direction. Charge injection from the semiconductor to the silicon nitride always dominates over charge injection from the Al electrode to the silicon nitride. Negative charge accumulation happens in silicon nitride when the Al electrode is positively biased, and positive charge accumulation occurs in silicon nitride when the Al electrode is negatively biased. The positive charge accumulation is much bigger than the negative charge accumulation under the same magnitude of stress voltage. Furthermore, the experimental results also show that the charge injection level exponentially increases with the applied voltage across the silicon nitride.

A charge injection model has been proposed for explaining these observed charge accumulation behaviors. This model proposes a balance of holes and electrons from the Fowler–Nordheim limited injection that is a major factor in the voltage dependence of charge trapping. An essential feature of the model has been that hole injection, in addition to electron injection, has been taken into account. We emphasize that our model is not intended as a numerically precise analysis of what is (in reality)a very complicated situation. Rather, it is a basic model intended to provide justification and support for our basic physical hypotheses. At this level, the model can well explain the experimental results. From the experimental and modeling results, it follows that the tunneling barrier heights for electrons and holes in a given MIS structure are very important parameters to evaluate charge injection behaviors,

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which will change as the bias polarity changes. The charge injection model developed in this paper may provide us with a possibility to control or change charge injection behaviors in the dielectric by changing the parameters related to charge injection in the model.

6.1.2 Charge relaxation in silicon nitride

For both positive and negative dc bias polarities, fast and slow discharge stages were clearly observed in the early and late charge relaxation process, respectively.The discharge ratio was found to depend on both the polarity and magnitude of the bias voltage,the discharge ratio decreases as the dc bias voltage increases, and moreover, negative bias voltage will lead to a very high hole injection level but very low discharge ratio, while positive bias voltage will lead to a very low electron injection level but very high discharge ratio in MIS device. It was further found that the hole relaxation reaches the steady state faster than the electron relaxation.

To explain the observed results we proposed a generalized charge relaxation model, in which charge escape from the traps close to the Si/Si_3N_4 interface plays an important role. From the charge relaxation model, we attribute the fast discharge rate in the early relaxation process to the back tunneling of the trapped carriers near the Si/Si_3N_4 as well as the thermal excitation from shallow traps levels, while attribute the slow discharge rate to the random thermal excitation in the later stage.It is concluded that the low discharge ratio of hole relaxation comes from the limited number of shallow traps in silicon nitride. We further suppose that the discharge ratio increases with the stress voltage comes from the different trapping mechanisms, because the traps close to the interface will have a low probability to capture charges under high stress voltage.

6.2 Charge accumulation in silicon oxide

The behaviors of charge injection in the silicon oxide are also systematically studied in an $Al/SiO_2/n$-Si metal–insulator–semiconductor (MIS) device. Charge injection behaviors in SiO_2 are different from that in Si_3N_4 films, the polarity of the bias voltage have little influence on the sign and magnitude of charge injection in silicon oxide. Independent on dc bias polarity, electrons injection in SiO_2 always dominates the charge accumulation either the

metal electrode is positively biased or negatively biased. The charge accumulation under negative bias voltage is only slightly different from that under positive bias voltage with same magnitude. Furthermore, the experiment results also show that charge injection level exponentially increases with the applied voltage in SiO_2. Taking into account the roles of electrons and holes in the process of charge injection, the observed experiment results can be simply explained by the tunneling barrier at each contact interface. The investigation of this work will enable us to have a better understanding of the effects on dielectric charging in Capacitive RF-MEMS switches.

6.3 Charge accumulation in multi-layer dielectrics

In order to develop a new solution to the problem of the irreversible stiction of capacitive RF MEMS switch attributed to the dielectric charging, we investigate how charge accumulates in multi- and single-layer dielectric structures by using metal-insulator-semiconductor (MIS) capacitor structure. Two multi-dielectric-layers are structured, which are $SiO_2+Si_3N_4$ and $SiO_2+Si_3N_4+SiO_2$ stack films. Meanwhile, Si_3N_4 single-layer dielectric structure is also fabricated for comparison. We found that the polarity of charge accumulated in the dielectric is influenced by the dielectric structure. When the metal electrode is positively biased, negative charge accumulates in the single- and triple-layer devices while positive charge accumulates in the double-layer devices. When positive bias voltage is applied to the metal electrode of MNOS device, the large potential barriers of oxide layer will suppress the electron injection from silicon substrate, thus, the probability of electron injection thus will be greatly reduced, as a result, the electron injection level becomes lower thanthe level of hole injection, hole injection dominates the charge injection in the MNOS device. Furthermore, the experiment results also show that the lowest charge accumulation can be achieved using double-layer dielectric structure even though the fastest relaxation process takes place in triple–layer dielectric structure, the lowest charge level in MNOS device must be attributed to the narrowed difference between electron and hole injection probabilities in comparison with MNS and MONOS devices. This paper proposes a new approach to the problem of the irreversible stiction of capacitive radio frequency (RF) microelectromechanical (MEMS) switch attributed to the dielectric charging.

6.4 Charge accumulation in double-layer dielectric

The behaviors of charge accumulation in double-layer dielectric can be strongly affected by the SiO_2 thickness between the Si_3N_4 and the Si substrate. When the metal electrode is positively biased, net negative charge accumulates in the thin-oxide Si_3N_4/SiO_2 dielectric structure while net positive charge accumulates in the thick-oxide Si_3N_4/SiO_2 dielectric structure. To explain the observed experimental results, we basically proposed a balance of holes and electrons from a modified Fowler-Nordheim limited charge injection model in combination with the interface trap assisted tunneling. It is demonstrated that the sign of the charge accumulated in the MNOS devices can be determined by the SiO_2 thickness between the Si_3N_4 and the Si substrate. For the thin-oxide MNOS structure, we attributed the negative charge accumulation to the enhancement of electron injection from silicon substrate, which is caused by Si_3N_4/SiO_2 interface trap assisted tunnelling due to lower distance from this interfaceto the electron injection interface. Conversely, the positive charge accumulation in the thick-oxide MNOS structure was assumed to come from the suppression of electron injection, because the oxide is too thick to allow the interface trap assisted tunnelling. The effects of SiO_2 thickness on charge accumulation in Si_3N_4/SiO_2 stacked dielectric may make it possible to balance the number of injected charges from the top and bottom electrodes by optimizing the thickness ratio of Si_3N_4 to SiO_2.

6.5 Charge accumulation in ion implanted dielectrics

In order to accelerate charge relaxation process for low charge accumulation, we investigated the charging and discharging behaviors in ion implanted dielectric. The experiments showed that:

1) Independent of the deposition methods (here LPCVD and PECVD), positive charges were observed in all samples before the electrical stress, e.g., annealed samples (annealing after deposition), implanted samples (ion implantation and then annealing after the deposition).

2) Compared with the annealed sample, both P and B ion implantation processes add more positive charges into the implanted samples which were deposited by LPCVD, on the contrary, the implantation processes reduce some positive charges in the implanted samples

which were deposited by PECVD.

3) Electrical stress with DC bias (80V, 30 seconds) injects negative charges in all samples used in this work. After remove of the bias voltage, some of the injected charges in the dielectric layer will disappear quickly, and some of the injected charges will remain in the dielectric layer for a relative long period. Thus, both fast and slow states exist in the samples.

4) At the same electrical stress, charges are much more easily injected into the samples deposited by PECVD than by LPCVD. We find that the discharging process happened much quicker in the PECVD samples than in the LPCVD samples.

6.6 Charge accumulation in SiO_2 films containing silicon nanocrystals

The relaxation processes of both positive and negative charges are discovered in SiO_2 films containing silicon nanocrystals under positive applied voltage. The negative charge injection is dominant under positive voltage stress, however, the relaxation process of negative charges injected in the dielectric is much faster than positive charges, as a result, the accumulation of net positive charge in the dielectric is observed at last. We confirmed that the charging and discharging characteristic can be modified by embedding nonocrystals into the dielectric, it is anticipated that the charge trapping and their relaxation in the dielectric of capacitive MEMS switch can be controlled by embedding nanocrystals into the dielectric in terms of materials (Ge, Si or other), density, size of nanocrystals and their distribution.

Chapter 7
Outlook

Chapter 7 Outlook

In this thesis, we employed a metal-insulator-semiconductor (MIS) capacitor structure to investigate the dielectric charging and discharging for high reliable capacitive rf MEMS switches. The dielectric charging and discharging kinetics were qualitatively and quantitatively characterized by comparing the measured capacitance-voltage (C-V) curveson MIS structure before and after charge injection. Finally, we come up with the possible approach to migrate the charge accumulation in the dielectric.

The experiments of dielectric charging and discharging characteristic shows that for a certain dielectric, the effects of positive and negative voltage stress on dielectric charging are different, therefore, the stress polarity will lead to more serious charge accumulation should be avoid. Furthermore, if we use bipolar waveform stress, we should determine the magnitude of positive and negative voltage stress (peak voltage), the actuation waveform should be asymmetrical in magnitude and stress time for eliminating the charge accumulation in switch dielectric.

The experimental results of charging and discharging prosperities in ion implanted dielectric also offer useful information for understanding the doping effecton the dielectric charging and discharging behaviors. Ion implantation and deposition methods will play a very important role to cause or delay the stiction failure of capacitive RF MEMS switch due to the charge accumulation in the dielectric layer. In order to improve the lifetime and reliability of the RF MEMS switch, we should determine the best impurity ions to create fast states to accelerate trapped charge to be detrapped, meanwhile, the case of the impurity which will form trap centers in the dielectric should be avoid.

From the experimental results and analysis of multiple dielectric layers, the behaviors of charge accumulation in double-layer dielectric can be strongly affected by the SiO_2 thickness between the Si_3N_4 and the Si substrate. When the metal electrode is positively biased, net negative charge accumulates in the thin-oxide Si_3N_4/SiO_2 dielectric structure while net positive charge accumulates in the thick-oxide Si_3N_4/SiO_2 dielectric structure. The effects of SiO_2 thickness on charge accumulation in Si_3N_4/SiO_2 stacked dielectric may make it possible

to balance the number of injected charges from the top and bottom electrodes by optimizing the thickness ratio of Si_3N_4 to SiO_2.

Acknowledgement

At first, I would like to thank the financial support of The China Scholarship Council (CSC) and Vestfold University College (VUC).

Many thanks give to my supervisors, Prof. Xuyuan Chen, Prof. Oddvar Søråsen and Assoc. Prof. Ulrik Hanke for their great support and guidance during my studies. Prof. Xuyuan Chen walked me through all the stages of the writing of this thesis. Without his consistent and illuminating instruction, this thesis could not have reached its present form.

I would like to thank the classmates, teachers and also engineers in Pen Tung Sah MEMS research center at Xiamen University, China, for helping me do experimental work of MEMS fabrication. I also thank the State Key laboratory for Physical chemistry of solid surface at Xiamen University, China, for allowing me to use their instruments to do electrochemical testing.

I would like to my colleague, Deokki Min for helping me to do experiments in the cleanroom at Vestfold University College. I also thank other colleagues at Vestfold University College who gave me their help and brought me a lot of fun.

Last my thanks would go to my beloved parents, my brother and my wife for their loving considerations, great confidence in me and strong supports all through these years. Otherwise, the thesis would not be completed.