Interfacial properties of heterojunctions between transparent conductive oxides and silicon for solar cells

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"If I have seen further it is by standing on the shoulders of giants."

-Isaac Newton

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Abstract

Thin films of transparent conductive oxides as active electrodes in combination with silicon substrates are pursued for new generation of solar cells. A main issue is to obtain structures with optimum interfacial properties in order to minimize charge carrier recombination and maximize cell efficiency. In this work we have investigated electronic properties and thermal stability of the interfacial states between indium tin oxide (ITO) and monocrystalline silicon. ITO films with thicknesses of 60 and 300 nm have been deposited by dc magnetron sputtering on n- and p-type (100) Si at room temperature. The samples were then annealed for 30 min at different temperatures in the range 100-600°C. Current-voltage (IV), capacitance-voltage (CV) and deep-level transient spectroscopy (DLTS) have been used to electrically characterize the interface between ITO and Si. DLTS measurements on the samples with p-type Si reveal a dominant hole trap at around 0.37 eV above the valence band edge. In the n-type samples, several major electron traps have been observed in the range 0.1-0.2 eV below the conduction band edge. These electron traps are characterized by broad DLTS peaks indicating a broad band of the electronic energy levels rather than isolated point defect levels. All the traps in both p- and n-type samples are found to be located near the ITO-Si interface. Investigation of thermal stability of the observed electronic states has revealed that the dominant hole trap can be annealed out at 250°C for 30 min, while the dominant electron traps can be stable up to 500°C. IV and DLTS measurements demon-

strate clear correlation between the annealing of the dominant electronic states and increase in the junction rectification.

Chapter 1

Introduction

"We are at the very beginning of time for the human race. It is not unreasonable that we grapple with problems. But there are tens of thousands of years in the future. Our responsibility is to do what we can, learn what we can, improve the solutions, and pass them on."

- Richard P. Feynman

From a large scale view, this thesis has the purpose of adding knowledge that in turn may help solar cells to take advantage of more of the sunlight that reaches it. Today, the solar cell marked is dominated by one technology which has about 95% marked share (2007) [1]. This is based on the material silicon (Si), and such a solar cell make use of around 15-25% of the sunlight depending on the method of production [2]. Ideally, it would be favourable to increase the efficiency without increasing the cost of production. In this way, solar cells could in the near future be a significant competitor on the global energy marked. To reach this ambition, development of the solar cells that today are beeing produced must advance to a new level.
In this thesis I have investigated a technology which is based on exchanging the front metal contacts of the solar cell with a thin film material that has the ability to conduct electrons and at the same time is transparent in

the visible and ultra violet wavelength regime. One such class of materials is called Transparent Conductive Oxides (TCO). This has the advantage of letting through more light to the active parts of the cell, and reducing the resistive loss in the contacts, if made properly. The main focus of this thesis is to deposit thin films of a TCO and investigate how the interface between the two materials in contact depends on the post deposition heat treatment. Both structural and electrical characterization are conducted in search of a better understanding of how the physics of the interface relates to the electrical current flowing across it.

Chapter 2

Background

"When it comes to atoms, language can be used only as in poetry. The poet, too, is not nearly so concerned with describing facts as with creating images."

- Niels Bohr

This Chapter gives an overview of the basic theory which this thesis is based upon. In doing so it is assumed that the reader has at least some background in physics. The basis of what makes a solar cell will be briefly discussed, but since this is more of a material study, the basic semiconductor theory will be the main focus. The Chapter starts with a brief introduction to the topic of solid state physics, and then introduces the semiconductor physics which is relevant to the thesis. Kittel [3] and Streetman [4] are the basis for most of the theory on crystals and semiconductors while Blood and Orton [5] is used in the derivation of the emission rate from trap states.

2.1 Introduction

Materials can be classified into metals, semiconductors and insulators after their ability to conduct electrons. The underlying property that separate

them from each other can be found when looking into solid state physics [3]. As atoms come together and form solids, they order themselves in a way as to minimize their total energy. This often means that the atoms form a periodic arrangement. Materials with a periodic arrangement are called crystals, with a corresponding crystal structure. The periodicity changes the energy levels of the electrons, from discrete levels (in a single atom) to continuous bands of energy (in the solid). The difference between metals, semiconductors and insulators can then be described by how the electrons of the solid fill the energy bands. Semiconductors and insulators have a completely filled valence band and an empty conduction band, but metals have partially filled or overlapping energy bands. Thus, electrons in metals have "lots of space" to move around in their bands, while electrons in semiconductors and insulators are much more restricted. As a consequence of the periodicity, there will be some energy regions without any electron states available. Such a region is called a band gap and is shown schematically in Fig.2.1. Semiconductors differ from insulators in the way that their band gap is low enough that thermal energy can excite electrons into empty energy bands where they are free to move. Figure 2.1 shows how one can distinguish the difference between insulators, semiconductors and metals by looking at the filling of their bands.

2.2 Crystal structure and charge carriers

As mentioned above, solid materials with a periodic arrangement of atoms are called crystals. All crystalline materials have a corresponding crystal structure. This structure is a way of describing how the atoms in the crystal are arranged in reference to a mathematical representation of points in a three dimensional (3D) lattice. Figure 2.2 shows the three different cubic lattices that are possible to separate mathematically. In all there are four-

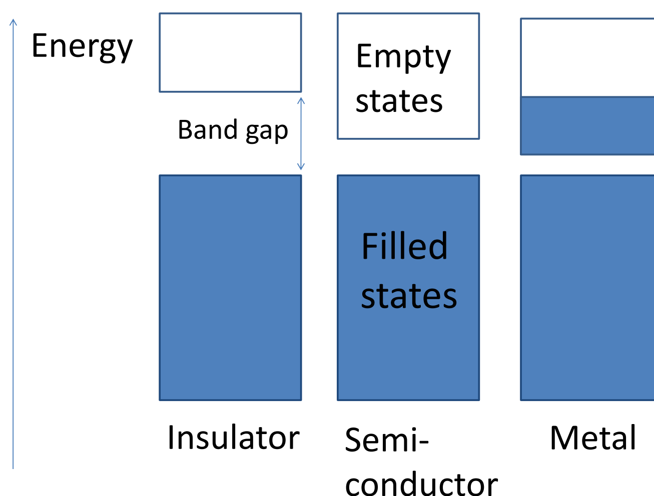


Figure 2.1: Schematic view of the difference in band filling between insulators, semiconductors and metals.

teen different lattices that are mathematically different. When describing the periodicity of the crystal, the concept of the unit cell is very useful. A unit cell is basically a bravais lattice, with a basis. The basis is given if there are some atoms in positions that are not lattice sites. Silicon has the crystal structure of diamond shown in Fig.2.3. It has a face-centered cubic (FCC) bravais lattice with a basis of $(0, 0, 0)$ and $(\frac{1}{4}, \frac{1}{4}, \frac{1}{4})$. This means that there is one Si atom at all the lattice sites in FCC and an additional atom at one quarter of the cube diagonal away from the lattice sites (see Fig.2.3).

As Si is a semiconductor, it has completely filled and empty bands at sufficiently low temperatures. This means that electrons within the filled bands move by exchanging positions with other electrons. Because of this, there is no net conduction in semiconductors unless some of the electrons in the filled band are excited to the empty band. The excited electron is now in an empty band, and has an excess of unoccupied energy states available, making conduction possible. In the filled band, which the electron was excited from, there is now an empty site that other surrounding electrons can fill. This empty site can move around in the band, leading to conduction.

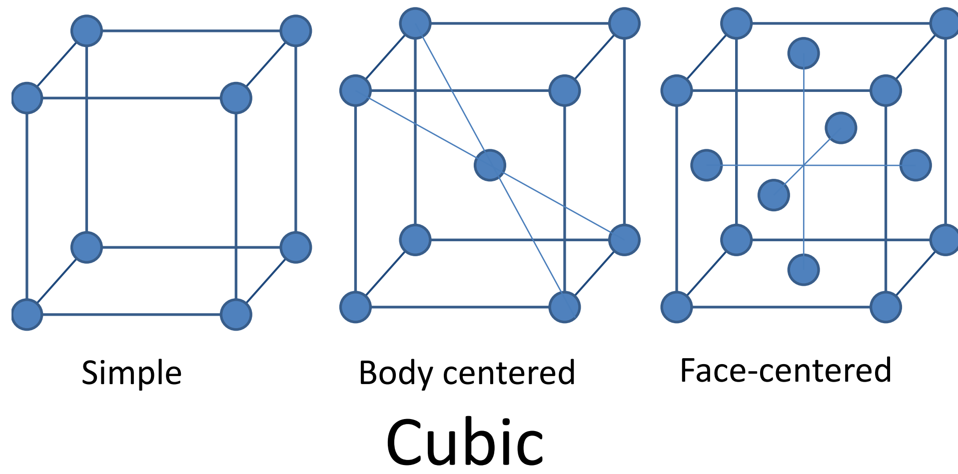


Figure 2.2: The three types of cubic bravais lattices. The round dots mark the lattice sites

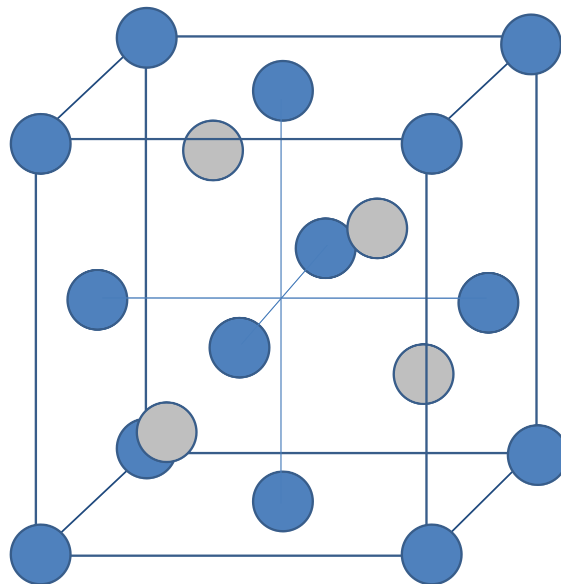


Figure 2.3: The diamond crystal structure. The blue dots are lattice sites in FCC

Since it is easier to count the empty site, than the enormous amount of electrons, the empty site is called a hole and exhibits the property of a positive charge. The filled band is called the valence band and the empty band is called the conduction band, and the conduction is described by holes and electrons, respectively. Figure 2.4 shows the process of excitation of electrons across the band gap. Excitation can occur by absorption of i) thermal energy from the lattice or ii) incident photons with energy greater than the band gap.

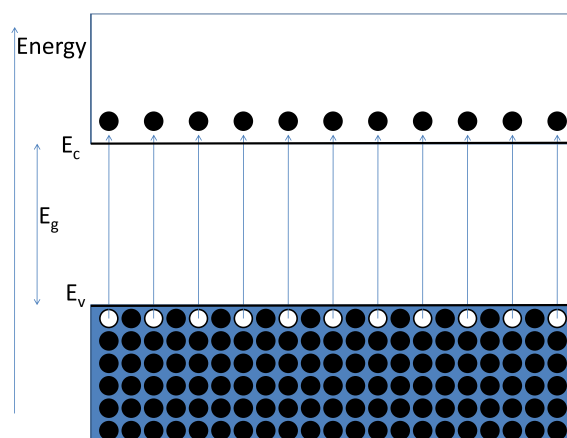


Figure 2.4: Excitation of electrons across the band gap leaving behind empty states (holes)

A pure semiconductor crystal with no impurities of any kind, is called an intrinsic semiconductor. If an electron is excited from the valence to the conduction band, the amount of holes p in the valence band must equal the amount of electrons n in the conduction band. So for a given temperature:

$$n = p = n_i \tag{2.1}$$

where n_i is called the intrinsic carrier concentration.

There are other means of varying the conductivity of a semiconductor. By introducing impurities in to the crystal (called doping) one can add holes in the valence band or electrons in the conduction band. The extra holes or

electrons come from impurities and defects in the crystals. Figure 2.5 shows a schematic view of some types of point defects in crystals. Substitutional atoms that have one more electron, in its outer orbit, than the host crystal atoms can donate its extra electron to the conduction band. Substitutional atoms with one electron less, can be able to accommodate electrons from the valence band. Thus, impurities can change the amount of electrons or holes that are free to move. Semiconductors with more electrons in the conduction band than holes in the valence band are called n-type conductors with a doping concentration N_d. More holes in the valence band than electrons in the conduction band makes a p-type conductor with doping concentration N_a. Figure 2.6 illustrates what happens when foreign atoms introduce donor and acceptor states in the band gap.

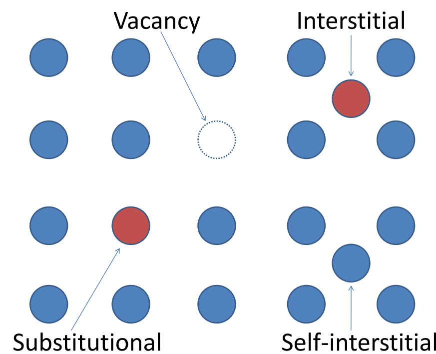


Figure 2.5: Different types of fundamental defects in crystals

Since electrons are fermions, we have to consider Fermi-Dirac statistics when calculating the concentration of electrons and holes. The concentration of electrons in the conduction band and holes in the valence band is given by:

$$p = \int_0^{E_v} (1 - f(E))N(E)dE \tag{2.2}$$

$$n = \int_{E_c}^{\infty} f(E)N(E)dE \tag{2.3}$$

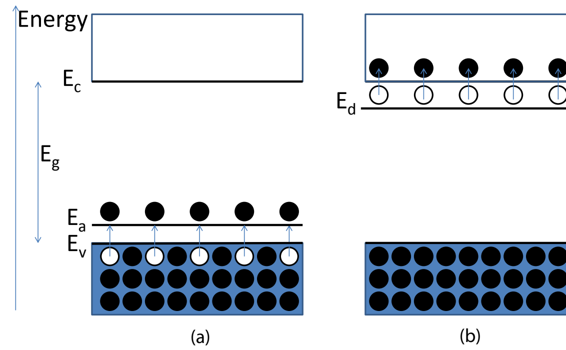


Figure 2.6: a) P-type doping. Excitation from valence band to acceptor state b) N-type doping. Excitation from donor state to conduction band

Where $f(E)$ is the *Fermi-Dirac function* and $N(E)$ is the density of states in the respective bands.

$$f(E) = \frac{1}{1 + e^{(E_c - E_f)/kT}} \approx e^{-(E_c - E_f)/kT} \tag{2.4}$$

$f(E)$ gives the probability that an electron will occupy an electron state of energy E. E_c is the energy position of the bottom of the conduction band and E_v is the top of the valence band. k is Boltzmanns constant, T is temperature and E_f is called the Fermi level, which is defined so that $f(E_f) = 1/2$. Since $f(E)$ is a step function at 0 K, all levels below E_f are filled and all above are empty. At elevated temperatures, the step in $f(E)$ is smoothed out and this gives a distribution of electrons in the conduction band and holes in the valence band. The approximation of $f(E)$ is valid when E_f is several kT below the conduction band edge E_C, and is often a good approximation. Due to the shape of $f(E)$ the states very close to the band edges will be occupied, and we can replace N(E) with an *effective density of states* at the band edges. The concentration of electrons and holes can then be expressed as:

$$p = N_v e^{-(E_f - E_v)/kT} \tag{2.5}$$

$$n = N_c e^{-(E_c - E_f)/kT} \tag{2.6}$$

With

$$N_{c,(v)} = 2\left(\frac{2\pi m^*_{n,(p)} kT}{h^2}\right)^{3/2} \tag{2.7}$$

Where $m^*_{n,(p)}$ is the effective mass of electrons (holes) and h is Plancks constant. The intrinsic carrier concentration n_i of a semiconductor introduced in Eq.2.1 can be calculated in the same manner as shown above. Given an intrinsic Fermi level E_i in a semiconductor, n_i, p_i is given as:

$$n_i = N_c e^{-(E_c - E_i)/kT} \tag{2.8}$$

$$p_i = N_v e^{-(E_i - E_v)/kT} \tag{2.9}$$

According to Eq.2.1, $n_i = p_i$. Combining Eq.2.8 with this, we can rewrite the equations for n, p into:

$$n = n_i e^{(E_f - E_i)/kT} \tag{2.10}$$

$$p = n_i e^{(E_i - E_f)/kT} \tag{2.11}$$

This way of calculating n, p will be useful in the derivation of the current flow across the junction given in appendix A.2

2.3 P-n junctions

Junctions between semiconductors are crucial for solar cells, light emitting diodes (LED), transistors and so on. Let us consider the situation where two semiconductors, one n-type and one p-type are joined together. The large gradient in charge carriers at the junction will lead to diffusion. When

electrons diffuse over the junction, they leave behind positively charged donor-atoms, and holes leave behind negatively charged acceptor-atoms. Thus, an electric field is set up in the depletion region (W) around the junction (see Fig.2.7) creating an energy barrier for the charge carriers. In equilibrium, the diffusion will balance the drift of carriers in the opposite direction. A contact potential V_0 is developed as a built-in potential barrier for the charge carriers, in order to maintain equilibrium conditions.

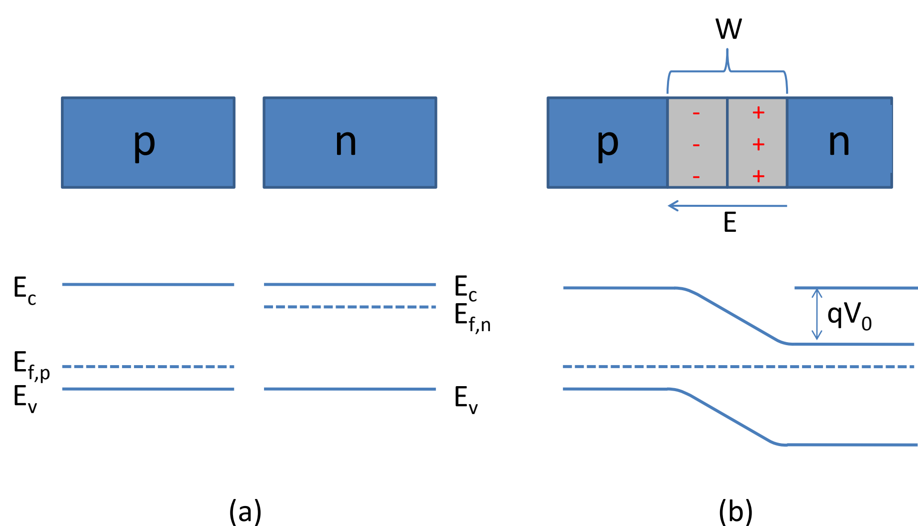


Figure 2.7: a) P- and n-type semiconductors and their energy bands b) P-n junction with the combined energy bands, depletion region, contact potential and electric field

2.3.1 Depletion capacitance of the p-n junction

This Section will discuss the depletion capacitance of a p-n junction, and the outline will follow that of Streetman [4]. The charge density $\rho_{p,(n)}$ in the depletion region on p- and n-side of the junction is given by:

$$\rho_p = -qN_a$$
$$\rho_n = qN_d \tag{2.12}$$

where q is the elementary charge and $N_{a,(d)}$ is the doping concentration on the p(n)-side of the junction. Due to charge neutrality considerations, the charge on both sides of the junction is given by:

$$qAx_{p0}N_a = qAx_{n0}N_d \tag{2.13}$$

where A is the cross sectional area of the junction, and x_{p0} and x_{n0} are the extension of the depletion region on the p- and n-side, respectively (see Fig.2.8). *Poisson's equation* relates the gradient of the electric field to the charge in W:

$$\frac{dE(x)}{dx} = \frac{q}{\epsilon}(p - n + N_d^+ - N_a^-) \tag{2.14}$$

where ϵ is the dielectric constant for the semiconductor material. Since there is an electric field across the junction, any charge carriers within a diffusion length away from the junction will be swept across it. This means that there will be very few free charge carriers within W, so that both p and n can be neglected. This is called the *depletion approximation* and simplifies 2.14 to:

$$\frac{dE}{dx} = \frac{q}{\epsilon}N_d, \qquad 0 < x < x_{n0}$$
$$\frac{dE}{dx} = \frac{-q}{\epsilon}N_a, \qquad -x_{p0} < x < 0 \tag{2.15}$$

As seen in Fig.2.8, the absolute electric field will have its highest value $|E_0|$ at the metallurgical junction, and decreases in both directions. E_0 can be found by integrating any of the equations in 2.15:

$$\int_{E_0}^{0} dE = \frac{q}{\epsilon} N_d \int_{0}^{x_{n0}} dx$$
$$\int_{0}^{E_0} dE = \frac{-q}{\epsilon} N_a \int_{-x_{p0}}^{0} dx \tag{2.16}$$

This gives us for E_0:

$$E_0 = \frac{-q}{\epsilon} N_d x_{n0} = \frac{-q}{\epsilon} N_a x_{p0} \tag{2.17}$$

The voltage V_j which is developed across the junction is the sum of V_0 and the external applied voltage V_{ext}, and can be expressed as the red area in Fig.2.8 c) or mathematically as:

$$-V_j = -(V_0 - V_{ext}) = \int_{-x_{p0}}^{x_{n0}} E(x) dx \tag{2.18}$$
$$V_j = -\frac{1}{2} E_0 W = \frac{q}{2\epsilon} N_d x_{n0} W \tag{2.19}$$

With the relation $x_{n0} = W N_a / (N_a + N_d)$ (see appendix A.1) this becomes:

$$V_j = \frac{q}{2\epsilon} \frac{N_a N_d}{N_a + N_d} W^2 \tag{2.20}$$

By solving for W we have:

$$W = \left[\frac{2\epsilon V_j}{q} \left(\frac{N_a + N_d}{N_a N_d} \right) \right]^{1/2} \tag{2.21}$$

Finally, we introduce the concept of capacitance C, which for a non-linear relation between charge and voltage is defined as:

$$C = \left| \frac{dQ}{dV_j} \right| \tag{2.22}$$

The charge on either side of the junction, assuming a parallel plate capacitor, is given by:

$$|Q| = qAx_{n0}N_d = qAx_{p0}N_a \tag{2.23}$$

$$|Q| = qA\frac{N_dN_a}{N_d+N_a}W = A\left[2q\epsilon V_j\frac{N_dN_a}{N_d+N_a}\right]^{1/2} \tag{2.24}$$

Using this in the derivation of $|Q|$ gives:

$$C = \left|\frac{dQ}{dV_j}\right|$$

$$C = \frac{A}{2}\left[\frac{2q\epsilon}{V_j}\frac{N_dN_a}{N_d+N_a}\right]^{1/2}$$

$$C = \epsilon A\left[\frac{q}{2\epsilon V_j}\left(\frac{N_aN_d}{N_a+N_d}\right)\right]^{1/2} \tag{2.25}$$

$$C = \frac{\epsilon A}{W} \tag{2.26}$$

For large differences in doping (e.g. $N_a \gg N_d$), Eq.2.25 simplifies to:

$$C = \epsilon A\left[\frac{qN_d}{2\epsilon V_j}\right]^{1/2}$$

$$C = \left[\frac{qN_d\epsilon A^2}{2V_j}\right]^{1/2} \tag{2.27}$$

The capacitance is thus defined by the low doping side of junction, which together with the charge neutrality in Eq.2.23 gives that the depletion region will extend primarily into the low doped side of the junction. Such a junction is generally referred to as a p^+-n junction. If the junction is between a semiconductor and a metal, a similar expression can be found, since the carrier concentration is generally many orders of magnitude higher in the metal than in the semiconductor. The depletion region and its capacitance will then be governed by the doping of the semiconductor.

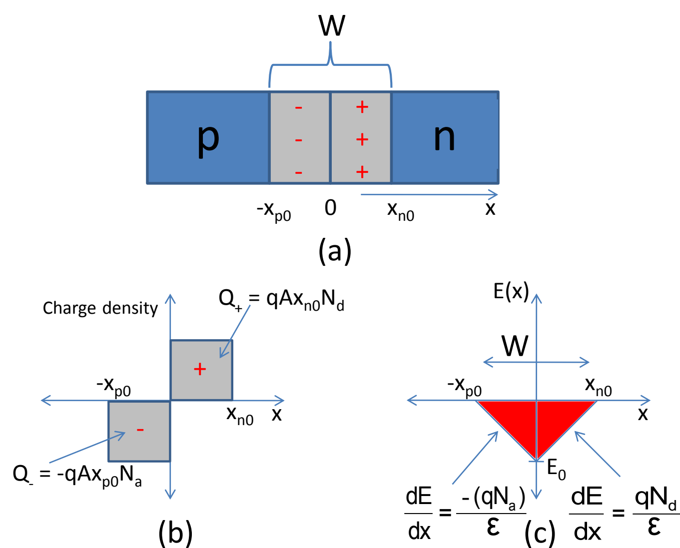


Figure 2.8: a) The depletion region W with 0 defined as the physical junction between the two semiconductors b) The charge density on both sides of the junction c) The electronic field distribution. The red area represents the contact potential V_0. Adapted from Ref.[4]

2.3.2 Applying a bias voltage to the p-n junction

As described in Section 2.3.1, the voltage across the junction is a combination of the contact potential V_0 and the external voltage applied V_{ext}. Looking at the expression for W (Eq.2.21) we see that the depletion region will be smaller if V_j is reduced and larger if V_j is increased. A consequence of this is that the barrier the charge carriers have to overcome to cross the junction (see Fig.2.9) will change with V_{ext}. Positive V_{ext} is called forward bias, and negative is called reverse bias.

2.4 Electrically active traps

Point defects can introduce, as described in Section 2.2, donor or acceptor states in the band gap. Such defects are called electrically active, and can change the population of charge carriers within the bands. Substitutional

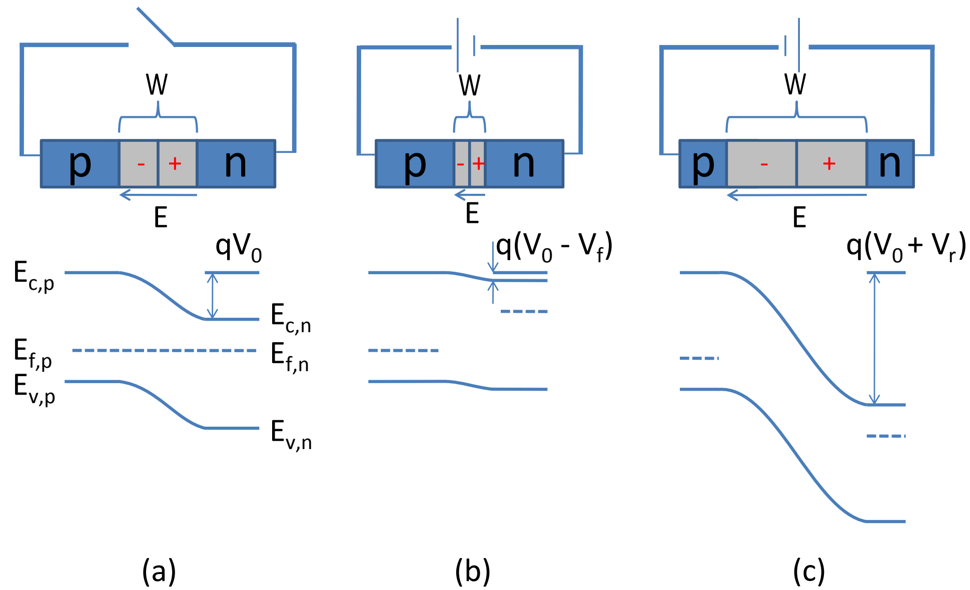


Figure 2.9: Effects of applying bias to the junction for a) No voltage applied (equilibrium conditions)b) Positive voltage applied (forward bias) c) Negative voltage applied (reverse bias)

defects that are usually used for doping a semiconductor, have states close to a band edge to maximize the doping efficiency, as a level close to a band edge will need less thermal energy to give up its charge carrier. More generally, defects in materials can introduce energy states within the whole band gap. If the levels are more than a few kT away from the band edges, they are not completely ionized at room temperature. These states have the ability to trap charge carriers, and are thus called traps. In Fig.2.10 one can observe that there are multiple options for capture and emission of charge carriers between an energy state E_t and the bands, and the charge of the trap will depend on its capture and emission rates.

If there are N_t traps in which n_t are occupied by electrons, the change in n_t can be expressed as:

$$\frac{dn_t}{dt} = (c_n + e_p)(N_t - n_t) - (e_n + c_p)n_t \tag{2.28}$$

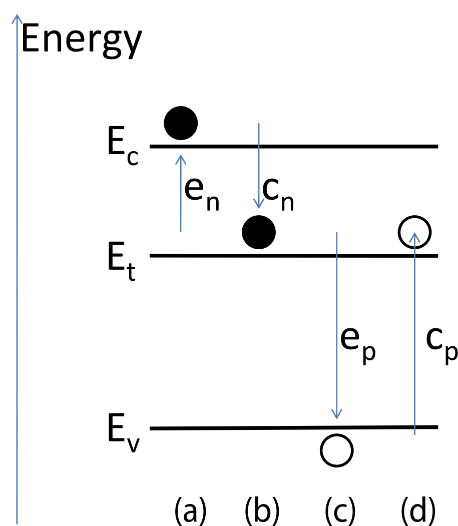


Figure 2.10: The possible emission and capture processes between an energy level E_t and the bands. a) Emission of electron from trap b) Capture of electron from conduction band c) Emission of hole from trap. d) Capture of hole from valence band

At thermal equilibrium, $dn_t/dt = 0$ must be satisfied. In addition, detailed balance demands that the emission and capture rate of the "individual" charge carriers must be the same. If this was not the case, a net transport of charge carriers between the bands could occur. This means that we can separate Eq.2.28 into one equation for electrons and one for holes:

$$c_n(N_t - n_t) = e_n n_t \tag{2.29}$$

$$e_p(N_t - n_t) = c_p n_t \tag{2.30}$$

Rearranging Eq.2.29-2.30 gives us the thermal occupancy of the traps:

$$\frac{n_t}{N_t} = \frac{c_n}{c_n + e_n} = \frac{e_p}{e_p + c_p} \tag{2.31}$$

The thermal occupancy can also be expressed by the *Fermi-Dirac function* given in Eq.2.4:

$$\frac{n_t}{N_t} = (1 + e^{(E_t - E_f)/kT})^{-1} \tag{2.32}$$

Inserting this into Eq.2.31 and rearranging (appendix A.3) one obtains:

$$\frac{e_n}{c_n} = e^{(E_t - E_f)/kT} \tag{2.33}$$

$$\frac{e_p}{c_p} = e^{-(E_t - E_f)/kT} = e^{(E_f - E_t)/kT} \tag{2.34}$$

2.4.1 Capture and emission rate

The capture rate of a trap state is defined as the flux of electrons crossing an area per unit time. If there are n free electrons with a thermal velocity of $v_{th,n}$ within a region of $(N_t - n_t)$ unoccupied traps with capture cross section σ_n in the time Δt, one obtains a capture rate per unoccupied trap:

$$c_n = \frac{n v_{th,n}(N_t - n_t)\sigma_n \Delta t}{(N_t - n_t)\Delta t}$$

$$c_n = \sigma_n v_{th,n} n = \sigma_n v_{th,n} N_c e^{-(E_c - E_f)/kT} \tag{2.35}$$

$$c_p = \sigma_p v_{th,p} N_v e^{-(E_f - E_v)/kT} \tag{2.36}$$

Where n is given by Eq.2.6. Inserting Eq.2.35 and 2.36 into Eq.2.33 and 2.34, respectively, one obtains the following emission rate:

$$e_n = \sigma_n v_{th,n} N_c e^{-(E_c - E_t)/kT} \tag{2.37}$$

$$e_p = \sigma_p v_{th,p} N_v e^{-(E_t - E_v)/kT} \tag{2.38}$$

According to Eq.2.35-2.38, the capture rate is dependent on the position of E_f, but the emission rate is not. The emission rate for electrons (holes) depends on the energy difference $E_c - E_t$ ($E_t - E_v$) and the *capture cross section* $\sigma_{n,(p)}$. E_t and $\sigma_{n,(p)}$ are characteristic properties of the trap, and

can for example be found if the emission rate is determined for different temperatures. The energy required for an electron to be excited from the trap into the conduction band, can be related to *Gibbs free energy* as $\Delta G(T) = \Delta H - T\Delta S = E_c - E_t$. The emission rate can then be expressed as:

$$e_n = \sigma_n v_{th,n} N_c e^{-\Delta G/kT} = \underbrace{e^{-\Delta S/k}\sigma_n}_{\sigma_{na}} v_{th,n} N_c e^{-\Delta H/kT} \tag{2.39}$$

$$e_n = \sigma_{na}\beta T^2 e^{-\Delta H/kT} \tag{2.40}$$

Here β contains all the temperature independent constants and σ_{na} is called the *apparent capture cross section*. Dividing this by T^2, means that a plot of $\ln(e_n/T^2)$ vs. $1/T$ (called an Arrhenius plot) will give the straight line:

$$ln(e_n/T^2) = -\Delta H/kT + ln(\beta\sigma_{na}) \tag{2.41}$$

$$\beta T^2 = v_{th,n} N_C = \sqrt{\frac{3kT}{m_n^*}} 2\left(\frac{2\pi m_n^* kT}{h^2}\right)^{3/2} = \underbrace{\sqrt{\frac{3k}{m_n^*}} 2\left(\frac{2\pi m_n^* k}{h^2}\right)^{3/2}}_{\beta} T^2 \tag{2.42}$$

ΔH can be found from the slope of the line in Eq.2.41 and σ_{na} is found where the extrapolated line and the e_n/T^2-axis intersect. ΔH is the activation enthalpy and ΔS is entropy. In the literature, thermal measurements of ΔH are often sited as $(E_c - \Delta H)$, ignoring the entropy factor (i.e. ΔH is interpreted as ΔG). This is not necessarily valid in all cases, as ΔS might give a significant contribution. The correct approach to find ΔG in thermal experiments would be to measure e_n and σ_n at a certain temperature, and calculate ΔG from Eq.2.39. However, it has been shown that for shallow hydrogenic states in Si there is no change in entropy and $\Delta H = \Delta G$, while for deep states this is generally not true [5].

In addition to these characteristics, traps are either labeled as electron or hole traps. Traps located in the upper half of the band gap have $e_n > e_p$ because $(E_c - E_t) < (E_t - E_v)$. They interact mostly with the conduction band and therefore capture and emit electrons. It is then labeled as an electron trap. The converse holds for hole traps. The precise energy level E_1 in which a trap is neither of the above, is when $e_n = e_p$. Rearranging Eq.2.37-2.38 (see appendix A.4) gives:

$$E_1 = E_i + \frac{kT}{2} ln\left(\frac{\sigma_p v_{th,p}}{\sigma_n v_{th,n}}\right) \tag{2.43}$$

Where E_i is given by:

$$E_i = \frac{E_c + E_v}{2} + \frac{kT}{2} ln\left(\frac{N_v}{N_c}\right) \tag{2.44}$$

E_i is the Fermi level in an intrinsic material. Figure 2.11 shows where the electron and hole traps are located within the band gap. The experimental technique used in this thesis to determine traps within the band gap is called Deep-Level Transient Spectroscopy (DLTS) and will be discussed in Section 3.5. In this thesis, measurements of ΔH will be presented as $(E_c - \Delta H)$ for electron traps and $(E_v + \Delta H)$ for hole traps, in order to emphasis the difference between electron and hold traps. This will be done, while keening in mind the possible contribution of ΔS.

2.5 Solar cells

This Section reviews some of the theory related to solar cells and introduce concepts which will illustrate the relevance of the investigated samples in this thesis. In the field of solar cells, the two regions in a p-n junction are called base and emitter (see Fig.2.13), adopted from the transistor terminology. Most of this Section is based upon discussions in Nelson [2], if not stated otherwise.

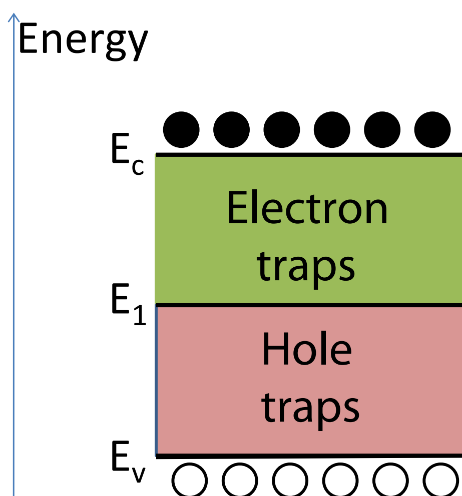


Figure 2.11: Schematic view of which part of the bang gap contains electron and hole traps

2.5.1 Current across the junction

If the recombination in the depletion region is neglected, the ideal diode equation becomes (see Appendix A.2 for derivation):

$$I = I_0(e^{qV/kT} - 1) \tag{2.45}$$

In solar cells this current is often called the dark current of the solar cell. The curve labeled "Dark" in Fig.2.12 shows the current voltage curve for an ideal pn-junction in dark. Often real diodes deviate from ideality, and an *ideality factor* η is added to the diode equation:

$$I = I_0(e^{qV/\eta kT} - 1) \tag{2.46}$$

If the ideality factor is around 2, recombination in the depletion region dominates the current [4] and for heterojunctions, values above 2 can be attributed to tunneling effects across the junction [2]. When a solar cell is illuminated, electron-hole pairs (EHP) will be generated if the incident photons have energy $E = h\nu > E_g$, where ν is the frequency of the photon.

Some of the photo generated carriers can diffuse into the depletion region, and will then be swept across the junction due to the electric field. During the time the carriers diffuse, it is essential that they do not recombine, through radiative band to band, trap-assisted or Auger recombination (see Fig.2.15). If they reach the contacts, they will give rise to a photo generated current. In Fig.2.12 the short circuit current I_{SC}, open circuit voltage V_{OC} and the maximum power point P_{max} are marked. The operating area of a solar cell is the fourth quadrant of the IV curve, that is in the voltage range $0 \leq V \leq V_{OC}$. This is the only area where the diode delivers power. At P_{max} the effect of the cell is obtained as:

$$P_{max} = I_{mp} V_{mp} \tag{2.47}$$

The relation between the ultimate operating point (I_{SC} and V_{OC}) is defined by the fill-factor FF as:

$$FF = \frac{I_{mp} V_{mp}}{I_{SC} V_{OC}} \tag{2.48}$$

The fill-factor describes the "squareness" of the IV curve, and should be as close to unity as possible. If the solar cell is illuminated by an incident solar spectrum of effect P_s, the efficiency η of the cell is defined as:

$$\eta = \frac{P_{max}}{P_s} = \frac{I_{SC} V_{OC} FF}{P_s} \tag{2.49}$$

By having a standard for testing solar cells, the values of I_{SC}, V_{OC}, FF and η can be compared for different technologies. The standard is defined to be 25°C and a incident power density of 1000 W/m^2 from a photon spectrum called air mass 1.5 (AM1.5).

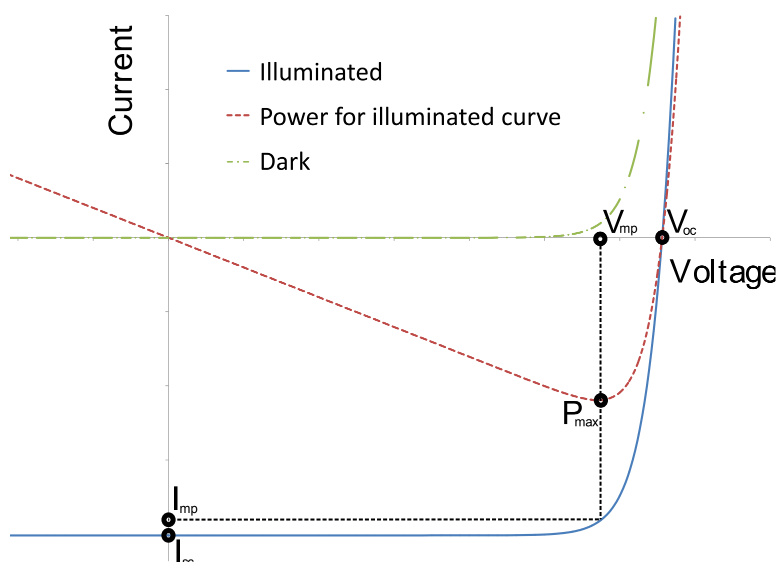


Figure 2.12: Current voltage curves for dark and illuminated solar cell, including power curve showing maximum power point.

2.5.2 Solar cell designs

There are many different solar cell concepts on the commercial market, and in research labs. However one can select three main groups. The first is the wafer[1] based cells, which use a "multicrystalline" (mc) or "singelcrystalline" (sc) wafer as the base, where Si is the main material. This technology had about 95% market share in 2007 [1]. The remaining two concepts are both, in principle, thin film based solar cells, but generally thin film solar cells refer to low cost thin films deposited on large areas. Amorphous Si (a-Si), copper indium gallium selenide (CIGS) and cadmium telluride (CdTe) are the leading thin film technologies. The last group is the high efficiency multi-junction cells based upon combinations of gallium indium arsenide (GaInAs) and gallium indium phosphide (GaInP). This is a high cost concentrator[2] cell with a world record efficiency of 40.8% at a concentration of

[1] A wafer is a thin (150-500 μm) slice of Si cut from a large ingot

[2] A small cell is monted under a concentrating lense or at the focal point of a parabolic dish

326 suns [6].

A conventional Si solar cell is based upon a mc or sc wafer (see Fig.2.13a). The surface is usually treated with a directional etchant to give a pyramid structure that reduce reflection at the surface. An emitter is created by diffusion of a dopant into the top layer of the wafer during a high temperature process, before a layer of insulating silicon nitride (SiN_x) is deposited on top of the cell. It act as an anti-reflecting (AR) layer[3] as well as surface passivation. The last step involves contacting the emitter to metal contacts on top of the AR layer by a high temperature firing of the contacts through the SiN_x layer. Researchers at Sanyo delevoped a new approach to wafer based solar cells. It is called the heterojunction cell, and use a-Si with hydrogen (a-Si:H) as the emitter [7],[8],[9]. Hydrogen passivates defects in the a-Si emitter [2] and the a-Si:H provides good interface passivation to Si [10]. This concept uses a transparent conductive oxide (TCO) as the AR layer.

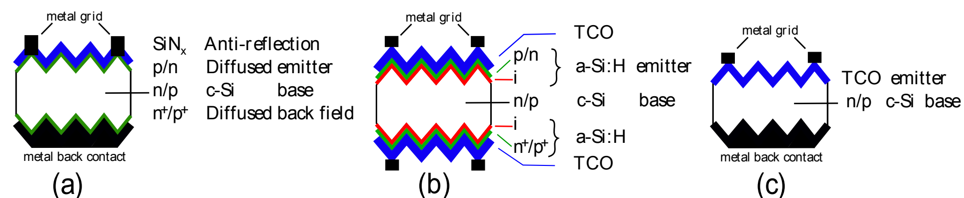


Figure 2.13: Different solar cell designs based on a Si-wafer as the base. a) Conventional Si solar cell b) Heterojunction cell proposed by Sanyo [9] c) Schottky cell

2.5.3 Heterojunctions

When two different materials make up a junction, it is referred to as a heterojunction. At the interface, there will be discontinuities in the valence and

[3]The use of an AR layer can reduce the reflection from a Si surface by making the reflected waves from the two surfaces destructively interfere (see Fig.2.14)

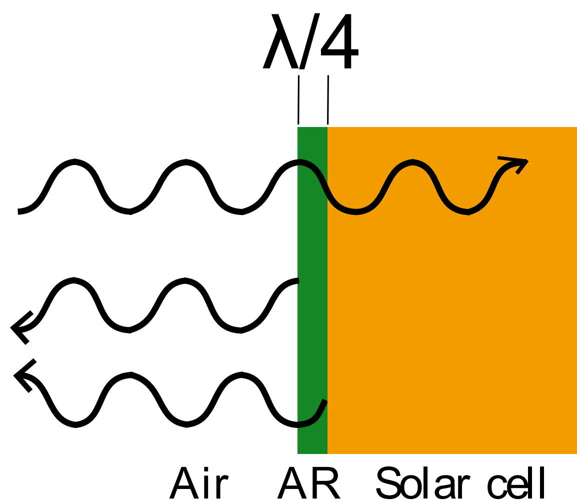


Figure 2.14: Illustration of how an anti-reflecting layer works. The two reflected waves destructively interfere.

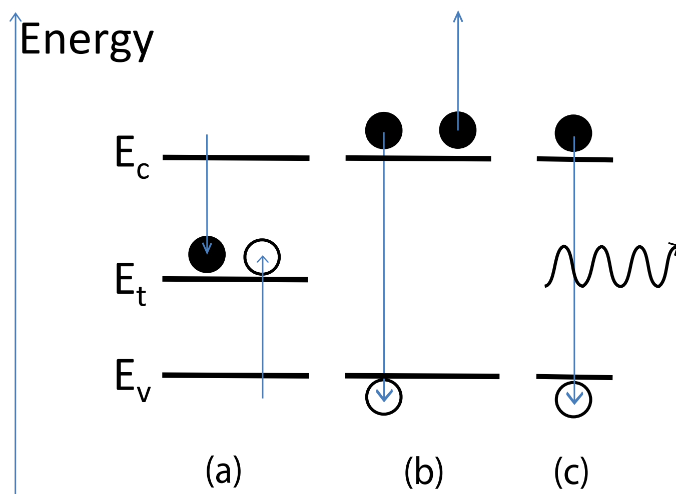


Figure 2.15: Recombination mechanisms that limit solar cell performance. a) Non radiative, trap-assisted b) Auger c) Radiative, band to band

conduction bands because of differences in band gap and electron affinities [2]. This can lead to increased recombination at the interface compared to a homojunction. In addition, differences in lattice constants and crystal structure can lead to strain around the interface, creating dislocations which also lead to recombination [6].

2.5.4 Transparent conductive oxides (TCO)

The first reported TCO was cadmium oxide (CdO), prepared by Bädeker in 1907 [11]. Since then, this material class has attracted much attention for applications in optoelectronics such as transparent electrodes for solar cells, liquid crystal displays and photo detectors [12]. TCOs are generally highly degenerate[4] wide band gap semiconductors ($\geq$ 3 eV), which gives a high transparency in the visible region of the solar spectrum and low resistivity. Indium tin oxide (ITO) is the most widely used TCO today and is based on Sn doped In_2O_3, a semiconductor first investigated by Rupprecht in 1954 [13]. The source of doping in TCOs can be both intrinsic (i.e. related to defects that occur natural in the material) and extrinsic (i.e. intentionally added impurities). As will be discussed for ITO, the nature of carrier formation is not always straight forward and can be difficult to controll. Zinc oxide (ZnO) is a popular candidate for replacing ITO in the future, as it has a similar band gap and transparency. The main reason is the low abundance of In, which is only present at a level of 0.2 ppm in the earths crust, in contrast to 83 ppm for Zn [14].
In a solar cell, the TCO layer can either act as a transparent front contact to the emitter, or as the emitter itself (see Fig.2.13). Used as a front electrode, the low resistivity reduces the resistive loss to the front metal contacts. In addition, low temperature metal contacts can be deposited and the stan-

[4]Degeneracy means that the Fermi level is inside the conduction band, leading to a very high carrier concentration

dard procedure of firing the contacts through the silicon nitride layer at elevated temperatures is eliminated. This reduce the chance of the contacts punching through the emitter and contacting to the base which would lead to shunting [15]. If the TCO layer can make a rectifying contact to the base, it can operate as the emitter. With a band gap $\geq$3eV, most of the visible and infrared light will be transmitted through the TCO and absorbed in the base. This can potentially improve the collection of photons, since absorption in the emitter can be neglected.

2.5.5 Indium tin oxide (ITO)

ITO consists of a solid state mixture of SnO_2 in In_2O_3, and has the same crystal structure as In_2O_3, called bixbyite [16],[17],[18] (see Fig.2.16(a)). As Sn is incorporated into the In_2O_3 structure, the Sn atom can donate one electron to the conduction band as it has four electrons in its outer orbital in contrast to In which has three. The understanding of the mechanism which leads to conduction is complicated by several factors: i) The unit cell contains 80 atoms, with two inequivalent In sites, complicating the analysis related to which In sites the Sn atoms occupy [19],[20] (see Fig.2.16(b)). Popovic et al. [17] reported that the substitution was non-uniform and dependent on doping levels of Sn. ii) A large concentration of oxygen vacancies leads to the formation of an impurity band which overlaps with the conduction band, donating a maximum of two electrons per oxygen vacancy [12]. iii) Frank and Köstlin [16] proposed a model where there is a clustering of Sn and O atoms in addition to the substitution of Sn for In. This model was supported by first-principles density functional calculations by Warschkow et al. in 2006 [21].

There have been reported numerous ways to deposit thin films of ITO. Electron Beam Evaporation (EBE) [22], Pulsed Laser Deposition (PLD) [23], Chemical Vapor Deposition (CVD) [24] and Magnetron Sputtering (MSP)

[25],[26] are some examples. These techniques give a semiconductor with a low resistivity ($\sim 10^{-4}\Omega$cm), high transparency in the visible region ($> 80\%$), carrier consentration of ($\geq 10^{20}$cm^{-3}) and a band gap of $\geq$3eV. Since MSP (see Section 3.1) has been used in this thesis, I will mainly focus on this technique when comparing result from other groups. Balasundaraprabhu et al. [25] deposited ITO on glass using MSP, and reported good optical and electrical properties for post-deposition heat treated samples at 300°C (see Fig.2.17). By introducing hydrogen to the sputtering gas, Zhang et al. [27] obtained a reduced resistivity of ITO films deposited at room temperature compared to pure argon gas. No post deposition heat treatment was needed to obtain high conductive transparent films. Mudryi et al. [28] studied sputtered ITO films and found a band gap in the range $4.1 - 4.4$eV. They attibuted the change in band gap to the Burstein-Moss effect [29],[30],[31]. Figure 2.18 shows an illustration of how the apparent band gap of a degenerate semiconductor change with increasing carrier concentration according to the Burstein-Moss effect.

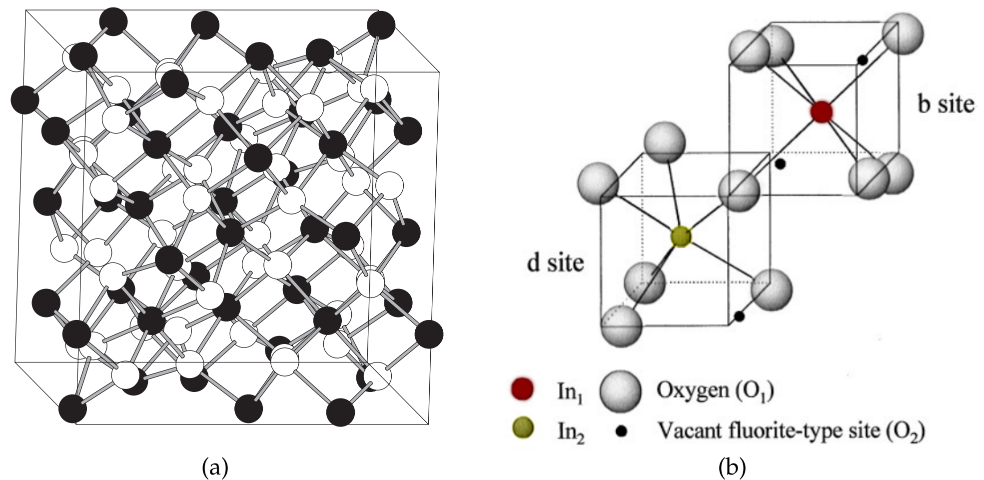


Figure 2.16: a) Unit cell of In_2O_3, called bixbyite. In and O are represented by black and hollow spheres, respectively [18]. b) The two inequivalent In sites in the bixbyite structure [19].

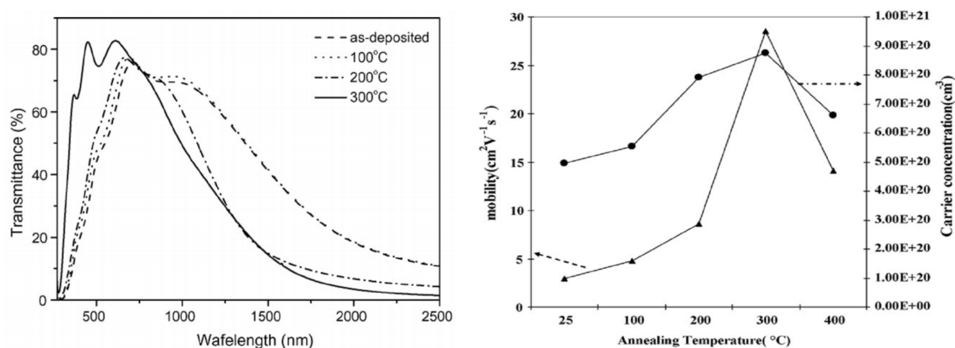


Figure 2.17: Electrical and optical properties of ITO deposited by MSP. Balasundaraprabhu et al. [25]

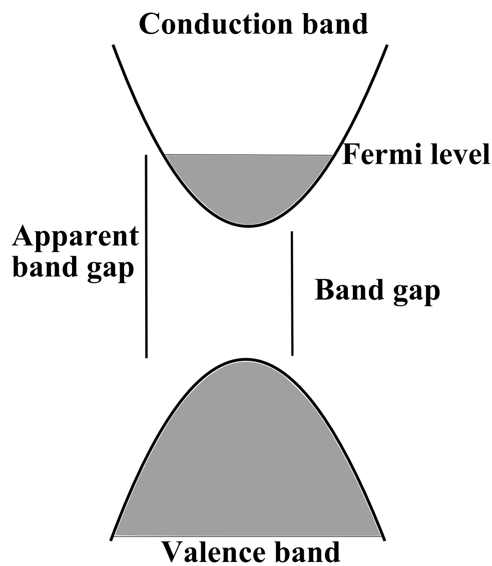


Figure 2.18: Illustration of the Burstein-Moss effect in a highly degenerate semiconductor.

2.6 Previous work

Some previous work on ITO/Si related junctions will be presented in this Section.

2.6.1 Junctions between ITO and Si

Figure 2.19 shows a schematic view of the ITO/Si junction with a native oxide layer and interface defect states as proposed by Refs.[32],[33],[34]. As mentioned previously, ITO is a highly degenerate semiconductor, i.e. ITO will behave almost like a metal compared to Si. The junction can then be thought of as a Schottky junction and the depletion region extends primarily into Si [35].

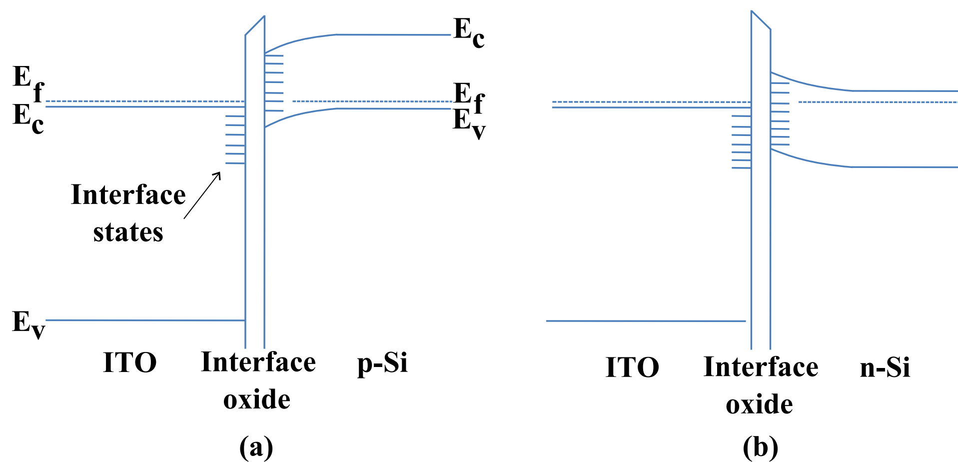


Figure 2.19: Band diagram for the junction between ITO and: a) p-Si b) n-Si

Kobayashi et al. [36] have reported that a cyanide pre-treatment of Si-substrates led to an increased efficiency of the ITO/Si junction. They related this to the passivation of dangling bonds by the cyanide ion.

2.6.2 DLTS studies of interface between ITO and Si

There have been published a few papers concerning DLTS (see Section 3.5) of ITO/Si junctions. Zettler et al. [37] investigated samples of sputtered ITO on (111) n- and p-Si in 1989. Samples were deposited in a mixture of Ar and O_2 and annealed in either N_2 or H_2 atmosphere. Table 2.1 lists the obtained trap parameters. Their conclusions were that: i) multiple hole and electron traps are present, related to respectively: radiation damage,

hydrogen or ITO elements. ii) for both ITO/n-Si and ITO/p-Si junctions, annealing temperatures of 400°C is insufficient to remove all trap states and iii) the levels found deep in the substrate can only be explained by a channeling effect during sputter deposition.

Defect label	Δ $E_{p,n}$ (eV)	$A_{p,n}$ (s^{-1})	Tentative defect identification
1H	0.16	7 X 10^9	In-level
H6	0.19	4 X 10^{10}	V-defect - diffusion
H2	0.28	9 X 10^{11}	H-corr
H3*)	0.36	1 X 10^{11}	C_sC_i
5H	0.56	1 X 10^{15}	?
H4	0.53	7 X 10^{13}	V_2 + diffusion
6H	0.58	8 X 10^{13}	?
1E	0.15	3 X 10^{11}	?
E4*)	0.15	3 X 10^{10}	O-V (A-center)
2E	0.17	4 X 10^9	Sn-level
3E	0.19	7 X 10^9	?
E6*)	0.22	4X10^9	V_2^-
E7	0.32	3 X 10^{11}	H-corr
E9*)	0.39	4 X 10^{10}	$V_2^=$
E10	0.46	7 X 10^{10}	H-corr
E11	0.45	7 X 10^9	H-corr

Table 2.1: *) Detected by optical excitation, too. Zettler et. al [37]

Kuwano and Ashok [38] conducted a similar experiment in 1997. They made samples of sputtered ITO on (100) Si and investigated hydrogen passivation of interface defects, and low temperature (<200°C) annealing. The obtained trap parameters are listed in Table 2.2. By prehydrogenating the

Si wafers the trap concentration was shown to be reduced by about 50%, and only one broad peak was obtained by DLTS for both p and n-type substrates. Annealing at 180°C for 12h showed some reduction for two of the electron traps.

Trap	Energy position (eV)	$\sigma_{p,n}(\text{cm}^2)$
Electron	$E_c - 0.10$	1.5 X 10^{-18}
Electron	$E_c - 0.19$	1.6 X 10^{-20}
Electron	$E_c - 0.25$	9.8 X 10^{-21}
Hole	$E_v + 0.20$	1.5 X 10^{-18}

Table 2.2: Trap states found at ITO/Si interface by Kuwano and Ashok [38]

Monakhov et al [39] reported the presence of a hole trap ($E_v + 0.3$eV) on the interface of sputtered ITO on (100) p-Si (see Fig.2.20) by DLTS (Section 3.5). Post heat treatment at 300°C for 30 min in air was found to be sufficient for annealing of the trap. Annealing was found to be correlated with improvement in both IV (Section 3.3) and CV (Section 3.4) characteristics.

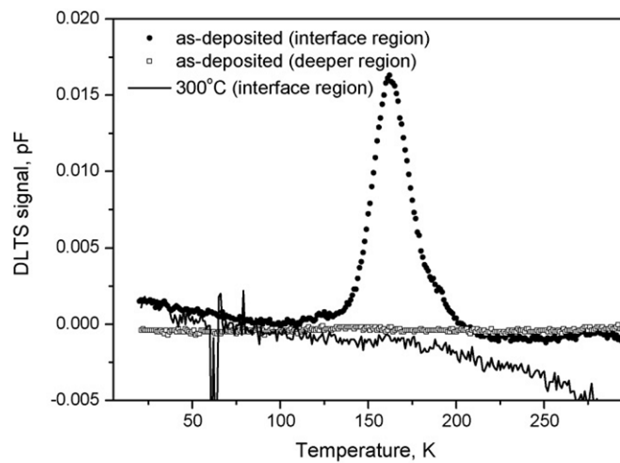


Figure 2.20: DLTS spectra with a rate window of (640ms)−1 for the ITO/p-Si junctions before and after annealing at 300°C [39]. The trap concentration is proportional to the DLTS signal

2.6.3 Structural studies of interface between ITO and Si

Christensen et al. [40] investigated the interface regions of: i) ITO/a-Si:H/Si and ii)ITO/Si by Secondary Ion Mass Spectrometry (SIMS) (see Section 3.7). They found that hydrogen was present in the ITO/Si interface (see Fig.2.21), and explained this by a gettering process during growth. A redistribution of hydrogen from the a-Si:H into ITO and Si was also seen. There was no deviation in SIMS profiles for different deposition temperatures, but peculiarities in some SIMS profiles related to inhomogeneous regions in ITO were reported. These regions could be related to nano-wells observed in ITO by Maknys et al. [41]. Ulyashin et al. [42] investigated the same ITO/a-Si:H/Si structures by SIMS and X-ray Photoelectron Spectroscopy (XPS). SIMS results (Fig.2.21) confirmed that In and Sn penetrate into the Si substrate during deposition. Si-O bonds at the ITO/a-Si:H interface were detected by XPS, confirming the presence of a thin SiO_x layer at the ITO/a-Si:H interface. This was reported to be related to a partial oxidation process of Si during the first stage of the deposition. Malar et al. [43],[44] also reported an interface oxide at the In_2O_3/Si interface (see Fig.2.21).

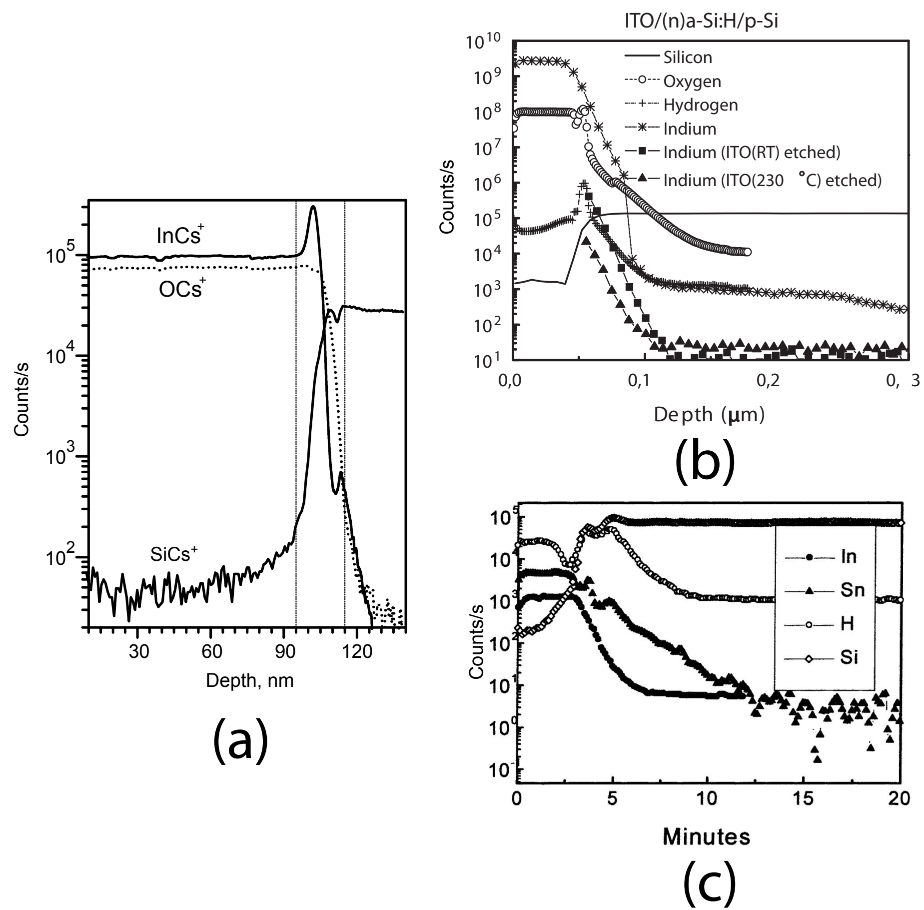


Figure 2.21: SIMS depth profiles a) In_2O_3/Si reported by Malar et al. [44] b) ITO(RT)/(n)a-Si:H/(p)Si reported by Christensen et al. [40] c) ITO/a-Si:H/Si reported by Ulyashin et al. [42]

Chapter 3

Experimental techniques

> *"The first principle is that you must not fool yourself - and you are the easiest person to fool."*
>
> *- Richard P. Feynman*

In this chapter the experimental techniques that have been used in this thesis will be presented, including the synthesis of ITO.

3.1 Magnetron Sputtering (MSP)

Sputtering was developed as a deposition technique in the 1920s, and was found to have a higher ability to produce alloys than evaporation methods [45]. The sputtering system used in this thesis is a *direct current* magnetron sputter (DC-MSP) CVC type AST-601 system. The basic components of a DC-MSP are shown in Fig.3.1. The sputtering chamber is evacuated by a cryo pump to a few μTorr after the samples are loaded. Then pure argon (Ar) gas is injected into the chamber. When a high voltage (>200V) is applied to the cathode, a spark between the cathode and anode will generate a plasma. The positively charged Ar ions generated will be accelerated toward the target which is placed on the cathode. Ar ions will transfer energy

to the atoms in the target, and some of them will be ejected from the target. These atoms will hit the substrate and lead to a growing film. The magnets in this setup are used to confine secondary electrons in the region close to the cathode. This increases the sputtering rate as more Ar ions are generated by colliding with the electrons. The ejected atoms typically have energy in the range $10 - 50$ eV [45].

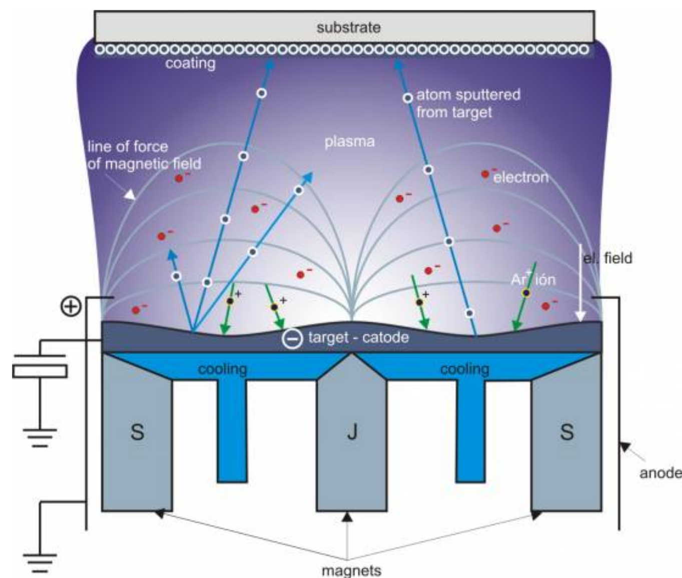


Figure 3.1: Illustration of particle flow in the magnetron sputtering chamber [46].

3.2 Sample preparation

3.2.1 Sputtering

All samples consists of ITO sputtered from a 99.98% In_2O_3:SnO_2 (90:10) 8 inch target, onto polished single crystalline (100) Si wafers (see table 3.1). The substrates were cleaned with ammonia (NH_3) and hydrochloric acid (HCl). The native oxide that always exist on a Si surface exposed to air [45], was etched by deluted hydrofluoric acid (HF 38%) before the samples

were loaded into the sputtering chamber. Figure 3.2 provides a step by step illustration of the sample preparation from substrate cleaning to finished diodes. Before sputtering began, a presputtering of the oxide target was conducted for 5 min to remove possible contaminations on the surface. The parameters found in table B.1 was used for the sputtering process. To increase the uniformity of the film, the sample holder was rotated during sputtering. One batch was made with 3 min sputtering time, and a second with 10 min. The first batch was only sputtered onto the p1-Si substrate.

Substrate name	Dopant	Resistivity (Ω cm)	Thickness (μm)
n-Si	Phosphorous (P)	$3-9$	$500-550$
p1-Si	Boron (B)	$25.5-42.5$	$505-545$
p2-Si	Boron (B)	$7-13$	$425-475$
SiO_2	-	-	-

Table 3.1: Substrate labeling and material specifications. The Si substrates were polished Cz-Si (100) and the SiO_2 substrate was fused silica.

3.2.2 Lithography

After the deposition, a lithography process described in Ref.[45] was carried out to separate small circular regions, to create multiple diodes on one substrate. In lithography, the wafer is often spin coated by an organic liquid and then heat treated on a hotplate (called softbaking). When the photoresist is exposed to light, it will become harder or easier to dissolve. These types are called negative and positive photoresist, respectively. The latter has been used in this thesis (see appendix B.1 for details on what chemicals were used). In order to take advantage of these effects, a piece of glass with a reflective pattern (mask) is placed on top of the wafer to leave some regions unexposed. A 350W short arc mercury lamp was used as the light source. After exposure, the wafer was immersed into a developer solution

to remove the exposed parts of the photoresist. Now there were open areas which could be etched by a suitable etchant, in this case hydrofluoric acid (HF). After the HF etch, the photoresist was removed by acetone. Diodes with a radius of 1mm and below were formed during this process. The 1mm diodes were used for most of the electrical measurements except for the four point probe and a few DLTS measurements.

3.2.3 Annealing experiments

The samples described above were annealed in the temperature range 200-600°C for 30 min in air. As all samples had to undergo the lithography process, there are no diodes which are "as-deposited" for the electrical measurements. The samples that did not undergo an additional heat treatment after the lithography, will therefore be referred to as 120°C when presented in results. For treatment at 200 and 250°C a hotplate was used, and the samples were placed onto an aluminum block, which had a liquid alcohol thermometer inside it and a lid on top. For 300-600 °C the samples were placed in an alumina boat and loaded into an alumina tube furnace.

3.3 Current - voltage (IV)

In Appendix A.2, the ideal Schottky diode equation was derived. It was then assumed that the barrier height is independent on bias. In the presence of an interface layer and/or with recombination in the depletion region, the barrier height will be bias dependent [47]. The diode equation can then be written as:

$$I = I_0 exp\left(\frac{qV}{\eta kT}\right)\left[1 - exp\left(\frac{-qV}{kT}\right)\right] \tag{3.1}$$

This is the general expression for a diode with ideality factor. Utilizing Eq.3.1, values of η can be found for reverse bias as well as forward bias. At

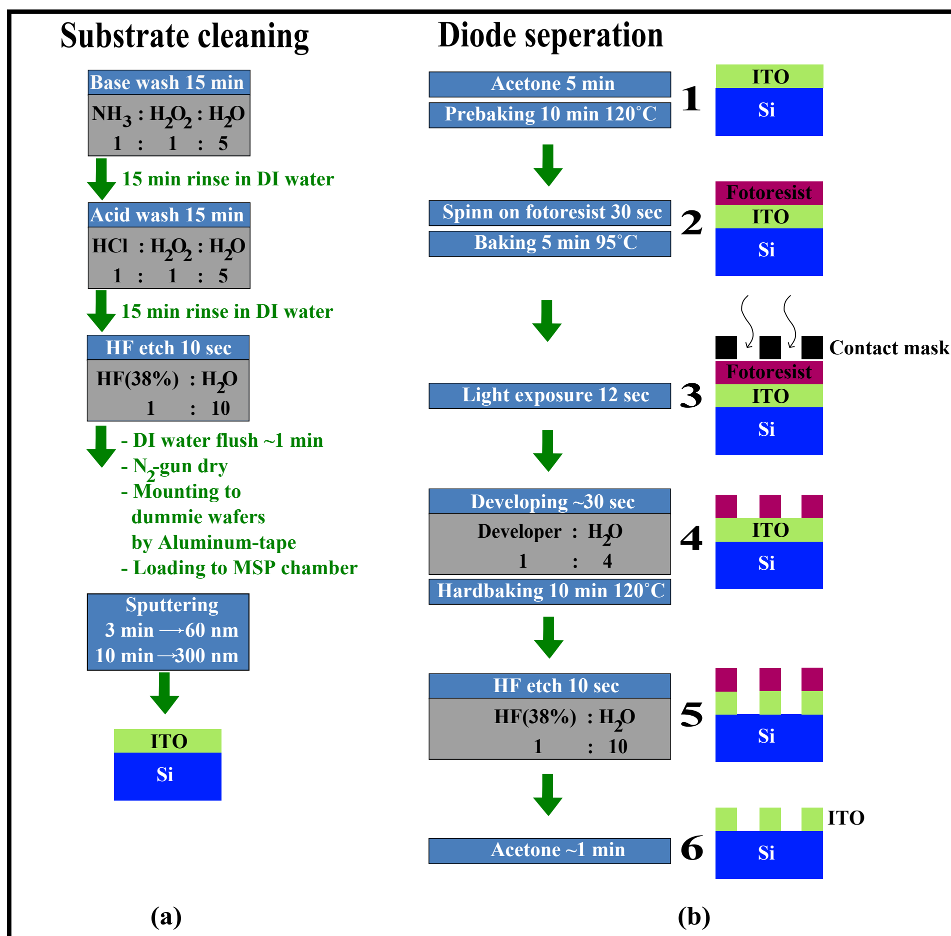


Figure 3.2: a) Details in substrate cleaning prior to sputtering. b) Procedure for etching of ITO-layer for diode separation.

V > $\frac{3kT}{q}$ the ideal form can be used. To find the ideality factor, Eq.3.1 can be differentiated with respect to voltage and rewitten as:

$$\begin{aligned}
exp\left(\frac{qV}{\eta kT}\right) &= \underbrace{\frac{I}{\left[1 - exp\left(\frac{-qV}{kT}\right)\right]}}_{\gamma}\frac{1}{I_0} \\
\frac{qV}{\eta kT} &= ln(\gamma) - ln(I_0) \\
\frac{\partial}{\partial V}\frac{qV}{\eta kT} &= \frac{\partial}{\partial V}ln(\gamma) \\
\frac{1}{\eta} &= \frac{\partial}{\partial V}\frac{kT}{q}ln(\gamma)
\end{aligned} \tag{3.2}$$

Thus, $\frac{1}{\eta}$ can be found from the slope of $\frac{kT}{q}ln(\gamma)$ vs. V.
The series resistance during forward bias can be included as a potential drop over the ideal diode (V > $\frac{3kT}{q}$) [2] yielding:

$$I = I_0 exp\left(\frac{q(V - R_s I)}{\eta kT}\right) \tag{3.3}$$

where R_s is the series resistance. It can be found by differentiating the current with respect to voltage:

$$\begin{aligned}
\frac{\partial I}{\partial V} &= I_0\frac{\partial}{\partial V}\left[exp\left(\frac{qV}{\eta kT}\right)exp\left(\frac{-qR_sI}{\eta kT}\right)\right] \\
\frac{\partial I}{\partial V} &= I_0\left[\frac{q}{\eta kT}exp\left(\frac{qV}{\eta kT}\right)exp\left(\frac{-qR_sI}{\eta kT}\right) + \left(\frac{-qR_s}{\eta kT}\right)exp\left(\frac{-qR_sI}{\eta kT}\right)exp\left(\frac{qV}{\eta kT}\right)\frac{\partial I}{\partial V}\right] \\
\frac{\partial I}{\partial V} &= \underbrace{I_0 exp\left(\frac{q(V - R_sI)}{\eta kT}\right)}_{I}\left[\frac{q}{\eta kT} - \frac{qR_s}{\eta kT}\frac{\partial I}{\partial V}\right] \\
\frac{1}{I}\frac{\partial I}{\partial V} &= \frac{q}{\eta kT} - \frac{qR_s}{\eta kT}\frac{\partial I}{\partial V}
\end{aligned} \tag{3.4}$$

Thus, by plotting $\frac{1}{I}\frac{\partial I}{\partial V}$ vs. $\frac{\partial I}{\partial V}$, one obtains a straight line $y = b - ax$ where $R_s = \frac{a}{b}$.
The barrier height ϕ_b introduced in Eq.A.15 can be found at reverse bias,

if the diode in this region has an ideality factor close to unity. Rewriting the ideal diode equation, one can observe that the barrier height can be calculated from I_0 in the extrapolated line:

$$ln(I) = ln(I_0) + \frac{q}{kT}V \tag{3.5}$$

When discussing IV curves, the expression "rectification" is often used. This relates to the difference between the forward and reverse current of the diode, as what makes a diode is the ability to carry more current in one direction than the other. Rectification will then be used as a measure of "how much more" current is driven in forward bias compared to the reverse. When an IV curve is plotted in a semilogarithmic plot, the rectification can be seen as the height difference of the saturated forward and reverse currents.

3.4 Capacitance - voltage (CV)

As described in Eq.2.27, the capacitance of an asymmetrical junction can be written as:

$$C = \left(\frac{qN_{d,(a)}\epsilon A^2}{2V_j}\right)^{1/2} = \left(\frac{qN_{d,(a)}\epsilon A^2}{2(V_0 - V_{ext})}\right)^{1/2} \tag{3.6}$$

with $N_{d,(a)}$ indicating the doping concentration of the lowest doped semiconductor. From a measurement of the capacitance vs. reverse bias voltage, the doping level in the lowest doped region and the contact potential V_0 of the junction can be deduced if Eq.3.6 is squared and rearranged:

$$\frac{1}{C^2} = -\frac{2}{qN_{d,(a)}A^2\epsilon}V_{ext} + \frac{2}{qN_{d,(a)}A^2\epsilon}V_0 = aV_{ext} + b \tag{3.7}$$

$N_{d,(a)}$ can be found from the slope of this linear plot, and V_0 from extrapolating the line to $1/C^2 = 0$ where $V_{ext} = V_0$.

3.5 Deep-Level Transient Spectroscopy (DLTS)

In this Section the theoretical principle of DLTS will be presented. This technique was introduced by Lang in 1974 [48]. It can give us information about electrically active defects (usually called traps in this setting) and their energy states within the band gap. From a basic DLTS-scan, information about the energy position, capture cross section and concentration can be deduced if a rectifying junction is used. This Section will be based upon similar discussions in Blood and Orton [5].

3.5.1 Basic principle of DLTS

The principle behind DLTS is to charge the traps in the near surface region (depletion region) of the material by changing the externally applied bias voltage V_{ext}. Usually, the diode is kept at a fixed reverse bias, and this bias is removed for a few ms. In the depletion region there are no free charge carries[1] and by pulsing the bias to zero, all the traps are filled with electrons or holes (given that the pulse is long enough to saturate the traps)[2]. When the pulse is over and we are back to reverse bias, the traps start to emit by thermal excitation their electrons or holes, and the change in capacitance of the depletion region as this occur is measured. Figure 3.3 shows the band diagram for the three situations; equilibrium, charging and emission. This is repeated several times for each temperature as the temperature is varied. It is also possible to vary the magnitude of the applied bias during the pulse, in order to probe different regions of the material. This can give a concentration of traps vs. depth profile. This will be discussed further in Section 3.5.4. To ease the analysis as to where the traps are located, an asymmetrically doped p-n or a Schottky junction is used. This is because the depletion region extends primarily into the lower doped side of the

[1] Because the electric field will sweep out all free charge carriers

[2] All DLTS spectra in this thesis have been obtained with a pulse width of 50 ms.

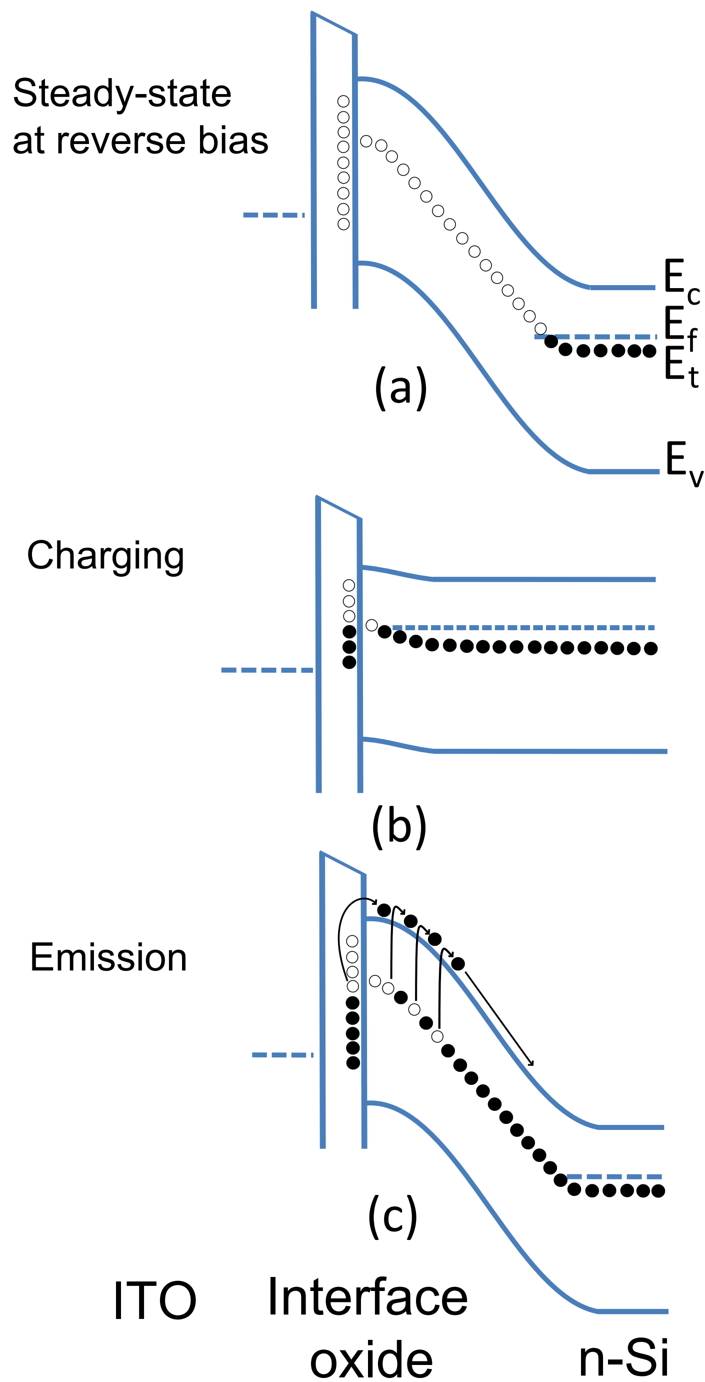


Figure 3.3: (a) Steady-state at reverse bias. (b) Charging of traps during pulsing bias. (c) Thermal emission from traps at reverse bias. E_t is the position of a trap in the band gap.

junction. A $p^+ - n^-$ junction will be used as an example. Thus, electron traps will be dominating the signal, and will be used in the derivation.

3.5.2 Foundation for the theory

The two equations that make up the basis for the DLTS theory are given in Section 2.4. An expression for the emission rate of charge carriers from a trap state was found by looking at the change in concentration of filled traps. The apparent capture cross section σ_{na} of the traps and the activation enthalpy ΔH could be found from an Arrhenius plot of Eq.2.41:

$$ln(e_n/T^2) = -\Delta H/kT + ln(\beta\sigma_{na}) \tag{3.8}$$

The change in occupancy of the traps was given by the rate equation (Eq.2.28). If it is assumed that all the traps are filled during the pulse and only interaction between the trap state and the conduction band is considered, the rate equation becomes:

$$\frac{dn_t}{dt} = -e_n n_t \tag{3.9}$$

Integrating with $n_t = N_t$ at $t = 0$ as boundary condition, gives the following exponential decay of occupied traps:

$$n_t(t) = N_t e^{-e_n t} \tag{3.10}$$

The signal that we measure comes from the emission of trapped carriers. The change in capacitance resulting from the change in bias is shown in Fig.3.4. The signal is called a transient, and shows how the emission of electrons occurs as a function of time. At $t = 0$, right after removing the pulse, all the traps are filled by electrons. This means that the effective doping in W has been reduced to:

$$N_d^{eff} = N_d - n_t(t) \tag{3.11}$$

Inserting Eq.3.11 into Eq.2.27 the capacitance after the pulse becomes:

$$C(t) = \left[\frac{q\epsilon A^2}{2}\frac{N_d - n_t(t)}{V_j}\right]^{1/2} = \underbrace{\left[\frac{q\epsilon A^2}{2}\frac{N_d}{V_j}\right]^{1/2}}_{C_{rb}}\left[1 - \frac{N_t e^{-e_n t}}{N_d}\right]^{1/2} \tag{3.12}$$

If $N_t \ll N_d$ we can use the following approximation on Eq.3.12:

$$f(x) = (1-x)^a \approx 1 - ax \tag{3.13}$$

This is valid as $x \to 0$. Eq.3.12 then becomes:

$$C(t) = C_{rb} - \Delta C(t) \tag{3.14}$$

where

$$\Delta C(t) = \frac{C_{rb} N_t}{2N_d} e^{-e_n t} \tag{3.15}$$

3.5.3 The DLTS spectrum

After measuring a collection of capacitance transients in a temperature scan, they can be made into a DLTS spectrum. Figure 3.5 shows how a series of transients taken at different temperatures give rise to a peak in the difference between two measuring points on the transient. This distance is called the "time window". By varying the lenght of the time window, the peak is shifted in temperature giving a set of DLTS spectra with different time windows.

In order to increase the signal to noise ratio, the "whole" transient is measured with a fixed time step τ. A weighting function is used to deduct the DLTS signal. In this thesis the lock-in weighting function has been used:

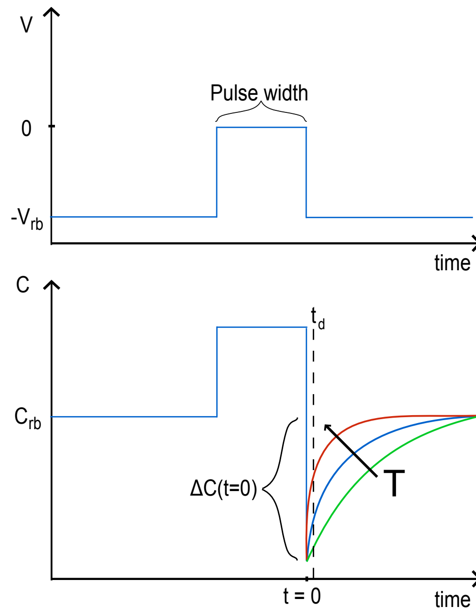


Figure 3.4: Top figure: The filling pulse. Bottom figure: The resulting capacitance changes as a result of the change in bias. The different transients show the effect of higher temperature. The dotted line represents the delay time t_d before the measurement starts

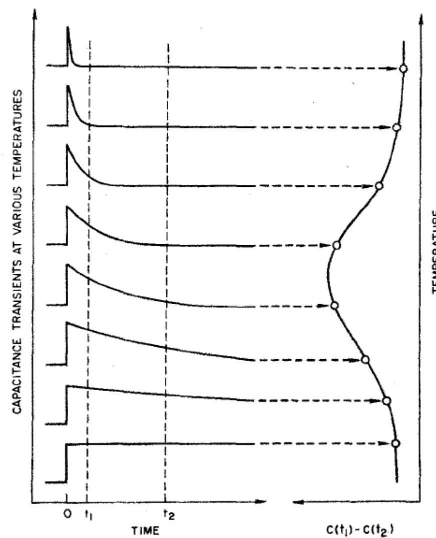


Figure 3.5: The left part shows transients at different temperatures. The right part shows why there is a peak in the DLTS signal when taking the difference in capacitance between two fixed measuring points. Lang [48]

Window no. i	No. points	Length (ms)
1	2	20
2	4	40
3	8	80
4	16	160
5	32	320
6	64	640
7	128	1280
8	256	2560

Table 3.2: The length and number of points in each time-window for the lock-in type weighting function with $\tau = 10ms$.

$$w(t) = \begin{cases} 1 & t_d + 2^{i-1}\tau < t \leq t_d + 2^i\tau \\ -1 & t_d < t \leq t_d + 2^{i-1}\tau \end{cases} \tag{3.16}$$

where t_d is the "delay time" before the measurement starts. In this thesis a delay time of 5 ms has been used. The weighting function makes the first half of all the $w(t)$-values in a time window negative, and the second half positive. This gives less noise as the length of the time-window is increased. The number of measurements in the time-window goes as $n_i = 2^i$ and the length is $t_i = n_i\tau$, where i is the time window. Table 3.2 shows the number of points, and length of eight time windows.

Applying the weighting function to the DLTS signal gives:

$$S_i(T) = \frac{1}{n_i}\sum_{t=t_d}^{t_d+t_i} \Delta C(T,t)w(t) \tag{3.17}$$

The values of $S_i(T)$ are a sum of positive and negative values. It is in a sense a difference in capacitance of the first and last measured values in the time-window. If there is a peak in the spectra, information about the traps that it results from can be deduced. A DLTS-spectrum can be made

from this by plotting the values of S vs. temperature for the different time-windows. Figure 3.6(a) shows such a spectrum for eight time-windows. The concentration of the traps can be found by rewriting Eq.3.17 to[3]:

$$S_i(T) = \underbrace{\frac{C_{rb} N_t}{2N_d}}_{\Delta C_0} \underbrace{\frac{1}{n_i} \sum_{t=t_d}^{t_d+t_i} e^{-e_n t} w(t)}_{F_i} \quad (3.18)$$

F_i is just a numerical factor which can be calculated. The general idea is that at the peak in the DLTS signal $dS/dT = 0$. This can be used to get values for the emission rate e_n at the peak. In appendix A.5 the values for the first time window have been calculated to show the principle. The values of both F_i and their corresponding $e_n t_i$ for the specific time-window at the peak are given in table 3.3. This means that the concentration is given by:

$$N_{t,i} = \frac{2N_d S_{i,peak}(T_{peak})}{C_{rb}(T_{peak}) F_i} \quad (3.19)$$

Window no. i	F_i	$e_n t_i$
1	0.12488	1.44896
2	0.15490	1.81717
3	0.17597	2.09799
4	0.18880	2.28229
5	0.19594	2.39056
6	0.19971	2.44976
7	0.20165	2.48079
8	0.20264	2.49669

Table 3.3: The values of F_i and $e_n t_i$ for each time-window with $t_d = 5$ms [49].

[3] Constant contributions to ΔC(T,t) like C_{rb} will be canceled out by the summation

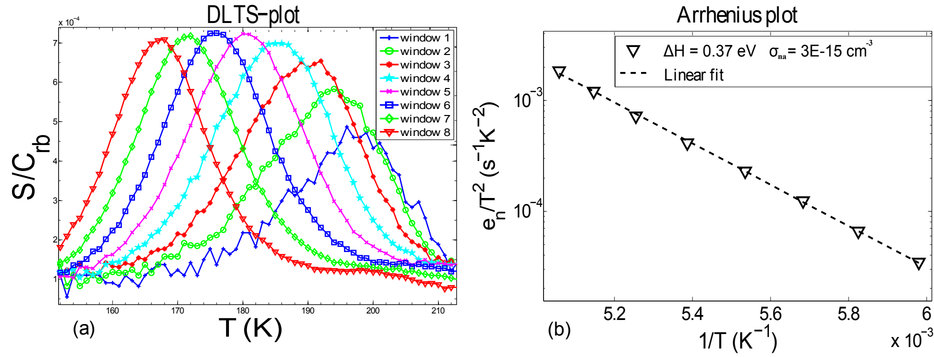


Figure 3.6: a) DLTS spectrum using the lock-in weighting function and eight time windows. The height of the spectrum is proportional to the concentration of traps. b) The corresponding Arrhenius plot from the peaks in the DLTS spectrum. The slope gives ΔH and the extrapolated value as $1/T \rightarrow 0$ gives σ_{na}. The DLTS spectrum and Arrhenius plot are obtained from one of the peaks observed in the 120°C annealed ITO(300nm)/p1-Si sample.

3.5.4 Profiling

In Section 3.5 it has been assumed that the pulsing bias has been kept constant throughout the whole experiment. By using a high reverse bias, and removing it completely during the pulse a large volume of the bulk of the sample is probed at the same time. If one instead of removing the bias completely, gradually reduce it for each measurement, the resulting transients will represent different regions in the bulk. In this way, one can start by probing deep in the bulk, and move towards the interface at the junction. In order for profiling to give sensible data, the temperature is kept fixed on a temperature where the DLTS signal peaks. Figure 3.7 shows a schematic view of which regions are probed at two different pulsing biases. If the defects are distributed homogeneously in the material, there will be no difference by varying the pulse. If a pulse higher than the reverse bias is applied, the diode will go into forward bias during the charging, and the build-in depletion region will be reduced. By varying the pulse from $V_p \ll V_{rb}$ to

$V_p > V_{rb}$ it is possible to determine if a trap is located inside the bulk, or near the interface of the junction.

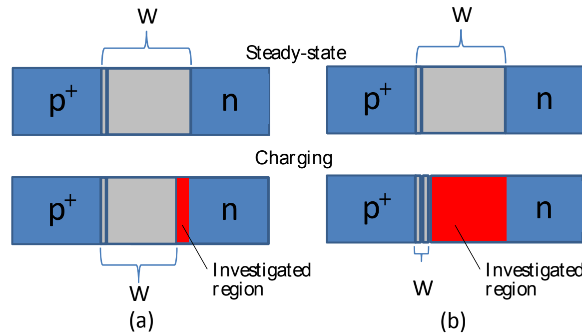


Figure 3.7: Red area indicates investigated area during a) $V_p < V_{rb}$ b) $V_p = V_{rb}$

3.6 The Asterix setup

The Asterix setup (see Fig.3.8) is made for undertaking electrical measurements in the temperature range $77 - 400$K and has been used for CV, IV and DLTS. The sample is placed on an alumina plate which is coated by a nickel film[4] and a needle connects the front of the sample. The holder has a protective metal cap, so that it can be lowered into a cylinder of liquid nitrogen (77K) for cooling. Heating can be done by a heating element under the alumina plate where a temperature sensor is also located. Silver paste was applied as back side contact to the samples. A small droplet of silver past was also placed on top of the ITO layer to improve the contact to the needle. Measurements were made both with and without silver paste, in order to ensure it did not affect the results. IV and CV measurements were used as a standard testing routine before all DLTS measurements. This was done to ensure that there was proper contact to both the needle and the back con-

[4]Since this film has become a rather bad conductor over the years, silver paste is used to connect the top of the plate to the contacts.

tact. Silver paste as a back contact to Si has been thoroughly described by Bleka [50]. A HP4280A capacitance meter was used for measuring CV and capacitance transients during DLTS, while a HP 8112A served as a pulse generator. For IV measurements a Keithley 617 Programmable Electrometer was used. The illuminated IV curves were obtained with a Keithley 6487 Picoammeter/Voltage Source.

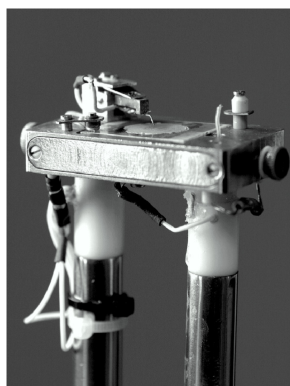


Figure 3.8: The sample holder in the Asterix setup (photo: Klaus Magnus Håland Johansen)

3.7 Secondary Ion Mass Spectrometry (SIMS)

SIMS is a technique where the surface of a sample is bombarded by an ion beam. The incident ions will penetrate into the sample and transfer energy and momentum to the atoms in the sample. Some of these atoms will gain enough energy to be ejected from the sample. The ejected atoms can be either neutral or ionized. The ionized species are extracted using an electric field, and a mass spectrometer. The ejected ions are deflected by both an electric and a magnetic analyzer to improve the mass resolution [51]. In the presence of both an electric and magnetic field, the force on the ions can be described by the *Lorenz force* [52]:

$$F = q[E + (v \times B)] \tag{3.20}$$

Where E is the electric field, B is the magnetic field and v is the velocity of the ion. If both fields are normal to the ion beam, the ions will experience a centripetal force:

$$F = \frac{mv^2}{r} \tag{3.21}$$

The two above equations can be combined to show that different $\frac{m}{q}$ mass-over-charge species (MOC) can be detected by varying the fields:

$$\frac{m}{q} = \frac{(Br_m)^2}{Er_e} \tag{3.22}$$

where r_m,r_e are the deflection radius of the two fields. The detector can be used to get three different types of outputs from the measurement: i) The fields can be systematically varied, to get a complete MOC spectrum and information about the amount of different species in the sample. ii) Keeping the fields fixed at on certain MOC, a depth profile can be deduced. iii) The incident beam can be swept across an area to get an image of where a certain specie is located on the surface. Figure 3.9 shows how the results from these measurement modes can be presented. In the present work a Cameca IMS 7F magnetic sector SIMS has been used.

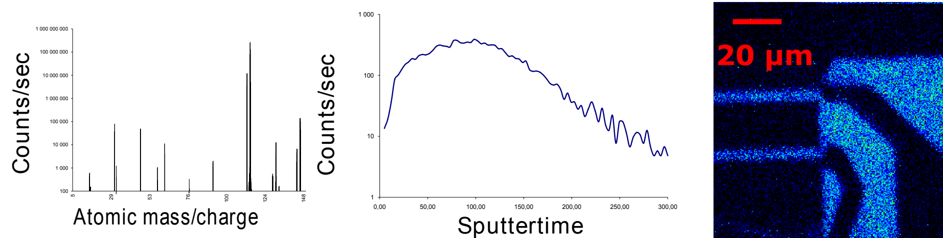


Figure 3.9: Mass spectrum, depth profile and ion image

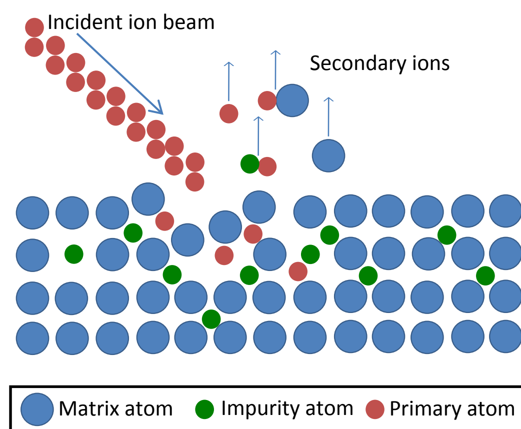


Figure 3.10: Schematic view of how the incident ion beam transfers energy to to atoms in the sample. Some of them will gain enough energy to escape the sample (so-called sputtering).

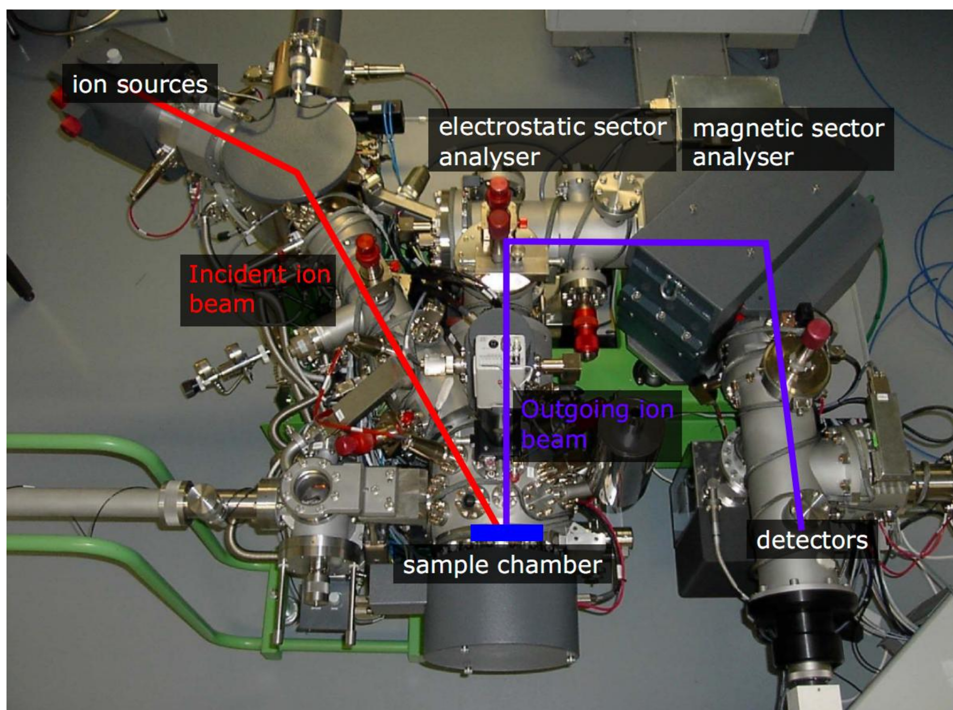


Figure 3.11: The SIMS setup in MiNa-Lab at the University of Oslo

3.8 Four point probe

Four point probe is commonly used to measure the resistivity of semiconductors. In this technique four needles are connected to the sample and a voltage is applied across the two inner needles. The resulting current is measured by the two outer needles (see Fig.3.12). If the film being measured is very thin compared to the needle spacing the resistivity ρ_r of the film is given by [53]:

$$\rho_r = \frac{\pi}{ln(2)} \frac{V}{I} z \tag{3.23}$$

where z is the thickness of the film. Two standard multimeters were connected to the four needles, in order to apply the voltage and measure the current.

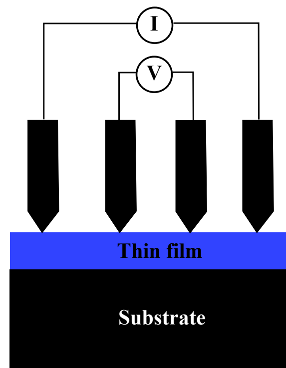


Figure 3.12: Schematic view of the setup in a collinear four point probe measurement

3.9 Atomic Force Microscopy (AFM)

In AFM a sharp tip on the edge of a cantilever is used to scan the surface of a sample. A laser beam is used to measure the deflection of the cantilever. There are two different modes of operation: i) constant force mode and ii) tapping mode [51]. As the names indicate, in contact mode the tip is in constant contact with the sample. During tapping mode, the cantilever is vibrated with a tunable frequency. In this thesis, tapping mode was the only mode used. It reduces the risk of dragging dust particles around during the measurement and also damaging of the sample surface. The software package "Nanoscope V6.12r1" has been used for analysing the AFM data received from a Veeco Dimension 3100 setup.

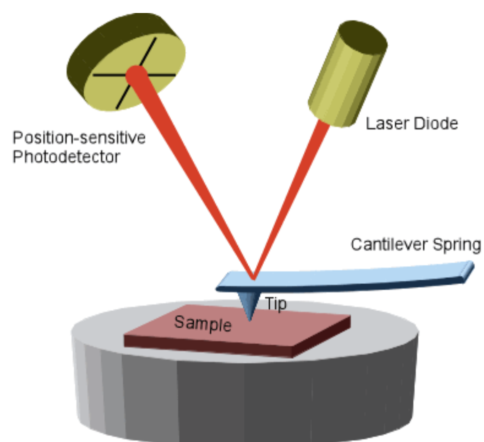


Figure 3.13: Schematic view of the probing in AFM [54]

Chapter 4

Results and discussion

"Science is facts; just as houses are made of stones, so is science made of facts; but a pile of stones is not a house and a collection of facts is not necessarily science."

- Henri Poincare

4.1 Electrical measurements

The first part of this Chapter will present the electrical measurements, which include four point probe, CV, IV and DLTS. All but the DLTS measurements were performed at room temperature. The thickness of the ITO films were measured by both an ellipsometer[1] and a *Veeco Dektak 8 stylus proiler*[2]. The thickness was found to be in the 60-70 nm range for the first batch, and 280-320 nm for the second[3]. Individual thicknesses were used in the resistivity calculations.

When discussing sample preparation, it was pointed out that all samples had to undergo a heat treatment during lithography at 120°C. Looking at

[1] In ellipsometry, the change in polarization of light reflected off the sample is analysed

[2] Here a needle is swiped across the sample, and the topography is measured by the deflection of the needle

[3] The first batch will hereafter be referred to as ITO(60nm) and the second as ITO(300nm)

the results of IV and CV from similar samples investigated by Balasundaraprabhu et al. [25], the difference between as deposited and 100°C is minor compared to higher annealing temperatures. This indicates that the 120°C might be comparable to an as deposited sample. However, the 120°C labeling will be used to avoid misunderstanding.

4.1.1 Four point probe

Figure 4.1 shows that there is a *low resistivity region* for the annealing temperatures 250-450°C, with a lowest value of $2.5 \cdot 10^{-4}\Omega$cm for the ITO(60nm) sample annealed at 300°C. This is the same value as was reported by Balasundaraprabhu et al. [25] on similar samples annealed at 300°C. These films were shown to have a carrier concentration of about $8{\cdot}10^{20}$cm^{-3}. As the films investigated in this thesis were deposited under very similar conditions as those in Ref.[25], one might assume similar bulk properties for the samples of same resistivity and annealing procedure. Table 4.1 lists some values for resistivity reported by other groups. Here it is shown that over a variety of techniques, with or without substrate heating, at 250-400°C ITO films possess resistivity in the $10^{-4}\Omega$cm range. This gives us an idea that there are some fundamental processes related to carrier generation, occurring in this temperature region. As will be discussed below, little emphasis has been put into the bulk properties of the ITO film in this thesis, as it is more a study of the interface properties than an optimalization study of the ITO film. To confirm that the measured resistivities were not influenced by the substrate, ITO films deposited on SiO_2 were also investigated. They showed similar values as for the Si substrates, confirming that the method described in Section 3.8 was valid.

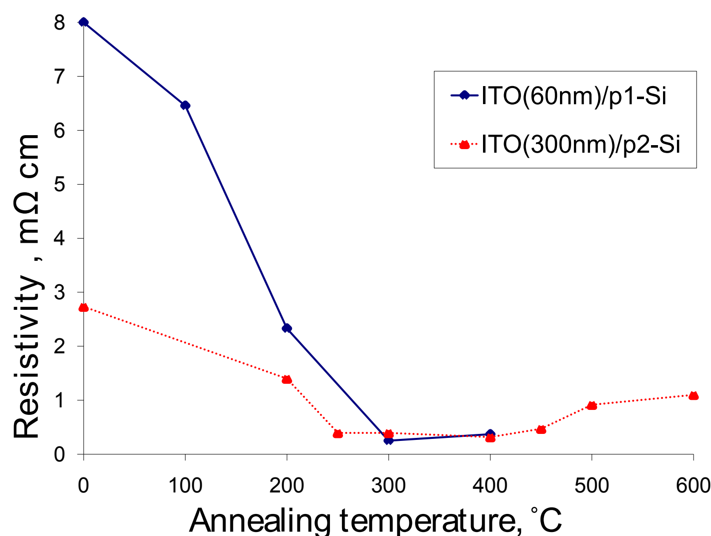


Figure 4.1: Resistivity of ITO film after different annealing temperatures

Deposition technique	Resistivity (Ωcm)	Annealing temperature	Substrate temperature	Reported by
E-Beam	$3 \cdot 10^{-4}$	-	350°C	[22]
PLD	$2 \cdot 10^{-4}$	-	300°C	[23]
CVD	$(1.6 - 1.8) \cdot 10^{-4}$	400°C, (30-45) min	RT	[24]
dc-MSP	$2.5 \cdot 10^{-4}$	300°C, 30min	RT	[25]
rf-MSP	$8.6 \cdot 10^{-5}$	-	250°C	[26]

Table 4.1: Reported values of ITO resistivity by other groups

4.1.2 CV results

From CV measurements (see Fig.4.2), the doping level of the substrate and the contact potential were deduced. The deviations from linearity for low reverse bias in the $1/C^2$ curves, was always seen for the 120°C and sometimes for the 200°C anneal. Balasundaraprabhu et al. [25] reported the same result for as deposited and 100°C annealed ITO/p-Si junctions. As

the gradient of the $1/C^2$ line is proportional to the doping level in the substrate, it is interesting to see that the deviation is in opposite direction for the n- and p-Si samples. This could support the hypotheses of counter-doping/additional doping by In and Sn penetration during sputtering as proposed by Ulyashin et al. [42] [4]. It could also be related to a considerable amount of interface defects as proposed by Ref.[25]. The contact potential for the ITO(300nm)/n-Si samples varied in the range $0.1 - 0.65$V with annealing as seen in Fig.4.2. The ITO/p-Si samples show a higher contact potential compared to Ref.[25] by about 0.1V. Table 4.2 summarizes the values obtained from the CV measurements.

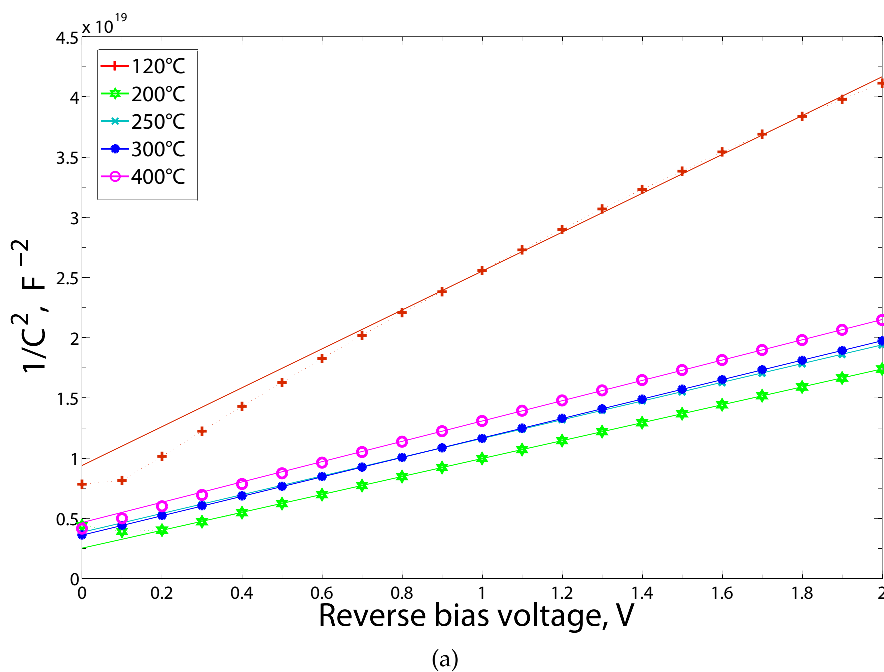
Sample name	$N_{d,(a)}(cm^{-3})$	V_0 (V) for 300°C anneal
ITO(300nm)/n-Si	$9.3 \cdot 10^{14}$	0.25
ITO(300nm)/p1-Si	$3.5 \cdot 10^{14}$	0.42
ITO(60nm)/p1-Si	$3.5 \cdot 10^{14}$	0.42
ITO(300nm)/p2-Si	$1.5 \cdot 10^{15}$	0.44

Table 4.2: Doping levels in the substrates and contact potential to ITO obtained by CV

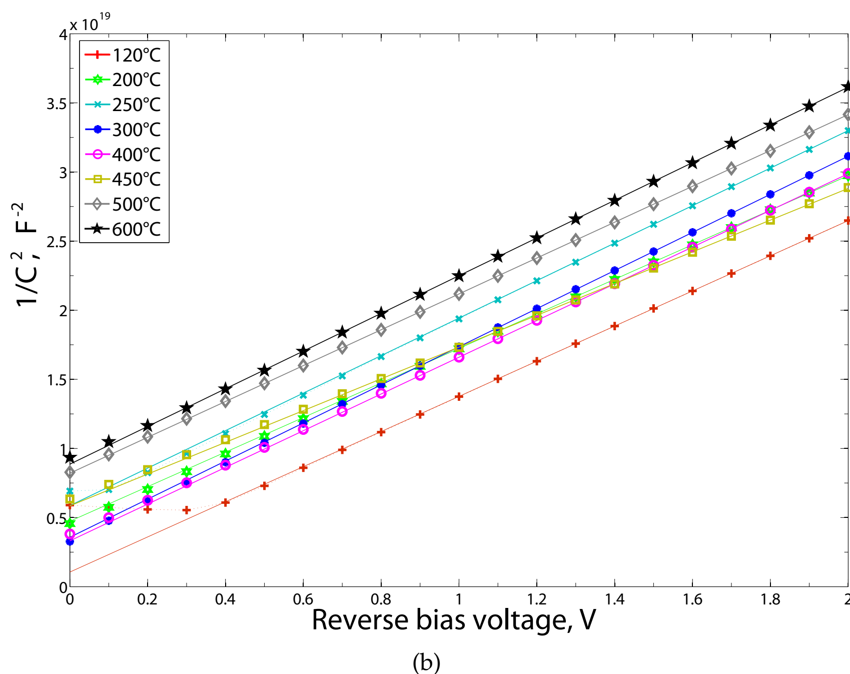
4.1.3 IV results

Figure 4.3 displays the IV characteristics for the four different samples. The n-Si samples exhibit rectification for all annealing temperatures, while rectification becomes substantially improved above 450°C (Fig.4.3(a)). Compared to p-Si samples (Fig.4.3(b)-4.3(d)), the n-Si samples generally show higher rectification. The p-Si samples have their highest rectification for 250 and 300°C, while annealing above 450°C results in an ohmic contact. This transition to ohmic contact at about 400°C correlates with results from

[4] The penetration of In and Sn will be discussed more when presenting the SIMS results.



(a)



(b)

Figure 4.2: $1/C^2$ vs. V plot for a) ITO(300nm)/p2-Si b) ITO(300nm)/n-Si.

Balasundaraprabhu et al. [25] and Chebotareva et al. [55]. The apparent "switch" in polarity seen for the ITO(60nm)/p1-Si annealed at 450°C (Fig.4.3(d)) was not reproducible in the second sputtering batch.
During reverse bias, all of the investigated diodes have an ideality factor close to unity, but going only a few hundred mV into forward bias the deviation becomes substantial (see Fig.4.5 for a typical example). Figure 4.4 shows how the ideality factor taken at 0.2 V in forward bias varies with annealing temperature, where it is seen that ITO(300nm)/n-Si annealed at 450°C has the lowest ideality factor of all samples. As seen from the IV curves, the forward current saturates quickly for all samples. Calculating the series resistance in this region, reveals values in the 0.2-0.8 kΩ range, which is significantly higher that the substrate resistance. Such high values can severely reduce the power delivered by a solar cell, as will be discussed in the next section.

From the IV curves in Fig.4.3, it is seen that the change in rectification mostly originates from a change in reverse current and thereby I_0. Calculations of the barrier height from I_0, therefore gives the same dependency on annealing temperature (see Fig.4.6). It is interesting to note that the sudden change in rectification and barrier height occur at 450°C for both n- and p-Si samples. This indicates that there could be a change in the interface at this temperature, working in opposite direction for the n and p-Si samples. This will be further illuminated when the DLTS and SIMS measurements are presented.

4.1.4 IV curves obtained under illumination

To check the photovoltaic behavior of the investigated samples, IV-curves were obtained under illumination by an AM 1.5 solar spectrum at room temperature. As seen from Fig.4.7, almost all of the photogenerated cur-

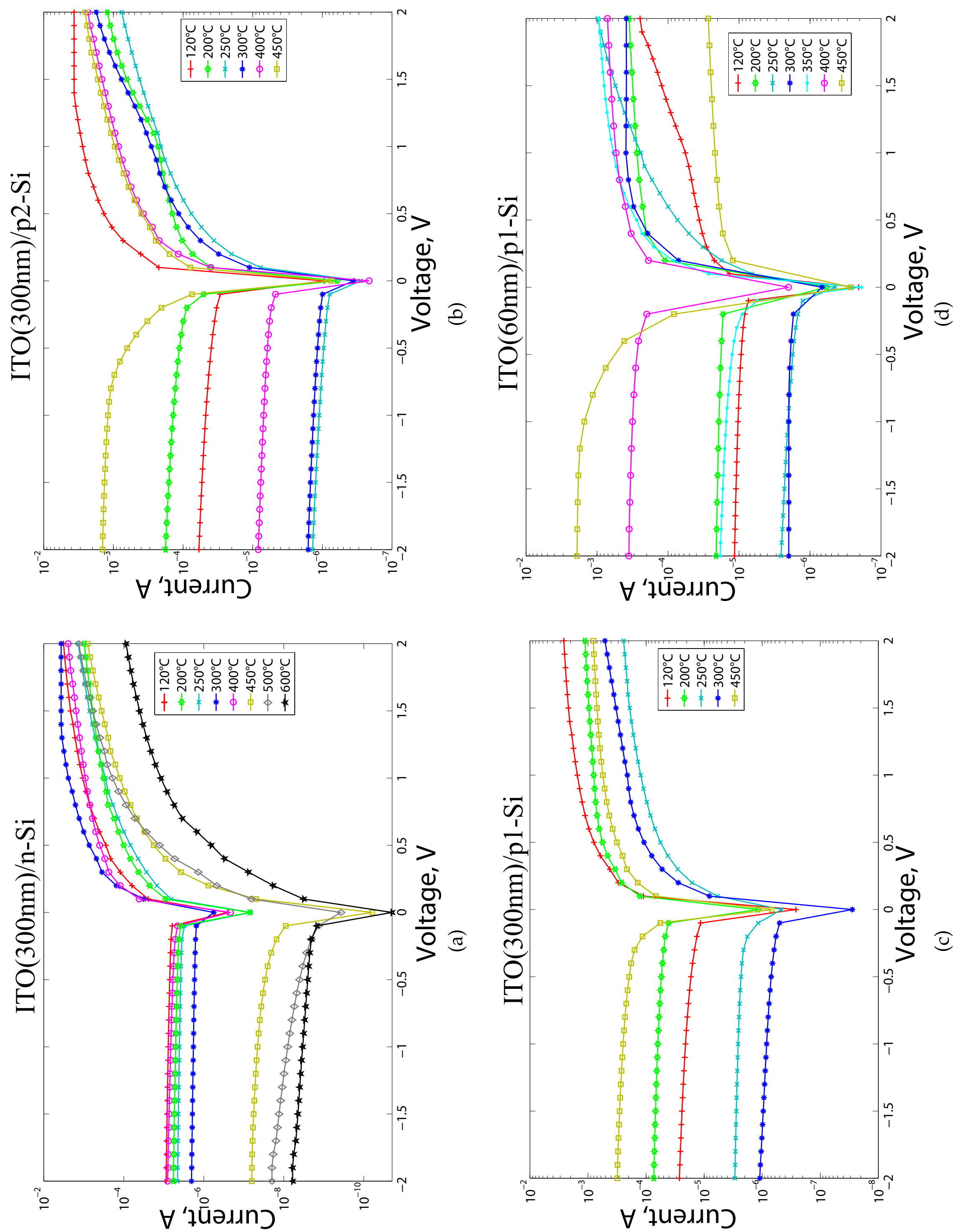


Figure 4.3: IV curves for the four different samples. Voltage axes is defined so that positive values are forward bias.

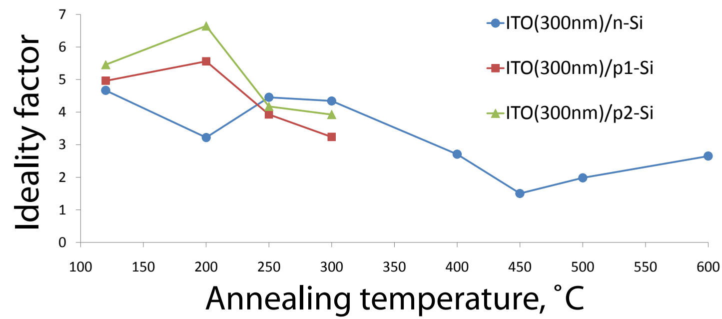


Figure 4.4: Ideality factor for IV curves in Fig.4.3 calculated at 0.2V in forward bias.

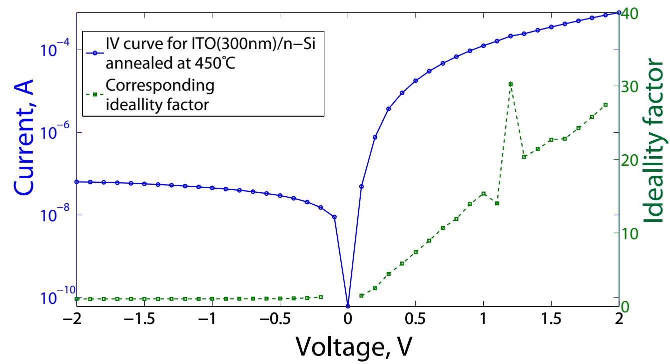


Figure 4.5: IV curve of the ITO(300nm)/n-Si annealed at 450°C with corresponding ideality factor vs. voltage. Similar ideality behavior was seen for all samples.

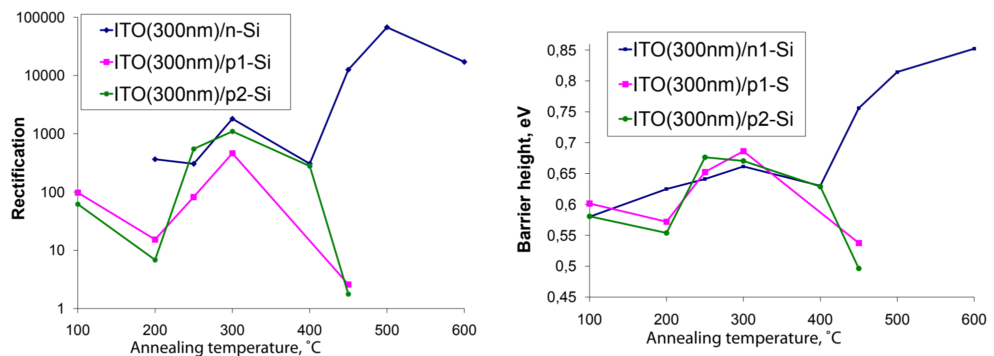


Figure 4.6: Rectification and barrier height calculated from IV measurements

rent is lost when the diode is moving into forward bias, and open circuit voltages V_{OC} of only about 0.1 V were obtained (as seen from the inset graphs in Fig.4.7). The low efficiency, and I_{SC} seen for the illuminated IV-curves could be related to an interfacial oxide suppressing hole tunneling from Si to ITO. This could lead to more recombination between photogenerated carriers and trapped charge at the interface as proposed by Mizrah et al. [35]. The hypothesis of tunneling suppression is supported by the high ideality factors and series resistance found for all the diodes in this thesis. No significant difference related to the low efficiency was seen when measurements were taken at about 85°C. It must be noted, that the use of silver paste as metal back contact as well as the experimental setup, may contribute to the observed high series resistance. However, similar results were obtained using a comparable setup.

To demonstrate the effect of series resistance in a solar cell, the software package PC1D [56] was used[5] to simulate IV curves for an ideal Si solar cell under illumination. Different series resistances were applied to the circuit, which resulted in considerable changes to the shape of the IV curves (see Fig.4.8). The experimental IV curves have similar drops in photocurrent as the simulated ones with 100Ω series resistance. This demonstrates that the high series resistance seen in the investigated samples can cause the observed drop in photocurrent.

[5]See appendix B.3 for a screenshot of the program window of PC1D with most of the relevant parameters used in the simulation.

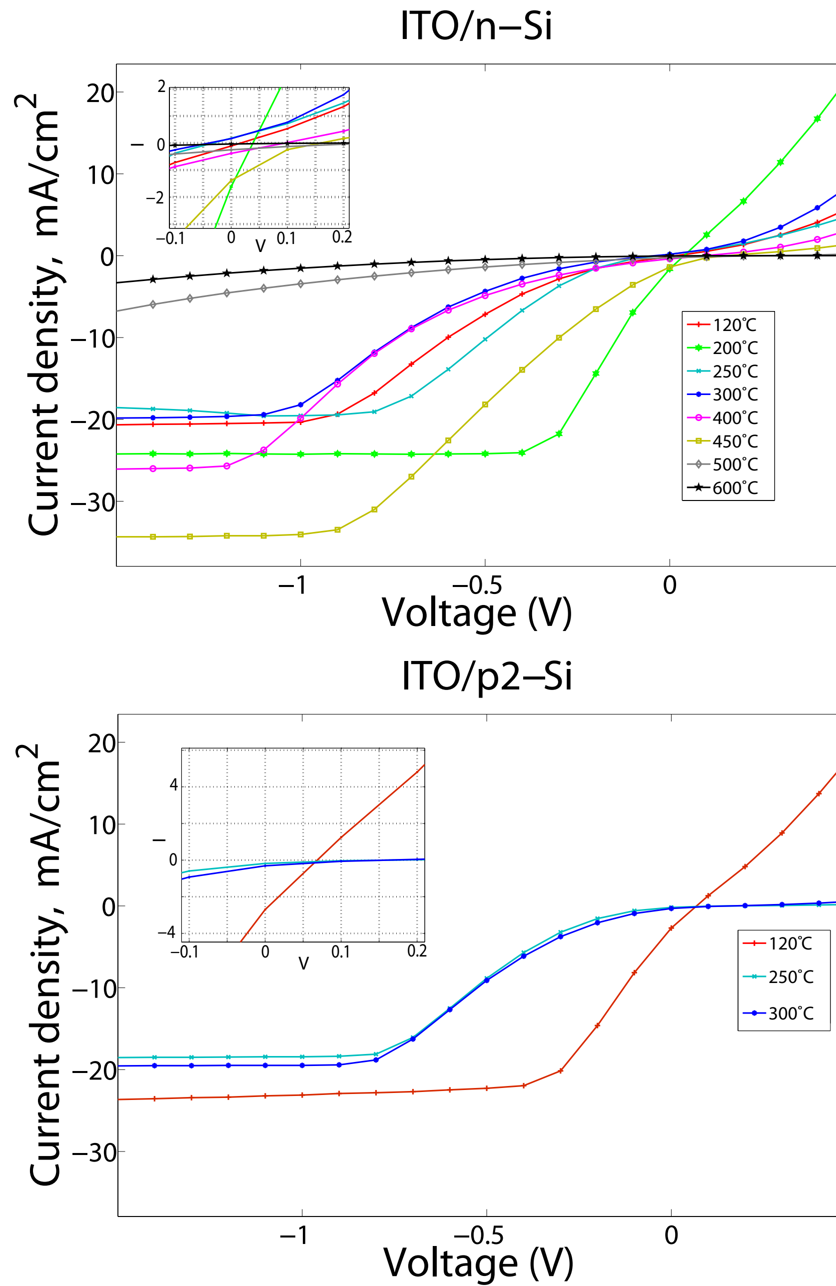


Figure 4.7: IV measurements during illumination under an AM 1.5 solar spectrum. Inset graphs show were the curves cross the y and x-axis.

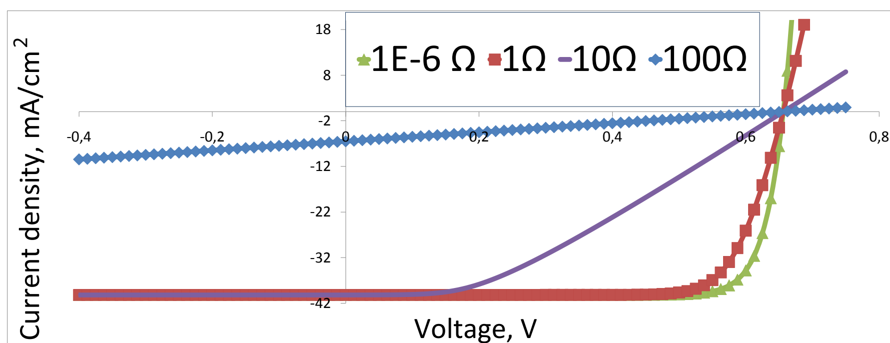


Figure 4.8: Simulated IV curves of a 1 cm^2 ideal diffused emitter silicon solar cell. Illumination under a AM 1.5 solar spectrum with four different series resistances.

4.1.5 DLTS results

To investigate the presence of defects at the interface of the ITO/Si junction, DLTS measurements were conducted. As the defects were considered to be located near the junction interface, spectra with and without a forward injection pulse were compared in my early measurements. It was seen that the DLTS signal was substantially larger when applying a forward injection pulse (see Fig.B.2). This was also supported by profiling, and will be discussed further in relation to Fig.4.15 and 4.16.
Figures 4.9 and 4.10 show DLTS spectra of the ITO(300nm)/n-Si samples with low and high injection pulse, respectively. The measurements revealed multiple shallow electron traps in the same energy range. They are located at $(E_c - 0.05) - (E_c - 0.15)$eV (labeled as E(0.1)), while the peak after the 250°C anneal, is in the range $(E_c - 0.14) - (E_c - 0.25)$eV (labeled as E(0.2)). It lies higher in temperature than all the other major peaks as seen from Fig.4.9-4.10. In addition to the shallow peaks, two deep electron traps were observed for the n-Si samples. After the 120°C anneal a level at $\sim (E_c - 0.5)$eV occurs (seen at about 240 K in Fig.4.9) and after the 600°C

anneal a level at $\sim (E_c - 0.4)$eV is found (labeled as E(0.4) in Fig.4.10). Table 4.3 summarize the trap properties for both n- and p-Si samples. Some of the peaks for the shallow electron traps are quite broad[6], and their corresponding Arrhenius plot is generally not linear for eight time windows, but have some curvature (see Fig.4.14 for typical examples). This indicates that some of the observed peaks are the sum of more than one level. After the 450°C annealing and low injection pulse (Fig.4.9), there are no longer any DLTS signal, except for a hole trap which is present in all n-type samples in the bulk[7]. Using a higher injection pulse (Fig.4.10), the major electron trap was still seen in the 450°C annealed sample but was substantially reduced at 500°C. Based upon this, it is evident that the traps are more confined to the interface at 450°C and anneals out at 500°C.
Figures 4.11-4.13 show the DLTS spectra for the p-Si samples. One major hole trap is observed at $(E_v + 0.37)$eV (labeled as H(0.37)), and a smaller one at $(E_c + 0.32)$eV (labeled as H(0.32)). For p-Si samples the trend is quite similar for the two film thicknesses and substrates used. H(0.37) decreases substantially at 200°C and even further at 250°C. The trap concentration is not below the detection limit before 400°C, but has decreased substantially already at 200°C relative to that at 120°C. The H(0.32) level is low in amplitude compared to H(0.37), and anneals out at 250°C. The tentative identification of the traps, and comparison with other reports, will be discussed after the SIMS results have been presented, since these results are relevant for the argumentation.

[6]Simulated DLTS spectra shown in Fig.B.3 have confirmed this. The simulated spectra were made by a Matlab script written by Lars Løvlie.

[7]This has been confirmed by doing DLTS of the n-type substrate with evaporated palladium (Pd) diodes.

Sample	Trap name	Energy level (eV)	$\sigma_{n(p)a}$ (cm^2)	Anneals out at
ITO/p-Si	H(0.37)	$(E_v + 0.37)$	10^{-15}	250°C
ITO/p-Si	H(0.32)	$(E_v + 0.32)$	10^{-13}	250°C
ITO/n-Si	E(0.1)	$(E_c - 0.05) - (E_c - 0.15)$	10^{-20}	500°C
ITO/n-Si	E(0.2)	$(E_c - 0.14) - (E_c - 0.25)$	10^{-20}	500°C
ITO/n-Si	E(0.4)	$(E_c - 0.4)$	10^{-18}	-

Table 4.3: Trap properties

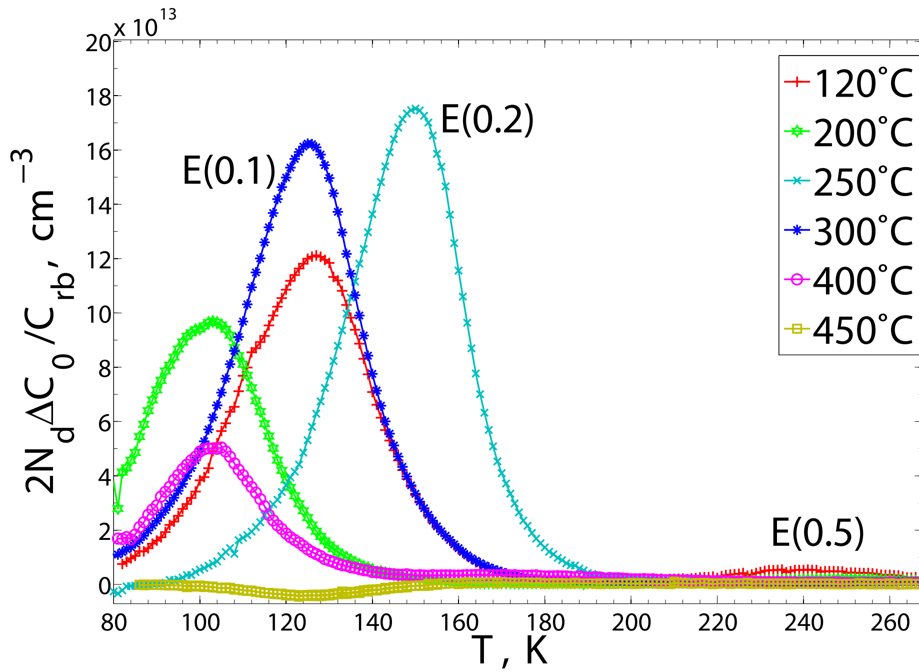


Figure 4.9: DLTS spectra of ITO(300nm)/n-Si. Time window 6 (640ms) and $V_r = -1V$ and $V_p = 1.5V$ (low injection pulse).

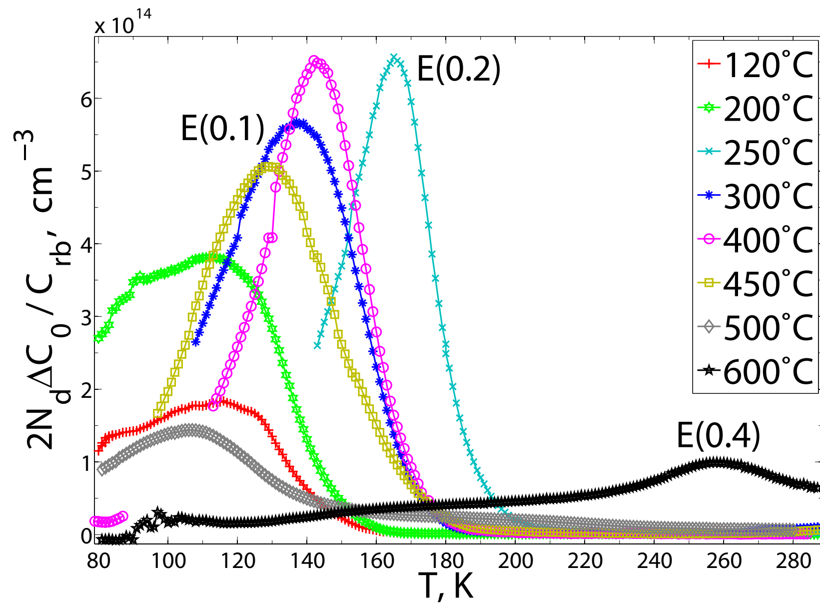


Figure 4.10: DLTS spectra of ITO(300nm)/n-Si. Time window 4 (160ms) and $V_r = -1V$ and $V_p = 3V$ (high injection pulse).

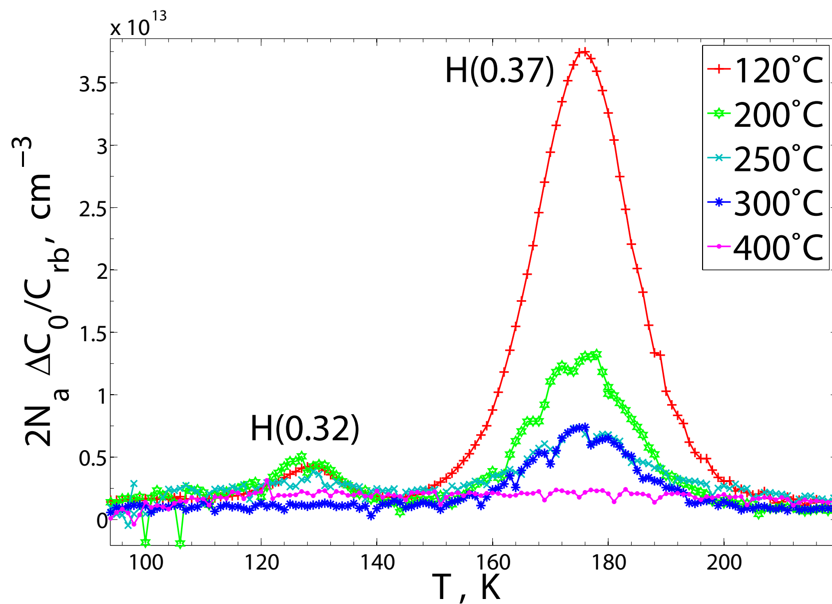


Figure 4.11: DLTS spectra of ITO(300nm)/p2-Si. Time window 6 (640ms) and $V_r = -1V$ and $V_p = 1.5V$.

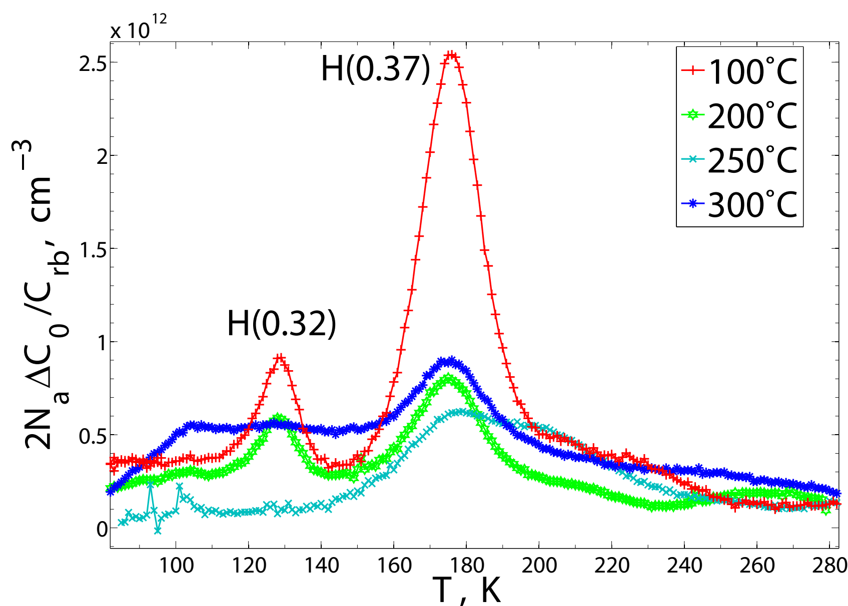


Figure 4.12: DLTS spectra of ITO(300nm)/p1-Si. Time window 6 (640ms) and $V_r = -1V$, $V_p = 1.5V$.

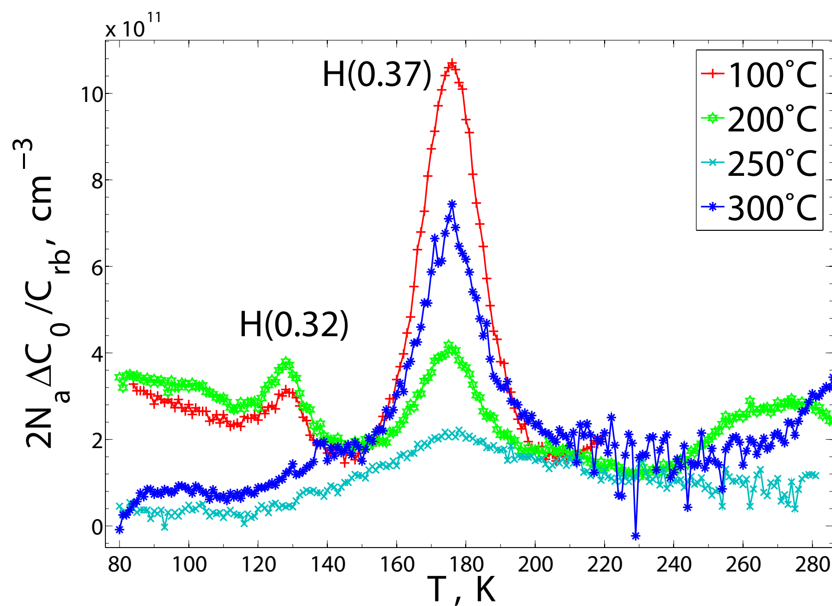


Figure 4.13: DLTS spectra of ITO(60nm)/p1-Si. Time window 6 (640ms) and $V_r = -1V$, $V_p = 1.5V$.

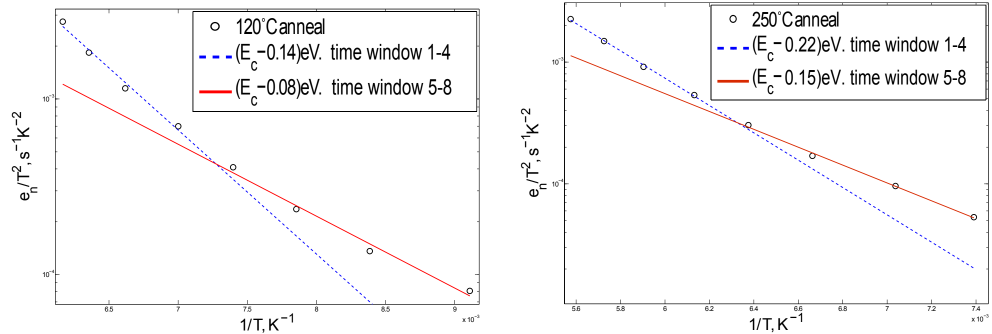
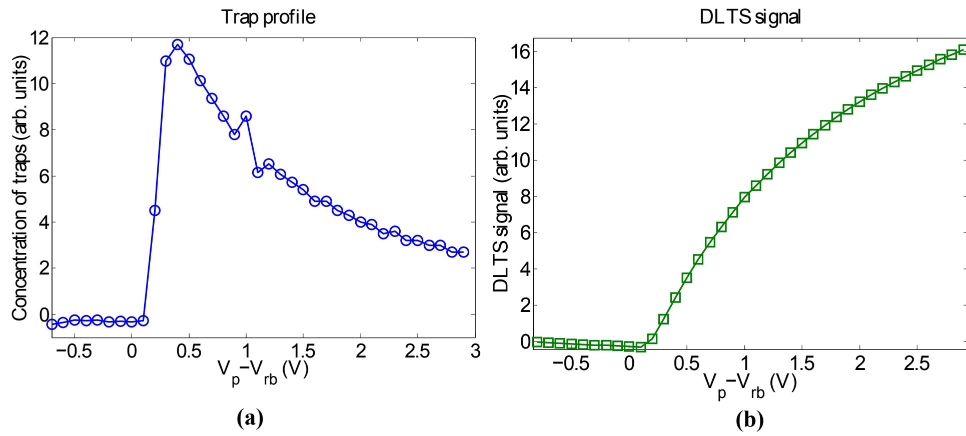


Figure 4.14: Arrhenius plot for E(0.1) and E(0.2) in two ITO(300nm)/n-Si samples annealed at 120°C and 250°C, respectively, showing the clearest deviations from linearity.

Figure 4.15-4.16 show a profiling of the E(0.2) and H(0.37) peaks respectively. One can see that the DLTS signal increases as the investigated region moves closer to the interface. This gives a clear indication that the traps are located near the interface, since operating the diode at forward bias during the pulse leads to collapse of the depletion region and injection of majority carriers across the junction. Looking at the profile for the E(0.2) peak (Fig.4.15), it is seen that even at high injection pulses the DLTS signal does not saturate. Some possible reasons for this can be: i) *Incomplete filling of the traps because of high local concentration of traps.* If the trap concentration is very high, there may not be enough charge carriers near the interface to saturate the traps during the pulse. As seen in Fig.4.17, there is a substantial drop in C_{rb} around the peak temperature for the n-Si samples. This could be considered as a carrier depletion (near the interface), as the free charge carriers start to freeze out at these temperatures. ii) *Small capture cross section.* As seen from Tab.4.3, σ_{na} is in about 10^{-20}cm^2 for the shallow electron traps, which can result in a reduced filling. Higher or longer injection pulses could have been used to saturate the signal. However, it was generally seen that high injection pulse ($V_p \geq 2$V) made it harder to achieve

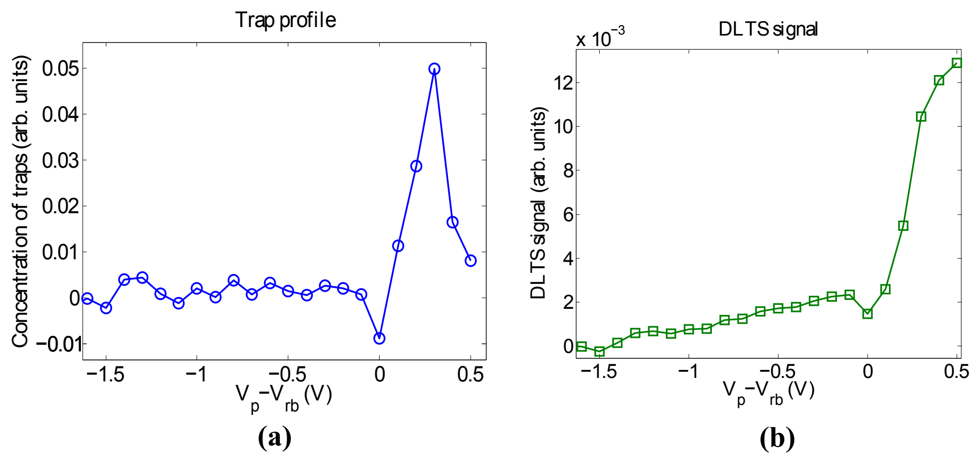
good measurements throughout the whole temperature scan. Often there was a loss of contact at some point, reflected by the spectra in Fig.4.10. But as the peak temperature was almost the same as with lower injection pulse, and most of the peak was obtained for these measurements, it was assumed to be a valid result (see appendix B.1 for a comparison between low and high injection pulse signals). The reason for using time window 4 in the high injection pulse figure (Fig.4.10), was an apparent "shift" in peak temperature observed for the 120°C and 200°C annealed ITO(300nm)/n-Si samples with storage time. For the latest measurements of the 120°C annealed sample, the peak appeared below 77 K using time window 6, which is below the limit of the setup. This indicates that the defects causing the levels, might be mobile at room temperature. As for the profiling of H(0.37) (see Fig.4.16), a sharp peak in the profile is seen as the pulsing bias becomes larger than the reverse bias. This gives a clear indication that the traps are confined to the interface of the junction.

When considering the relative concentrations for the different annealing temperatures it is important to consider the reverse bias capacitance C_{rb}. If the concentration of traps is very high, the electrons in the conduction band (for the n-Si case) may become depleted before the temperature is reached where the peak occurs in the long time windows. This can result in a lower peak height, as there are less electrons available to fill the traps. As seen from Fig.4.17, there is a substantial drop in C_{rb} for the n-Si samples around the peak temperature. The shape of the drop, indicates that a trap is starting to cause "freeze out". Together with the unsaturated DLTS signal in Fig.4.15, this indicates that the relative height between the DLTS peaks of the different anneals must be regarded as rough estimates with substantial uncertainties ($\sim$ 25%).



(a) **(b)**

Figure 4.15: ITO/n-Si annealed at 250°C. Measurement was taken at 154K with time window 6 (640 ms). a) Trap distribution with changing pulsing bias b) DLTS signal with changing pulsing bias.



(a) **(b)**

Figure 4.16: ITO/p1-Si annealed at 120°C. Measurement was taken at 176K with time window 6 (640 ms). a) Trap distribution with changing pulsing bias b) DLTS signal with changing pulsing bias.

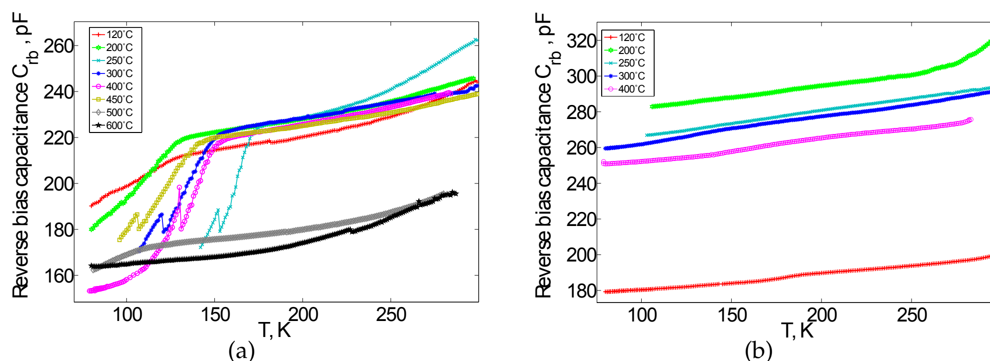


Figure 4.17: Reverse bias capacitance vs. cooling temperature taken during the DLTS measurements. a) ITO(300nm)/n-Si b) ITO(300nm)/p2-Si.

4.2 SIMS measurements

SIMS measurements were obtained with a 10keV O_2^+ primary beam at a current of 20nA. The beam was swept over an area of 200x200μm, and positive ions were extracted and detected. Figure 4.18 shows a mass spectrum taken for the as deposited sample. Based on results from the mass spectrum, a depth profiling was conducted for the labeled atoms in Fig.4.18, and shown in Fig.4.20. Only relative intensities are shown, in counts/s, since reference samples were not available. The as deposited, 300°C and 600°C samples were investigated to see if there were any clear trends related to the annealing temperature. As seen in Fig.4.20 for the as deposited sample, the metal impurity levels are quite constant within the ITO film. The same was found for the two samples annealed at higher temperature. Depth profiles of H, C, O, Si, In and Sn were then obtained for all annealing temperatures, leaving out the metal impurities to improve depth resolution[8]. Looking at Fig.4.19, some trends in the depth profiles can be observed: i) A stable interface region of about 50 nm occur for all temperatures, and the

[8]Compared to the full spectrum in Fig.4.20.

In and Si levels seem to be stable with increasing annealing temperature. ii) The H and C levels have a clear peak within the interface region, with a decreasing concentration for H with increasing temperature, while the C peak appears to be stable. iii) The level for Sn shows a higher level near the surface, but at 450°C and above, an accumulation of Sn takes place at the interface (see Fig.4.21). However, it must be mentioned that the ionization efficiency of the sputtered ions can change in the interface region, and this must be taken into account when interpreting the results in Fig.4.18-4.21. In retrospect, it could have been better to use the Cs^+ source as the primary beam, since H and C were found to be the most interesting impurities, and detection of H and O is better using a Cs^+ source compared to O_2^+. The reason for using O_2^+, was the ability to detect metal impurities with a high sensitivity.

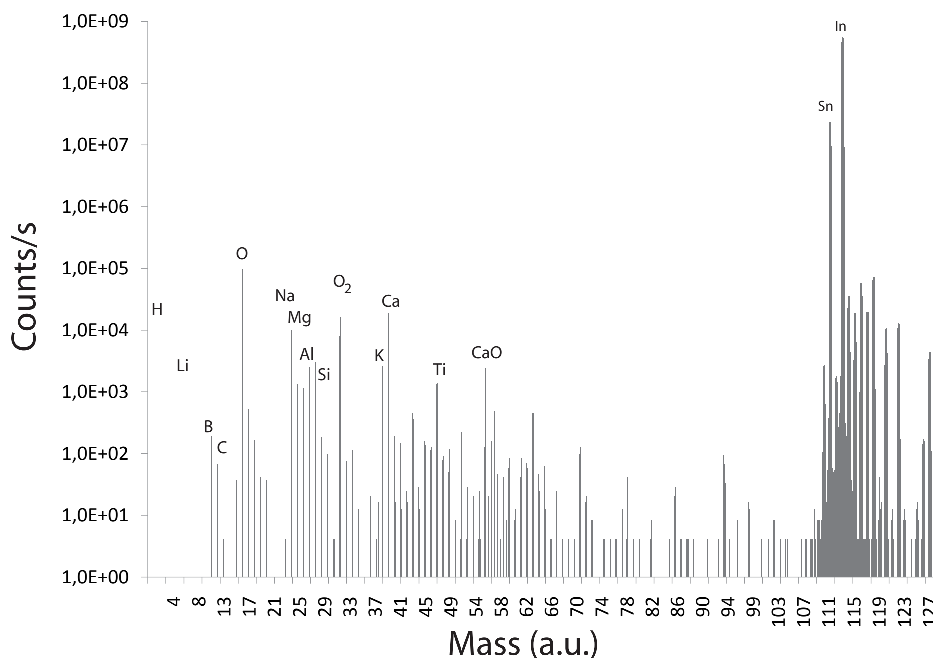


Figure 4.18: Mass spectrum obtained by SIMS for as deposited ITO(300nm)/p2-Si.

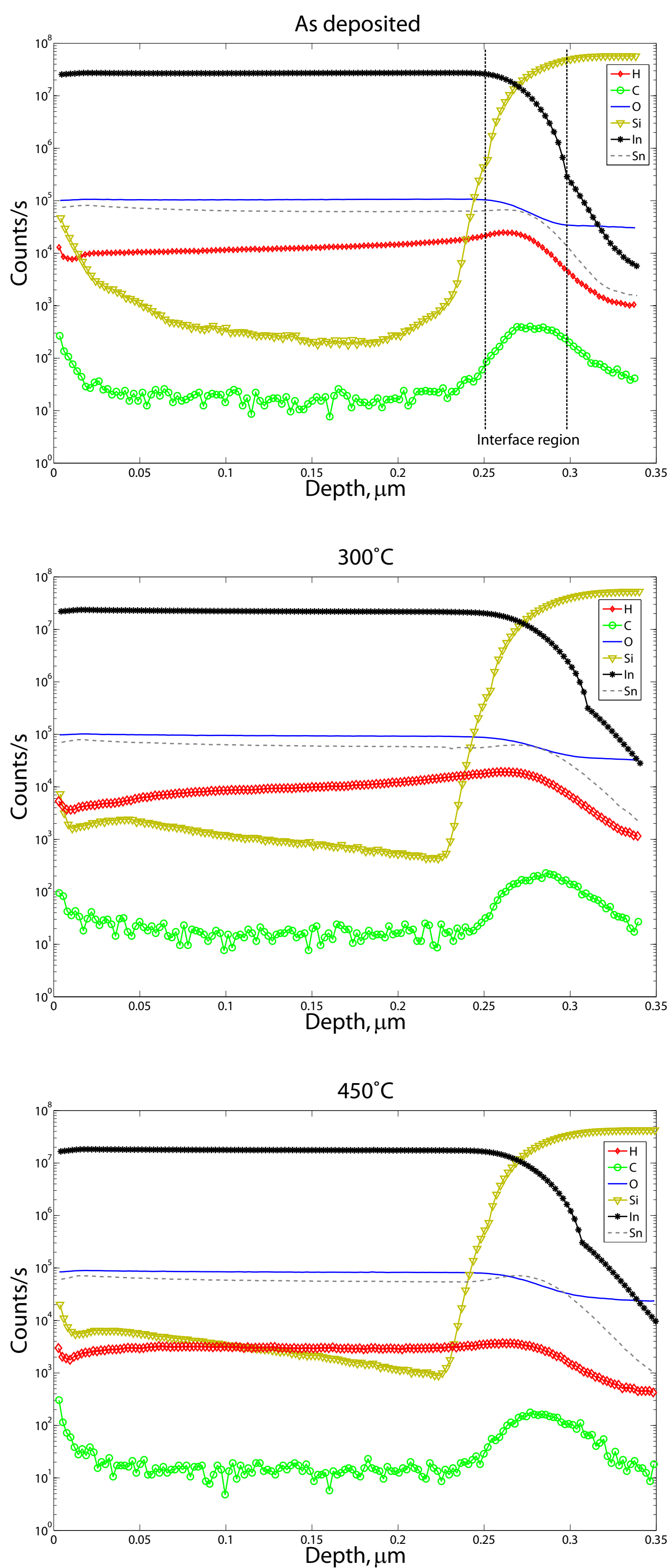


Figure 4.19: Depth profiles for ITO(300nm)/p2-Si samples. Profiles of the remaining annealing temperatures are shown in Fig.B.4

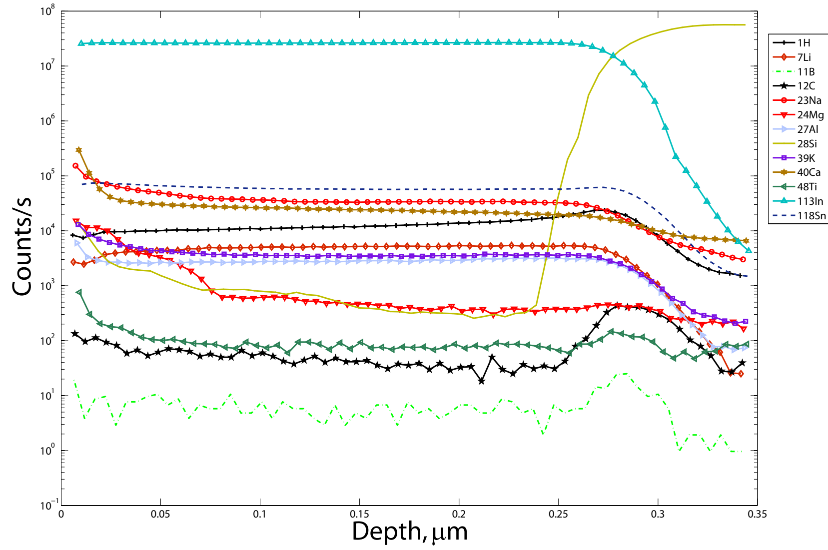


Figure 4.20: Depth profile obtained by SIMS for as deposited ITO(300nm)/p2-Si.

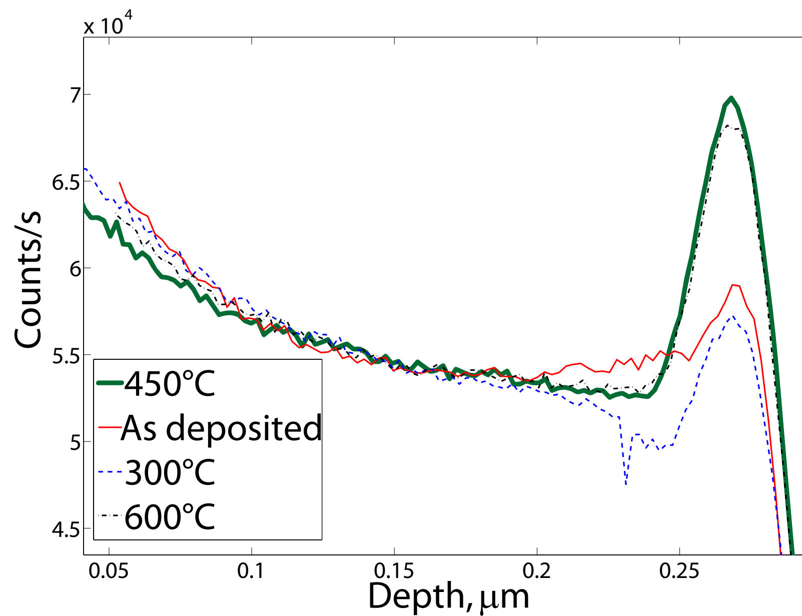


Figure 4.21: Depth profiles of Sn at various annealing temperatures. The signals are normalised to a joint bulk level.

4.3 AFM measurements

Figure 4.22 shows the AFM results obtained for all annealing temperatures. It shows a surface with grain sizes ranging from 20 to 150 nm, and a slight increase in roughness for higher annealing temperatures (see Fig.4.23). According to these results it is plausible that the films are polycrystalline in nature, but the apparent "grains" observed by AFM could very well be related to nano sized channels, a porous structure or grains only at the surface of the ITO layer. Sputtered ITO films deposited at room temperature are generally amorphous [57], but annealing enhance crystal growth, resulting in a polycrystalline film [25],[58]. To shed more light on the structure of the investigated films, x-ray diffraction (XRD) was conducted on some of the samples. The as deposited and 450°C annealed samples gave inconclusive results, as the 450°C sample only showed very weak signals for the (400) and (222) planes of In_2O_3 compared to that for similar samples reported in the litterature [25],[58]. The as deposited sample did not show the normal broad peak usually observed in amorphous films, either. The instrument used for XRD was later reported to have some issues related to low detection when measuring on thin films. This might give an answer to the low intensities observed for the films investigated in this thesis. To reveal the true nature of the film structure, crossectional Transmission Electron Microscopy (x-TEM) could have been performed, but was excluded due to time limitations.

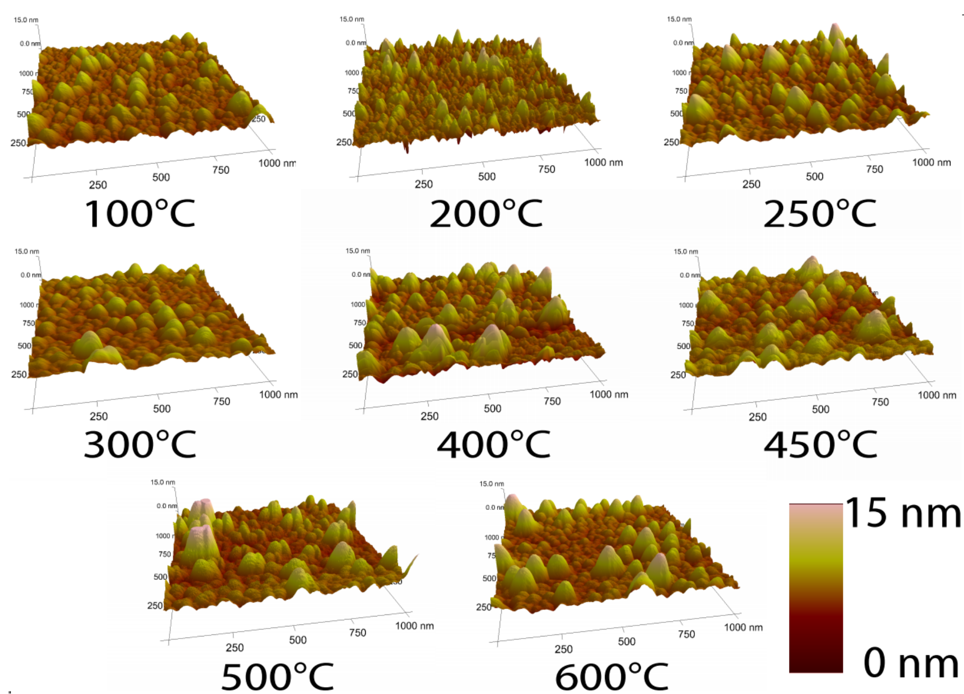


Figure 4.22: AFM images for different annealing temperatures of ITO(300nm)/p-Si. The reader is reminded of the considerable difference in scale between the xy plane and the z-axis

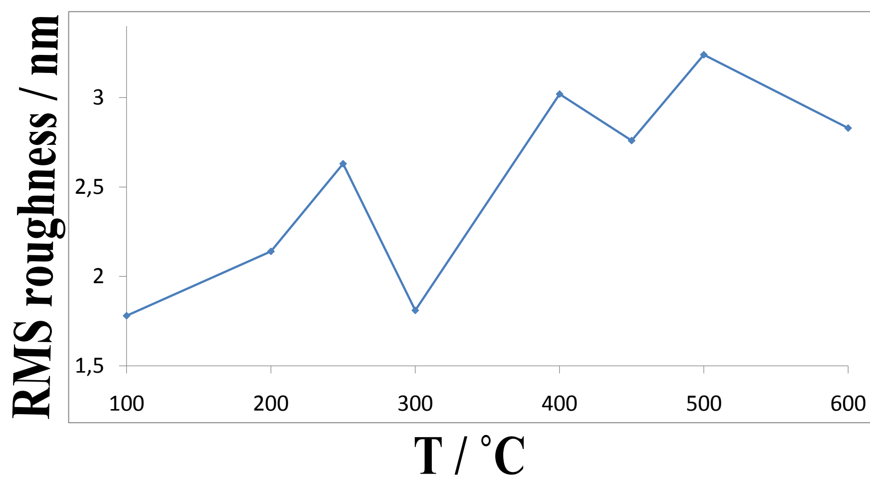


Figure 4.23: Root mean square (RMS) roughness of the surface of the samples in Fig.4.22

4.4 Tentative identification of the traps observed

As of identification of the traps, H(0.37) has been observed in similar samples by Zettler et al. [37] and proposed to be C_sC_i[9]. Taylor et al. [59] reported a similar level in irradiated Si as C_s-Si_i-C_s, while Libertino et al. [60] and Petasecca et al. [61] assigned a similar level to C_iO_i. The fact that there is a considerable concentration of C at the interface, supports the possibility that H(0.37) can be related to C in these samples as well. Looking at the results reported by the RD48 collaboration [62], values obtained for C_iO_i and a level at (E_v+0.312)eV show good agreement of both energy level and σ_{na} to H(0.37) and H(0.32), only that C_iO_i is seen to increase with annealing temperature in those results. The labeling of H(0.37) as C_iO_i is supported by Svensson [63] (and references therein) and Asom et al. [64]. Svensson discussed in Ref.[63], that the C(3) center has been shown to have a donor level at $\sim (E_v + 0.35)$ eV. This level was suggested to have the C_iO_i configuration by local-density-functional cluster calculations carried out by Jones et al. [65]. Annealing experiments carried out by Svensson et al. [66] reported an annealing of the C(3) level at about 300°C, which is close to the observed annealing temperature of H(0.37) (250°C). This gives a strong indication that H(0.37) could originate from the C_iO_i defect.

The shallow electron traps observed in this thesis, are close in energy to the traps found in similar samples by Kuwano et al. [38]. As discussed in Section 2.6.2, they found three electron traps at 0.25eV, 0.19eV and 0.10eV below the conduction band edge. Their corresponding capture cross section, are in the same range as E(0.1) and E(0.2), indicating that they might be related. No possible identification was given in Ref.[38], but it was shown that a pretreatment of H reduced the signal substantially. Zettler et al. [37] found multiple electron traps in the range 0.15-0.22eV below the conduction band edge (as shown in Tab.2.1). The trap at (E_c-0.15)eV was proposed

[9] *s* refers to a substitutional defect, and *i* to an interstitial.

as the vacancy oxygen defect (VO), while a trap at (E_c-0.22)eV was reported as the divacancy (V_2) . If the observed E(0.2) trap were to originate from V_2, one would expect to see another charge state of V_2 at (E_c-0.42)eV as well [62],[67], which was not seen in the present investigation. In addition to this, reported values for capture cross section of VO and the V_2 levels, are about five orders of magnitude higher than E(0.1) and E(0.2) [62].
As mentioned above, the annealing of the electron traps coincides with an increase in Sn concentration at the interface. This indicates that Sn is mobile at elevated temperatures, and it may then interact with defects at the interface. It has been shown by Loferski et al. [68] that the threshold energy to create a frenkel pair[10] in Si is about 13 eV. As the sputtered atoms hit the Si wafer with energies above this value, vacancies can be created in the first part of the sputtering process. Doping of Si with isovalent Sn has shown that Sn can trap vacancies *V* and create SnV pairs [69],[70]. Watkins et al. [71] proposed a level at (E_v+0.35)eV as the SnV pair, which annealed out at about 500K. This is not far from the properties observed for H(0.37). Another Sn defect, labeled as $(Sn_2V_2)^-$ was reported to anneal out at 690K by Kaukonen et al. [72]. This is the temperature range in which the electron trap anneals out in the ITO(300nm)/n-Si samples. However, more recent reports related to SnV levels in Si suggest that the SnV defect has two levels at (E_c-0.214)eV and (E_c-0.501)eV with an annealing temperature of $\sim$425K [73]. This weakens the possible identification of H(0.37) as a SnV level. Sn has also been shown to make complexes with C_i. Lavrov et al. [74] reported that C_i has a level at (E_c-0.1)eV, which could corresponds to E(0.1). They calculated that this level is shifted to (E_c-0.35)eV if C_i reacts with Sn to make a C_i-Sn complex, which is in the range of the E(0.4) level observed for the ITO(300nm)/n-Si sample annealed at 600°C. A shallow electron trap state of C_i at (E_c-0.06)eV was also reported by [75]. However, as C_i has been

[10] A frenkel pair is a vacancy and a self-interstitial.

shown to be mobile even at room temperature [76],[64] it would unlikely be stable up to the observed annealing temperature of E(0.1) (500°C).
It has been shown that dangling Si bonds at the Si/SiO_2 interface create traps labeled as P_b centers [77],[78],[79]. These centers can produce levels close in energy to both the valence and conduction band as well as levels in the range of H(0.37) and E(0.1)/E(0.2). However one might expect a similar annealing behavior of both the electron and hole traps, if they were to result form a common P_b center. This is not the case, as described in Section 4.1.5. Because of the 77K temperature limit of the DLTS setup used in this thesis, shallow hole traps (resulting from possible P_b centers), which could have given more information about the nature of E(0.1)/E(0.2), were not possible to detect.

Chapter 5

Summary

"The important thing is not to stop questioning."

-Albert Einstein

5.1 Conclusions

This thesis has shown that rectifying heterojunctions can be made of ITO deposited on p-Si up to a post deposition annealing temperature of about 400°C, and ohmic contacts above 450°C. For ITO/n-Si there will be a rectification for all investigated temperatures up to 600°C. One major hole trap, and two major electron traps were found at the interface between ITO and Si using DLTS. Reviewing all the results and annealing temperatures, there seems to exist three temperature transition regions where the samples obtain different electronic characteristics.

i) Below 250°C: All samples show high trap concentrations and poor rectifications as well as high resistivity of the ITO films.

ii) 250°C-300°C: The resistivity of the films are at the lowest value, and the rectification for the p-Si samples peaks as the dominant hole trap is annealed out. The n-Si samples still show high trap concentrations and similar IV/CV characteristics as before annealing.

iii) Above 450°C: There is a substantial increase in rectification for the n-Si samples, while the p-Si samples become ohmic. This coincides with a confinement of the electron traps to the interface[1] and an accumulation of Sn at the interface, while the resistivity of the ITO films increase.
IV and DLTS measurements demonstrate clear correlation between the annealing of the dominant electronic states and increase in the junction rectification. However, most of the photogenerated current was lost before the solar cell structure started to deliver power. This effect was not seen to change with annealing of the interface traps, and it was argued that the high series resistance observed for all the investigated diodes might be responsible for this effect. Tentative identification of the traps was discussed, and properties of the H(0.37) level were found to be closely related to that of the C_iO_i defect. As for the observed electron traps, no plausible identification was given, and further investigation by supplementary techniques must be done in order to gain more understanding of the defect formation.

5.2 Suggestions for further work

Annealing in hydrogen atmosphere would have been interesting, as a means of possible low temperature annealing. In addition, the effect of hydrogen pretreatment or mixing hydrogen into the sputtering gas could give information of possible defect passivation. Samples deposited with substrate heating, would be interesting to examine for any interfacial differences compared to the current investigated samples. The resistivity of the interface region could have been probed by Scanning Spreading Resistance Microscopy (SSRM), while cross sectional Transmission Electron Microscopy (x-TEM) could give information of the abruptness of the junction and structure of the film. As a next step, DLTS studies of ITO/n(p)-a-Si:H/p(n)-Si

[1] Which anneals out at 500°C.

junctions would be very interesting to perform as well as related ZnO/Si structures for future solar cell applications.

Appendix A

Detailed derivations of some relations

A.1 Derivation of capacitance of the depletion region

The balance of charge requires that:

$$x_{n0}N_d = x_{p0}N_a \tag{A.1}$$

$$W = x_{n0} + x_{p0} \tag{A.2}$$

$$x_{n0}N_d = (W - x_{n0})N_a$$

$$x_{n0}N_d = WN_a - x_{n0}N_a$$

$$x_{n0}(N_d + N_a) = WN_a$$

$$x_{n0} = \frac{WN_a}{N_d + N_a} \tag{A.3}$$

A.2 Current across the junction

This Section is based upon similar derivations given by Rhoderick [47] and Streetman [4]. The current flow across the barrier consists of drift and diffusion as mentioned in Chapter 2.3. It was then concluded that the field at the junction was a consequence of the diffusion of carriers from both sides.

These drift and diffusion parts of both electron and hole currents can be expressed as:

$$I_n(x) = \underbrace{qA\mu_n n(x)E(x)}_{drift} + \underbrace{qAD_n \frac{dn(x)}{dx}}_{diffusion} \tag{A.4}$$

$$I_p(x) = qA\mu_n p(x)E(x) - qAD_p \frac{dp(x)}{dx} \tag{A.5}$$

where $n(x), p(x)$ is the electron and hole concentration at position x, μ is mobility, D is the diffusion constant and A is the cross sectional area of the diode. The reason for the different sign on the diffusion parts is due to the different charge of electrons and holes. A change in bias will change the diffusion current directly, while the drift current will be less affected. This is because of the two different mechanisms controlling the two currents. Diffusion is directly related to the hight of the barrier, where a high barrier will give almost no diffusion current and a low barrier the opposite. Drift however is limited by how often a charge carrier wander into the depletion region and swept across the junction by the field. This will not be affected by a change in the barrier, as the charge carrier will be swept across both by a low and a high field. The equations above can be simplified if we introduce the concept of quasi-fermi levels. Near the junction, the Fermi level in the neutral regions will not describe the electron and hole concentrations accurately. So the Fermi levels on p and n-side $E_{f,p}, E_{f,n}$ (seen in Fig.2.9) will be changed with the quasi-fermi levels F_p, F_n. From here on I will consider electron currents, but similar arguments are valid for holes. Using the quasi-fermi level in Eq.2.8, the gradient in electron concentration in Eq.A.4 is given by:

$$\frac{dn(x)}{dx} = \frac{d}{dx}[n_i e^{(F_n - E_i)/kT}] = \frac{n(x)}{kT}\left(\frac{dF_n}{dx} - \frac{dE_i}{dx}\right) \tag{A.6}$$

From the definition of the potential across the junction in Eq.2.18 we see

that the electric field is given as:

$$E(x) = -\frac{dV(x)}{dx} \tag{A.7}$$

If we choose E_i as a reference point in the band diagram, this can be written as:

$$E(x) = -\frac{dV(x)}{dx} = -\frac{d}{dx}\left(\frac{E_i}{(-q)}\right) = \frac{1}{q}\frac{dE_i}{dx} \tag{A.8}$$

Insert Eq.A.6 and A.8 into Eq.A.4 one obtains the following:

$$\begin{aligned}
I_n(x) &= qA\mu_n n(x)E(x) + qAD_n\frac{n(x)}{kT}\left(\frac{dF_n}{dx} - \frac{dE_i}{dx}\right) \\
I_n(x) &= qA\mu_n n(x)E(x) + A\mu_n n(x)\left(\frac{dF_n}{dx} - \frac{dE_i}{dx}\right) \\
I_n(x) &= qA\mu_n n(x)E(x) - qA\mu_n n(x)E(x) + A\mu_n n(x)\left(\frac{dF_n}{dx}\right) \\
I_n(x) &= A\mu_n n(x)\left(\frac{dF_n}{dx}\right)
\end{aligned} \tag{A.9}$$

Here we have used the *Einstein relation* $\frac{D}{\mu} = \frac{kT}{q}$. The current is described by the gradient in the quasi-fermi level. It can be shown that the resulting current from the discussion above has the following dependence:

$$I \propto (e^{qV/kT} - 1) \tag{A.10}$$

Now if we assume that the junction is between a semiconductor and a metal, and that the current-limiting process is the flow across the interface. We can describe the current by the *thermionic-emission theory*. The reason for doing this, is that the junctions which have been investigated in this thesis, behaves like a metal-semiconductor junction (which is called a Schottky-junction). In the thermionic emission theory it is assumed that the Fermi-level is close to constant throughout the depletion region, and on the same level as in the metal. If a voltage V is applied to the junction, the electron

concentration on the semiconductor side will change by a factor of $e^{qV/kT}$. The electron concentration will then be given by:

$$n = N_c e^{-q(\Phi_b - V)/kT} \tag{A.11}$$

where $q\Phi_b$ is the barrier height between the metal and the semiconductor (see Fig.A.1). If the kinetic energy of the electrons are given by $n\bar{v}/4$, where $\bar{v}$ is the average thermal velocity of the electrons, then the current from semiconductor to metal is given by:

$$I_{sm} = \frac{ApqN_c\bar{v}}{4} e^{-q(\Phi_b - V)/kT} \tag{A.12}$$

where p is the probability that the electrons will tunnel through the interface. At zero applied bias, the current from metal to semiconductor and vice-versa must cancel out. This implies that:

$$I_{ms} = \frac{ApqN_c\bar{v}}{4} e^{-q\Phi_b/kT} \tag{A.13}$$

$$I = I_{sm} - I_{ms}$$

$$I = \frac{ApqN_c\bar{v}}{4} e^{-q\Phi_b/kT}(e^{qV/kT} - 1) \tag{A.14}$$

If we finally assume that: i) $p = 1$ ii) there is a Maxwellian distributions of velocities giving $\bar{v} = (8kT/\pi m^*)^{1/2}$. Then we can put all the constants in the expression into A^* which is called the Richardson constant, and get the following voltage dependence of the current:

$$I = \underbrace{AA^*T^2e^{-q\Phi_b/kT}}_{I_0}(e^{qV/kT} - 1) \tag{A.15}$$

where

$$A^* = \frac{4\pi m^* qk^2}{h^3} = 1.2 \cdot 10^6 (m^*/m) Am^{-2}K^{-2} \tag{A.16}$$

and m^* is the effective mass of the electron in the semiconductor.

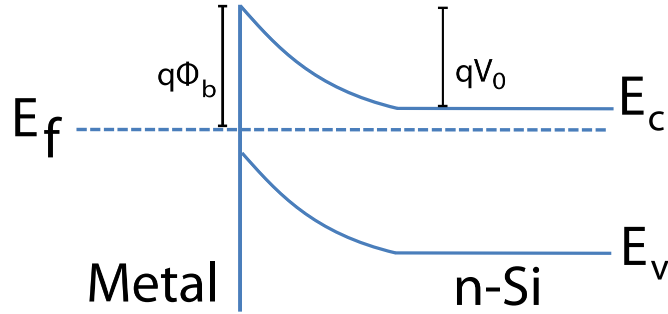


Figure A.1: Schematic view of the band structure of a Schottky-junction, including the barrier height $q\Phi_b$

A.3 Thermal occupancy of traps

Supplementary to the derivation in Section 2.4.

$$\frac{n_t}{N_t} = \frac{c_n}{c_n + e_n} = \frac{e_p}{e_p + c_p} = \frac{1}{1 + \underbrace{exp((E_t - E_F)/kT)}_{x}}$$

$$c_n = \frac{c_n}{1+x} + \frac{e_n}{1+x}$$

$$c_n\left(1 - \frac{1}{1+x}\right) = \frac{e_n}{1+x}$$

$$\frac{e_n}{c_n} = \left(1 - \frac{1}{1+x}\right)(1+x)$$

$$\frac{e_n}{c_n} = 1 + x - 1 = x$$

$$\frac{e_n}{c_n} = e^{(E_t - E_F)/kT} \tag{A.17}$$

$$\frac{e_p}{c_p} = e^{(E_F - E_t)/kT} \tag{A.18}$$

A.4 Mid band gap level E_1

Supplementary to the derivation in Section 2.4.1.

$$\begin{aligned}
e_p &= e_n \\
\sigma_p v_{th,p} N_v exp(-(E_1 - E_v)/kT) &= \sigma_n v_{th,n} N_c exp(-(E_c - E_1)/kT) \\
\left(\frac{\sigma_p v_{th,p} N_v}{\sigma_n v_{th,n} N_c}\right) &= exp(-(E_1 - E_v)/kT) exp((E_c - E_1)/kT) \\
2E_1 - (E_c + E_v) &= kTln\left(\frac{\sigma_p v_{th,p} N_v}{\sigma_n v_{th,n} N_c}\right) \\
E_1 &= \underbrace{\frac{E_c + E_v}{2} + \frac{kT}{2} ln\left(\frac{N_v}{N_c}\right)}_{E_i} + \frac{kT}{2} ln\left(\frac{\sigma_p v_{th,p}}{\sigma_n v_{th,n}}\right)
\end{aligned} \tag{A.19}$$

$$E_1 = E_i + \frac{kT}{2} ln\left(\frac{\sigma_p v_{th,p}}{\sigma_n v_{th,n}}\right) \tag{A.20}$$

A.5 The numerical values used for lock-in DLTS signal

As mentioned in Section 3.5 the values for the emission rate e_n could be found from the peak of the DLTS spectrum. As $dS/dT = 0$ at the peak, the following derivation has to be done to find e_n:

$$\frac{dS}{dT} = \left(\frac{dS}{de_n t}\right)\left(\frac{de_n t}{dT}\right) = \frac{d}{de_n t}\left(e^{-e_n 2\tau} - e^{-e_n \tau}\right)\frac{de_n t}{dT} = 0 \tag{A.21}$$

$$-2e^{-e_n 2\tau} + e^{-e_n \tau} = 0 \tag{A.22}$$

$$ln2 - e_n 2\tau = -e_n \tau \tag{A.23}$$

$$e_n \tau = ln2 \tag{A.24}$$

$$e_n t_1 = e_n 2\tau = 1.386 \tag{A.25}$$

To get the value for F_1, $e_n \tau$ is put back into the expression for F_i:

$$F_i = \frac{1}{n_i} \sum_{t=t_d}^{t_d+t_i} e^{-e_n t} w(t) \tag{A.26}$$

$$F_1 = \frac{1}{2} \left(e^{-2ln2} - e^{-ln2} \right) \tag{A.27}$$

$$|F_1| = 0.125 \tag{A.28}$$

In this illustrative calculations, the delay time of the measurement has been neglected, resulting in a small error. If the values for e_n are calculated by a numerical method, it is easy to generate a simple script, to do the calculation of the values of F_i:

```
e_n=[0.72448 0.45429 0.26225 0.14264 0.074705 0.038278 0.019381 0.0097526];
for i=1:8
    a = 2^i;
        for j=1:a/2
                pos(j) = exp(-j*e_n(i));
                neg(j) = exp(-(a-j+1)*e_n(i));
        end
    F(i) = ((1/a) * (sum(pos) - sum(neg)));
end
```

Appendix B

Chemicals, sputtering parameters and supplementary results

B.1 Chemicals and sputtering parameters

Base pressure	3μTorr
Ar pressure	2.5 mTorr
Voltage	340V
Current	2.5 A
Substrate temperature	Room temperature (RT)

Table B.1: The parameters used during sputtering.

Positive photoresist	Microposit S1813
Developer	Microposit 351

Table B.2: Lithography chemicals

B.2 Supplementary results

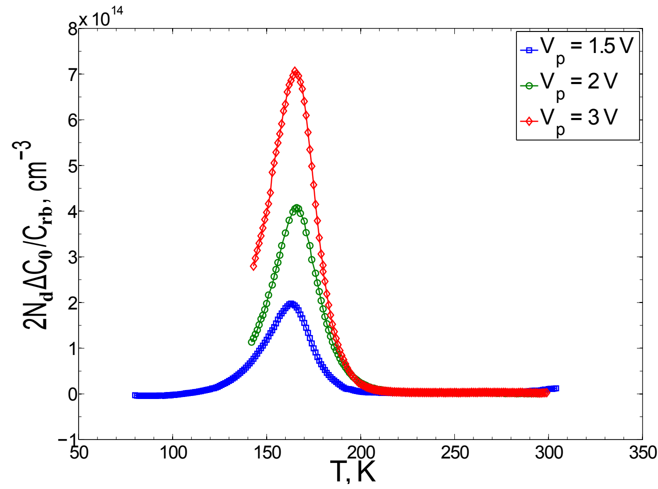


Figure B.1: Comparison between peak hight and pulsing bias for the ITO(300nm)/n-Si annealed at 250°C. As the peak temperature is almost the same, the peak was assumed to be valid even though the peaks were not complete. Time window 4 (160ms).

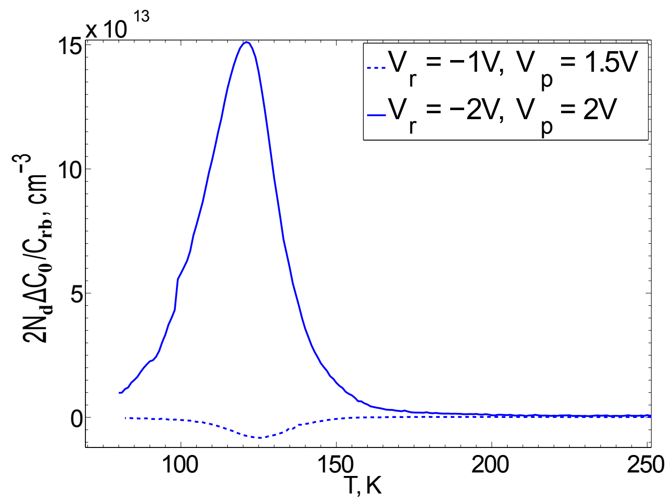


Figure B.2: DLTS spectra of ITO(300nm)/n-Si annealed as 300°C. Comparison between bulk and interface measurement. Time window 6 (640ms).

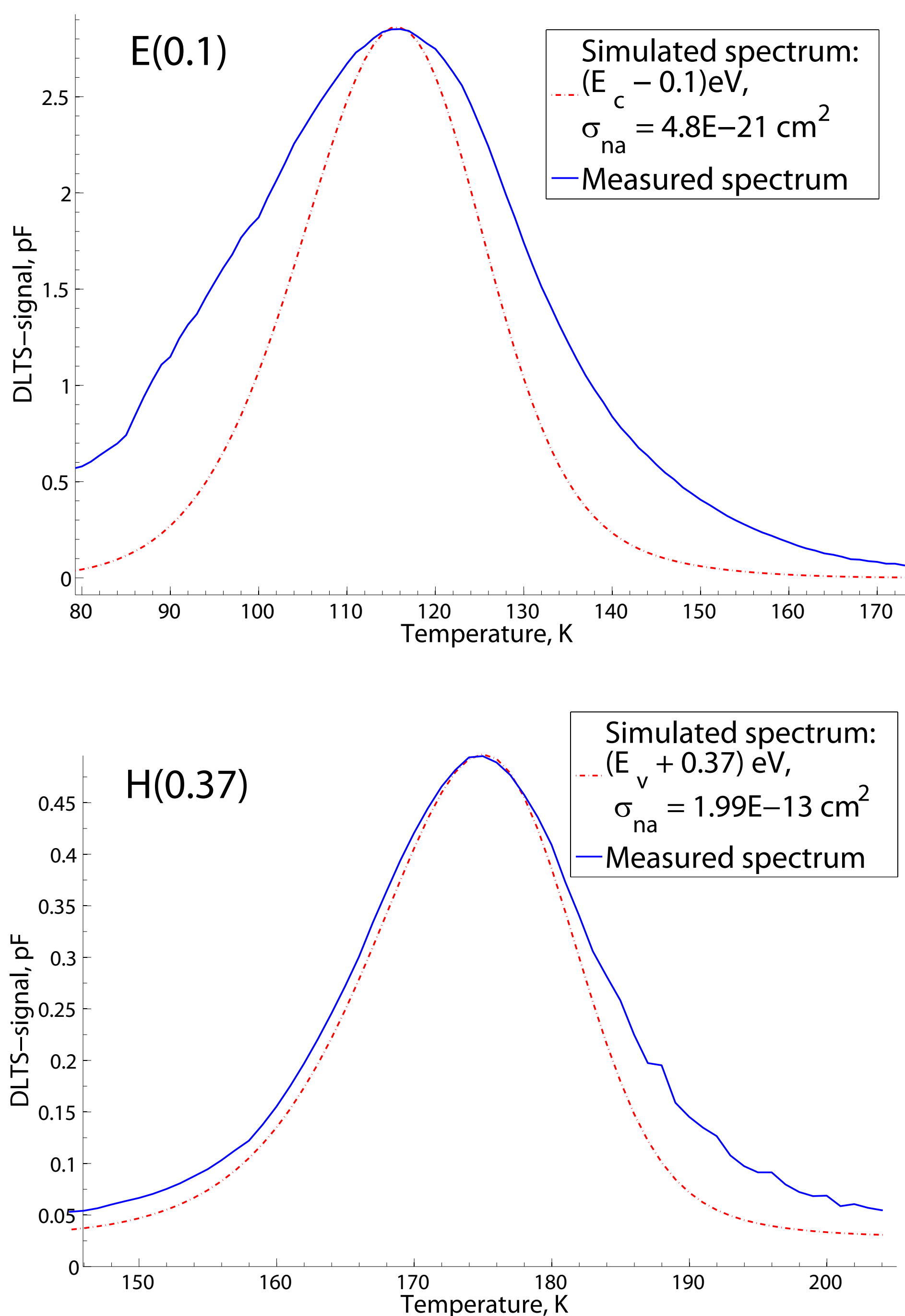


Figure B.3: Comparison between measured and simulated DLTS spectra for typical peaks resulting from E(0.1) and H(0.37). The simulated spectra were made with a Matlab script written by Lars Løvlie.

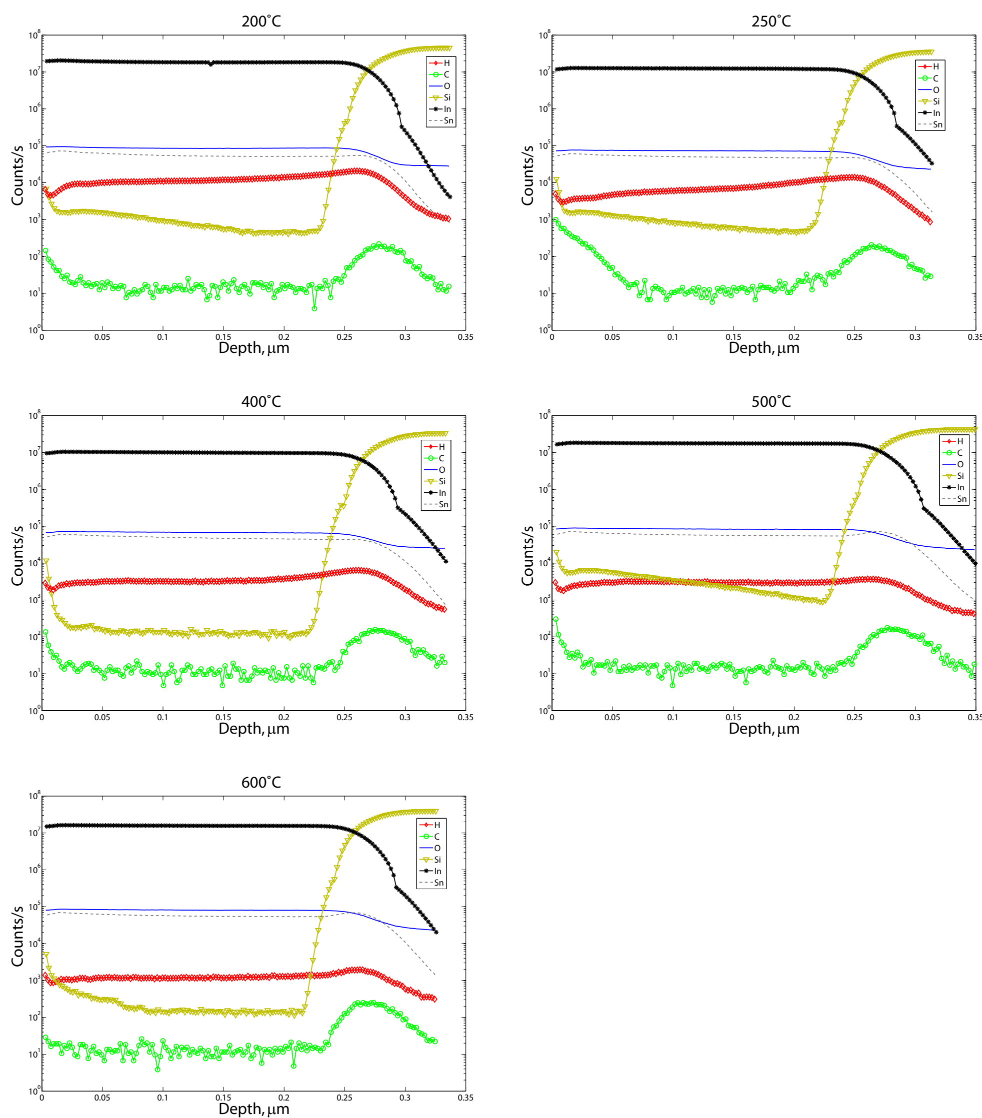


Figure B.4: Depth profiles for remaining annealing temperatures of ITO(300nm)/p2-Si samples.

B.3 PC1D simulation software

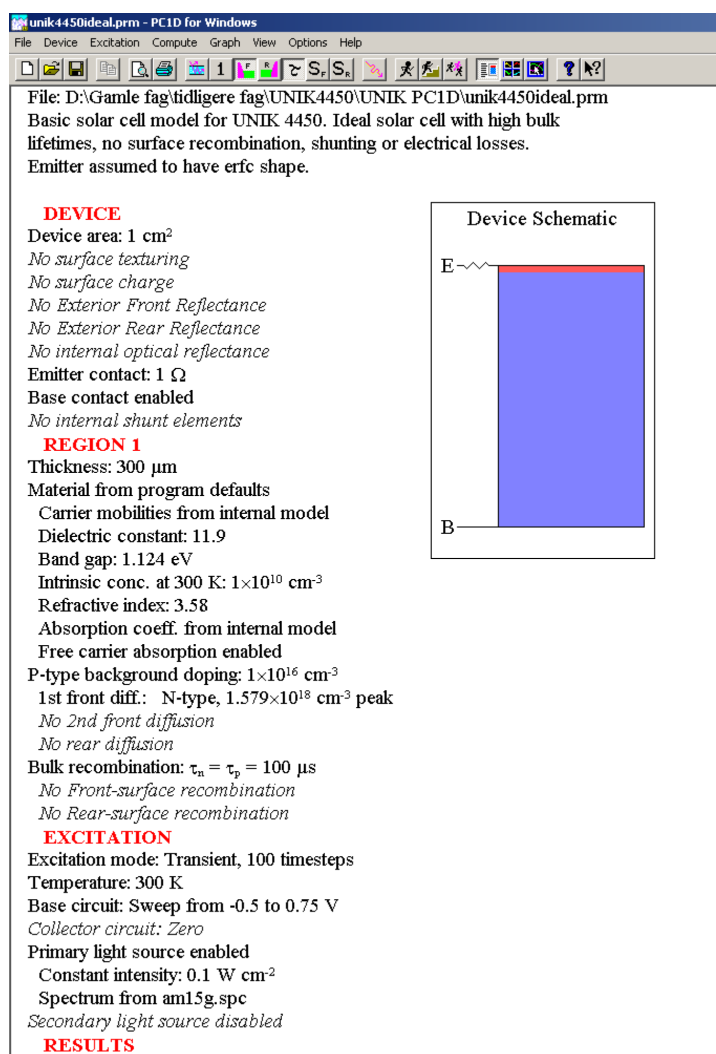


Figure B.5: Screenshot of the program window in PC1D showing some of the parameters used in the simulation.

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