UNIVERSITY OF OSLO
Department of Physics

Low Power and Low Voltage Operational Amplifier

Master thesis (60pt)

Kjetil B. Stiansen

1st September 2008

Preface

This thesis concludes my work for the Master of Science degree in Microelectronics at the Department of Physics, Faculty of Mathematics and Natural Sciences, University of Oslo.

I would like to thank my supervisor, Senior Research Scientist at SINTEF and Associated Professor II at the University of Oslo, Joar Martin Østby for his help and feedback during the project. In addition, tanks goes to Scientist Roy Bahr at SINTEF for help and guidance during the layout and tape out of the operational amplifier. Morten Berg deserves thanks for good advice and help with the EAGLE Layout Editor and my co-student Øyvind Fjellang Sæther deserves thanks for teaching me LaTeX and for many motivating talks.

I would like to thank my family and friends for supporting me through this last years challenges and my girlfriend for always being there for me, especially during the last weeks of writing.

Lørenskog, September 2008

Kjetil Bertin Stiansen

Abstract

Reducing the supply voltage of operational amplifiers and analog circuitry in general, is of great importance as it will ensure the future coexistence of analog and digital circuits on the same silicon die. While digital circuits greatly benefit from the reduction in feature size and supply voltage, analog circuits on the other hand only benefit marginally because minimum size transistors cannot be used due to noise and offset requirements. This trend towards low voltage and low power, effects the fundamental limits of operational amplifiers. The gain and bandwidth are restricted by minimum voltages and currents. Also the dynamic range is degraded by these strict limits. Upwards, the dynamic range is lowered due to the reduced signal headroom as a result of reduced supply voltage. Downwards, the dynamic range is limited by larger noise voltages due to smaller supply currents. The only way to make the operational amplifier survive the trend towards lower supply voltages without deteriorate its characteristics, is by developing very efficient operational amplifier topologies that combines low voltage and low power operation and contemporary be as simple as possible to save die area.

This thesis presents some of the main aspects of low voltage and low power operational amplifiers and their ability to work from rail to rail on both input and output. The input referred offset voltage was also characterized. Theory around input and output stages are studied. A low voltage operational amplifier was processed in $0.35\,\mu$m CMOS. Measurements were done on the operational amplifier and compared with the simulation results.

Contents

Chapter 1

Introduction

During the last few years portable electronic equipment have become increasingly sophisticated. To keep up the trend, more complex digital and mixed signal circuitry have to be included on the same silicon die. As the density of components on a chip increases, the power dissipation per component must decrease to ensure that the temperature of the silicon die are kept within safe limits. In digital circuitry where package density and thereby dissipated power is largest, the whole system will benefit because of the reduced power needed. Reducing power in digital systems is done by reducing the supply voltage. The average power consumption of CMOS digital circuit is to a first order approximation, proportional to the square of the supply voltage, hence the great prize in power reduction. The lower supply voltages reduces the dynamic range of operational amplifiers (op amps). To cope with the reduced dynamic range, the signal voltage has to be as large as possible, preferably from rail to rail. Since the signal can extend from rail to rail, the input and output stage of an op amp must be able to handle such signals. Traditional circuit solutions will not meet these demands and new one has to be found.

The operational amplifier is one of the most important analog building blocks. The ongoing work and research in the field of low voltage and low power op amps is very important to keep up with the developments in digital circuit design.

1.1   Previous work and history

The operational amplifier has been around for about 60 years. It is difficult to establish the exact the date of birth, but the name operational amplifier was first coined out in 1947 by Professor John Ragazzini[25]. Quoting from his paper on the naming:

> "As an amplifier so connected can perform the mathematical operations of arithmetic and calculus on the voltages applied to its input, it is hereafter termed an 'operational amplifier'"

Much work was done before Ragazzini's operational amplifier. The background of the op amp began early in the 20th century, starting with certain fundamental inventions[17]. There were two key inventions in the beginning of the century. The first was not an amplifier, but a two-element vacuum tube-based rectifier, the " Flemming diode", by J. A. Flemming, patented in 1904.

The second development was the invention of the three-element triode vacuum tube by Lee De Forest, the "AUDION," in 1906. This was the first active device capable of signal amplifaction.

For op amps, the invention of the feedback amplifier principle at Bell Telephone Laboratories during the late 1920's and 30's were truly an enabling development. This landmark invention led directly to the first phase of vacuum tube op amps, a general form of feedback amplifier using vacuum tubes. Harold S. Black was the first who developed feedback amplifier principles. The work done by Black plus the work done by Harry Nyquist and Hendrick W. Bode on avoiding instability in feedback amplifiers, forms the foundation of modern feedback amplifier design. It is not possible to mention all who have contributed to the development of op amp, but there are many.

George Philbrick and his company, GAP/R (George A. Philbrick Researches, Inc), introduced the world's first commercially available op amp in January 1952. It is known as K2-W. The K2-W used two 12AX7 dual triodes, with one of the tubes operated as a long tailed pair input stage. The input stage offered fully differential operation. Powered from $\pm 300\,\text{V}$ at $4.5\,\text{mA}$ the op amp achieved $\pm 50\,\text{V}$ signal range at both input and output, not exactly rail to rail operation.
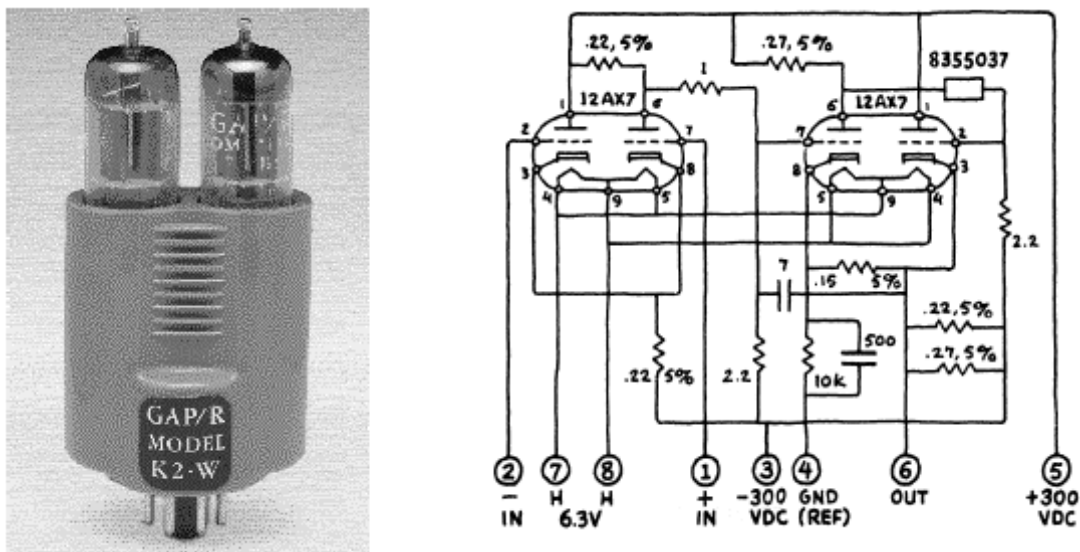
Figure 1.1: Photo and schematic of the K2-W operational amplifier

The vacuum tube based op amps where large and power hungry devices. A decade or two after World War II, vacuum tube op amps began to be replaced by miniaturized solid-state op amps. The μA702 was the first monolithic IC op amp. The μA702 was designed by Robert J. (Bob) Widlar at Fairchild Semiconductor Corporation in 1963. This op amp was far from perfect and had many shortcomings. In 1965 the μA709 was announced. The 709 was the first monolithic circuit that approached discrete design in general performance and usefulness and could be manufactured with high yields in volume production [35]. The 709 had better performance than the 702.

This retrospective glance on the op amp revealed that they were working under other conditions and surroundings than today. The circuit topology were similar to the amplifiers we use today, except from the tubes, which are rarely in use any more.

During the 90's, and at present, the technological trend is towards very large scale integrated (VLSI) low voltage and high speed circuits for portable equipment and wireless communication systems [32]. The trend towards low voltage operation tries to ensure compatibility with digital technology, and to meet the needs of battery-operated equipment [32]. Fig 1.2 illustrates the enormous increase in transistor count in Intel® Microprocessor for the last 33 years (2004).

Thus, the modern op amp has to cope with the reduced supply voltage as it's main limitation. As power is concerned, analog circuitry is usually only a small fraction of a VLSI system, additional area or power dissipation can be afforded, if this is the price to pay for operation with lower supply voltages [6]

A great deal of the work in this thesis is inspired by Huijsing, Hogervorst, De Langen and Eschauzier for their work on low voltage input/output stages and frequency compensation of low voltage op amps. Also the work by Seevinck and Wiegerink on class AB output stages, has been most useful.

Microprocessor	Year of Introduction	Transistors
4004	1971	2,300
8008	1972	2,500
8080	1974	4,500
8086	1978	29,000
Intel286	1982	134,000
Intel386™ processor	1985	275,000
Intel486™ processor	1989	1,200,000
Intel® Pentium® processor	1993	3,100,000
Intel® Pentium® II processor	1997	7,500,000
Intel® Pentium® III processor	1999	9,500,000
Intel® Pentium® 4 processor	2000	42,000,000
Intel® Itanium® processor	2001	25,000,000
Intel® Itanium® 2 processor	2003	220,000,000
Intel® Itanium® 2 processor (9MB cache)	2004	592,000,000

Figure 1.2: Intel® Microprocessor Transistor Count Chart 2004.

Chapter 2

Power consumption in digital and analog CMOS

2.1 Power consumption in digital CMOS

The task of estimating the power of a large digital circuit is fairly complex. Some fundamental understanding of the basic mechanisms contributing to the power consumption will nevertheless gain some insight on how to model these mechanisms. There are three major components of power dissipation i complementary metal-oxide-semiconductor circuits[30]:

1. *Switching(Dynamic)Power*: Power consumed by the circuit node capacitances during transistor switching.

2. *Short circuit power*: Power consumed because of the current flowing from power supply to ground during transistor switching.

3. *Static power*: Power consumed due to leakage and static currents while the circuit is in stable state.

The first two is referred to as dynamic power, which constitutes the majority of the total power in CMOS VLSI circuits since the third component usually is negligible in a well designed CMOS circuit [29]. The total power consumed in digital CMOS is given by [29, 30]:

$$P_{total} = P_{dynamic} + P_{shortcircuit} + P_{static}$$
$$= V_{DD}f_{clk}\sum_{i}^{allnodes}(V_{iswing}C_{iload}\alpha_i) + V_{DD}\sum_{i}^{allnodes}I_{ishort} + V_{DD}I_l \qquad (2.1)$$

Where V_{DD} is the power supply voltage, V_{swing} is the voltage swing at node i (Ideally equal to V_{DD}), C_{load} is the load capacitance at node i, αi is the switching activity factor at node i and I_{short} and I_l are the short circuit and leakage currents. Reducing any of these components will give lower power consumption, although it is of equal importance to increase the system clock frequency for faster operation.

4

As we can see from equation 2.1, when the V_{swing} is equal to V_{DD}, which it is in conventional CMOS gates [6], we have the $P \propto V^2$ relation and therefore it is beneficial to scale the power supply voltage from a power point of view. The scaling of V_{DD} is beneficial from a power point of view, but not on the delay of the circuit. Lowering the supply voltage reduces the power but at the expense of the speed. The Power delay product (not discussed in detail here) helps the designer to make a trade off between the delay and the power. The power delay product is a useful measure when sizing transistors for minimizing the power consumption of a circuit under delay constraint. In order to keep the same computing capacity under reduced voltage, we need more parallelism to compensate for the reduced speed [22].

2.2 Power consumption in analog CMOS

Unlike digital circuits, most conventional analog circuits operate in Class A. (Nonzero static or quiescent currents). This means that all transistors connected between V_{ss} and V_{DD} must be on at the same time [6]. The power consumed in analog signal processing circuits is to maintain the signal energy above the fundamental thermal noise in order to achieve the required signal-to-noise ratio (SNR) [8, 34]. This condition can be expressed as a minimum power per functional pole: $P_{min} = 8fkTS/N$, where f is the signal frequency bandwidth [34]. To clarify this let's consider a basic integrator with an ideal 100% current efficient transconductor described by Enz and Vittoz(1996) in figure 2.1. All current drawn from the power supply is used to charge the integrating capacitor.

(a) 100% current efficient transconductor

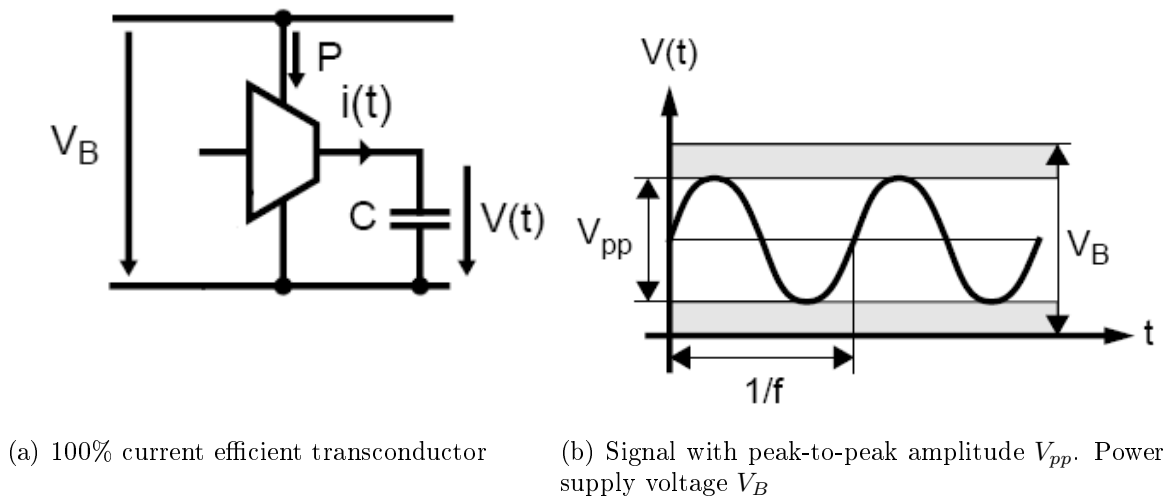(b) Signal with peak-to-peak amplitude V_{pp}. Power supply voltage V_B

Figure 2.1: Basic integrator used to evaluate the power necessary to realize a single pole [8]

.

The power to create the sinusoidal voltage across the capacitor can be expressed as:

$$P = V_B \cdot fCV_{PP} = fCV_{PP}^2 \cdot \frac{V_B}{V_{PP}} \tag{2.2}$$

The signal to noise ratio is given by:

$$SNR = \frac{V_{PP}^2/8}{kT/C} \tag{2.3}$$

Combining 2.2 and 2.3 gives:

$$P = 8kT \cdot f \cdot SNR \cdot \frac{V_B}{V_{PP}} \tag{2.4}$$

As we can see from 2.4 the minimum power consumption of analog circuits at a given temperature is mainly set by the required SNR and bandwidth. To reduce the power consumption further, analog circuits should be able to handle signal that extend from rail to rail. The minimum power for rail to rail circuits when $(V_{PP} = V_B)$ is reduced to:

$$P_{min} = 8kT \cdot f \cdot SNR \tag{2.5}$$

Equation 2.5 neglects the possible limitation of bandwidth B due to the limited transconductance by the active device [8]. The maximum value of B is proportional to g_m/C. Replacing C by g_m/B in 2.3 and represent it as $B \cdot SNR$ yields:

$$B \cdot SNR = \frac{V_{PP}^2 \cdot g_m}{8kT} \tag{2.6}$$

The transconductance of a MOS transistor operating in the active region can be given by

$$g_m = \frac{2I_D}{V_P} \tag{2.7}$$

Scaling down the supply voltage V_B by a factor K requires a proportional reduction of the signal swing V_{PP}. Maintaining the bandwidth and SNR is therefor only possible if the transconductance is increased by a factor K^2. In equation 2.1 V_P is the saturation voltage of the MOS device biased in strong inversion. This voltage has to be reduced proportionally to the supply voltage V_B. If V_P is reduced by factor K we only need to increase the current by factor K so that the g_m is increased by K^2, and hence the power is unchanged.

From this we can conclude that if we want to maintain the SNR and bandwidth, decreasing the supply voltage does unfortunately not reduce the power consumption of analog circuits. The situation is often at the contrary, the power of low voltage op amps will increase because more elaborate and complex circuit topologies are needed to remedy the disadvantages the reduced supply voltage causes.

It should be mentioned that rail-to-rail output stages can utilize the full supply voltage range except for two small saturation voltages near each rail [15, 19]. This entails a power penalty factor above the power dissipation bounds by: $1 + \frac{2V_{Dsat}}{V_{DD} - 2V_{Dsat}}$ [19].
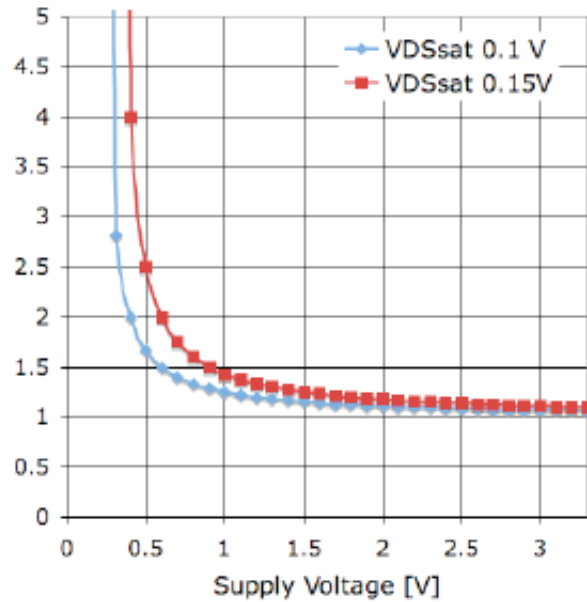

Figure 2.2: Power penalty factor with respect to supply voltage for two different assumptions of V_{Dsat} [19].

This factor also introduces a practical limit on the scaling of the supply voltage on analog circuits unless device or circuit solutions can be found to overcome the saturation voltage limitations [19].

2.2.1 The effect of process scaling on power consumption in analog CMOS circuit

As reported by [1], the minimum power consumption as a function of supply voltage for different process generations: 0.8-,0.5-,0.35-,0.25-,0.18-, and $0.13\,\mu\mathrm{m}$ CMOS, the power consumption slowly decrease down to the $0.25\,\mu\mathrm{m}$, and then increases with newer and smaller processes.
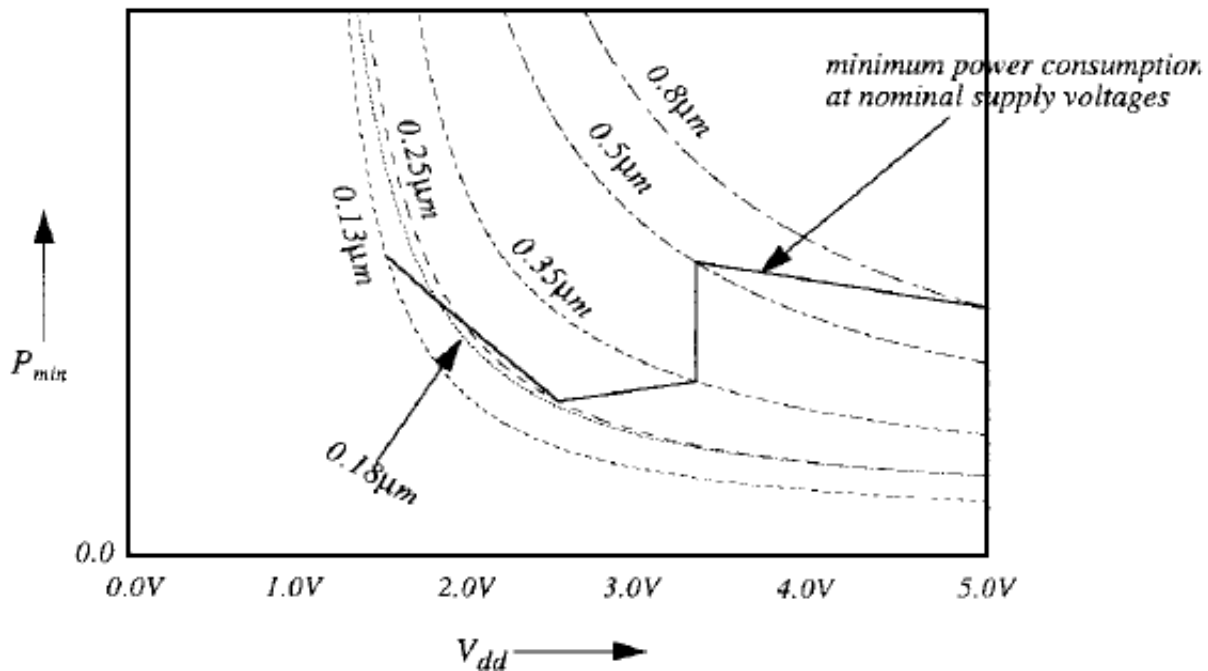
Figure 2.3: Minimum power consumption as a function of V_{dd} for various processes [1].

This article concludes two trends:

- The MOS transistor improves with newer CMOS generations, which tends to decrease power consumption.

- The supply voltage decreases with newer CMOS generations, which tends to significantly increase power consumption.

The overall effect is that power consumption decreases with novel CMOS processes down to circa $0.25\,\mu\mathrm{m}$ depending on specifications and circuit topology. In novel CMOS generations, either circuit performance decreases or power consumption increases significantly. All this is because the improvements of the MOS transistor is overshadowed by the effects of the reduced supply voltage.

One proposed solution is to operate critical analog parts at higher supply voltages; exploiting combinations of thin- and thick-oxide transistors may solve the low voltage as well as the gate leakage problem.

Chapter 3

Low voltage design considerations in analog CMOS

3.1 The gate-source voltage

The gate-source voltage is one of the most important properties of the MOS transistor when concerning low voltage analog design [11]. The gate-source voltage along with the saturation voltage of the transistor determines how many transistors that can be stacked and thereby the suitable supply voltage for the amplifier. These voltages do not scale down in the same manner as the supply voltage nor with reduced feature sizes, and therefore impose a serious problem to common circuits topologies when the supply voltage is scaled down.

The gate-source voltage is usually separated into two parts; the threshold voltage V_t and the voltage above the threshold, $V_{GS} - V_t$. The latter is called the effective gate-source voltage V_{eff} or overdrive voltage Vov. See appendix A.2.2 for further details on threshold voltage and the different operating modes of the MOS transistor. Assuming square-law behavior the effective gate source voltage is

$$V_{eff} = V_{GS} - V_t = \sqrt{\frac{2I_D}{\mu C_{ox}W/L}} \tag{3.1}$$

The overdrive voltage depends directly on the current, but not on the source-body voltage

3.2 Gain stages

Many basic analog building blocks such as switched capacitor filters, algorithmic A/D converters, $\Sigma\Delta$ converters, sample-and-hold amplifiers and pipeline A/D converters, speed and accuracy are determined by settling behavior of op amps [2]. Fast and precise settling is achieved by high unity-gain frequency and high DC-gain, respectively. The most common method to enhance the gain without degrading the high frequency performance, is by cascoding. Since these stages have reduced output swing (by n times the gate overdrive voltages, where n is the number of cascode transistors) [2], and are not suitable for low

voltage operation (< 1.5) [36], a cascade of simple stages are needed to obtain comparable gain to that of cascoded stages. Common-source stages are preferred for maximum gain and voltage swing. Cascaded gain stages have the drawback of more complicated frequency compensation because compensation has to be done over several gain stages. Also, the frequency compensation have to be power efficient.

The lowest supply voltage can be obtained by biasing the transistors in weak inversion. This gives the smallest gate source voltage, but at the expense of bandwidth and slew rate. High bandwidth and high slew rate circuits require transistors biased in strong inversion, this raises the gate source voltage and thereby also raise the minimum supply voltage.

3.3 Classification of low voltage circuits

The classification of low voltage circuits is determined by the number of stacked gate and saturation voltages [11]. The term low voltage is used for circuits that are able to operate at a supply voltage of two stacked gate-source voltages and two saturation voltages, expressed like this:

$$V_{sup,min} = 2(V_{GS} + V_{Dsat}) \tag{3.2}$$

We also have circuits that only need a minimum supply voltage of one gate source voltage and one saturation voltage. Such circuits is referred to as extremely or ultimate low voltage circuits. This is expressed by

$$V_{sup,min} = V_{GS} + V_{Dsat} \tag{3.3}$$

As we can see from equation 3.3, the ultimate low-voltage circuits need a supply voltage which is about half the supply voltage for low voltage circuits.

Chapter 4

Input stages

The purpose of the input stage of an op amp is to sense and amplify the differential signal and to reject common-mode voltage input voltages [15, 11]. A large portion of the rail-to-rail range should be available for common-mode signals. Other important specifications of the input stage are the input referred noise, offset and the common-mode voltage [11].

4.1   Single differential input stage, resistive load
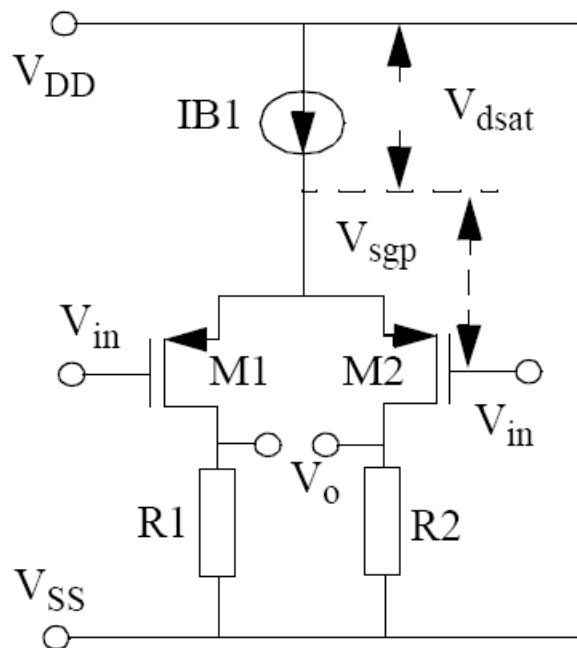
Figure 4.1: Single differential pair with resistive load.

The gain of a single differential stage with resistive load can be given by

$$A_{dm} = \frac{-2I_D R_D}{V_{GS} - V_t} \tag{4.1}$$

Equation 4.1 shows that the $I_D R_D$ product must be increased to increase the gain with constant overdrive voltage. As a result, a large power supply is usually required for large gain, and large resistance is usually required to limit the power dissipation.

If the supply voltage is only slightly larger than the voltage drop over the resistors, the common-mode range, where the transistors operate in the active region, is drastically limited [10].

Due to bad matching of resistors in CMOS processes and place limitations the silicon die, resistive load is not an appropriate choice, neither from the low voltage and low power point of view.

4.2 Single differential input stage, current mirror as active load

To provide large gain without large supply voltages or large resistors, the r_o of a transistor can be used as load. This is called active load since the load element is a transistor instead of a resistor. Active loaded differential pairs is often used in practical amplifiers. The load consists of a current mirror, providing a differential to single-ended conversion. The common-mode range of current mirror loaded differential pairs is also limited. This is because the source of transistor M1 can only reach the negative power-rail within one gate-source voltage. When the common-mode voltage is decreased, the current mirror will eventually push M1 out of saturation [11]. In order to minimize noise and offset, the overdrive voltage of current mirrors is often increased, with the result of further reduction of the common-mode range. For this reason current mirrors is not a good choice as load in differential pairs.
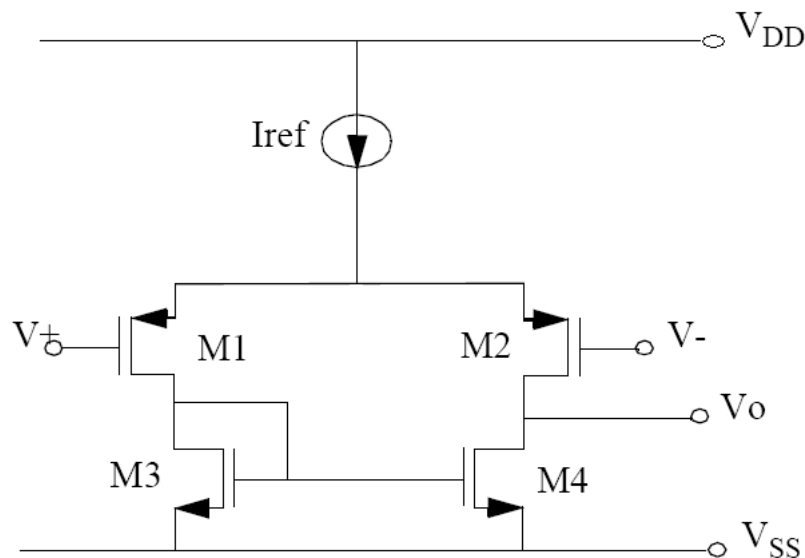
Figure 4.2: Single differential pair with resistive load.

4.2.1 Folded cascoded input stage

Folded cascode input stages overcomes the aforementioned problem with reduced common-mode range, though it just include one of the rails by one saturation voltage.

From figure 4.3 we can see that both input transistors can reach the negative rail within one saturation voltage of the current sources M_9 and $M_1 0$. This saturation voltage
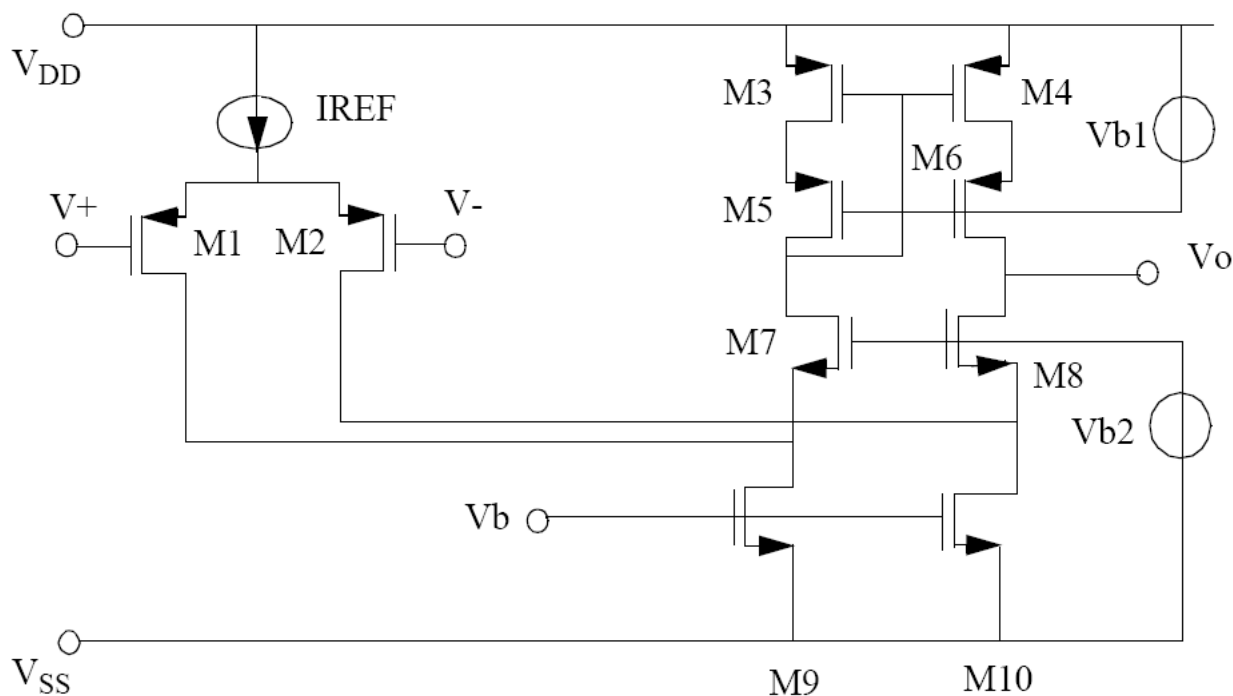
Figure 4.3: Folded cascode input stage

is generally much smaller than the gate-source voltage, so this stage can (allmost) include the negative rail in the common-mode range.

4.3 common-mode range of single differential pairs

We will now take a closer look at the common-mode input rang of single differential pairs.
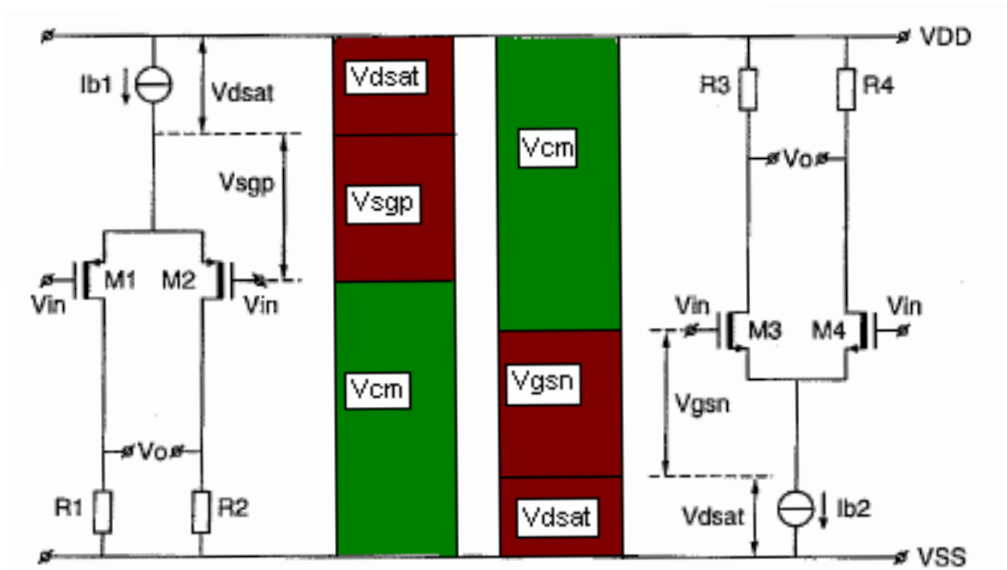
Figure 4.4: common-mode range of P-MOS and N-MOS differential pair

From fig 4.4 we can express the common-mode input range of the P-channel input

13

pair as in equations 4.2 and 4.3 [15].

$$-V_{GS} + V_{Dsat} + V_{R1,2} + V_{ss} < V_{CM} < V_{DD} - V_{GS} - V_{Dsat} \qquad (4.2)$$

The common-mode range of the N-channel input pair is given by

$$V_{ss} + V_{GS} + V_{Dsat} < V_{CM} < V_{DD} + V_{GS} - V_{Dsat} - V_{R3,4} \qquad (4.3)$$

The CM range of the P-pair may downwards exceed the negative rail by $-V_{GS} + V_{Dsat} + V_{R1,2}$, and the CM range of the N-pair may upwards exceed the positive rail by $V_{GS} - V_{Dsat} - V_{R3,4}$. These stages are individually able to reach one of the supply rails.

4.4 Rail-to-Rail input stages

To obtain good SNR, it is important that the output of op amps are able to operate from rail-to-rail. So why do we need input stages with the same capability? Rail to rail input stages are not necessary in all amplifier configurations, but if the amplifier is connected as a voltage follower, the signal range at the input is as large as the signal itself.

Configuration	Input common-mode voltage swing
Inverting	$\cong 0$
Non-inverting	$V_{supply}R_1/(R_1 + R_2)$
Voltage follower	Rail-to-rail

Table 4.1: CM voltage swing in different configurations [36]

.

To make the op amp work under any configuration, an input stage which is capable of handle signals that extend from tail-to rail is needed.

As the previous section reveals, one possible solution to obtain rail-to-rail capability, is to place the N-channel and the P-channel input pair in parallel. There are then three different modes of operations that can be distinguished [6]:

- The common-mode input voltage is somewhat lower than the intermediate range or near the negative rail; signal transfer will only take place in the P-type differential pair. The drain voltage of the P-pair should be kept close to the ground voltage.

- The common-mode input voltage is in the intermediate range, both the N- and P-type differential pair will be active.

- The common-mode input voltage is above the intermediate range, near the positive supply rail; signal transfer will only take place in the N-type differential pair.

A simple input stage like this have some drawbacks; the transconductance changes from the sum of both pairs in the intermediate range to one pair only, when the input common-mode voltage is near one of the rails. This impedes an optimal frequency compensation of the amplifier [36, 11, 15, 12].

Because of the different offset voltage between the P and N pair, the input referred offset voltage will also change with the common-mode input voltage swing [12, 15]. The change of offset voltage will degrade the common-mode rejection ratio of the input stage [15, 10].

The low voltage capability of the complementary input stage is also limited. If the supply voltage is reduced, it will result in a dead zone in the intermediate common-mode range, where non of the input pairs are working and the stage is not completely from rail-to-rail. The supply voltage has to be at least $V_{sup,min} = V_{sgp} + V_{gsn} + 2V_{Dsat}$ [11].

4.4.1 gm regulation

To achieve rail-to-rail common-mode input voltage swing, two complementary differential pairs are placed in parallel. The transconductance in such stages varies by a factor of two

Figure 4.5: Rail-to-rail CMOS input stage consisting of complementary input stage

Figure 4.6: Variation of the transconductance versus common-mode input voltage [10].

over the whole common-mode input range. This variation of the g_m prevents frequency compensation from being optimal since the unity-gain frequency is proportional to g_m [14]. If the op amp is connected in a feedback configuration, the variation of the g_m will also cause the loop gain to vary by a factor of two. This causes an undesired additional distortion [11]. To overcome these drawbacks, the g_m has to be regulated at a constant value over the common-mode range.

By constant sum of roots of tail currents

The transconductance of a CMOS transistor can be expressed by $g_m = \sqrt{2\mu C_{ox}\frac{W}{L}I_{tail}}$ If the tail current of the N and P pair are constant, and they are sized to match the condition:$\frac{(\frac{W}{L})_P}{(\frac{W}{L})_N} = \frac{\mu_n}{\mu_p}$, then the transconductance of the transistors will equal:$\sqrt{\beta_N I_{tail}} = \sqrt{\beta_P I_{tail}} = \sqrt{\beta I_{tail}}$. When both pairs are active, the transconductance of the N and P pair will be added, and the total transconductance will be twice to that of one pair.
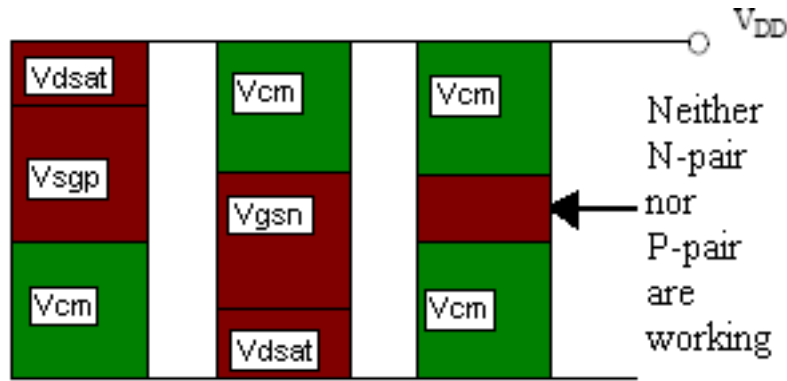
Figure 4.7: Dead zone in the CM range when supply voltage is smaller than $V_{sup,min}$

$g_{mtot} = 2\sqrt{\beta I_{tail}}$. This can also be written $g_{mtot} = \sqrt{\beta 4 I_{tail}}$. This increase in tail current can be done with three-times current mirrors [12].
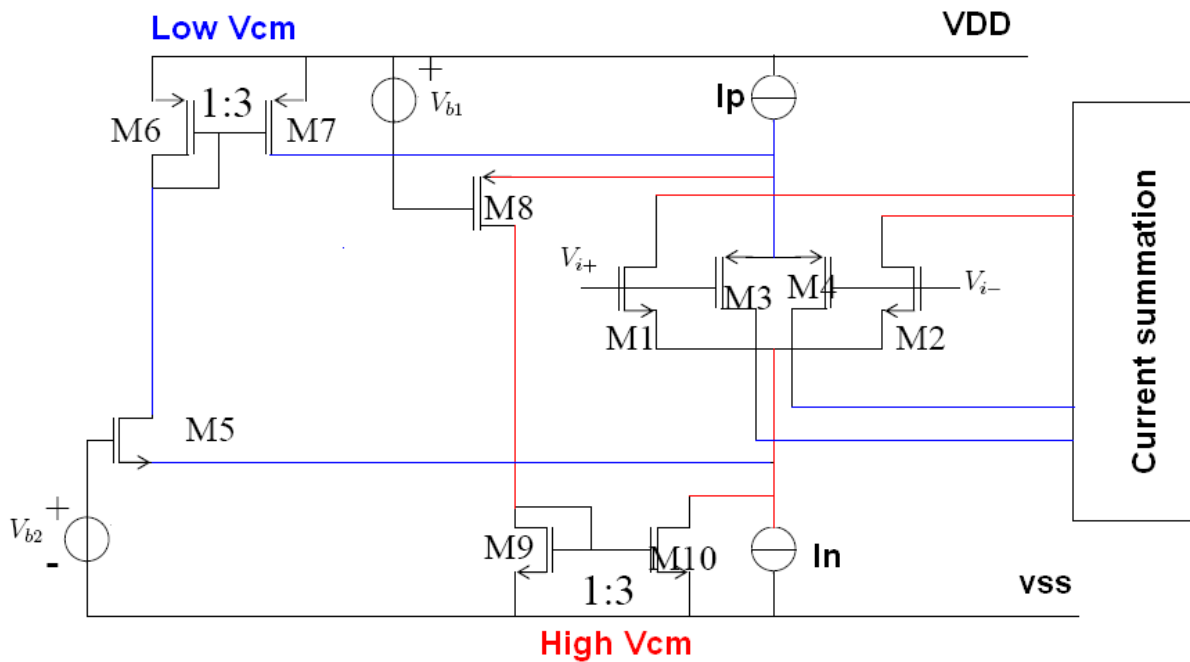

Figure 4.8: gm regulation with three-times current mirrors

As mentioned before, there are three different modes of common-mode input ranges; low, intermediate and high range. If low common-mode input voltage are applied, only the P-channel input pair operates. See figure 4.8. Transistor M8 is not conducting while M5 is conducting. Since the N-pair is not operating, current I_n is drawn through M5 and scaled by a factor of three in the current mirror M6-M7. This current is added to I_p at the drain of M7. Since $I_p = I_n = I_{tail}$ the result is that the tail-current of the P-channel input equals $4I_{tail}$.

If intermediate common-mode input voltages are applied, the P-channel as well as the N-channel are operating. Now both current switches (M5 and M8) are off. The tail current of both the N and P pair are now equal to I_{tail}.

When high input common-mode voltages are applied, transistor M8 is conducting while M5 is not. Since the P pair is not conducting, I_p is drawn through M8 and scaled by a factor of three in the current mirror M9-M10. At the drain of M10, this current is added to I_n which entails that the tail current in the active N-pair is $4I_{tail}$. In this manner the transconductance is regulated to about $2g_m$ over the whole common-mode input range, see fig 4.9
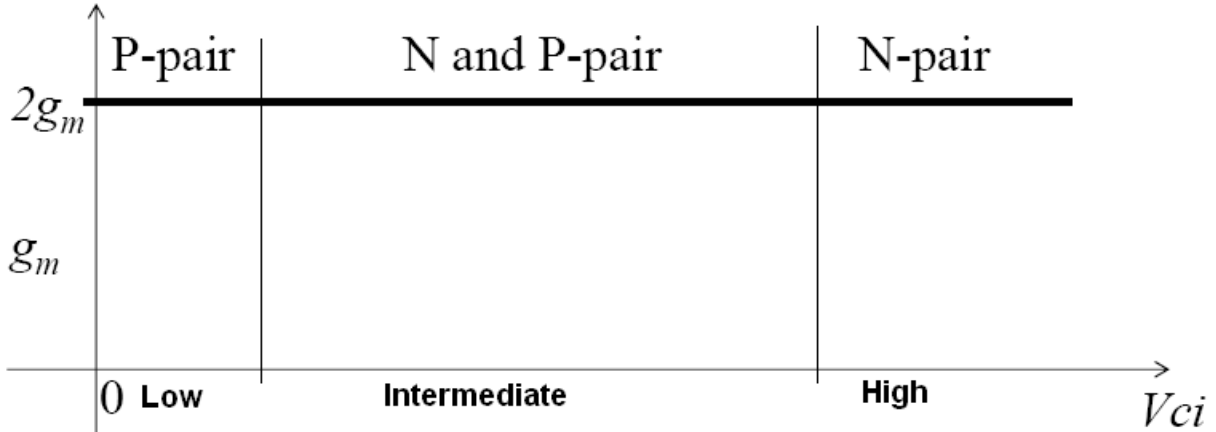

Figure 4.9: gm is stabilized over the entire common-mode input range

Some variations in the μ_n over μ_p ratio and in the normalized oxide capacitance due to process variations are to be expected and thereby some variations in the transconductance.

In the take over regions, where one of the current switches gradually steers the tail-current from one input par to the other, the g_m varies with 15%.

At low supply voltages we have to avoid the two three-times current mirrors being active at the same time. Otherwise a large current is generated by positive feedback [12, 15]. This can be avoided by preventing that the gate voltage V_{G8} becomes lower than $VG5$ at low supply voltages by using a clipping circuit, like it is done in article [12].

By constant sum of V_{gs}

In strong inversion the g_m of a MOS transistor is proportional to its gate source voltage. The g_m of a rail to rail input stage can therefore also be made constant by keeping the sum of the gate source voltages of the input transistors constant. To keep the gm constant the gate source voltage of the input devices have to follow equation 4.4 [11]:

$$V_{sgp,eff} + V_{gs,eff} = V_{ref} \tag{4.4}$$

This is done by placing a constant voltage source between the tails of the input pairs. This voltage source is a zener diode realized by two complementary diode connected transistors [13]. In order to obtain a constant g_m the zener is given a zener voltage of

18

$$V_{ref} = V_{TN} - V_{TP} + 2KV_{gs,ref}$$

$$with V_{gs,ref} = \sqrt{\frac{1}{K} I_{ref}} \tag{4.5}$$

V_{TN} and V_{TP} are the threshold of the N and P channel transistors. $V_{GS,ref}$ is the effective gate-source voltage of an input transistor biased at $4I_{ref}$. The K factor is the transconductance factor of the input transistors.

To obtain a zener voltage according to this equation, the W over L ratio of the two diodes is chosen six times larger than those of the input transistors. The input stage will then act similar to an input stage with ideal zener diode [13].

The input common-mode range can be divided into three regions: Low, intermediate and high. In the lower part of the input common-mode range, only the P-channel of the input pairs is operating. The voltage over the two complementary diode connected transistors is lower than the zener voltage and there are therefore no current flowing through these transistors. Since there are no current flowing in the two diodes the tail current in the active input pair is $8I_{ref}$, see figure 4.10. The same happens in the upper part of the common-mode range, except that only the N-pair is active, the tail current is the same, $8I_{ref}$. When the input common-mode voltage is in the intermediate region where both input pairs are operating, the two diodes takes away $6I_{ref}$. Each of the two pairs will then have a tail current with a value of $2Iref$. In the same manner as in the circuit that used three times current mirrors, the tail current is a factor of four larger in the outer common-mode range, than in the intermediate range. The g_m is then (almost) regulated at a factor of $2g_m$ over the common-mode range.

The current through the diodes and thereby the voltage over them changes through the common-mode range. The sum of the gate source voltages will change and again make the g_m change. With such a solution, the g_m of the input stage varies about 28% over the common-mode range. A more precise solution is designed by Hogervorst et al. (1996) [13], which ensures a constant current through the diodes and thereby a constant voltage over them. This solution only shows 8% variation in g_m over the common-mode range.
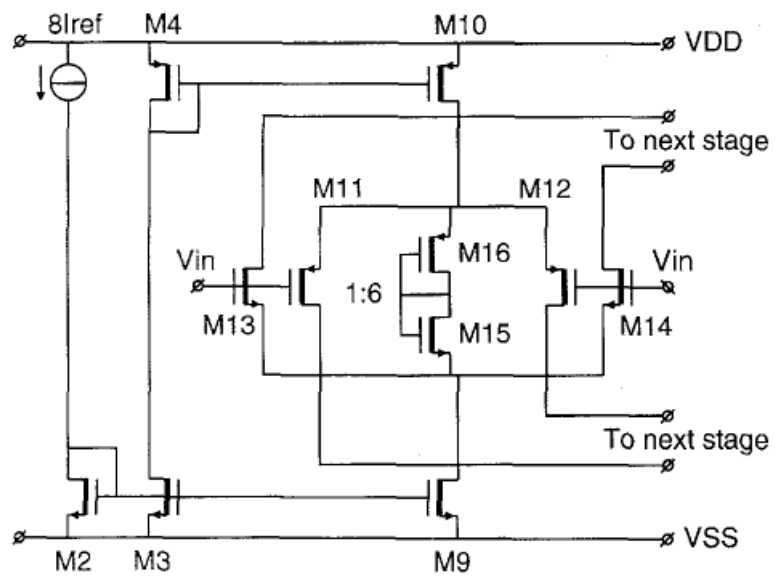
Figure 4.10: gm regulation by constant sum of V_{GS}

Chapter 5

Output stages

The output stage is an important part of the op amp. It must be able to drive the load impedance of the op amp without disturbing the unloaded performance and without introducing unnecessary distortion. The output stage is usually the most power consuming stage of the amplifier. For good power efficiency the maximum peak-to-peak output voltage should be close to rail-to-rail. The output stage should be biased by very small quiescent current and at the same time be capable of driving much larger output currents.

An output stage which combines a rail-to-rail output voltage range and a low quiescent power consumption requires class-AB controlled output transistors in a common source configuration [14]. The class-AB biasing is a bias point between class-A and class-B biasing.

The requirement of high output current with low quiescent current, makes the class-B biasing appropriate. Class-B biasing performs a large output current and approximately zero quiescent current. Class-B rail-to-rail output stage has a power efficiency of about 75% for a rail-to-rail output sine wave. A drawback of class-B biasing is that it introduces a large cross-over distortion. That is when the signal transfer is switching between the push and pull transistor or vice versa. From a power point of view class-B biasing is a good choice.

To minimize the distortion, class-A biasing can be used. The maximum output current is equal to the quiescent current in a class-A biased output stage, and therefore the power efficiency is only 25% for a rail-to-rail output sine wave. This makes the class-A biased output stage undesirable from a power poit of view. A good compromise between power efficiency and cross-over distortion is the class-AB biasing scheme.

Huijsing et al. (1995) [16] states that an efficient class-AB biasing must satisfy:

- High ratio between maximum current I_{max} and the quiescent current I_{quisc} for high efficiency.

- A minimum current that is not much smaller than the quiescent current to obviate HF distortion.

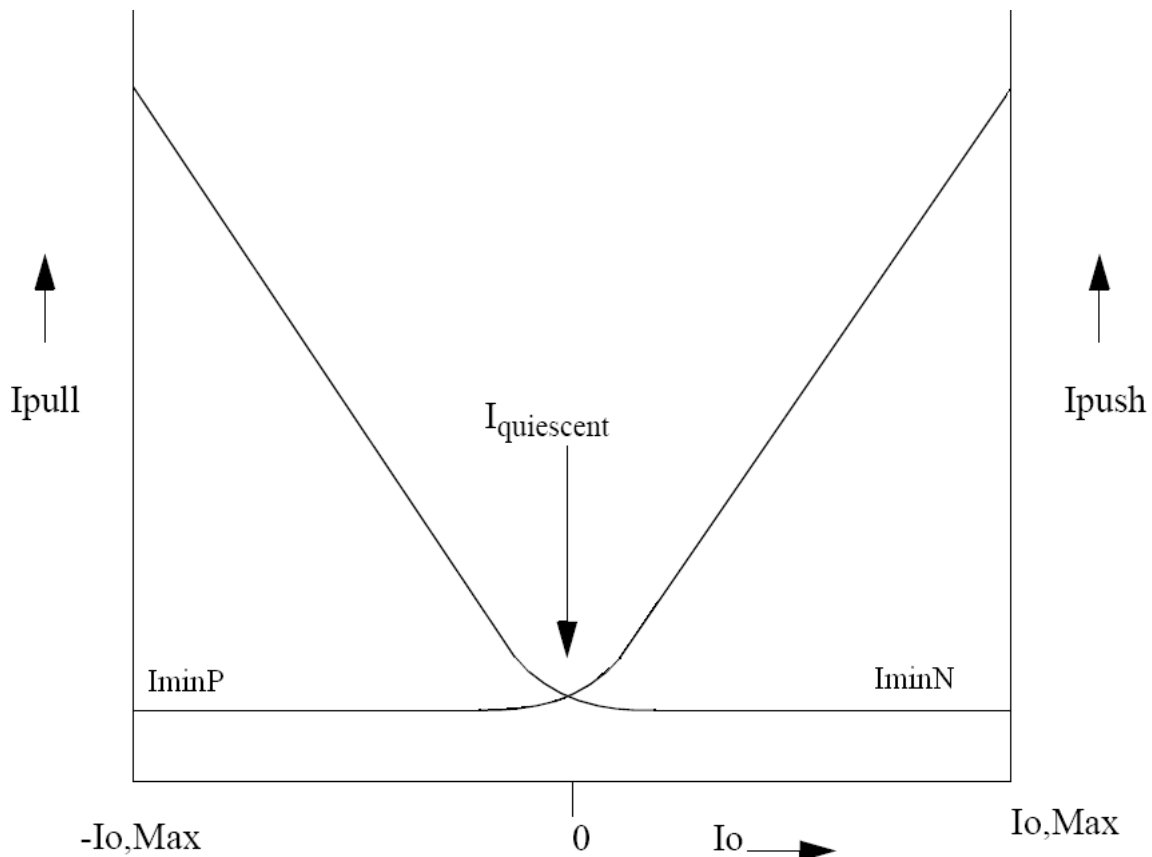- Smooth AB transition to obviate LF distortion(Cross-over distortion).

Figure 5.1: Desired characteristic of the push and pull currents as a function of the output current of a class-AB stage [16].

As we can see from fig 5.1, the maximum output current is much larger than the quiescent current. The transistor which is not delivering the output current, is biased with a small current, I_{min}. This minimum current ensures continuous conduction of both output transistors at the same time, which prevents turn on delay and cross-over distortion [27].

There are two main types of class-AB control circuits used in op amps, the feedforward class-AB control for use in low voltage op amps, and the feedback class-AB control for use in amplifiers that have to run under extremely low voltage conditions.

5.1 Feedforward class-AB control

The term "Feedforward biasing" is used if the biasing is fixed by components in series or in parallel with the signal path [15]. There are some output stages with resistive class-AB controls. These output stages have some drawbacks; the quiescent current in the output-transistors is sensitive to supply voltage variations. The resistors occupy considerable die area. These problems are overcomed by using transistor coupled AB-control instead. Since transistor coupled AB-control is the type used in the the processed op amp, the resistor AB-control is lef out from the theory.

Class-AB biasing of an output stage can be achieved by setting the voltage between
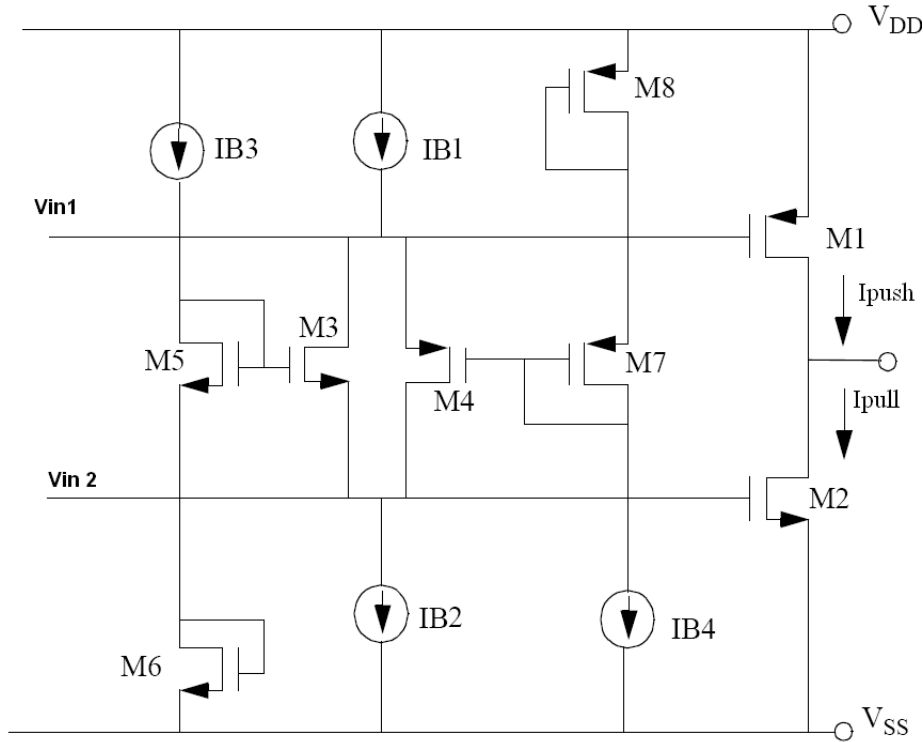
the gates of the output transistors.

Figure 5.2: Rail-to-rail output stage with transistor coupled feedforward class-AB control [15]

.

In fig 5.2, each of the output transistors are given a separate translinear loop [28].

1. M1, M8, M7 and M4

2. M2, M6, M5 and M3

These two loops fixes the voltage between the gate of the output transistors. When there is no signal applied to the output stage, the current I_{B1} is equally divided over M3 and M4. To compensate for the body effect, M5-M3, M7 and M4 are biased at the same gate source voltage. Then, M2-M6 and M1-M8 will have equal gate source voltage. Let the $(\frac{W}{L})_P$ of the P-channel transistors be three times larger than the $(\frac{W}{L})_N$ of the N-channel transistors to compensate for the mobility difference in order to keep the g_m of the N and P-transistors equal at equal currents. All $(\frac{W}{L})_N$ are equal and all $(\frac{W}{L})_P$ are equal, except for M1 and M2 which are scaled a factor of α larger. If the quiescent current through the translinear loop transistors are chosen to be equal, the following relation between the bias currents are needed: $\frac{1}{2}I_{B1} = \frac{1}{2}I_{B2} = I_{B3} = I_{B4} = I_B$. When we describe the gate-source voltage with $V_{GS} = V_{th} + \sqrt{\frac{2I_D}{\beta}}$ and $\beta = \mu C_{ox}\frac{W}{L}$, the relation between push and pull currents can be expressed by: $(\sqrt{I_{push}} - 2\sqrt{I_{quies}})^2 + (\sqrt{I_{pull}} - 2\sqrt{I_{quies}})^2 = 2I_{quies}$ [15]. In general form it is expressed by equation 5.1 [11].

$$(\sqrt{I_{push}} - \alpha\sqrt{I_{quies}})^2 + (\sqrt{I_{pull}} - \alpha\sqrt{I_{quies}})^2 = 2(\frac{L}{W})_5(\frac{W}{L})_6 I_{quies} \qquad (5.1)$$

In equation 5.1 α is given by:

$$\alpha = 1 + \sqrt{(\frac{W}{L})_6 (\frac{L}{W})_5} \qquad (5.2)$$

The push and pull current obey relation 5.1 until either the push or pull current exceed a value of

$$I_{max} = \alpha^2 I_{quies} \qquad (5.3)$$

The output transistor who is not delivering the largest current to the output, will not be completely cut off but regulated at a minimum value of

$$I_{min} = (\alpha - \sqrt{2}(\alpha - 1))^2 I_{quies} \qquad (5.4)$$

With the aforementioned transistor size relations α becomes 2. $I_{quies} = 2I_B$ and $I_{min} = (2 - \sqrt{2})^2 I_{quies} = 0.34 I_{quies}$ at a max current of $I_{max} = 4I_{quies}$. If one of the push or pull currents becomes four times larger than the quiescent current the other becomes 0.34 times the quiescent current. At this value the full bias current of $I_{B1} = I_{B2}$ flows through one of the transistors M3 or M4, while the other is cut off. The smallest of the push or pull currents will not become any smaller and stays at $0.34I_{quies}$ while the largest one is allowed to increase far above $4I_{quies}$.

A drawback of this class-AB control is that the quiescent current of the output transistors depends on supply voltage variations. The supply voltage variations are directly put, by the gate-source voltage of the output transistors, across the finite output impedances of the floating class-AB transistors. The result is a power supply dependent variation of the quiescent current [12].

The output stage needs two stacked gate-source voltages and one saturation voltage as a minimum supply voltage.

5.2 Feedback class-AB control

The feedback class-AB control is different from the feedforward class-AB control in that it does not directly control the current of the output transistors. The push and pull output currents are measured and compared with a bias reference and then regulated in a class-AB way. If the biasing is not correct in a class-AB relation, the output transistors receive a correction signal by a feedback signal.

Here, three somewhat similar feedback class-AB output stages are presented. Each of them used in practical realizations of op amps. First a straightforward implementation of a feedback class-AB controlled output stage is presented. This output stage is used in the article by Hogervorst et al.(1992) [14].
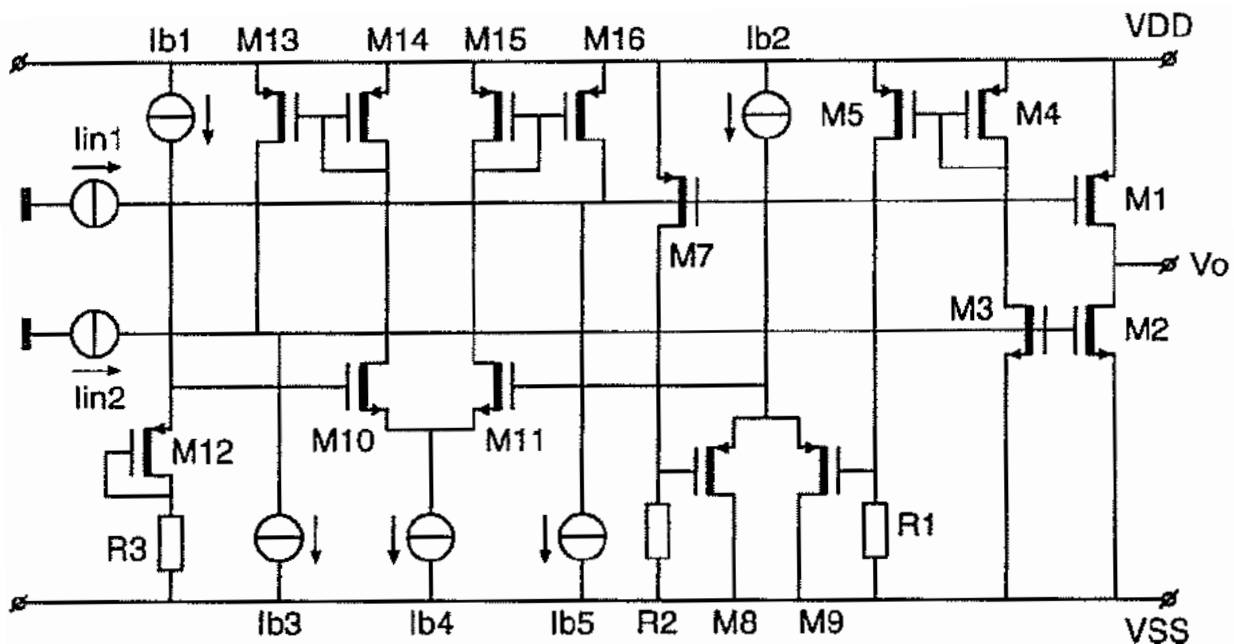

Figure 5.3: Feedback class-AB rail to rail output stage [11]
.

The current in the output transistors are measured by M3 and M7. The measured current are converted to a voltage in the resistors R1 and R2. The voltage over R1 represents the current through output transistor M2. The voltage over R2 represents the current trough transistor M1. In quiescent state, the current in the output transistors are equal, and thereby the voltage over R1 and R2. M8 and M9 are then biased equally which entails the tail current to be split equally between them. M8 and M9 are called the decision pair, and the common source voltage of this pair represents the quiescent current in the output transistors. This common source voltage is compared by the control amplifier M10 and M11, with a reference voltage created by R3, M12 and I_{b1}. If there is a difference between the two voltages, the control amplifier feed a correction signal to the gates of the output transistors. The quiescent current in the output stage is now set.

To make the output stage insensitive to process and temperature variations, R3 has to match R2 and R1, $I_{b1} = \frac{1}{2}I_{b2}$ and $(\frac{W}{L})_{12}$ should be half the W over L ratio of M8 or M9. Under these conditions, the quiescent current is given by

$$I_q = \frac{(\frac{W}{L})_1}{(\frac{W}{L})_7}\frac{R_3}{R_2}I_{b1} \tag{5.5}$$

The current in the the output transistor which is not delivering current to the output node, is regulated to a minimum value in the following manner: Suppose M1 is pushing a large current to the output node. The voltage over R2 will then be much larger than the voltage over R1. Transistor M8 in the decision pair is in cut off and the tail current flows only through M9. The common source voltage of the decision pair is now only due to the voltage over R1, which represents the current in the output transistor M2. The common-source voltage of the decision pair is checked with the reference voltage and a correction signal is sent to the output transistors by the control amplifier if a difference is present. In this way the current in M2 is regulated to a fixed minimum value I_{min}. The same happens if M2 pulls a large current from the output node. The current in M1 will be regulated to the same minimum value. The minimum current of the output transistors is given by Hogervorst and Huijsing (1996)[11]:

$$I_{min} = I_q - (\sqrt{2} - 1)\frac{(\frac{W}{L})_1}{(\frac{W}{L})_7}\frac{V_{gs12,eff}}{R_2} \tag{5.6}$$

This output stage requires a supply voltage of minimum one gate-source voltage and one saturation voltage. A disadvantage of this output stage is the bad matching between the PMOS gate-source voltage of the decision pair and the gate source-voltage of the NMOS control amplifier. This circuit is therefore unreliable at very low supply voltages [5]. As we can see from equation 5.6 the current I_{min} depends on process parameters and the absolute value of R_2, which makes it impossible to be controlled exactly.

The next output stage, used in the article by Eschauzier et al (1994) [9], is rather similar to the previous one except that the current in the output transistors is now converted to a voltage over folded diode-coupled transistors, and that the decision pair and the control amplifier are combined
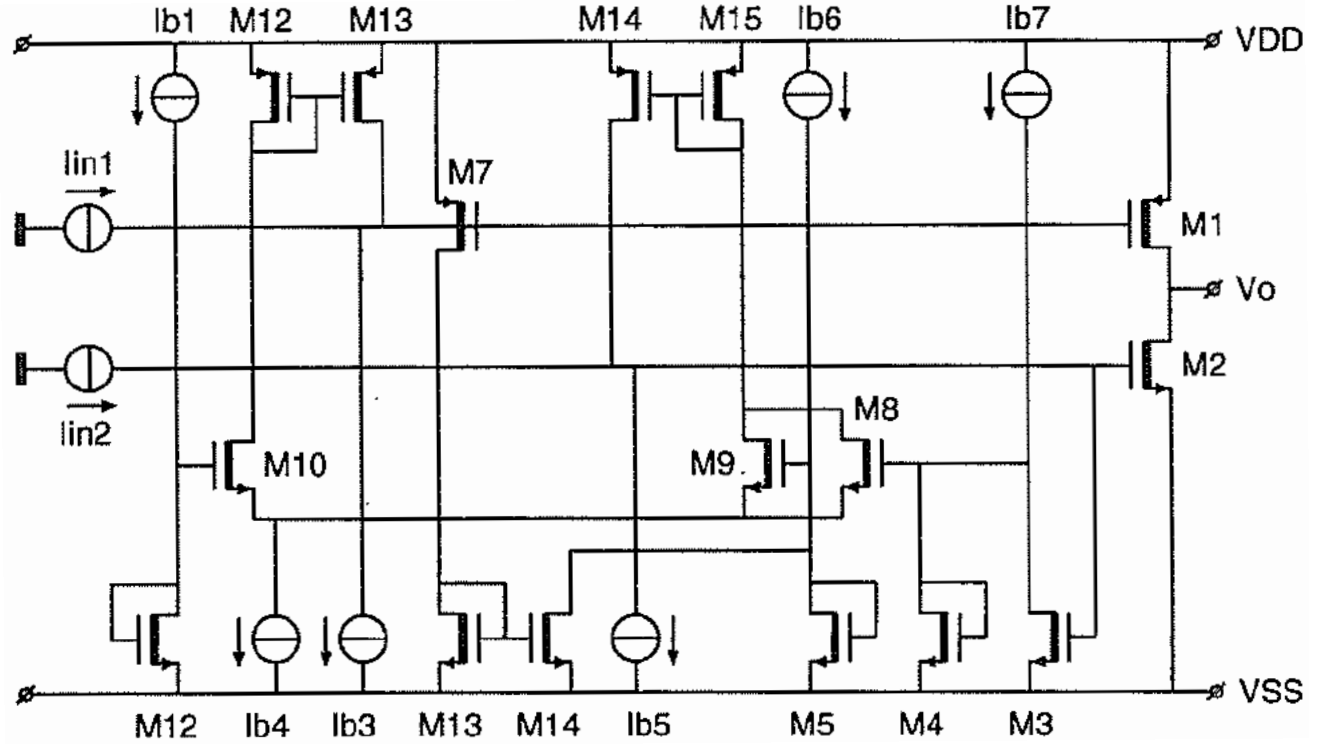

Figure 5.4: Feedback class-AB rail to rail output stage with combined decision pair and control amplifier (M8, M9 and M10). The voltage over M4 and M5 emulates the current in the output transistors [11]

.

The current in the output transistor M1 is measured by M7. The current in M2 is measured by M3. The current in M7 is mirrored to the drain of M5 by the current mirror M13-M14. The current through M4 is the bias current I_{b7} minus the drain current of M3. It is similar for the current through M5, which is the bias current I_{b6} minus the drain current of M14. In this manner the voltage across M4 represents the current through M2, and the voltage across M5 represents the current through M1. Similar to the output stage with resistors, the voltage over M4 and M5 are equal when the stage is in the quiescent state. The current in M1-M2 in quiescent state is regulated by the control amplifier M8-M10 which compares the voltage over M4-M5 with a reference voltage set by I_{b1} and M12.
To make the quiescent current independent of process and temperature variations, the diode M12 has to match the folded diodes M4 and M5, and $(\frac{W}{L})_1 0$ is two times the W over L ratio of M8 or M9, the currents I_{b6} and I_{b7} have to be equal.
The quiescent current is given by:

$$I_q = \frac{(\frac{W}{L})_1}{(\frac{W}{L})_7}(I_{b6} - I_{b1})$$ (5.7)

27

This output stage sets the minimum current in the transistor which is not supplying the current to the output node by shutting off the part of the decision pair representing the output transistor supplying the large current [9]. If M1 is pushing a large current to the output node, the gate-voltage of M9 will be pulled down by M14 and the gate voltage of M8 will therefore be much grater than the gate-voltage of M9. With M9 turned off, the control amplifier (now represented by M8 and M10) regulates the voltage over M4 which emulates the current in M2, which is the transistor not supplying the current to the output node.

In strong inversion, the minimum current of both output transistors are given by equation 5.8 [11]:

$$I_{min} = I_q - \frac{(\frac{W}{L})_1}{(\frac{W}{L})_7} \frac{(\frac{W}{L})_{12}}{(\frac{W}{L})_{10}} (1 - \frac{1}{2}\sqrt{2})^2 (1 + 2\sqrt{\frac{(\frac{W}{L})_{10}}{(\frac{W}{L})_{12}} \frac{I_{b1}}{I_{b4}}}) I_{b4} \qquad (5.8)$$

This output stage also have a minimum supply voltage of one gate-source voltage and one saturation voltage. Like the quiescent current in the output stage with resistors, the quiescent current in this stage is not dependent of process parameters. One drawback of this stage is that it becomes quite complex in practical amplifiers [9], and requires a relatively large amount of bias current.

The last output stage presented here is compact and simple, and do not use resistors. It is used in op amp realizations in the article by De Langen and Huijsing (1998) [5]. It contains a minimum selector, but its manner of operation is a bit different.

Figure 5.5: Feedback class-AB output stage with simple minimum selector.

The way of measuring the currents in the output transistors is much in the same way as the two previous stages. The current in M1 are measured by M11 and the current in M2 are measured by M12. In this circuit, the minimum selector is made by transistors M11, M15 and M17, and the class-AB control amplifier is made by M4 and M6. This control amplifier regulates the signal at the gates of the output transistors so the current in M13 is equal the reference current I_{ref} that also flows through M14.

In the quiescent state, the current in the output transistors, M1 and M2, are equal. The minimum selector is designed in a way that in quiescent state the gate-source voltage is also equal. M15 now operates in the linear region and appends to M11. M15 and M11 can then be considered as one transistor with double length. Transistors M17 and M15 works as a 2:1 current mirror, from M17 to M15. This implies that the current in transistor M17 and M12 is two times larger than in transistor M13. Suppose the scaling between M2-M12 and M1-M11 is equal, the current in quiescent state will now be regulated to $2I_{ref}$, since the current in M13 is regulated to I_{ref}.

The minimum current in the transistor which is not delivering the large output current to the output node, is performed in the following manner: When M1 is supplying the larger current to the output node, the voltage over M15 is large enough to make it work in the saturated region. The minimum selector is now working as a cascoded current mirror and mirrors the current in the measuring transistor M12 into M13. The current mirror M17-M15 do no longer have the 2:1 relation, so the current in the inactive transistor is regulated to the same as through M13, I_{ref}, which is half the quiescent current.

When M2 delivers a large current to the output node, there is also a large current in

M17 and M12. M15 pulls the source of M11 almost to the positive rail, M1 and M11 will now form a current mirror which mirrors the current of output transistor M1 to transistor M13. In this way, the current in M1, the inactive transistor, is regulated to a constant value equal to $Iref$ which is half the quiescent current.

Chapter 6

Rail-to-rail $\mathbf{3.3\,V}$ Operational amplifier designed in $\mathbf{0.35\,\mu m}$ CMOS

6.1 Basic architecture and schematic

The op amp implemented, (Figure 6.1) is based on the one in [12], where it is realized in a $1\,\mu m$ BiCMOS process. The op amp is rail to rail on both input and output. The input stage is g_m regulated with three times current mirrors. The output stage is a feedforward class-AB type. This practical implementation has some extra circuitry to circumvent some of the drawbacks of the elementary input and output stages. The voltage supply dependency of the quiescent current in the output stage is avoided by biasing the current summation circuit by a floating current source with the same circuit topology as the class-AB control. In addition, a "clipping" circuit (M1-M2) is applied that turns off M4 at low supply voltages to prevent a positive feedback loop to be created through the current switches and the three-times current mirrors.

Additional transistors are added: M36 and M39 are added to provide bias current for the PMOS differential pair and the biasing of the NMOS part of the class AB-regulation and floating current source. M40 and M35 provides biasing for the NMOS differential pair and the bias circuit for the PMOS part of the class-AB regulation and the floating current source.
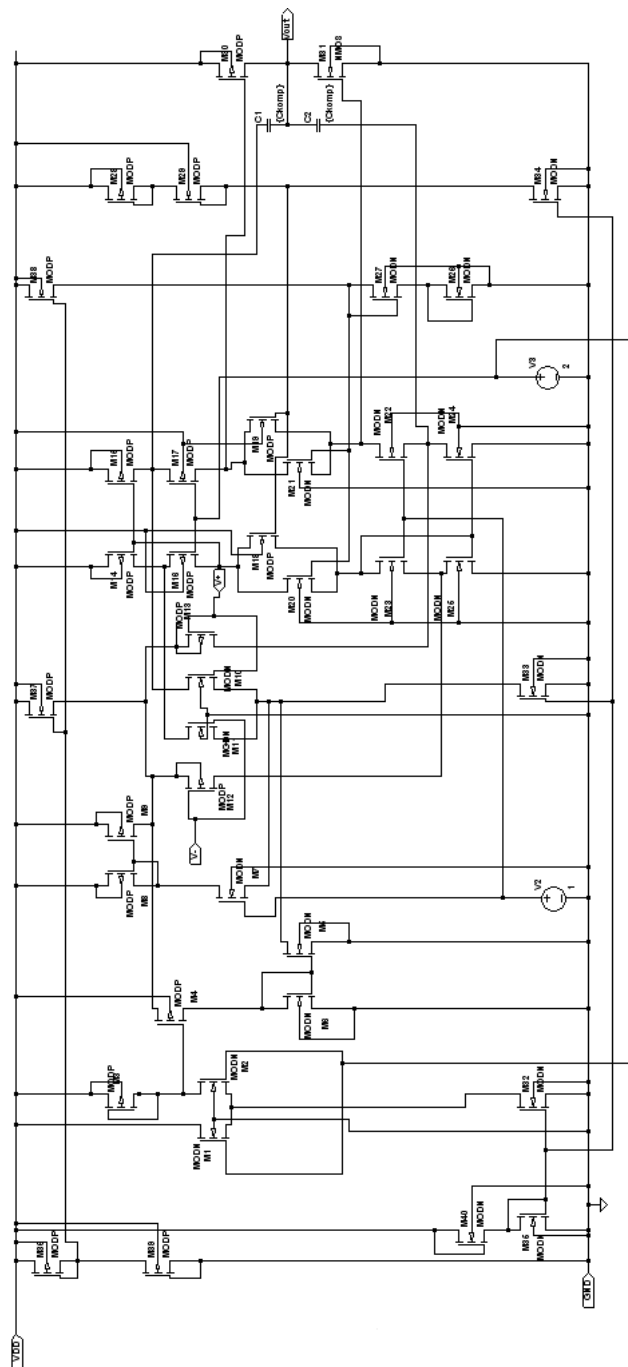
Figure 6.1: Complete operational amplifier. Transistor sizes are listed in Appendix.

6.2 Architecture advantages, challenges and limiting factors

This architecture is compact and power efficient. The frequency compensation technique (Cascoded Miller) increases the gain-bandwidth without increasing the power consumption. The power supply voltage is not critical and the amplifier works from 3.3 V, limited by the process, and down to 2.5 V where DC-gain is unity. This op amp architecture reduces the noise and offset contribution of the class-AB control by shifting it into the current summation circuit.

One drawback of this op amp is that the input stage is complementary which conduces to a change in offset voltage in the transitions from one active input pair to the other. This is because NMOS and PMOS in nature have different offset voltages. In those transitions areas, the common-mode Rejection Ratio (CMRR) is degraded. The CMRR is the ratio between the change in input common-mode voltage and input offset voltage: $\frac{\Delta V_{ic}}{\Delta V_{OS}}$. The offset in the stable areas can be minimized with larger input devices and a careful layout of the input transistors. This behavior by the offset voltage may require external offset compensation, especially if it is used in precision analog to digital converters (ADC).

The supply voltage is limited downwards by the output and input stage. If the power supply voltage is too low, a dead zone in the middle of the common-mode input range will appear. The amplifier will no longer be rail-to-rail, but still work in the upper and lower part of the common-mode range. If the voltage is decreased further, then also the output stage will cease to operate. The output stage needs a minimum supply voltage of two stacked gate source voltages and a saturation voltage, while the input stage needs two stacked gate source voltages and two saturation voltages. The gain-bandwidth can be adjusted by the tail current of the differential pair. An increase in the gain bandwidth will increase the power consumed by the amplifier.

6.3 Simulation and performance

The simulations were done in switcherCAD III from Linear Technology. The transistor models are the BSIM3V3 3.3 V model. Typical mean value of the threshold voltages are: NMOS-0.4979 V and PMOS--0.6915 V.

6.3.1 Offset

In high precision mixed signal systems, the accuracy is depending on the offset voltage of the comparator/op amp [33]. The offset is not fully predictable and causes chip to chip variations. The offset can and should be reduced as much as possible.

Because of the high gain, the offset voltage of an op amp is referred to the input stage. The offset relates to variance in the gain factor β and the threshold voltage V_{th} [11, 10]. The error in gain and threshold voltage is inversely proportional to $\sqrt{WL}$, and can thereby be reduced by increasing the size of the input transistors [33, 18, 20, 21, 23]. The input transistors are increased by a factor five. The simulations will not give us the final answer on how the offset in the final prototype chip will look like, but show some dependencies. The final chip is expected to show larger offset voltage because variations

in the rest of the circuit will also contribute to the total offset voltage.
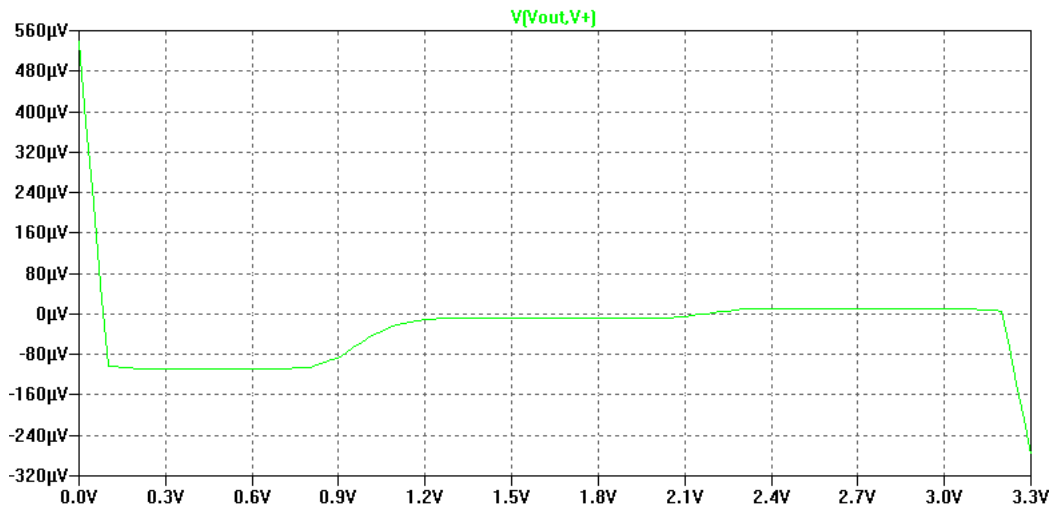

Figure 6.2: Equally sized transistor in the differential pair. common-mode input voltage on the x-axis and offset voltage on the y-axis. The curve shows the input referred offset over the common-mode voltage input range. In the lower common-mode range the offset voltage is $112\,\mu$V
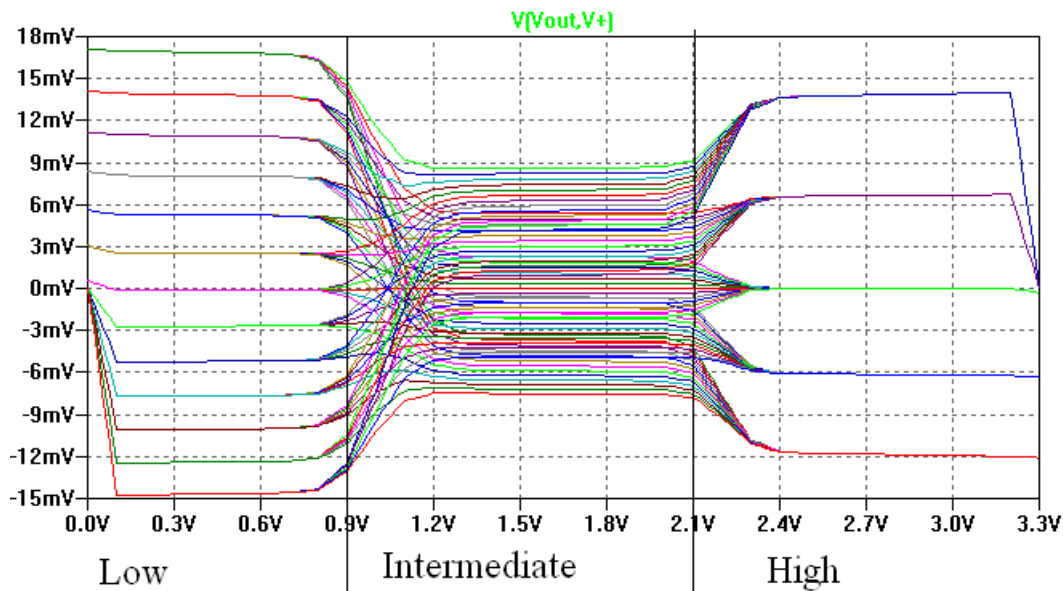

Figure 6.3: $\pm 10\%$ variation of the size of one PMOS and one NMOS transistor in the input stage. The offset voltage is very dependent of transistor size variations in the input stage. common-mode input voltage on the x-axis and offset voltage on the y-axis.

In figure 6.3, a $\pm 10\%$ variation in the width of one of the transistors in each differential pair is shown. We can see that the offset voltag is strongly related to size variations in the input stage. In figure 6.2 the transistors are of equal size and the simulated offset is $112\,\mu$V.

34

There is as far that I can see, now way of setting the threshold voltage of one individual transistor in this Spice simulator. The one I have found that treats parametrization of the threshold voltage is: ".step nmos modn (modp)(VTH0)", but this parametrize the threshold voltage for the model file, and thereby for all NMOS or PMOS transistors in the circuit. The effect of different threshold voltages in the same input channel is then lost. This Spice command can be used to investigate the effect of the different threshold voltages between the complementary input transistors. There are not performed any simulations where individul threshold voltages are varied.

6.3.2 common-mode input range

The common-mode input range is the common input voltage were the op amp is functional. It was fond by sweeping the input of the op amp in follower configuration and see if there were any discontinuity in the output signal. In the figure 6.4 the red graph shows the output voltage and the blue graph shows the intput voltage. The output follows the input from GND $+0.4\,$V and completely to the positive rail.
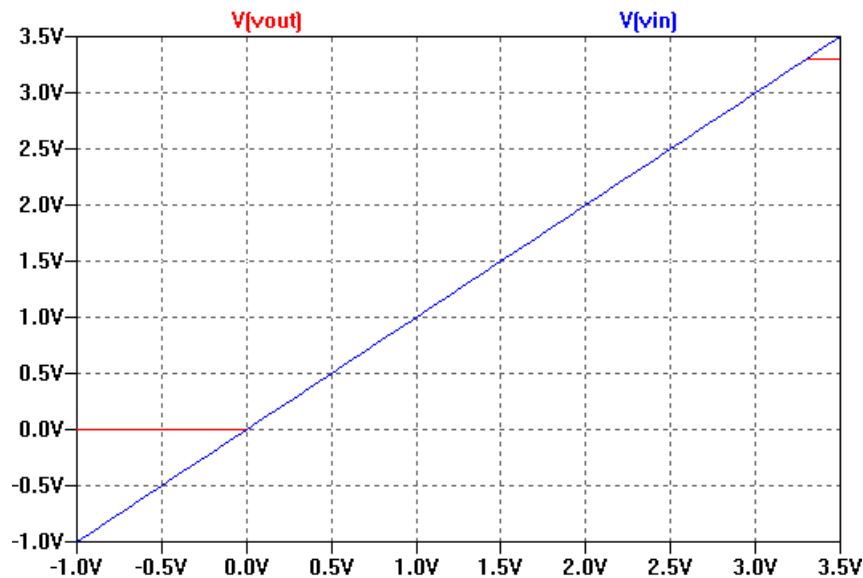
Figure 6.4: common-mode input range

6.3.3 DC-gain

The DC-gain was not dependent on loading but it was very dependent of the supply voltage. The simulated DC gain with 3.3 V supply voltage was 79 dB, see figure 6.5.
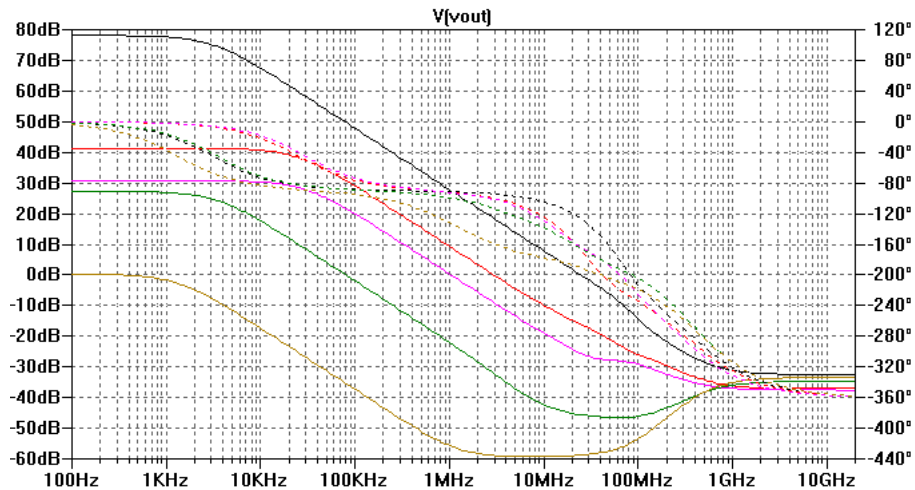

Figure 6.5: The gain is very dependent of the supply voltage. The graph shows the AC response with supply voltage from 3.3-2.5 V. The DC gain is 79 dB
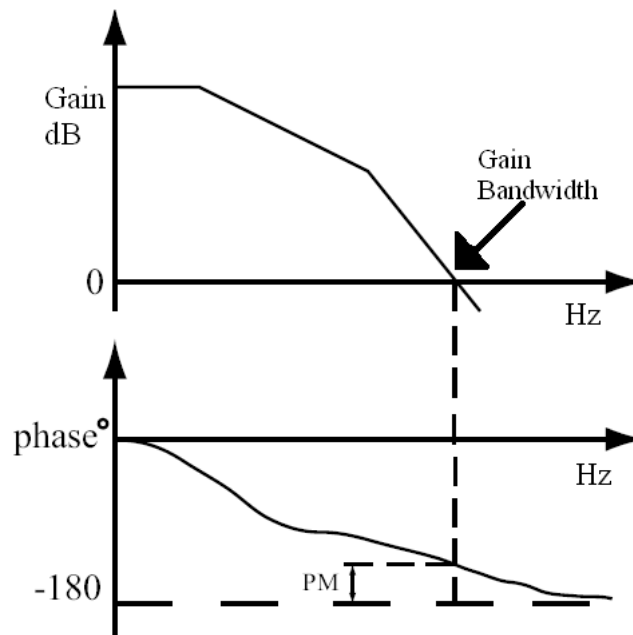
6.3.4 AC response

Figure 6.6: AC respons and phase margin

The gain bandwidth is the product of the open loop gain and its -3 dB point. The gain bandwidth product of an op amp is constant if there is a -6 dB per octave roll off in

the AC response. If the gain bandwidth product of the op amp is 10 MHz, then the gain will fall to unity at 10 MHz.

The phase margin (PM) is the difference between the phase of the op amp at the 0 dB crossover and −180°. It is a good measure for stability of op amps. If the phase of the op amp reaches −180° before the gain drops to unity then we have a loop with positive feedback and a gain larger than one and sustained oscillation will occur. For good stability a phase margin of at least 45° and 60° is preferable.

AC simulations have been done with no load (Figure 6.7) and with a 10 pF capacitor as load (Figure 6.8). The no load simulation showed gain-bandwidth of 24.65 MhZ and phase margin of 55°. The 10 pF capacitive load showed a gain-bandwidth of 14 Mhz and phase margin of 20°.
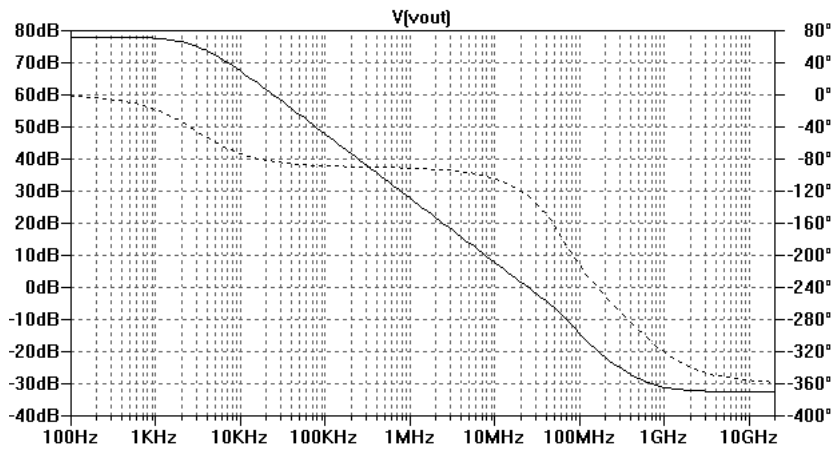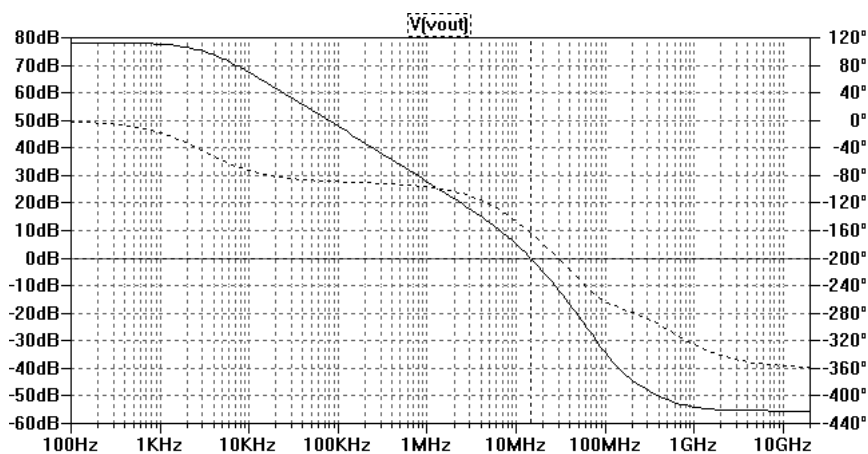

Figure 6.7: AC simulation with no load

Figure 6.8: AC simulation with 10pF load

6.3.5 Power consumption

To simulate the power consumption a resistor at $0.0001\,\Omega$ was added in series with the power supply. This is shown in figure 6.9. The op amp was configured as a follower and the input was swept from rail-to-rail. The current through the resistor was measured and integrated over the entire common-mode range to find the RMS (Root mean square). The RMS of the current, $273.15\,\mu A$, was multiplied with power supply voltage and gave $0.9\,\text{mW}$.
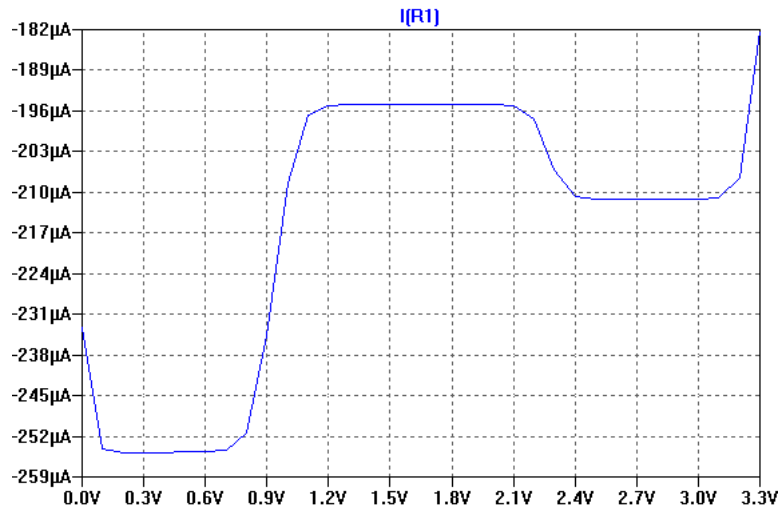

Figure 6.9: Current consumption. The graph shows the current through the $0.0001\,\Omega$ resistor when the common-mode input voltage is swept from rail-to-rail. common-mode input voltage on the x-axis and current consumed by the circuit through the resistor on the y-axis

6.3.6   Noise

The noise of an amplifier is often referred to the input [3]. In CMOS the noise is dominated by flicker (1/f) noise, which is inverse proportional to the current and size of the device. Reducing the noise therefore costs both power and die area. A noise simulation showing the relations mentioned is shown in figure 6.10. When the power supply voltage is reduced, the current through the transistors will also be lowered and thereby increase the noise of the amplifier. The simulated output noise is referred to the input of the op amp by dividing the output noise by the gain. At $10\,\text{kHz}$ the input referred noise was $30\,\text{nV}/\sqrt{\text{Hz}}$.
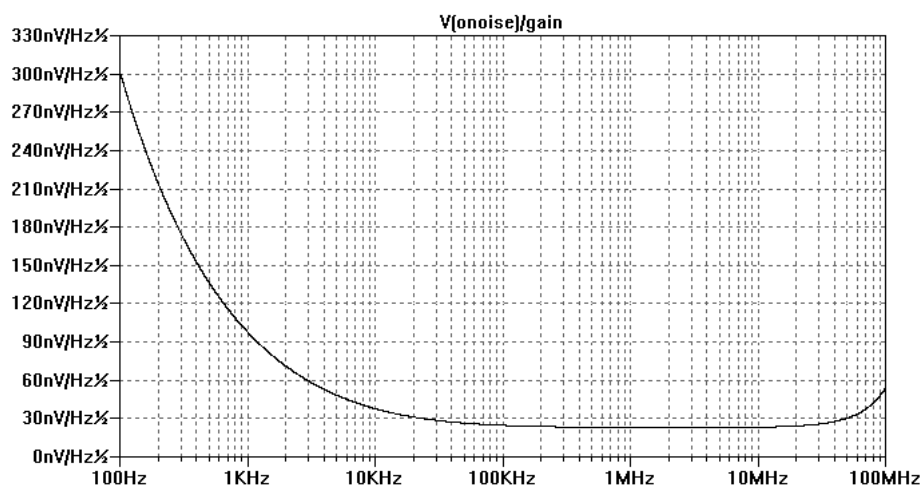

Figure 6.10: The input referred noise, dominated by flicker noise.

6.4 Layout and layout considerations

The layout is produced in Mentor Graphics IC station using design kit Hitkit version 3.70.

6.4.1 Matching

The transistors in analog circuits are usually much wider than in digital circuits were minimum sized transistors often are used. They are therefore not laid out as one wide transistor but with multiple gate fingers [4]. When to transistors have to be matched, both transistors are divided into unit sized transistors and the fingers for one transistor are interdigitaded with the fingers from the other transistor. This method is called *common-centroid layout* [4]. Common-centroid layout helps match error caused by temperature or the gate-oxide thickness changing across the die. For even better matching the interdigited fingers should be inside dummy fingers. The dummy fingers will prevent under etching of the transistor-fingers on the edges of the multiple finger structure.

In this op amp special care has been taken when the differential pair, current-summation circuit and the current mirrors were laid out. They were laid out using the common centroid layout technique. The gate and source of these transistors are in common, which simplifies the routing. The matched pairs should also have dummy structures, but the time did not permit that. Chip layout and pad frame are shown in appendix D.

6.4.2 Noise

The PMOS and NMOS-channel in the input stage are surrounded by individual guard rings. Guard rings are a chain of nwell-contacts for PMOS transistors, and a chain of substrate contacts for the NMOS. Guard rings prevents substrate coupled noise to come out of or into the ring. Guard rings are generally placed around noise sensitive and/or noisy devices. The other NMOS transistors were placed in a common guard ring, so was the same for the other PMOS transistors. Guard rings also prevents latchup. Latchup is forward biased parasitic bipolar transistors which can cause an excessive large current to flow from the positive supply to ground and destroy the circuit.

Chapter 7

Test setup and measurements

It is more complicated to make measurements on a chip then performing PC simulations of the circuit. Noise and disturbances from the "real world" will influence on the measurements.

When op amps are in open loop configuration the gain is very high and only a small portion of noise and offset can cause the op amp to saturate at one of the power supply rails. Methods for measuring open loop gain reported by [24], requires delicate instruments and a complicated calibration procedure of the measurement setup and open loop gain measurements are therefore not considered here. Instead, closed loop configurations are used to evaluate the performance of the op amp.

In the tests, the following instruments where used:

- Kithley 617 Multimeter

- Hewlett-Packard HPE3631 power supply

- Hewlett-Packard HP33120 signal generator

- Hewlett-Packard HP54622 Oscilloscope

Measurements performed:

- Current consumption

- common-mode input range

- Output voltage swing

- Offset voltage over the common-mode range

- Gain bandwidth and phase margin

7.0.3 Test strategy

To test the op amp, the unity gain configuration was used. When gain bandwidth and phase margin were measured, an inverting configuration with a common-mode voltage of 1.65 V was used. The lowest output voltage from the signal generator was $0.1\,\mathrm{V_{p-p}}$ so the gain was set to 30 times which ensured that the amplifier did not saturate.

Initially, the supply voltage was carefully increased from zero while measuring the current drawn by the circuit. No sudden current rush appeared while increasing the supply voltage to the final value, which is a good sign.

To measure the power consumption, the current drawn by the circuit were measured with the Keithley617 multimeter in series with the power supply. The input common-mode range was tested by measuring the output voltage while sweeping the input from 0 to 3.5 V and then detecting the linear area. The output voltage swing was found by keeping the voltage on the inverting input constant(0.5 V) and vary the non-inverting input around the same voltage with no feedback applied. The output will then swing from rail-to-rail without being limited by the input stage. The input referred offset voltage was measured by sweeping the input from rail-to-rail and then measured the difference between the input and output voltage.

The instruments were controlled by scripts in MATLAB via a General Purpose Interface Bus (GBIB) which is a short range digital communications bus. The bus was standardized in 1975 and got the name IEEE-488.

7.0.4 Design of test board

The test board was designed in EAGLE layout editor V4.16r2. The printed circuit board is shown in figure 7.1. The chip contains three different circuits where two of them have been tested: arrays of different X-ray pixels and the compact op amp. Different test setups were therefore required and one test board was designed to enable testing of all three circuits on the same test board.

Some time was spent on defining what contacts should be used to interface the board and to check that all signals where represented on the correct pins and so on. The X-ray arrays were interfaced with Labview and an FPGA. The interface against Labview is a SCSI2 connector and a 40 pin header for ribbon cable were used to interface the FPGA board. The ADC was interfaced with a 40 pin ribbon cable. The board was equipped with a power switch so that only the circuits under testing were connected to the power supply.
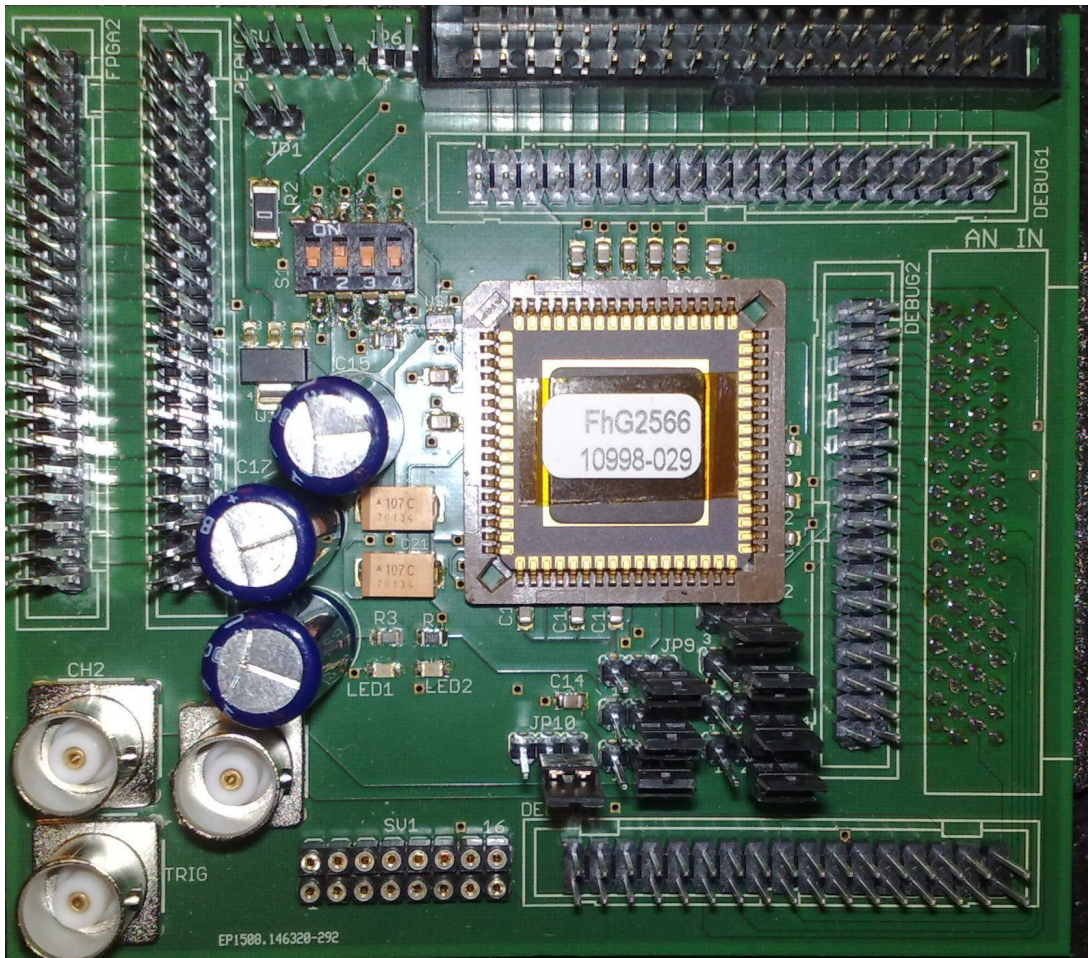
Figure 7.1: The printed circuit board for testing the ASIC

Some noise considerations were taken when designing the board. The digital signals were routed in every other layer so that the coupling between them were reduced. The analog signals were kept away from the digital routing by routing the analog signals in a different layer, or by using distance where it was not possible to route the signals in a different layer. DC signals and power were decoupled by 100 nF ceramic capacitors in close proximity to the application-specific integrated circuits (ASIC) input pins. This will decouple higher noise frequencies superimposed on the DC voltage. The power supply were decoupled by 100 μF capacitors in order to decouple the slower variations in the power supply. The circuit board has four layers, where the two in the middle are 3.3 V and ground, this will also have a capacitive decoupling effect on the power supply. The 5 V power needed by the X-ray circuit, is routed as a signal and decoupled near the ASIC. The ceramic decoupling capacitors were coupled to the ground plane through individual VIAS's in order to reduce the series inductance from the capacitor to the ground plane. See appendix C for schematics of the printed circuit board.

7.0.5   Measurements

Current consumption

First the current consumption was measured. The current in the power wires was measured with Keithley multimeter. At first glance, the current looked too high. There are also some light emitting diodes (LEDs), which indicates whether or not the 3.3 V and 5 V are present. The current in the power wires is the sum of the current drawn by the op amp and the LED. After subtracting the current in the LED from the one in the supply lines the graph in fig 7.2 were obtained. The average of the current was about $114\,\mu$A.
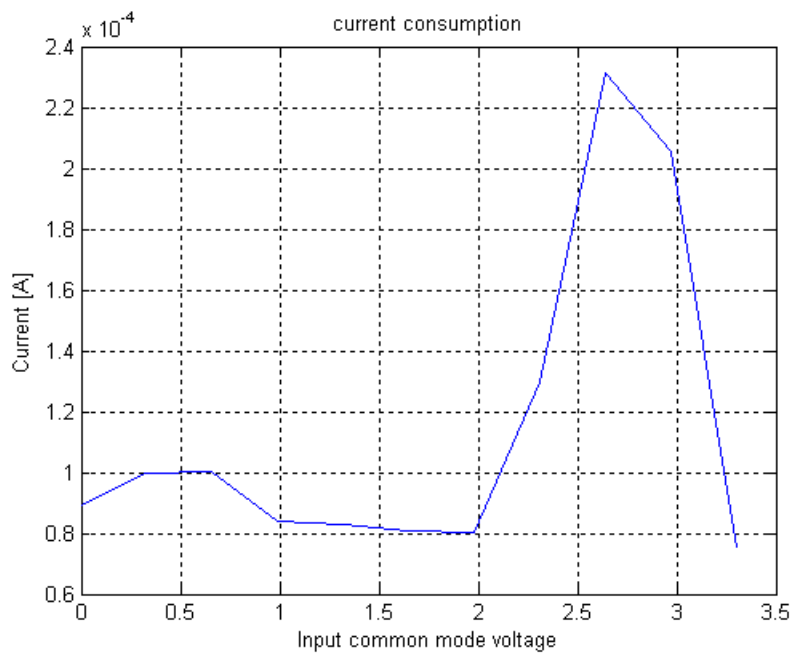

Figure 7.2: Current consumption through the common-mode range

common-mode input range

The common-mode input range was measured by stepping the input voltage to the follower with the second output of the power supply in two hundred steps from 0 V to 3.5 V. The maximum voltage was chosen a bit higher than the power supply in order to easier see the maximum output voltage. The usable input range was from VDD-30 mV and GND+20 mV.
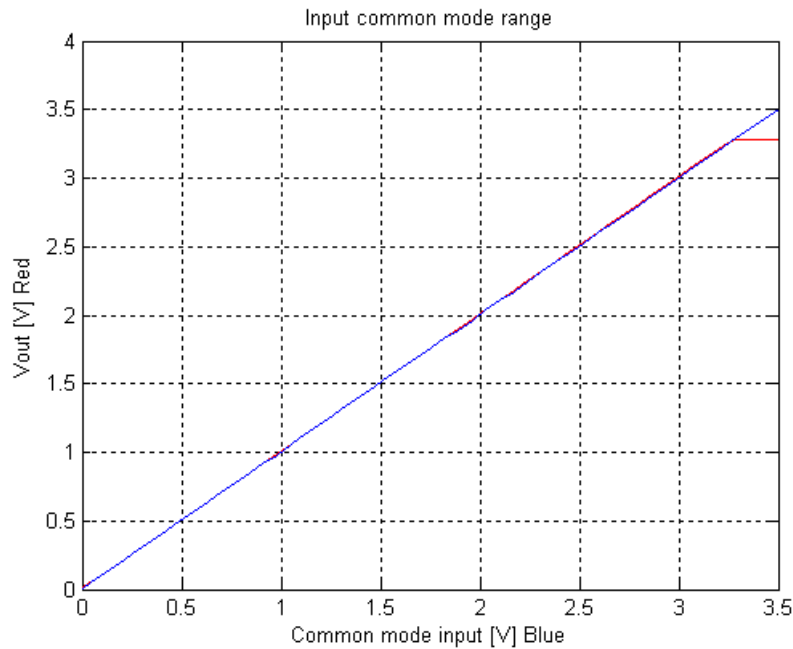

Figure 7.3: common-mode range. The input was swept from rail to rail and the output voltage was measured

Output voltage swing

The output voltage swing was measured by letting the op amp saturate at both rails and measure the output voltage. The output was capable of reaching the VDD by -3 mV and GND by 1.2 mV. The op amp can be considered as rail-to-rail output capable.
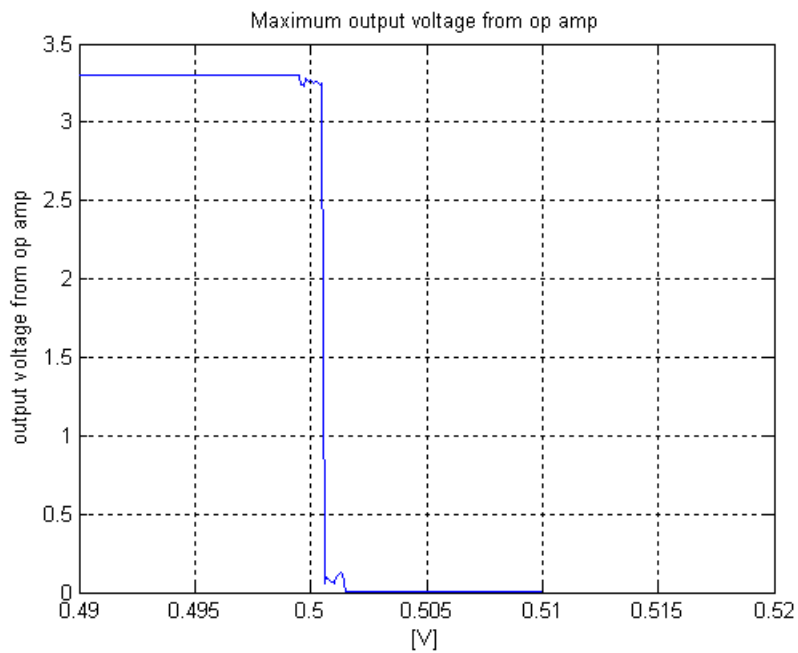
Figure 7.4: Maximum output voltage from the operational amplifier.

Offset voltage over the common-mode range

The offset voltage was measured as the difference between the input and output of the voltage follower. 12 chips were tested. In the lower common-mode range, all except one op amp showed offset voltage lower than 5 mV. Seven out of twelve op amps were within ±2 mV. The lowest of them were 0.3 mV and 0.8 mV. In the intermediate range the offset voltage became higher. The largest were respectively 8 mV and −13 mV. In the upper common-mode range the offset voltage showed a strange behavior. At about 2.3 V the offset voltage increased by about 5 mV to 10 mV, and continued to increase to the common-mode input voltage was about 2.5 V and then started to decrease.
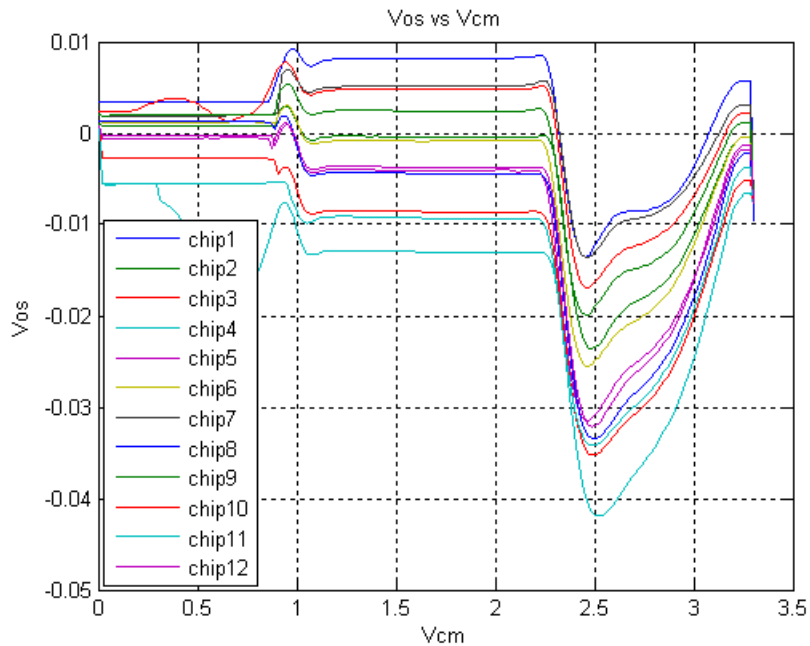
Figure 7.5: Offset voltage measured over the entire common-mode range.

Gain bandwidth and phase margin

Gain bandwidth and PM were measured in the inverting configuration, results are seen i figure 7.6. The gain was set to 30 by a $90\,\mathrm{k\Omega}$ and a $3\,\mathrm{k\Omega}$ in feedback. A $10\,\mathrm{pF}$ capacitor was used as load. When approaching the unity gain frequency, the amplitude of the output signal of the op amp became to low for the oscilloscope to trigger properly when measuring the phase between input and output of the op amp, the phase measurement stopped at $4\,\mathrm{MHz}$. Since this was an inverting configuration the PM was measured directly and was the phase of the op amp at unity gain frequency. The PM measurements were performed by stepping the input frequency with HP 33120 at a constant amplitude. The oscilloscope, HP 54622 measured the phase between its two input channels which were connected to the input and output of the op amp. The amplitude response were measured almost in the same way, one channel measure the peak to peak value of the output signal, while the signal generator produces a input signal at constant amplitude of varying frequencies.
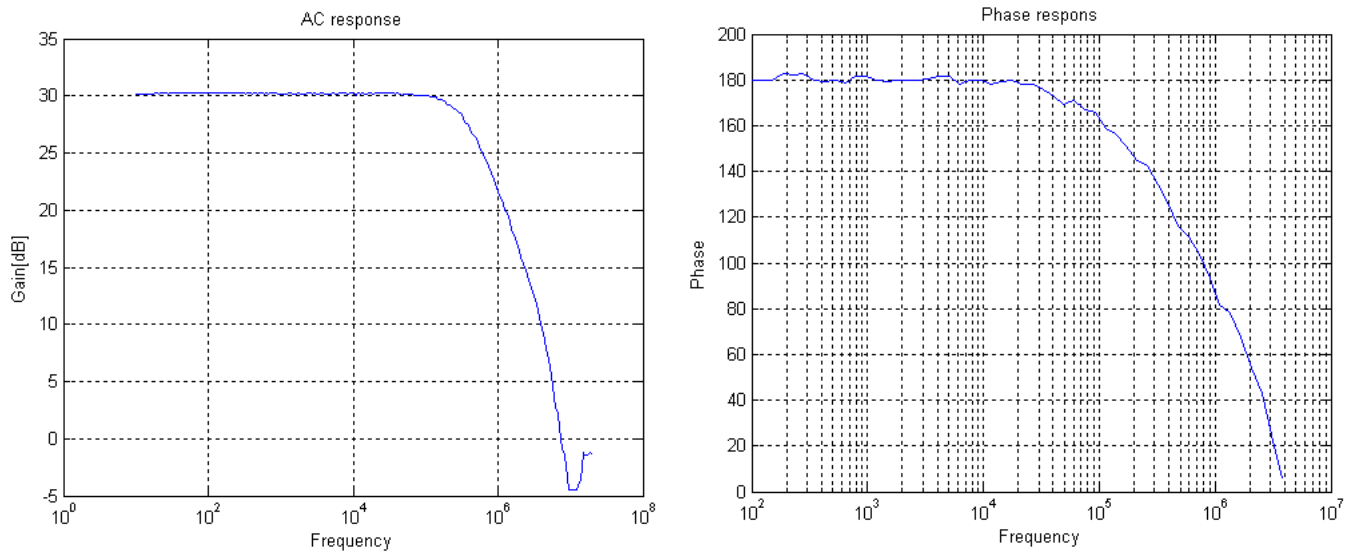
(a) Amplitude response in closed loop configuration. The unity gain frequency is about 7 MHz. The little top in the bottom is caused by trigger problems on the oscilloscope.

(b) Phase response. The phase margin is lower than 10°

Figure 7.6: Amplitude and phase response

7.0.6 Comparing simulations and measurements

The measured current consumption was about $150\,\mu$A smaller than the simulated one. It i difficult to know the exact reason for this observation. It may relate to inaccurate measurements of the total current and the current through the LED. The DC characteristic (input common-mode range and output voltage swing) were in accordance with the simulated results, and shows that the op amp is rail-to-rail capable. It include both rails at input and output.

The measured input reffered offset voltage is larger than simulated and vary over the common-mode range. I actually expected an even smaller absolute value and lower chip to chip variation due to the larger input devises. The offset shows an unexpected behavior in the upper common-mode range. This is probably due to an error in the PMOS pair in the layout, because I were not able to create the same behavior in repeated simulations. The simulated offset voltage is a few μA.

The measured AC response is different from the simulated one. The unity gain frequency is about twice as high in the simulation. This was unexpected. Because of the behavior of the offset in the upper common-mode range, I believed that it was due to an erroneous PMOS pair. But the effect of the feedback was checked in simulation, with feedback and a capacitive load of 10 Pf referred to the common-mode voltage. Unity gain frequency actually increased to 17 MHz compared to the simulated open loop gain with load. Without the capacitive load the unity gain frequency increased to 31.62 MHz. A closer look at the "roll off" of the AC-response was revealing that it is steeper than $-6\,$dB per octave near the unity gain frequency. A second pole is present below the unity gain frequency, the op amp is undercompensated. This was also distinctly from the phase

margin, which is below 15°. The unity gain frequency is therefore not constant and is dependent of feedback. New simulations were performed supporting this, see appendix E.1 for figure. With this compensation capacitor, the unity gain was constant at about 9 MHz, with or without the feedback and with capacitive loads from 10 to 40 pF. This partly explains the difference is AC response.

7.0.7 Discussion and Conclusion

An rail-to-rail op amp was processed in $0.35\,\mu$m CMOS. It is rail-to-rail capable at both input and output. Offset was attempted reduced by increasing the transistors in the differential pair. Increasing the transistor size will reduce offset voltage in the low, intermediate and high common-mode range, but there will still be transition regions between them. Due to an likely error in the PMOS pair, the offset voltage in the upper common-mode range was higher than expected and showed irregular behavior. The offset voltage in the intermediate range was therefore also higher, probably caused by influence by the PMOS pair. If the offset voltage in the lower common-mode range is what we can expect from such an op amp, then the measurements shows that seven out of twelve op amps will have an offset voltage below ± 2 mV. The offset will change in magnitude when the diffent input channels are active. This is due to different offset voltage between the NMOS and PMOS pair. The CMRR is degraded in these areas. Due to process variations, this is not a predictable way of reducing the offset voltage, and it consumes die area.

If this change in offset voltage through the common-mode range is not suitable for its intended use, for example in high resolution ADCs or precision comparators, external offset compensation techniques can or should be used.

Two articles mentioning external offset compensations techniques are [26] and [7]. The auto-zero and offset cancellation technique tries to eliminate the offset in comparators or op amps by using switches and capacitances. One switch sets the op amp in unity gain while a second switch allows the input capacitance to be charged to the input offset voltage. The sampled offset voltage on the capacitor is subtracted from the input or output of the op amp. Since the offset voltage in rail-to-rail amplifiers is not constant, the offset voltage needs to be sampled several times. The op amp is taken "off line" during the sample period. Such offset cancellation methods should be considered in future work.

The phase margin is too low for the op amp to be used in all configurations, this is a design flaw that should have been detected before the chip was sent to processing. The phase margin should have been 60° or even higher to account for process variations and the additional capacitive loading from the output pad.

More work needs to be done to clarify the difference between the simulated and measured AC response.

Appendix A

MOS modelling

A.1   The threshold voltage

The threshold voltage is the voltage between gate and source needed to create an inversion layer in the channel. A basic expression based on charges is given by [10]:

$$V_t = \phi_{ms} + 2\phi_f + \frac{Q_b}{C_{ox}} - \frac{Q_{ss}}{Qox} \tag{A.1}$$

$$= \phi_{ms} + 2\phi_f + \frac{Q_{b0}}{C_{ox}} - \frac{Q_{ss}}{Qox} + \frac{Q_b - Q_{b0}}{C_{ox}}$$

$$= V_{t0} + \gamma(\sqrt{2\phi_f + V_{SB}} - \sqrt{2\phi_f}) \tag{A.2}$$

This voltage consists of three main components: First a work-function difference ϕ_{ms} exists between the gate metal and the silicon. Second, a voltage of magnitude $2\phi_f + Q_b/C_{ox}$ is required to sustain the depletion-layer charge Q_b, where C_{ox} is the gate oxide capacitance per unit area. Third, positive charge density Q_{ss} always exists in the oxide at the silicone interface. This charge is caused by crystal discontinuities at the Si-SiO2 interface and must be compensated by a gate-source voltage contribution of $-Q_{ss}/Cox$. V_{t0} is the threshold voltage when there is no source to bulk voltage present. This voltage is adjusted by implanting additional impurities into the channel region. γ is the bulk threshold parameter and ϕ_f is the Fermi level of the bulk.

When there is an inversion layer and there is no substrate bias, the depletion region contains a fixed charge density Q_{b0} which is given by $\sqrt{2qN_A\epsilon 2\phi_f}$, where N_A is the substrate doping level, ϵ is the permittivity of silicon and ϕ_f is the bulk Fermi potential.

A.2   The drain current

The following analytical derivation of the expressions of the drain current is from [10, 31] and assumes that the depletion layer width is constant along the channel. The drain current I_D is

$$I_D = \frac{dQ}{dt} \tag{A.3}$$

dQ is the incremental channel charge at a distance y from the source in an incremental length dy of the channel. dt is the required time for this charge to cross the length dy. dQ is given by

$$dQ = Q_I W \, dy \qquad (A.4)$$

where W is the width of the channel and Q_I is the induced electron charge per unit area of the channel. The gate to channel voltage at distance y is $V_{GS} - V(y)$. When this voltage exceeds the threshold voltage, the induced electron charge per unit area in the channel is

$$Q_I(y) = C_{ox}[V_{GS} - V(y) - V_t] \qquad (A.5)$$

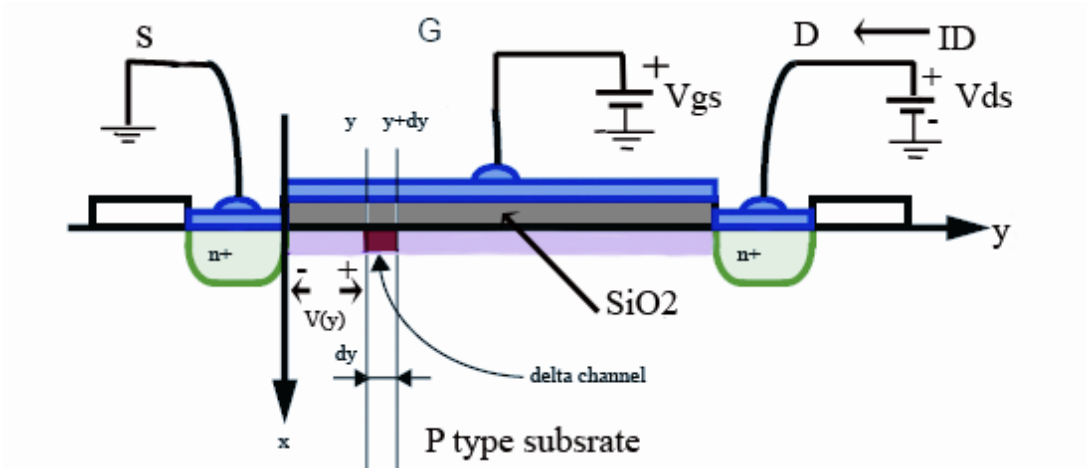This equation describes the induced mobile charge in the channel at point y.

Figure A.1: NMOS device with bias voltages applied

In A.3 dt is given by

$$dt = \frac{dy}{v_d(y)} \qquad (A.6)$$

where v_d is the electron drift velocity at a distance y from the source. When the horizontal electric field$\xi(y)$ is small, the drift velocity is proportional to the electric field:

$$v_d(y) = \mu_n \xi(y) \qquad (A.7)$$

Inserting A.4 into A.3 and substituting dy by $dt V_d(y)$, the drain current can be expressed by

$$I_D = W Q_I(y) v_d(y) \qquad (A.8)$$

and the drift velocity by $\mu_n \frac{dV}{dy}$. Now, by substituting the different expressions for Q_I and $v_d(y)$ into A.8 gives

$$I_D = W C_{ox}[V_{GS} - V - V_t]\mu_n \frac{dV}{dy} \qquad (A.9)$$

which is a simple separable differential equation. Performing the separation of variables and integrate gives

$$\int_0^L I_d dy = \int_0^{V_{DS}} W\mu_n C_{ox}(V_{GS} - V - V_t)dV$$

$$I_D = \frac{\mu_n C_{ox} W}{L}[(V_{GS} - V_t)V_{DS} - \frac{1}{2}V_{DS}^2] \tag{A.10}$$

This fundamental equation can be used to define the voltage-current relation in the different modes of operation.

A.2.1 Modes of operation

The following equations just holds for MOS transistors operating in strong inversion. In the subthreshold region, the transistor is more accurately modeled by an exponential relationship between its control voltage and current, somewhat similar to a bipolar transistor.

When the transistor is operated in strong inversion, and the drain-source voltage is greater than $V_{GS} - Vt$, the gate-drain voltage is less than the threshold voltage, and a conducting channel is no longer present at the drain end. This is called *pinch-off*. If we, in equation A.10, substitutes V_{DS} by $V_{GS} - Vt$ we get

$$I_D = \frac{\mu_n C_{ox} W}{2L}(V_{GS} - V_t)^2$$

Equation A.11. Valid in the active region

As we can see from equation A.11, the drain current is independent of V_{DS}, and the transistor is said to operate in the saturated or active region. This equation is one of the most important one, and describes the large signal operation of a MOS transistor. It states the square-law behavior of a MOS device in active region.

When the drain current is dependent of V_{DS} the transistor is said to operate in the ohmic or triode region. In the upper bound of the triode region, equation A.10 is suitable. In the lower bound of the triode region, the square term of that equation can be ignored, and the resulting equation is

$$I_D = \frac{\mu_n C_{ox} W}{L}(V_{GS} - V_t)V_{DS}$$

Equation A.12. Valid in the lower bound of the triode region

A.2.2 Small signal modelling in the active region

In active region, the MOS transistor can be modeled as a voltage-controlled current source. A key parameter of this model is the transconductance g_m which is defined as

$$g_m = \frac{\partial I_D}{\partial V_{GS}} \tag{A.13}$$

When we apply this derivative to equation A.11, we obtain:

$$\frac{\partial I_D}{\partial V_{GS}} = \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_t) \tag{A.14}$$

It is sometimes preferable to express g_m in terms of I_D rather than V_{GS}. After some algebraic manipulation of A.11 and A.14 two new expressions can be obtained:

$$g_m = \sqrt{2\mu_n C_{ox} \frac{W}{L} I_D} \tag{A.15}$$

$$= \frac{2I_D}{V_{GS} - V_t} \tag{A.16}$$

The body effect

When there is a non-zero voltage between bulk and source, there is a slight increase in the threshold voltage and the drain current is somewhat smaller for a given V_{GS}. The substrate is acting as a second gate. This is modeled as a decrease in the transconductance factor g_m by the body effect, g_s.

The body effect is given by [10, 4]

$$g_s = \frac{\partial I_D}{\partial V_{SB}} = \frac{\partial I_D}{\partial V_t} \frac{\partial V_t}{\partial V_{SB}} \tag{A.17}$$

Applying this derivative to the equations giving the threshold voltage and the transconductance factor, respectively, results in

$$g_s = \frac{\gamma g_m}{2\sqrt{V_{SB} + 2\phi_f}} \tag{A.18}$$

The ratio g_s/g_m is typically in the range 0.1 to 0.3 [10];therefore, the transconductance from the main gate is typically 3 to 10 times larger than the transconductance from the body or the second gate.

The equations presented above is a first order approximation and are ment for hand calculations. Therefore many second order effects is not taken into account. When low voltage and low current circuits emerge, there is a need for precise MOS transistor models which is continuous between the different modes of operation and also models second order effects like [32]: non quasi-static effects, nonuniform substrate effects, noise, channel length modulation, drain induced barrier lowering, substrate currents and their influence on body effect and noise, parameter dependence on geometry, velocity saturation and many more, all modeled with their temperature dependence.

Appendix B

Transistor sizes

Transistor	W/L ratio in μm
M1	40/2
M2	40/2
M3	3/5
M4	90/2
M5	90/3
M6	30/3
M7	30/2
M8	30/3
M9	90/3
M10	50/2
M11	50/2
M12	150/2
M13	150/2
M14	90/2
M15	90/2
M16	90/2
M17	90/2
M18	60/2
M19	24/2
M20	20/2
M21	8/2
M22	50/2
M23	50/2
M24	30/2
M25	30/2
M26	10/2
M27	10/2
M28	30/2
M29	30/2
M30	120/2
M31	40/2
M32	20/2
M33	60/2
M34	70/2
M35	10/2
M36	10/2
M37	70/2
M38	70/2
M39	1/50
M40	1/70

Table B.1: Transistor dimensions

Appendix C

PCB test board

C.1   The signal routing on the PCB

Figure C.1: Routing through the PCB with interface and debug connectors

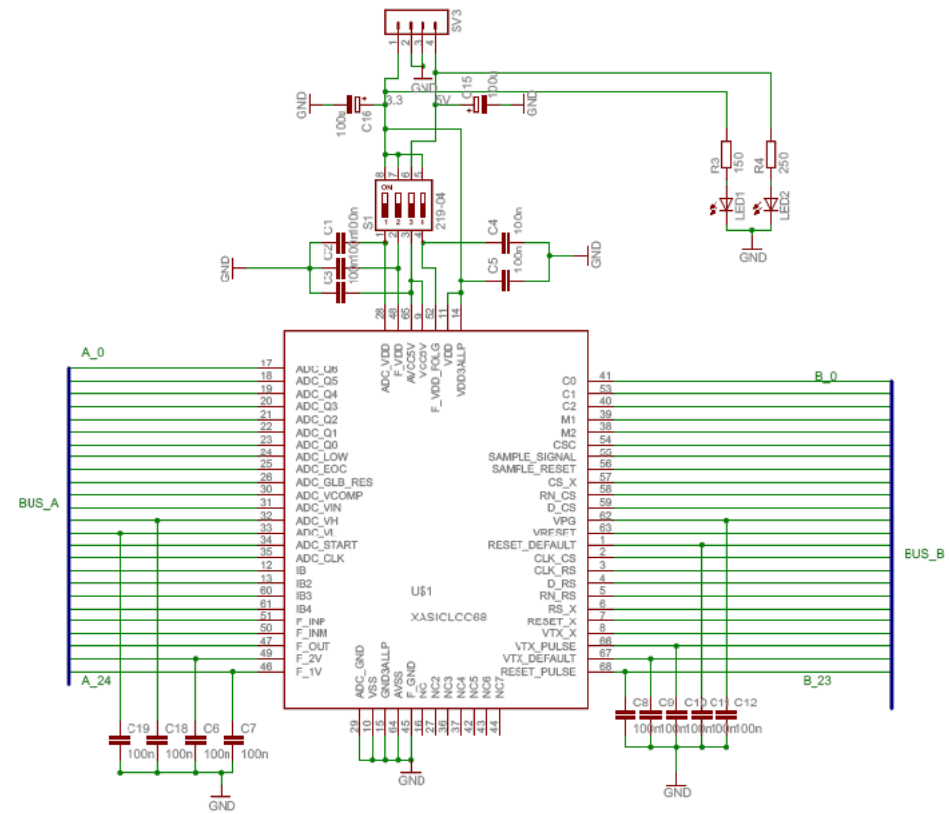# C.2   ASIC and power connections

Figure C.2: ASIC and power connections.

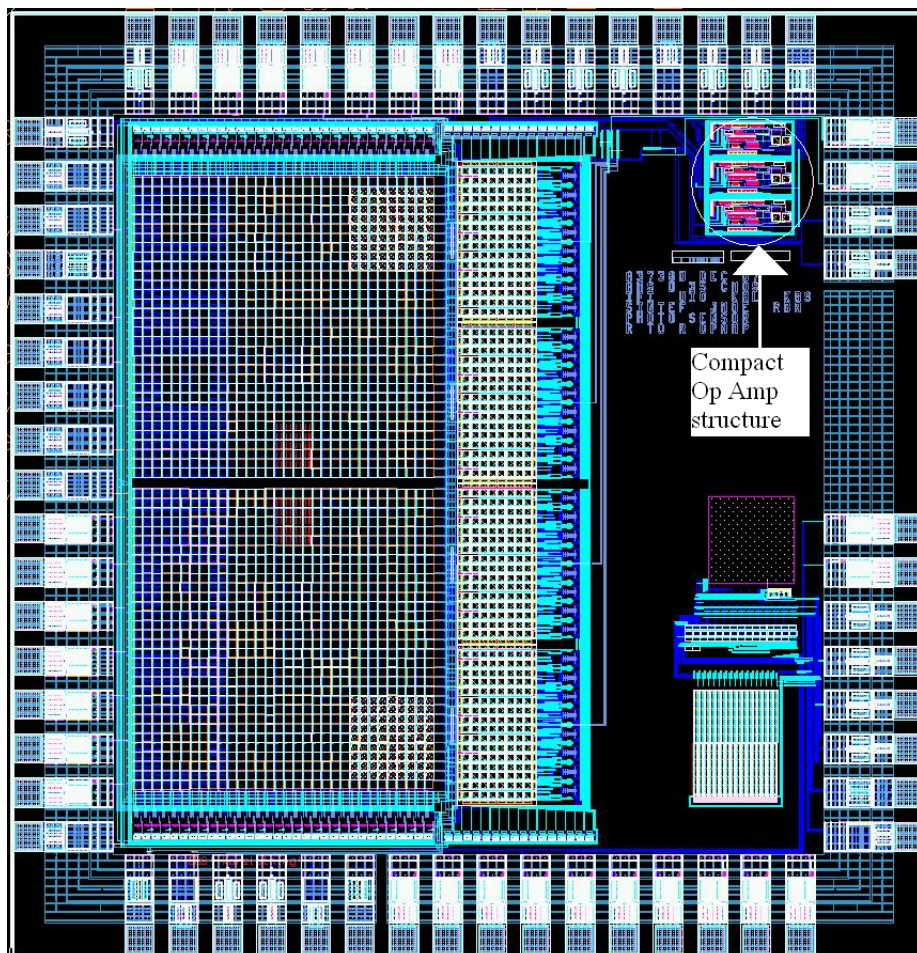# Appendix D

Chip Layout

D.1   Pad frame

Figure D.1: The pad frame of the prototype chip. The other structures are, to the left Pixel array and at the right bottom a SAR ADC
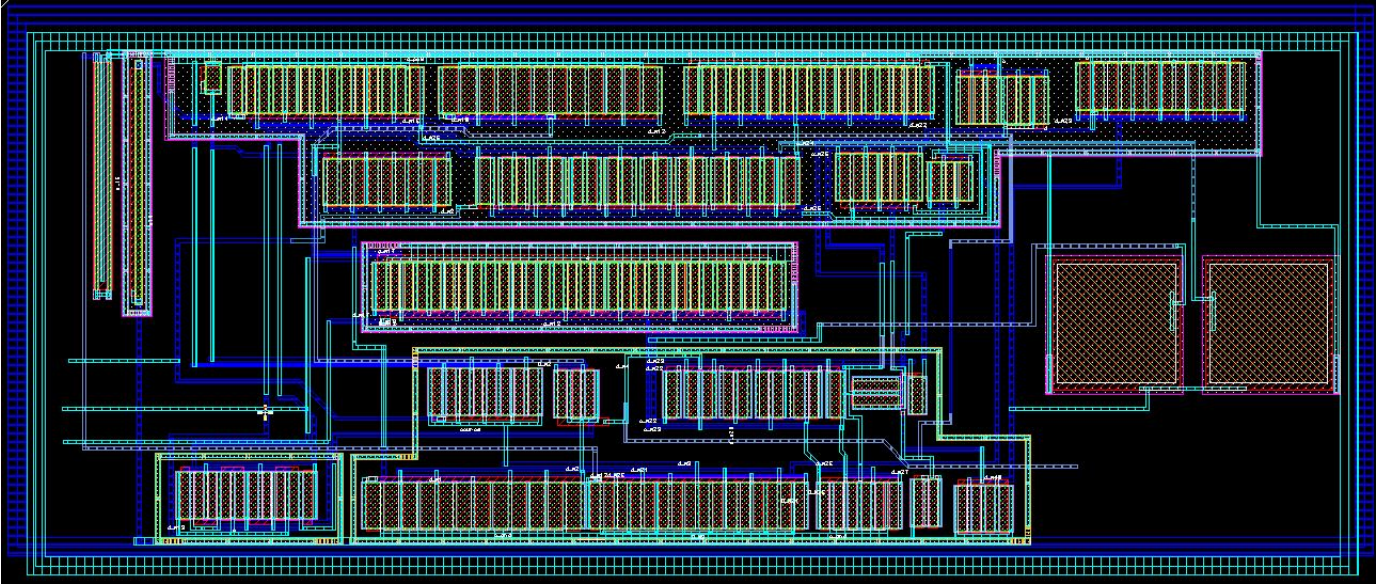
D.2 Operational amplifier

Figure D.2: Layout of the op amp. The size of the op amp is about $300\,\mu$m x $128\,\mu$m

Appendix E
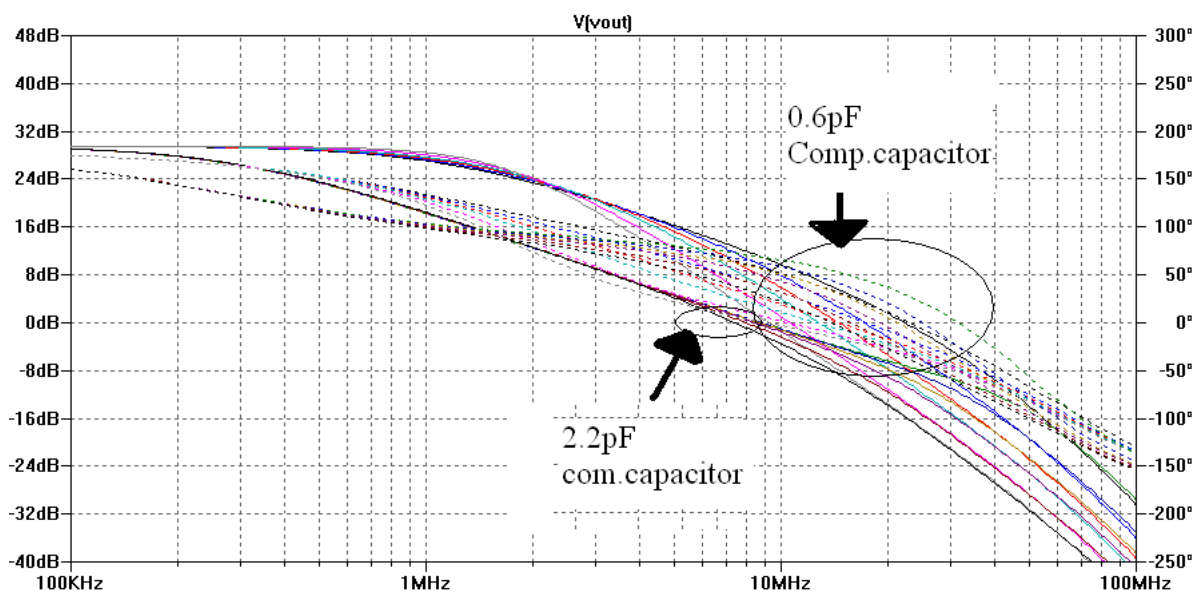
Repeated simulations for chapter 7.0.6

Figure E.1: New simulations with improved frequency performance. With 2.2 pF compensation capacitor the unity gain frequency is almost stable.

Appendix F

MATLB script for controlling the instruments

F.1   Measure AC amplitude response

```matlab
function[freqVin,Vout]=take_acsveep(Vin_pp,n)
addpath(genpath('~mes/src/matlab/gpib/linux'))
HP33120_Init
HP33120_SetTerm('HZ')
HP33120_SetSignal('SIN',Vin_pp)
freqVin=logspace(freq_min,freq_max,n);
pause(0.5)
for i=1:length(freqVin)
    HP33120_SetFreq(freqVin(i));
    pause(0.3)
    HP54622_AutoScale(1)
    Vout(i)=HP54622_MeasVpp(1);
    pause(0.3)
end
a=fopen('ac_sveep_data_inv','w');
for i=1:length(freqVin)
    fprintf(a,'%f,%f\n',freqVin(i),Vout(i));
end
fclose(a);
%clear log_gain;
log_gain=20*log10(Vout./0.1);
semilogx(freqVin,log_gain),xlabel('frequency'),ylabel('dB'),grid, title('AC response')
```

Figure F.1: Script for measuring AC amplitude response

F.2 Phase response

```matlab
function[freqVin,fase]=take_phase_meas(Vin_pp,n)
%addpath(genpath('~mes/src/matlab/gpib/linux'))
HP33120_Init
HP33120_SetTerm('HZ')
HP33120_SetSignal('SIN',Vin_pp)
freqVin=logspace(freq_min,freq_max,n);
pause(0.5)
for i=1:length(freqVin)
    HP33120_SetFreq(freqVin(i));
    pause(0.3)
    pause(0.2)
    fase(i)=HP54622_MeasPhase(1,2);
    pause(0.3)
end
a=fopen('phase_meas_data_inv','w');
for i=1:length(freqVin)
    fprintf(a,'%f,%f\n',freqVin(i),fase(i));
end
fclose(a);
semilogx(freqVin,fase),xlabel('frequency'),ylabel('phase'),grid
```

Figure F.2: Script for measuring phase response

F.3 Current

```matlab
function[Vin,Iout]=take_current(vdd,Vmin,Vmax,n)
addpath(genpath('~mes/src/matlab/gpib/linux'))
K617_Init
HPE3631_Init
K617_SetMode('A')
HPE3631_Operate;
Vin=(Vmin:(Vmax-Vmin)/n:Vmax);
HPE3631_SetVolt(2,vdd);
%HPE3631_SetVolt(1,vin(i));
for i=1:length(Vin)
    HPE3631_SetVolt(1,Vin(i));
    pause(0.25)
    Iout(i)=K617_ReadQuick;
end
a=fopen('current_data','w');
for i=1:length(Vin)
    fprintf(a,'%double,%double\n',Vin(i),Iout(i))
end
fclose(a);
plot(Vin,Iout),xlabel('Vin'),ylabel('I'),grid, title('Current consumption'
HPE3631_Disable;
```

Figure F.3: Script for measuring current

F.4 Voltage

```matlab
function[Vin,Vout]=takeDCvoltage(Vdd,Vmin,Vmax,n)
K617_Init
HPE3631_Init
K617_SetMode('V')
HPE3631_Operate;
Vin=(Vmin:(Vmax-Vmin)/n:Vmax);
HPE3631_SetVolt(2,Vdd);
for i=1:length(Vin)
    HPE3631_SetVolt(1,Vin(i));
    pause(0.25)
    Vout(i)=K617_ReadQuick;
end
a=fopen('dcvolt','w');
for i=1:length(Vin)
    fprintf(a,'%f,%f\n',Vin(i),Vout(i))
end
fclose(a);
plot(Vin,Vout),xlabel('Vin'),ylabel('Vout'),grid, title('linplot')
HPE3631_Disable;
```

Figure F.4: Script for measuring voltage

Bibliography

[1] A.-J. Annema. Analog circuit performance and process scaling. *Circuits and Systems II: Analog and Digital Signal Processing, IEEE Transactions on [see also Circuits and Systems II: Express Briefs, IEEE Transactions on]*, 46(6):711–725, Jun 1999.

[2] K. Bult and G.J.G.M. Geelen. A fast-settling cmos op amp for sc circuits with 90-db dc gain. *Solid-State Circuits, IEEE Journal of*, 25(6):1379–1384, Dec 1990.

[3] J.A Conelly C.D. Motchenbacher. *Low Noise Electronic System Design*. Wiley Intercience, 1993.

[4] Ken Martin David A. Johns. *Analog Integrated Circuit Design*. John Wiley & Sons, 1997.

[5] K.-J. De Langen and J.H. Huijsing. Compact low-voltage power-efficient operational amplifier cells for vlsi. *Solid-State Circuits, IEEE Journal of*, 33(10):1482–1496, Oct 1998.

[6] E. Edgar Sanchez-Sinencio and Andreas G. Andreou. *Low -Voltage/Low Power Integrated Circuit and Systems*. IEEE Press, 1999.

[7] C.C. Enz and G.C. Temes. Circuit techniques for reducing the effects of op-amp imperfections: autozeroing, correlated double sampling, and chopper stabilization. *Proceedings of the IEEE*, 84(11):1584–1614, Nov 1996.

[8] C.C. Enz and E.A. Vittoz. Cmos low-power analog circuit design. *Designing Low Power Digital Systems, Emerging Technologies (1996)*, pages 79–133, 1996.

[9] R.G.H. Eschauzier, R. Hogervorst, and J.H. Huijsing. A programmable 1.5 v cmos class-ab operational amplifier with hybrid nested miller compensation for 120 db gain and 6 mhz ugf. *Solid-State Circuits, IEEE Journal of*, 29(12):1497–1504, Dec 1994.

[10] Paul J. Hurst Stephen H.Lewis Meyer R.G. Gray, P.R. *Analysis and design of analog integrated circuits*. John Wiley & Sons, 2001.

[11] R Hogervorst and J.H. Huijsing. *Design of low-voltaga low-power operational amplifier cells*. Kluwer Academic Publishers, 1996.

[12] R. Hogervorst, J.P. Tero, R.G.H. Eschauzier, and J.H. Huijsing. A compact power-efficient 3 v cmos rail-to-rail input/output operational amplifier for vlsi cell libraries. *Solid-State Circuits, IEEE Journal of*, 29(12):1505–1513, Dec 1994.

[13] R. Hogervorst, J.P. Tero, and J.H. Huijsing. Compact cmos constant-gm rail-to-rail input stage with g m-control by an electronic zener diode. *Solid-State Circuits, IEEE Journal of*, 31(7):1035–1040, Jul 1996.

[14] R. Hogervorst, R.J. Wiegerink, P.A.L. de Jong, J. Fonderie, R.F. Wassenaar, and J.H. Huijsing. Cmos low-voltage operational amplifiers with constant-gm rail-to-rail input stage. *Circuits and Systems, 1992. ISCAS '92. Proceedings., 1992 IEEE International Symposium on*, 6:2876–2879 vol.6, May 1992.

[15] J.H. Huijsing. *OPERATIONAL AMPLIFIERS Theory and Design*. Kluwer Academic Publishers, 2001.

[16] J.H. Huijsing, R. Hogervorst, and K.-J. de Langen. Low-power low-voltage vlsi operational amplifier cells. *Circuits and Systems I: Fundamental Theory and Applications, IEEE Transactions on [see also Circuits and Systems I: Regular Papers, IEEE Transactions on]*, 42(11):841–852, Nov 1995.

[17] Walt Jung. Op-amp history.

[18] P. Kinget and M. Steyaert. Impact of transistor mismatch on the speed-accuracy-power trade-off of analog cmos circuits. *Custom Integrated Circuits Conference, 1996., Proceedings of the IEEE 1996*, pages 333–336, May 1996.

[19] P.R. Kinget. Designing analog and rf circuits for ultra-low supply voltages. *33rd European Solid State Circuits Conference, 2007. ESSCIRC*, pages 58–67, Sept. 2007.

[20] P.R. Kinget. Device mismatch and tradeoffs in the design of analog circuits. *Solid-State Circuits, IEEE Journal of*, 40(6):1212–1224, June 2005.

[21] K.R. Lakshmikumar, R.A. Hadaway, and M.A. Copeland. Characterisation and modeling of mismatch in mos transistors for precision analog design. *Solid-State Circuits, IEEE Journal of*, 21(6):1057–1066, Dec 1986.

[22] D. Liu and C. Svensson. Trading speed for low power by choice of supply and threshold voltages. *Solid-State Circuits, IEEE Journal of*, 28(1):10–17, Jan 1993.

[23] M.J.M. Pelgrom, A.C.J. Duinmaijer, and A.P.G. Welbers. Matching properties of mos transistors. *Solid-State Circuits, IEEE Journal of*, 24(5):1433–1439, Oct 1989.

[24] R. Pintelon, Y. Rolain, G. Vandersteen, and J. Schoukens. Experimental characterization of operational amplifiers: a system identification approach-part ii: calibration and measurements. *Instrumentation and Measurement, IEEE Transactions on*, 53(3):863–876, June 2004.

[25] J.R. Ragazzini, R.H. Randall, and F.A. Russell. Analysis of problems in dynamics by electronic circuits. *Proceedings of the IRE*, 35(5):444–452, May 1947.

[26] J. Ramirez-Angulo, A. Garimella, L.M.K. Garimella, A.J. Lopez-Martin, and R.G. Carvajal. Input offset compensation scheme with reduced sensitivity to charge injection and leakage. *Electronics Letters*, 42(6):340–341, March 2006.

[27] E. Seevinck, W. De Jager, and P. Buitendijk. A low-distortion output stage with improved stability for monolithic power amplifiers. *Solid-State Circuits, IEEE Journal of*, 23(3):794–801, Jun 1988.

[28] E. Seevinck and R.J. Wiegerink. Generalized translinear circuit principle. *Solid-State Circuits, IEEE Journal of*, 26(8):1098–1102, Aug 1991.

[29] A.M. Shams and M.A. Bayoumi. A novel high-performance cmos 1-bit full-adder cell. *Circuits and Systems II: Analog and Digital Signal Processing, IEEE Transactions on [see also Circuits and Systems II: Express Briefs, IEEE Transactions on]*, 47(5):478–481, May 2000.

[30] A.M. Shams, T.K. Darwish, and M.A. Bayoumi. Performance analysis of low-power 1-bit cmos full adder cells. *Very Large Scale Integration (VLSI) Systems, IEEE Transactions on*, 10(1):20–29, Feb 2002.

[31] Ben G. Streetman and Sanjay K. Banerjee. *SOLID STATE ELECTRONIC DEVICES*. Prentice Hall, 2000 / sixth edition.

[32] Y.P. Tsividis and K. Suyama. Mosfet modeling for analog circuit cad: problems and prospects. *Solid-State Circuits, IEEE Journal of*, 29(3):210–216, Mar 1994.

[33] K. Uyttenhove and M.S.J. Steyaert. Speed-power-accuracy tradeoff in high-speed cmos adcs. *Circuits and Systems II: Analog and Digital Signal Processing, IEEE Transactions on*, 49(4):280–287, Apr 2002.

[34] E.A. Vittoz. Low-power design: ways to approach the limits. *Solid-State Circuits Conference, 1994. Digest of Technical Papers. 41st ISSCC., 1994 IEEE International*, pages 14–18, Feb 1994.

[35] R.J. Widlar. Design techniques for monolithic operational amplifiers. *Solid-State Circuits, IEEE Journal of*, 4(4):184–191, Aug 1969.

[36] Shouli YAN and Edgar SANCHEZ-SINENCIO. Low voltage analog circuit design techniques: A tutorial. *IEICE TRANS. ANALOG INTEGRATED CIRCUITS AND SYSTEMS,*, E00-A:1–17, 2000.