UNIVERSITY OF OSLO
Department of Informatics

CMOS Ultra Wide-Band Impulse Radio Receiver Front-End

Master thesis

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Acknowledgments

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Preface

This thesis is submitted as a part of my degree in Master of science in microelectronics at the department of physics at the University of Oslo. The work on the thesis project was initiated in January 2004 and concluded the following year, in June 2005.

The work has been challenging in many ways, regarding the design and measurement of the prototype chip and the design of the Print Circuit Board (PCB) used for measurements. However, I have learned a lot during the project, and believe that I have benefited from the work. The thesis addresses a relatively new and popular topic in short range communication and covers a wide range of issues, and I feel that I have gained significant experience in several aspects of implementing an ASIC and developing a PCB.

In this thesis a novel low power front end for Ultra WideBand Impulse Radio (UWB-IR) receivers suitable for implementation in standard Complementary Metal Oxide Silicon (CMOS) technology is presented. The front-end is implemented as a pre-conditioner for a RAKE receiver.

The proposed front end is implemented together with a RAKE receiver in STM 120nm CMOS process distributed by CMP. The PCB was produced in a FR4 epoxy resin laminate at ELPRINT.

Abstract

As most radio communication is based on a narrow banded carrier technique, the technique this thesis is based on utilizes single impulse transmissions and wide bandwidths. The technique is called Ultra WideBand Impulse Radio (UWB-IR) and is based on emission of single pulses and time domain processing. Through modulation and pulse shaping energy is contained within a specific band in the frequency spectrum. This implies that the technique is low power compared to narrow banded techniques wasting energy on a carrier wave conveying no info. Most radio receivers even UWB radio receivers is based on a template sampling scheme for signal detection and the utilization of a Digital Signal Processing (DSP) unit for signal processing.

In this thesis a novel low power front-end for impulse radio receivers suitable for implementation in standard Complementary Metal Oxide Silicon (CMOS) technology is presented. The novel architecture is exploring thresholding and continuous-time delay lines avoiding high speed sampling clocks. The thresholding scheme is based on simple inverter structures, the topology consists of a Low Noise Amplifier (LNA), integrator, thresholding pulse shaper and pulse shape detector all in standard digital CMOS technology. The continuous time front-end utilizes no sampling clock and is designed to work with a RAKE receiver for low power ultra wideband applications. As reflections are destructive for most types of radio communication, the combined topology with the front-end and RAKE receiver utilizes reflections constructively as a gain in Signal to Noise Ratio (SNR).

Contents

Chapter 1

Introduction

1.1 Introduction

The focus on short range wireless communication technology is increasing. Although standards like Bluetooth should address such demands, there seem to be intense development of increased bandwidth using lower power. An interesting technology is Ultra Wide Band (UWB) or Impulse Radio. With the recent Federal Communications Commission (FCC) approval of wideband transmission between 3.1GHz-10.6GHz with a EIRP emission level at -41.3 dB several efforts have emerged achieving in excess of 100Mbit/s data rates for short range communication.

The focus on UWB is primarily on the Orthogonal Frequency Division Multiplexing (OFDM) approach by exploiting the bandwidth combining several traditionally single band frequencies. The Impulse radio approach exploits the bandwidth by sending shaped pulses and by using Pulse Position Modulation (PPM), avoiding the carrier. The concept of base band radio using very short pulses has other interesting advantages. The wide transmission band makes penetration through different materials better than narrow band transmission [1, 2]. The lack of carrier may be traded for low power solutions. Traditionally narrow-band based transmissions are wasting energy on a High Frequency (HF) carrier which in itself is transferring no information. There is however, demand for short-range low bandwidth communication links in wearable and implantable microelectronics and Personal Area Networks (PAN) [3]. In several of these applications, like implantable devices, ultra low power is important. Exploring impulse radio for robust wireless communication in medical applications is also interesting.

Within the IEEE 802.15 standard for Wireless Private Area Networks (WPAN) several different technologies addressing low power short range commu-

nication exists. One example is ZigBee which applies to the IEEE 802.15.4 standard, utilizing several different bands and achieving 20 kbps to 250 kbps data rates, depending on the band. The IEEE 802.15.3a standard addressing high data rate UWB application is regulated between 3.1GHz and 10.6 GHz and can achieve data rates of several hundred Mbps. Compared to other technologies within the IEEE 802.15 standard, like ZigBee and Bluetooth based technologies, UWB technology data rate is superior. A new upcoming standard IEEE 802.15.4a applies to the UWB-IR technology for low data rates and low power consumption. Early experiments have been performed showing data rates of 100kbps with a total power consumption of 1mW [4], and for a even lower data rate of 10 kbps an average power consumption of 5μW is achieved [5], which is much lower than existing technologies, e.g one example of ZigBee [6] using between 20mW to 80mW at a data rate of 250 kbps. ZigBee is today one of the most power efficient short range technologies available. However the ability to obtain low power, short range and multi user communication also indicate that UWB-IR technology has a bright future within short range and low power communication.

Due to the FCC regulations on ultra wide-band signal emission, the spectrum response of the signal must be located between 3.1 GHz and 10.6 GHz, and with a spectral power density less than white noise. If the UWB signal were to show up in the frequency spectrum it would cause interference or jamming for other communication within the same frequency band.

As most existing UWB solutions is based on OFDM and the use of multiple carriers, the receivers are based on a template mixing scheme. The front-end presented in this thesis is to be based on the detection of impulses shaped to keep the spectrum energy within regulations. This is done by a thresholding and pulse shape verification scheme without the use of a sampling clock. The reception is based on the use of a dual monocycle pulse, which may have two phases. The shape of the dual monocycle is illustrated in figure 1.1. The two phases used in this thesis are illustrated in the figure below.

Additional techniques for gaining spectrum control can be various kinds of modulation, which are briefly presented in the thesis. The major challenges in this thesis is to design a LNA and a thresholding and shape detection scheme that can cope with the high frequencies. A major part of the challenges is of course the short channel effects, the low power supply and the fact that a frequency operation up to 10 GHz is at the limit of the technology used for the implementation. To justify the use of a thresholding and pulse shape recognition compared to a template sampling scheme, the performance and efficiency of the to topologies of detectors are briefly compared. The circuit topologies presented are

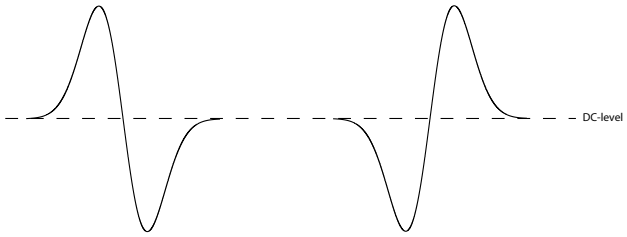

Figure 1.1: Illustration of the two phases of the dual monocycle with a DC level of zero.

designed by the author of the thesis, simulations are done on schematic in a combination with manually added parasitic capacitors. This is done because the parasitic extraction from layout failed to work for the combination of design kit and software used in the design process.

In this thesis a novel front-end for impulse radio receivers suitable for implementation in standard CMOS technology is presented. The novel architecture is exploring thresholding and continuous-time delay lines avoiding high speed sampling clocks. The proposed solution is implemented in STM 120nm CMOS process. Two publications have been made on the combination of the basis in a RAKE scheme for symbol correlation and the topology presented for signal detection [7, 8]. One publication with more focus on the front-end scheme, also here as a pre-conditioner for the RAKE receiver, is prepared and pending for publication [9]. All publications can be found in appendix F.

1.2 Overview of the thesis

Chapter two in the thesis give an introduction in the theory on regulations for UWB and theory regarding pulse shaping and modulation to obtain a level of spectrum energy within regulations. A template sampling receiver topology is also explored, and its detector efficiency vs. noise is presented and briefly compared to a thresholding scheme. In chapter three the different amplifier structures is explored and compared for performance, with a discussion that converges to a final LNA scheme. The fourth chapter introduces the comparator/quantizer idea by using a threshold technique. The output buffers from thresholding and pulse shaping pre-phase detection is also presented in this chapter. Chapter number five presents the dual slope phase detection scheme with an additional noise discrimination feature. In chapter six the relation between the delay line, RAKE inputs, reflections and the shaping of

pulses accordingly are presented with the output buffers from the pulse shaping scheme. Chapter seven presents the whole system combined with simulations from the shape recognition scheme. Outputs from the chip to the RAKE structure and the I/O from the circuit are also presented with pads. The system implementation in silicon and the different isolation techniques used are presented in chapter eight. Chapter nine presents the different simulations and chapter ten presents the measurements and its preparations which consisted of a Print Circuit Board (PCB) design. Discussions and proposal for improvements together with a conclusion is presented in chapter eleven.

A listed outline of the thesis:

1. Introduction with motivation and challenges in the thesis
2. Introduction to UWB regulations and how to stay within, together with a presentation and calculations of detector efficiency vs. noise briefly compared to a thresholding scheme
3. Amplifiers are compared with a discussion converging to a scheme implemented in silicon
4. The comparator/quantizer technique based on thresholding is presented with its output buffers
5. The dual slope and phase detection scheme are presented together with pulse shaping and output buffers
6. The final pulse shaping and its relation to the delay line, RAKE inputs and reflections are presented
7. A combination of all the elements making out the front-end is presented as a system and simulated, together with the output to the RAKE and I/O to the chip combined with pads
8. Implementation in silicon and the isolation techniques used combined with pad selections are presented
9. Presentation of the simulation of single parts of the system together with the simulations of the whole front-end
10. The measurements and its preparations are presented with descriptions of PCB design and measurement environments
11. Final discussions with proposal for improvements and conclusion

Chapter 2

Pulse shape, modulation and detector efficiency vs. regulations

In conventional radio communication as in UWB electromagnetic energy which is used as the information carrying medium. Conventional radio uses a continuous frequency compared to UWB-IR which emits single separated pulses. In this chapter the difference between conventional radio and UWB-IR is explored, explaining how it is possible to gain control of the spectrum by shaping a single pulse. The existing spectrum and radiation regulations of UWB emission is presented, and different pulse shapes are compared for use in this application. Modulation, receiver topologies and detection efficiency are also explored. This chapter is based mostly on the books called "Ultra-wideband radio technology" [2] and "UWB theory and applications" [1].

2.1 Spectrum and radiation regulations

Many users occupying and coexisting in the same limited radio spectrum is made possible by regulations, which are developed together with the radio technology. Since the earliest regulations the radio technology and regulations have converged into a narrow band regulation, and at that time wide band signal transmission was a contrary to the progress possible due to regulations. As technology has developed and made UWB transmissions an effective way to utilize the spectrum, regulations have adapted to permit UWB signal emission. The first to permit UWB signaling was the US federal communications commission FCC in 2002, the European technical telecommunications administration ETSI

followed with a proposal of regulation that are expected to come into force within 2005.

The regulations mentioned is the Effective Isotropically Radiated Power EIRP regulations, describing the product of the antenna gain and the power supplied to it in a given direction relative to an isotropic antenna.

Frequency	Indoor EIRP ($\frac{dBm}{MHz}$)	Handheld EIRP ($\frac{dBm}{MHz}$)
960 MHz - 1.610 GHz	-75.3	-75.3
1.610 GHz - 1.990 GHz	-53.3	-63.3
1.990 GHz - 3.1 GHz	-51.3	-61.3
3.1 GHz - 10.6 GHz	-41.3	-41.3
Above 10.6 GHz	-51.3	-61.3

Table 2.1: FCC regulatory scheme for EIRP level within the bandwidth for indoor and outdoor handheld UWB systems. UWB regulations between 3.1 GHz and 10.6 GHz has the same restrictions for indoor as for outdoor handheld devices.

Frequency	Indoor EIRP ($\frac{dBm}{MHz}$)	Handheld EIRP ($\frac{dBm}{MHz}$)
< 3.1 GHz	$-51.3 + 87 \cdot \log\left(\frac{f}{3.1}\right)$	$-61.3 + 87 \cdot \log\left(\frac{f}{3.1}\right)$
3.1 GHz - 10.6 GHz	-41.3	-61.3
> 10.6 GHz	$-51.3 + 87 \cdot \log\left(\frac{f}{3.1}\right)$	$-61.3 + 87 \cdot \log\left(\frac{f}{3.1}\right)$

Table 2.2: ETSI regulatory scheme for EIRP level within the bandwidth for indoor and outdoor handheld UWB systems. UWB regulations between 3.1 GHz and 10.6 GHz has a 20 dB more restrictive regulation for handheld EIRP than for indoor.

The data in table 2.1 and 2.2 is from an extract of the FCC part 15 regulation [10] and the ETSI technical report [11].

For indoor limits the regulations defined by FCC and proposed by ETSI are the same, but for handheld systems the EIRP regulation proposed by ETSI is as much as 20 dB more restrictive than the one defined by FCC.

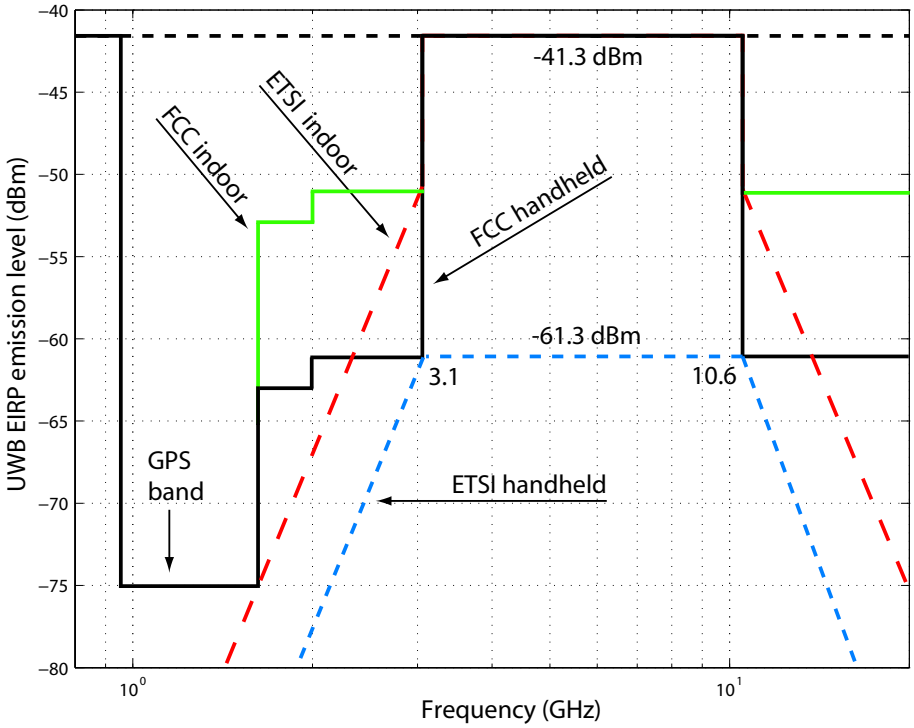

Figure 2.1: Comparison of the ETSI and FCC regulations for UWB communication regarding indoor and outdoor handheld devices. FCC indoor represented by the green graph, FCC handheld by black, ETSI indoor by the red dashed and ETSI handheld by the blue dashed graph. The regulation within the Global Positioning System (GPS) band is also illustrated.

FCC regulation limits for indoor and handheld systems are given by table 2.1, and in figure 2.1, they are illustrated in the spectrum with the ETSI proposal for emission limits for comparison. ETSIs proposal for regulation is given by table 2.2.

The level of -41.3 dBm is the much spoken of part 15 limit, which regards operation of unlicensed low power RF communication. These regulations attend to a power spectral density mask PSD to be used when designing a UWB signal, making sure the signals spectral energy stays within regulations. The PSD mask for indoor systems are illustrated in figure 2.2, and is given by the relationship between regulation limits and the best possible spectral shaping of a signal.

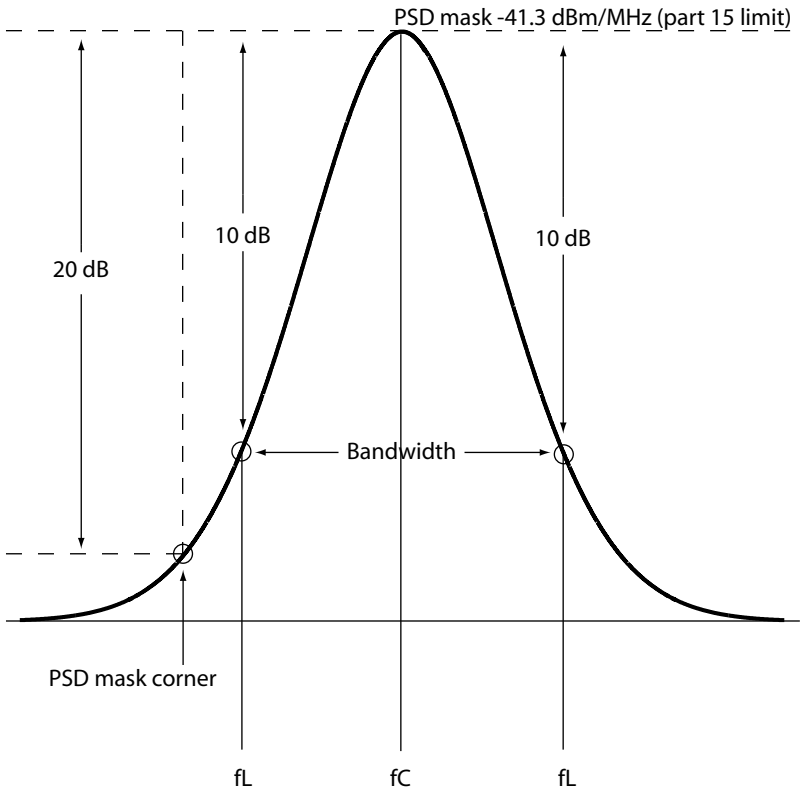

Figure 2.2: The optimal signal shape within regulations illustrating the 20 dB PSD mask corners, the part 15 limit and the 10 dB minimum bandwidth requirements.

The 10 dB limits illustrated in figure 2.2 is the minimum bandwidth limit of 500 MHz. To ensure compliance with the minimum bandwidth requirements, the signal must remain below the 20 dB PSD mask corners and the part 15 limit of -41.3 dB.

2.2 Pulse shape and spectrum control

Conventional radio signals occupy a unique location in the radio spectrum and are distinct and narrow banded. They are crafted that way due to the interplay between the technological evolution of RF technology and regulations, which brought order to the radio spectrum. By occupying a fraction of spectrum each the radio signals share the limited spectrum, enabling multiple users to coexist. Separating signals by channels, bands and frequency is not the only way to share the spectrum. Another

way is to separate signals in time, especially in short fractions of time. Which implies emission of short duration pulses. These signals occupy wide bandwidths, and the shorter the fraction of time for one pulse, the wider the bandwidth. Using coding, modulation and packing techniques of signals in time, enables the signals to be separated and thus renders it possible to distinguish users.

Generating UWB pulses can be done in many ways, and the most basic approach is to send a sharp signal edge, which will occupy a bandwidth relative to the rise or fall time off the signal edge. This approach can occupy an extremely wide bandwidth, but with a spectrum content that is hard to control. An improvement of this approach is to add a band pass filter which shapes the signals spectral appearance, but adding a filter will cause the signal to gain a lot of ringing, as illustrated in figure 2.3.

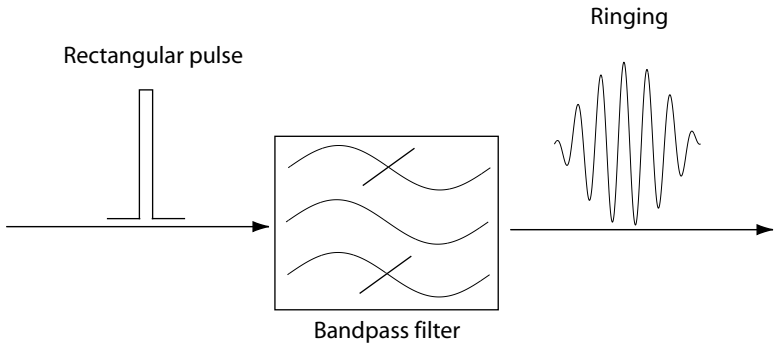

Figure 2.3: Illustration of the ringing effect gained by emitting a rectangular pulse through a band pass filter.

The signal being a step or a narrow pulse appears as a complex elongated signal. This can be sufficient for some kinds of UWB-IR systems using HF sampling techniques, but the method lacks the finesse to precisely shape and control the signal energy in the frequency spectrum. There are several existing methods to achieve precise signal design in UWB-IR and to illustrate how to gain spectrum control the spectrum energy of three pulses are compared. The three pulses are a rectangular pulse r(t), a cosine shaped pulse c(t) and a Gaussian shaped monocycle g(t) all illustrated in time and frequency domain in figure 2.7.

The rectangular pulse r(t) has a width of T picoseconds and is centered at t=0 given by equation 2.1.

$$r(t) = \begin{cases} 1 \text{ if } -\frac{T}{2} < t < \frac{T}{2} \\ 0 \, otherwise \end{cases} \tag{2.1}$$

By Fourier transforming r(t) an frequency domain representation R(f) is described by equation 2.2:

$$R(f) = \frac{T \cdot \sin(\pi T f)}{\pi T f} \tag{2.2}$$

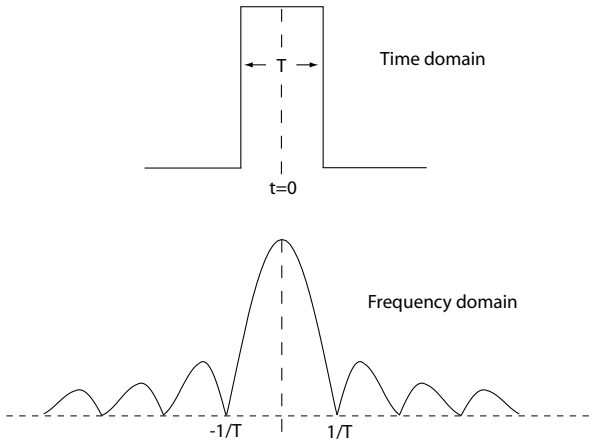

Figure 2.4: Illustration of a rectangular shaped pulse in time and frequency domain related by Fourier transformation and with the applied relation T.

The relation between time and frequency domain is plotted in figure 2.4, where the width T of the pulse corresponds to a width $\frac{2}{T}$ in frequency, thus giving the relation between the signals spectral width and the pulse duration. The frequency representation of the signal indicates a large main lobe between $f = -\frac{1}{T}$ and $f = \frac{1}{T}$. The rectangular pulse also generate significant spectral energy in the side lobes. Due to the side lobes these pulses spectral energy might exceed regulatory levels, thus reducing the energy in the side lobes of the signal would apply to the regulations in UWB applications.

An important relation between time and frequency domain of a signal is that the more continuous and smooth the rise and fall of the time domain signal is, the lower is the energy content in the side lobes. Thus the energy in the side lobes can be controlled by shaping the edges of the signal in time domain, which makes the cosine and Gaussian shaped

pulses more relevant for UWB-IR applications. The cosine-shaped pulse c(t) is described by equation 2.3.

$$c(t) = \begin{cases} \cos(\frac{2\pi f_a}{2}) \text{ if } |t| < \frac{1}{2f_a} \\ 0 \; otherwise \end{cases} \tag{2.3}$$

By looking at figure 2.5 and comparing it to the rectangular pulse in figure 2.4, the top of the pulse is now rounded, and the energy in the side lobes is reduced. But due to abrupt corners in the lower part of the pulse there is still some energy remaining in the side lobes.

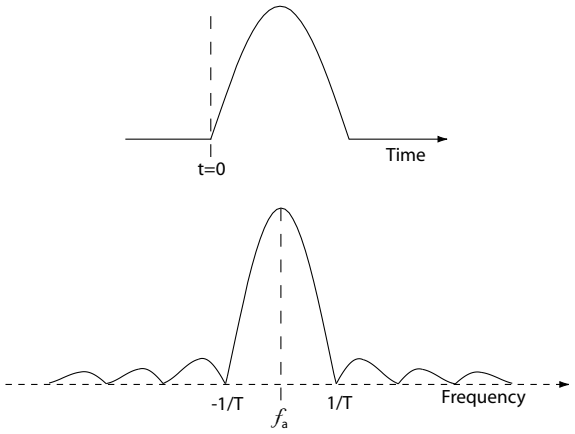

Figure 2.5: Illustration showing the time and frequency domain relation for a cosine shaped pulse.

The frequency representation of c(t) is described by equation 2.4.

$$C(f) = \frac{\cos(\pi \frac{f}{f_a})}{1 - (2\frac{f}{f_a})^2} \tag{2.4}$$

Now exploring the rectangular and cosine shaped pulse it becomes obvious that smooth transitions in time domain avoids energy to be waisted on the side lobes of the signal in frequency domain. This applies to a pulse shape with continuous smooth transition in time domain. A widely used pulse shape applying to these characteristics is the Gaussian shaped pulse.

The Gaussian shaped pulse g(t) is given by equation 2.5.

$$g(t) = \exp(\frac{-0.5t^2}{u^2}) \tag{2.5}$$

And its frequency representation by equation 2.6.

$$G(f) = \exp(-2(\pi f u)^2) \tag{2.6}$$

The width parameter $u = u_B$ is calculated to give $G(f)^2 = 0.1$ with the value f_B in GHz to obtain the bandwidth requirements at -10 dB illustrated in figure 2.2. With the width parameter u given by equation 2.7.

$$u = u_B = \frac{1}{2\pi f_B (\log(e))^{\frac{1}{2}}} \tag{2.7}$$

Where f_B represents the desired half bandwidth from figure 2.2 and e=2.7182... which is the natural logarithm base.

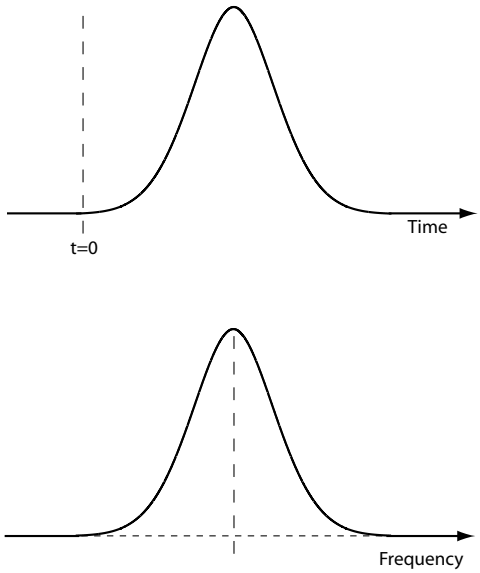

Figure 2.6: Showing the time and frequency domain relation for a Gaussian shaped pulse.

As shown in figure 2.6 the Gaussian pulse is continuous and has continuous smooth transitions, which in the frequency representation appears as a Gaussian shaped main lobe with suppressed side lobes. By comparing the three main lobes in figure 2.7 it is clear that between the 10 dB points they appear nearly identical, but when looking at the area outside the difference is considerably large.

From the figure it is clear that the smoother the transition, the more suppressed are the lobes, thus giving more control over the spectrum.

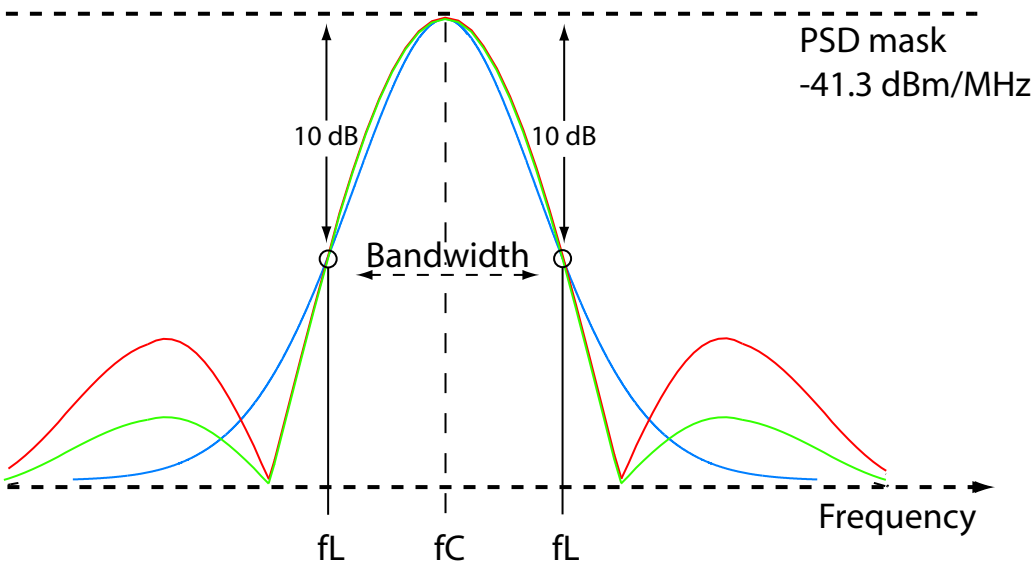

Figure 2.7: Illustrating the relation of smooth transitions and spectrum energy with focus on the energy in the side lobes, by comparing the three previously introduced pulse shapes. The red line is the frequency domain for the rectangular shaped pulse, green is the cosine shaped and blue is the Gaussian shaped pulse.

The objective of pulse shaping and spectrum control adds up in generating a pulse with a spectrum representation that fills up the whole bandwidth between 3.1 GHz to 10.6 GHz. This can be done by generating a baseband pulse (e.g Gaussian) containing the correct bandwidth relative to the PSD mask in figure 2.2, and then shift it up in frequency using Armstrong's heterodyne technique illustrated in figure 2.8. This implies mixing the baseband pulse with a sinusoidal waveform like e.g $\cos(2\pi f_C)$.

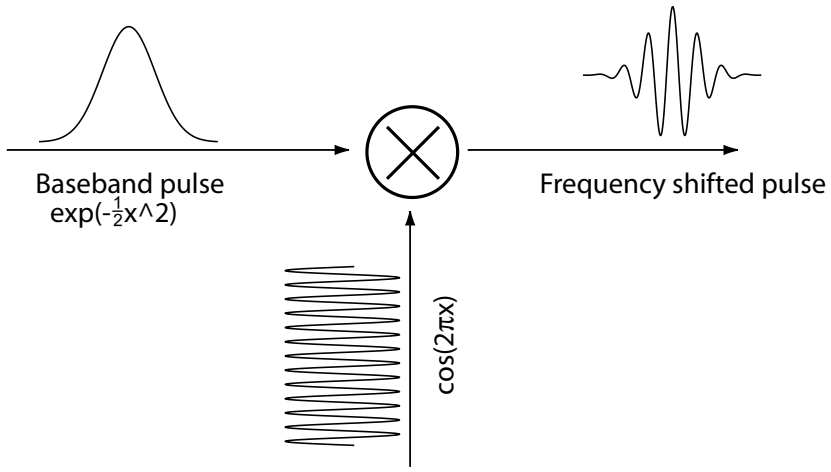

Figure 2.8: Illustrates the basics of Armstrong's heterodyne technique with a mixing between a baseband pulse and a sinusoidal waveform.

This technique is illustrated in figure 2.8 and is often used in UWB communication, thus making it relatively simple to control the spectrum content of the signal. But this technique usually requires a HF sampling in the receiver, and since the front-end scheme presented in this thesis is based on reception and detection of dual sloped monopulses. The technique does not apply to this approach of UWB-IR signal emission.

The shape of dual slope Gaussian monocycles in time domain is described by equation 2.8.

$$\nu(t) = 6A \cdot \sqrt{\frac{e\pi}{3}} \cdot \frac{t}{\tau} \cdot e^{-6\pi(\frac{t}{\tau})^2} \tag{2.8}$$

Where A is the peak amplitude of the monocycle, τ is the duration of the monocycle, t is the time and e is the natural base of logarithms. And by Fourier transforming the frequency domain is given by equation 2.9.

$$\nu(f) = -j \cdot \frac{2f\tau^2}{3} \cdot \sqrt{\frac{e\pi}{2}} \cdot e^{\frac{\pi}{6}f^2\tau^2} \tag{2.9}$$

with the center frequency f_c as:

$$f_c = \frac{1}{\tau} \tag{2.10}$$

The relation between time and frequency domain is illustrated in figure 2.9.

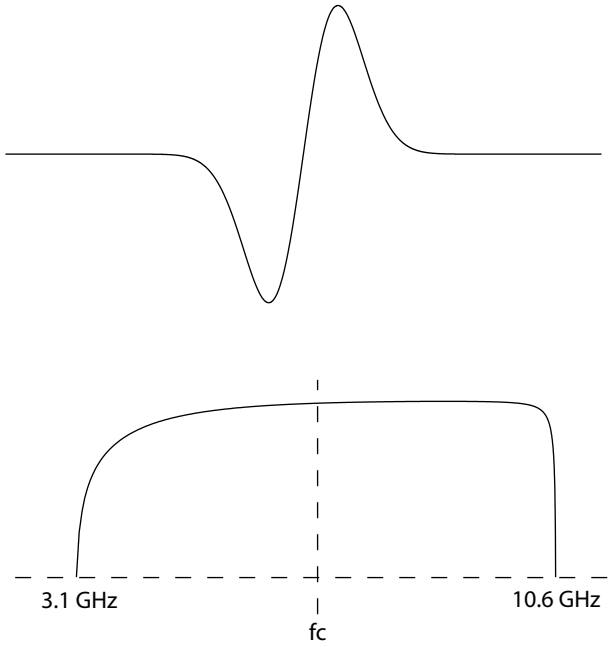

Figure 2.9: Illustration of the dual monocycle in time and frequency domain. Simulated in Matlab.

By using a dual sloped Gaussian monocycle, as illustrated in figure 2.9, the spectrum energy of the pulse is easily controlled. The dual sloped shape of the pulse is actually the derived shape of the previously presented Gaussian monocycle, thus the smooth transitions. The pulse shape can be considered carrier based. A advantage of the pulse shape over the baseband signal is that the peak of the energy spectrum of a single pulse is not at zero frequency. As the pulse itself has a DC level of zero, no coding is necessary to avoid the need for a DC offset between the pulses, which potentially could suppress weak signals in between pulses.

By emitting any of the pulses used in UWB-IR in a repetitive pattern, it will cause the appearance of the repetitive frequency in the spectrum, thus violating the emission regulation limits illustrated in figure 2.10. This implies that the technique of transmitting pulses most be combined with a modulation scheme to prevent a repetitive pattern in transmission, thus staying within the regulatory levels and not appearing in the

frequency spectrum. As this thesis is based on the reception of dual sloped pulses the illustrations also contains dual sloped pulses.

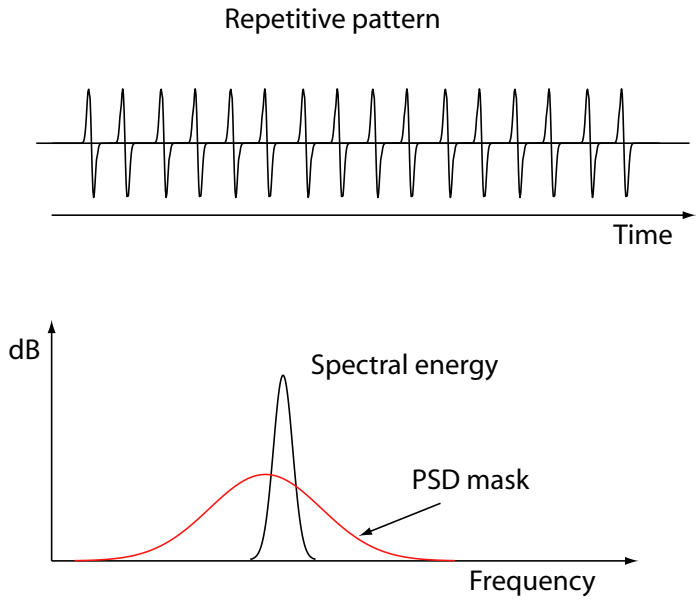

Figure 2.10: Illustrates the effect of sending pulses in a repetitive pattern, where the spectrum energy exceeds regulations.

2.2.1 Modulation

Modulation is the technique of modifying a signal wavelet or impulse in such a way that it carries information. Through the process of developing UWB-IR technology various encoding/modulation techniques have evolved.

The following techniques are commercially useful as UWB-IR modulation enabling a wide range of implementation possibilities.

1. Pulse Position Modulation (PPM)
2. M-ary Bi-Orthogonal Keying modulation (MBOK)
3. Pulse Amplitude Modulation (PAM)

PPM modulation involves transmitting pulses at high rates (millions pr. second), with the time between the pulses pseudo-randomly spaced also

called pseudo-noise (PN) time intervals. By applying this technique the signal will be noise-like in both time and frequency domain, hence spreading the energy out in time to maintain the spectrum energy within the PSD mask. This is illustrated in figure 2.11.

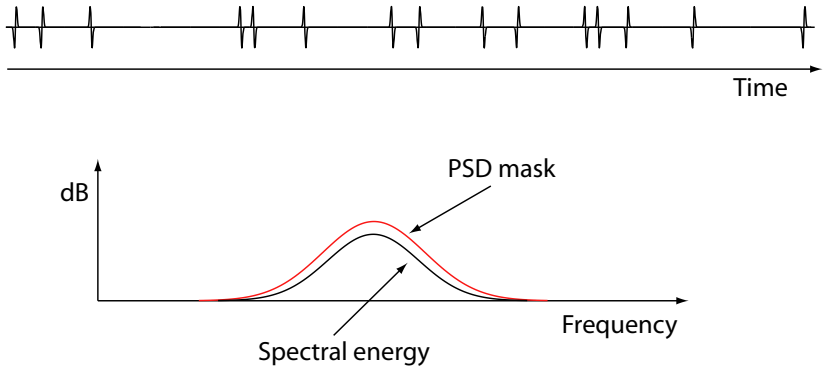

Figure 2.11: Illustrates the effect of applying pseudo random coding on a pulse sequence to maintain control of the spectrum energy.

Systems using this modulation technique have demonstrated impressive data links both for short and long range. It also enables position measurements to be accurate within a few centimeters, and through wall motion sensing radar applications. The modulation techniques error probability P_F in additive white Gaussian noise (AWGN) follows by equation 2.11.

$$P_F = \frac{1}{2} erfc(\sqrt{\frac{\gamma_b}{2}}) \tag{2.11}$$

where erfc is a complementary error function and γ_b is the received signal to noise ratio (SNR) per information bit. By using a fine pitch pulse positioning modulation and combining it with the dual slope pulse polarity which is enabled by the phase detection scheme presented in this thesis, a modulation scheme called MBOK is enabled.

As the **MBOK** modulation is a combination of clever coding and pulse polarity using a length of ternary codes (-1, 0, +1), it can result in a modulation efficiency that approaches the Shannon limit [2]. The use of pulse polarity itself is a coding possibility that applies to the phase detection scheme in this thesis, and is analogous to binary phase shift keying (BPSK) used in conventional carrier based technology.

The bit error probability P_P for pulse polarity coding is given by equation 2.12.

$$P_P = \frac{1}{2} erfc(\sqrt{\gamma_b}) \tag{2.12}$$

By combining the PN PPM modulation with pulse polarity coding the total bit error probability can theoretically be significantly reduced to $\frac{\sqrt{2}}{8} erfc(\sqrt{\gamma_b})$.

While pulse shaping and modulation has a major effect on the SNR itself, it is in combination with an effective detector scheme the total SNR for the front-end receiver is given.

2.3 Receiver topologies and detector efficiency vs. noise

Several different structures has been proposed for UWB receivers, using miscellaneous signal detection techniques. In this section different sampling techniques are compared for efficiency in a template sampling scheme, making it possible to compare the performance between sampling and thresholding. The overall performance of a receiver is limited by its SNR, thus making noise an important factor to focus on.

2.3.1 Noise

Noise exists everywhere, and is a combination of “natural” and “man made” noise. The noise referred to as “natural” is also known as “white noise”, and is the wideband channel thermal noise often idealized as additive white Gaussian noise (AWGN). “Man made” noise is interference from other systems occupying the frequency spectrum. Together the combination of noise sets a limit on the range and capacity of wireless systems.

An expression used to describe the noise in an environment is the noise power density, which is the noise power in a bandwidth of 1 Hz. Described by the equivalent noise temperature and Boltzmann’s constant it makes up the noise to power density that is contributed to the incoming signal by a receiving system. The noise power density in any lossy element, described from quantum mechanics considerations in watts per hertz is given by equation 2.13.

$$N_o = h \cdot f \left[\frac{1}{\frac{e^{h \cdot f}}{k_b \cdot T} - 1} + 1 \right] \tag{2.13}$$

Where h=Plank's constant, K_b=Boltzmann's constant, f=frequency in hertz and T= the absolute temperature in kelvin.

For frequencies that is low enough to comply with the UWB application (3 GHz - 10 GHz), the noise power density expression is simplified and can be reduced to equation 2.14.

$$N_O = k_b T \tag{2.14}$$

Which is a representation of the noise power density for a bandwidth of 1 Hz. This implies the noise power N for any bandwidth to be the noise power density multiplied with the bandwidth B giving equation 2.15.

$$N = k_b TB \tag{2.15}$$

This relation implies that the wider the bandwidth the more noise power is applied to the signal.

2.3.2 Receiver efficiency

The receiver efficiency describes how well the signal detector scheme copes with the SNR at the input of the receiver, compared to the SNR on its output. Thus the receiver SNR which is the relation between SNR in and SNR out, indicates the receiver structures efficiency and robustness to noise. SNR and bit energy E_b to noise density ratio are related to AWGN by taking the bit duration T_b and bandwidth B into account. The SNR in general for any receiver is given by the equation 2.16.

$$SNR = \frac{S}{N} = \frac{\left(\frac{E_b}{T_b}\right)}{N_O \cdot B} \tag{2.16}$$

And when the signal bandwidth is equal to the inverse of the bit duration the SNR is given by equation 2.17.

$$SNR = \frac{E_b}{N_O} \tag{2.17}$$

The receiver efficiency often referred to as the detector efficiency e_C is for digital signals described by equation 2.18.

$$e_C = 10 \log \left[\frac{\left(\frac{E_b}{N_O}\right)_{out}}{\left(\frac{E_b}{N_O}\right)_{in}} \right] \tag{2.18}$$

This equation is a general expression for the SNR in a system, and by looking at a receiver scheme with template mixing an equivalent expression can be written. The system this expression applies to is illustrated in figure 2.12 and is a system where the signal from the antenna is filtered by a filter with the response h(t). The signal is then mixed with a template p(t).

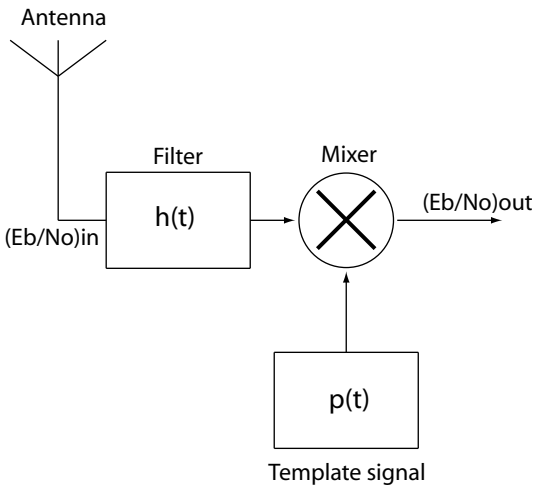

Figure 2.12: Shows a basic template mixing structure with an antenna and a filter at the input before the mixer.

The equivalent expression for analogue signals can be written by applying equation 2.16 with equation 2.18. In order to simplify, the filter is made an "all pass" filter, and the signal supplied to the mixer from the antenna is s(t), making its impulse response remain an impulse. Giving the following relation:

$$h(t) = \delta(t) \; with \; p(t) = s(t) \tag{2.19}$$

where the $\delta(t)$ is a Dirac delta function of the template which is expected as input. This receiver structure is referred to as "matched template" receiver or a "matched filter". Provided the filter is causal the receiver detection efficiency e_C of such a receiver can in general be described by equation 2.20.

$$e_C = 10\log\left[\frac{\left|\int\int s(\tau)\cdot h(\tau-t)d\tau\cdot p(t)dt\right|^2}{\int s(t)^2dt\cdot\int\left|\int p(\tau)\cdot h(\tau-t)d\tau\right|^2 dt}\right] \tag{2.20}$$

and is maximized when:

$$C \cdot \int p(\tau) \cdot h(\tau - t) d\tau = s(t) \tag{2.21}$$

where the constant C is the RMS value of the signal s(t). The receiver efficiency described in equation 2.20 implies that the shape of the signal s(t) and the filter response relative to the template p(t), strongly affects the level of detection/correlation in the mixer. From the expression it is obvious that the timing or synchronization between the template and the signal is essential to obtain an efficient sampling.

The use of an rectangular pulse as a sampling template can relative to the synchronization and timing result in a output equal to or close to a rough shape of the input pulse itself. This can be compared to the continuous-time thresholding technique presented in this thesis. The only difference is that the technique presented in this thesis is independent of the sampling template and thus the synchronization issues.

As an receiver usually is constructed with an amplifier as the first element, makes the design of such an element crucial, since its contribution to the total SNR propagates through the whole receiver structure. The amplifier and the issues related to its design is presented in the next chapter.

2.4 Summary

Due to the FCC regulations on ultra wide band signal emission, the spectrum response of the signal is located within the PSD mask, which implies a restriction between 3.1 GHz and 10.6 GHz, and with a spectral power that is less than the one for white noise. If the UWB signal were to appear in the frequency spectrum outside regulation limits it would cause interference or jamming for all other communication within the same frequency band. This is avoided by using Gaussian shaped pulses, by spreading the pulses pseudo-randomly in time and by controlling the amplitude of the pulse, which for one emitted pulse is between 3 dB to 10 dB larger than for the white noise. The amplitude, duration and phase of dual sloped pulses are properties of the UWB pulses that can be utilized for detecting the signal in a receiver front-end scheme. Thus reducing the bit error probability and increasing the receiver structures total SNR.

Chapter 3

Wide band low voltage low noise amplifier (LNA)

In a radio receiver front-end the LNA is one of the most essential components which performance affects the performance of all the following circuitry. The UWB impulse radio area of application sets certain requirements to the LNA design. Three main properties feasible for the LNA is a wide-band operation of 6.5 GHz, a fairly flat gain within the operating band and a low noise factor giving an acceptable signal to noise ratio (SNR). In this chapter several different topologies within single ended and differential input approaches are discussed and compared for performance. The decision for which design that will work best for this area of application is made by focusing at the gain factor and frequency performance. The noise issue, matching issues and power consumption are also briefly discussed. A brief introduction to earlier work is also done.

3.1 Earlier work

There has been a lot of publication regarding LNA and front-end designs for UWB and UWB-IR receivers. There exists both single ended and differential topologies, but few of the approaches have been implemented in a pure CMOS process. The majority of the approaches are implemented in Bi-CMOS or SI-Ge processes, where most of the implementations in pure CMOS technology are operating at a lower frequency band e.g. 3 GHz -7 GHz [12, 13, 14]. By searching the IEEE database there were two publications on LNA front ends for UWB applications which operated in the 3.1 GHz to 10.6 GHz frequency range [15, 16], where only one seems to be implemented. The implementation is done in a 0.18 μm CMOS techno-

logy from IBM, achieving 10 dB in gain within the operating frequency band.

3.2 Single ended approach

3.2.1 Common source

The single ended approach can be a trivial design which in its simplest form can consist of only one transistor and a resistor [17]. Since the amplifier is a transconductance amplifier, its gain is relative to the input transistors transconductance. The most efficient transistor to use in such a configuration is the n-channel transistor due to the better mobility.

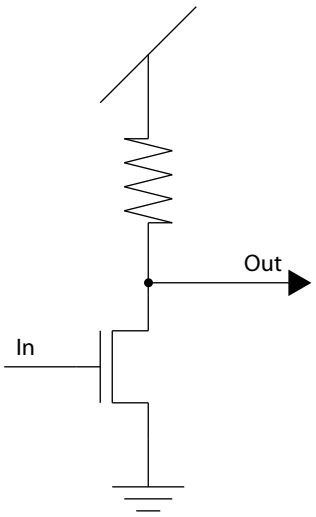

Figure 3.1: Schematic of the common source amplifier with passive load.

By using a n-channel transistor as input and a resistor as a load to regulate the current showed in figure 3.1, the gain of the amplifier can be simplified to the form given in equation 3.1.

$$A_V \simeq -g_m * r_{ds} \tag{3.1}$$

Where g_{m} is the transistor transconductance and r_{ds} is the output impedance of the amplifier. The common source is a single end amplifier at its simplest form, but with simple modifications it gains properties that makes it popular as a single ended approach in a variety of applications.

The modifications thought of is the folded cascode and the telescopic cascode configurations, and there are two major reasons for their popularity [18]. First of all they can have a quite large gain for a single stage amplifier approach due to the large impedances at the output. Second that by using cascode stages the voltage across the input transistor is limited. This technique is presented shortly. This minimizes any short-channel effects which is an important issue due to the technology used in this implementation.

The resistor illustrated in figure 3.1 can be replaced with a transistor, this is also known as an active load. The advantage of using active load compared to passive is higher gain due to the large effective load resistance [19]. Due to the low supply voltage of 1V the possibility to stack transistors is limited, one design technique that complies to this issue is known as folding.

3.2.2 Folded cascode

By applying two single transistors to the common source with active load, the configuration gain properties making it a good solution for low supply voltage solutions. The folded cascode configuration showed in figure 3.2 has a n-channel common source input transistor, an active load and a p-channel folding transistor. This is called a folded cascode stage [18], where “bias2” and “bias3” from the figure sets the point of operation on the output node. The output voltage from the first stage is the source node of the p-channel folding transistor, thus functioning as the “supply” voltage of the folding stage.

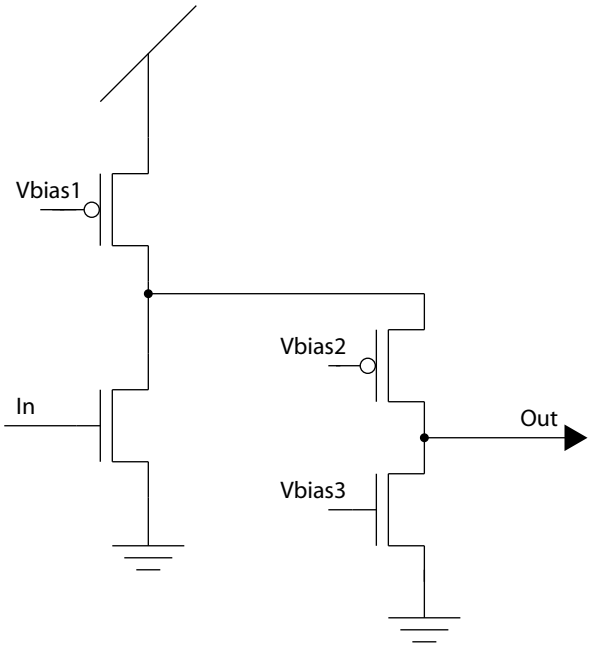

Figure 3.2: Schematic of the folded cascode amplifier with an active load and p-channel folding transistor.

The advantage of this configuration is that it can allow the dc level of the output signal to be the same as for the input, and that it applies to configurations with a low supply voltage. A drawback is that this configuration usually is slower than the telescopic cascode amplifier. This is due to the difference in transconductance, which is roughly tree times larger for the n-channel transistor than the p-channel transistor used for folding.

3.2.3 Telescopic cascode

The telescopic cascode is a one transistor modification of the common source with active load configuration. A n-channel transistor is added in series with the input transistor, at the source side as shown in figure 3.3. By using cascode stages the voltage across the input transistor is limited, which implies that channel shortening effects is reduced. It also implies that the input transistor is isolated from the output capacitive load, thus eliminating the Miller effect [18].

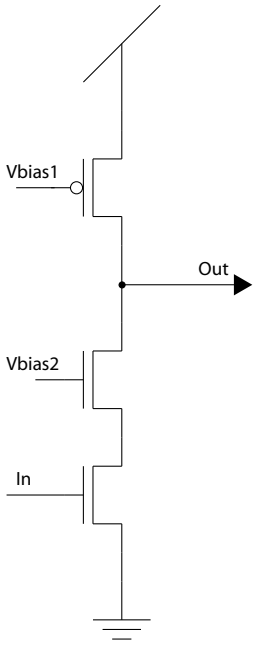

Figure 3.3: Showing the schematic of the telescopic cascode amplifier with active load.

The configuration has a advantage on the folded cascode stage by using two n-channel transistors compared to applying a p-channel transistor and reducing the mobility factor. The gain of the configuration is given by its transconductance and the output impedance which in a simplified form assuming all elements are matched can be described by equation 3.2.

$$A_V = \frac{V_{S2}}{V_{in}} \frac{V_{out}}{V_{S2}} \simeq -\frac{1}{2}(\frac{g_m}{g_{ds}})^2 \tag{3.2}$$

Where V_{S2} is the node between the two lower transistors, g_m is the combined transconductance and g_{ds} is the output admittance.

The single ended input approach is simple and commonly used, but another popular approach is the differential input to single ended output approach.

3.3 Differential approach

3.3.1 Differential pair

To realize a differential input a commonly used differential transistor pair is used together with a biasing current source controlling the "tail-current". A current mirror is added as a active load, making the differential input single ended output configuration possible to realize. The schematic of such an topology is illustrated in figure 3.4.

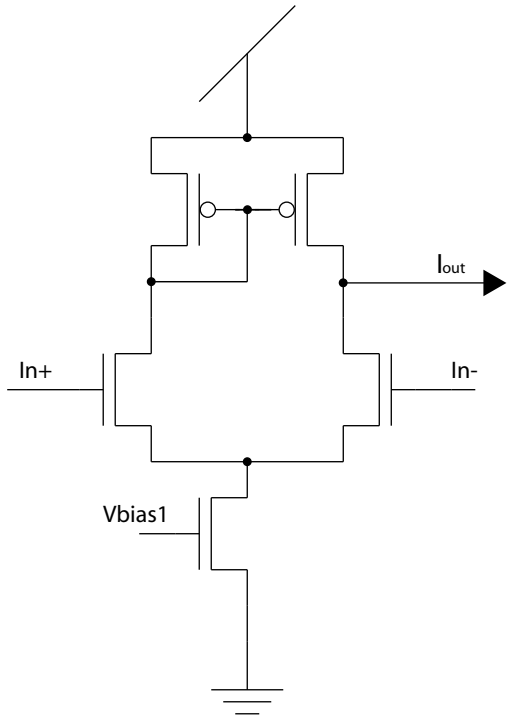

Figure 3.4: Schematic of the differential pair amplifier with current mirror and tail current limiter.

The input voltage is defined in equation 3.3, and the output current is given by equation 3.4. By assuming that the output impedance is purely resistive the gain of the configuration is given by equation 3.5.

$$V_{in} \equiv V^{+} - V^{-} \tag{3.3}$$

$$i_{out} = g_{m1} * V_{in} \tag{3.4}$$

$$A_V = \frac{V_{out}}{V_{in}} = g_{m1} * r_{out} \tag{3.5}$$

Where g_{m1} is the combined input transconductance, i_{out} is the output current and r_{out} is the output impedance. The differential pair approach gives high gain an differential input to single ended output, which can be combined with RF-input schemes for effectively utilizing the differential input. By using two input transistors the input gain can potentially be doubled compared to a single ended input approach. And using differential inputs also implies that any common mode noise is rejected, but this rejection is reduced in high frequency operation, due to the increasing common mode gain at high frequencies. However the topology also has a major drawback to it. The model described implicitly assumes that the time constant at the output node is much larger than the internal time constant due to parasitic capacitances at the source node of the "tail" transistor (Vbias1) and the differential pair transistors. But this does not apply when high frequency effects are important, as it is in this area of application.

3.3.2 Differential pair with folded cascode

A differential pair with a folded cascode and second gain stage was attempted as a possible solution, but it was limited by the frequency performance of the differential pair configuration, and therefore discarded as a possible solution for implementation in the technology used in this thesis.

3.4 Simulations

By comparing the topologies discussed, it is clear that there is a trade off between frequency and gain, and that there is a big difference in performance. The first simulation in figure 3.5 shows the AC response of the common source with active load, differential tailed pair and the telescope cascode, simulated between 100 MHz and 100 GHz.

The simulation is performed with the schematics described in appendix A, in the same environment with a capacitive load of 10 fF. From the simulation results it is clear that the telescope cascode approach is the one with the highest gain within the range of operation. The differential approach has a relatively flat but low gain, less than the common source approach with a higher gain but lower frequency response.

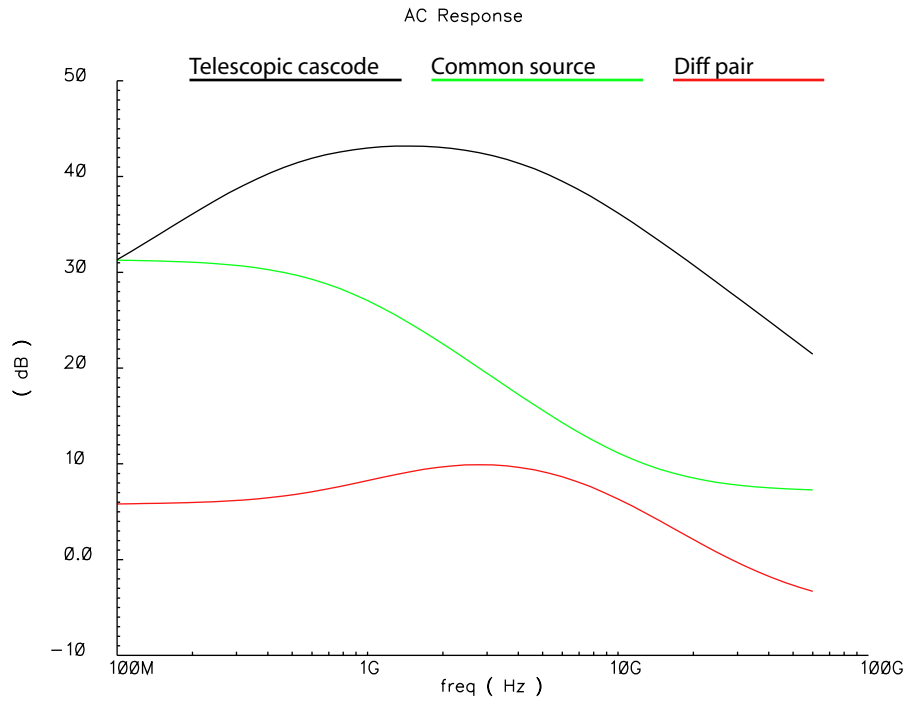

Figure 3.5: AC simulation of the LNA schemes, showing the telescopic cascode in black, common source in green and differential amplifier in red.

The next simulation is a transient simulation (figure 3.6) of the same topologies and with a sinusoidal input signal with a offset at 600 mV and amplitude of 10 mV. The environment is the same as for the previous AC simulation, which gave the best result for the different topologies.

The different DC levels in the simulation results can be adjusted by changing the sizes of the transistors, level of input signal and bias voltages. The telescopic cascode approach is the easiest to adjust, and the one giving the highest gain. By connecting the telescopic cascode amplifier with the serial connected capacitor and by adding a capacitor to ground on its output, it is simulated in its operating environment. The simulation reveals that the gain stays above 30 dB in the range between 3.1 GHz - 10.6 GHz, and with a highly adjustable gain level achieved by tuning the gate voltage on the cascode transistor, shown in figure 3.7.

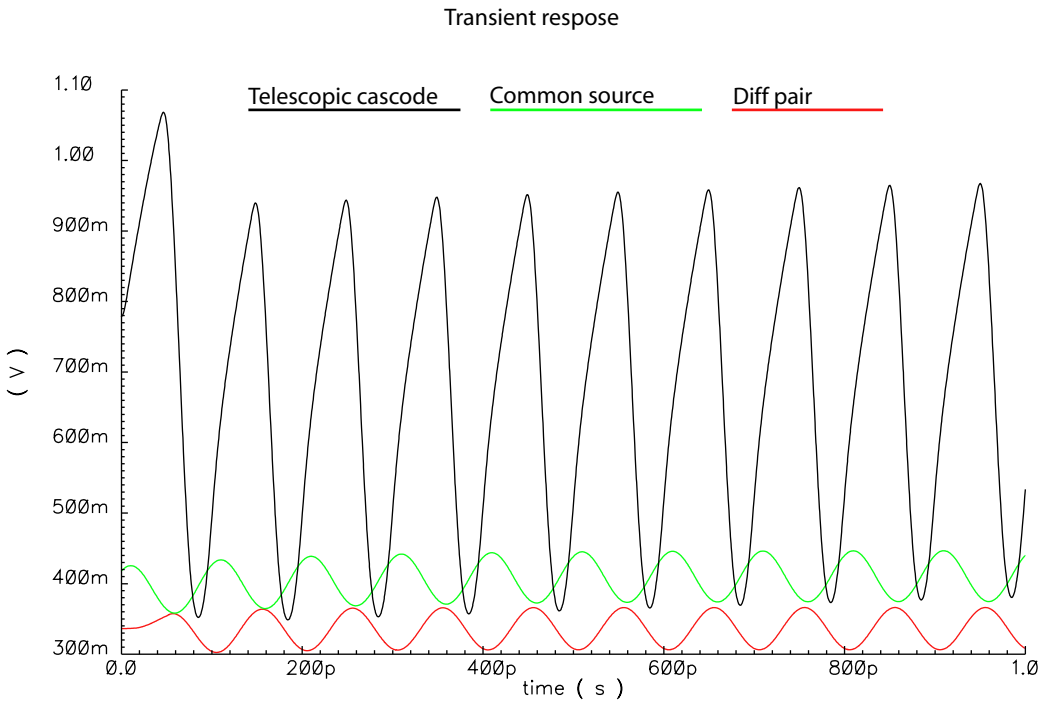

Figure 3.6: Transient simulation of the LNA schemes, showing the telescopic cascode in black, common source in green and differential amplifier in red.

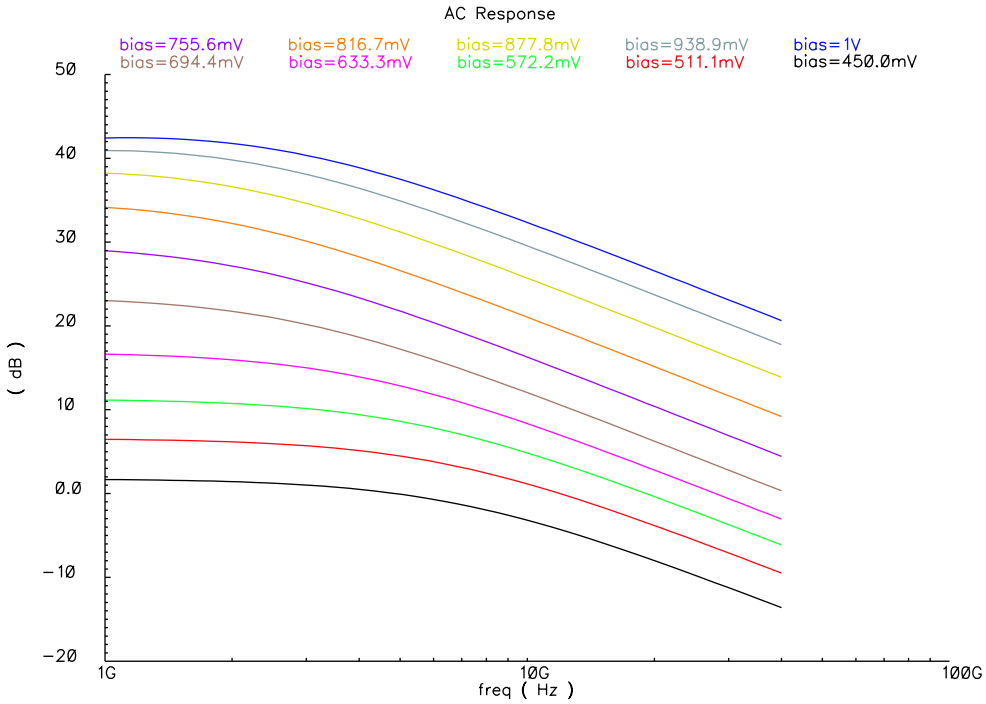

Figure 3.7: Parametric AC response of the telescopic cascode amplifier with linear steps of the bias voltage between 450 mV and 1 V.

3.5 LNA selection

3.5.1 Trade-offs

A LNA can be achieved by using a lot of different designs, but with a frequency range from 3.1 GHz to 10.6 GHz, and with a supply voltage of approximately 1 Volts in a standard CMOS process, it narrows down. Due to the high operating frequency and the short channel effects in the fine pitch process, it is a difficult task to obtain sufficient gain at the same time as the frequency response of the amplifier is maintained. The limited supply voltage brings on another challenge when it comes to stacking transistors on top of each other, as in telescopic designs. All these factors combined are limiting the amount of different design approaches possible for implementation.

A lot of different approaches were tried out for the LNA design, they were all based on either the differential pair or the cascade approach. The differential approach has an advantage in high gain and common mode noise rejection, but was limited by the high frequency operation. A fully differential approach, with differential thresholding topologies could have been a solution, but was not further explored due to the differential pair low gain in high frequency operation. All designs had limitations due to the low power supply, and by trying out a folded cascode approach which reduces that problem, the low gain during folding was getting problematic. It resulted in a design that collapsed on its own parasitic capacitors, as a result of the low folding gain. The telescopic cascode approach shows a high gain and frequency operation and has an advantage since the cascode transistor eliminates the miller effect. By doing Monte Carlo simulations in every corner with temperatures of 0, 30 and 60 degrees Celsius it was possible to verify how affected the performance of the LNA can be by mismatch and temperature. Additional corner and Monte Carlo simulations are added in appendix C. The simulations show that the performance is severely affected in low temperatures and weak NMOS structures. Some of the effect is probably due to biases which need to be adjusted to compensate for temperature.

3.6 Noise

The topology selected for LNA will affect the amount of noise created by the device, and the amount of noise amplified an relayed into the other circuits. In a design with a low supply voltage, accuracy and noise must often be traded for maximum voltage amplitude. This section is based

on the book from Motchenbacher [20]. By using MOSFET transistors it is possible to create a high impedance input, which is preferable due to the low shot noise I_n described in equation 3.6. An disadvantage of using MOSFETs is that the flicker noise is 10 to 100 times larger than in a Bi-CMOS transistor. The flicker noise has a $\frac{1}{f}$ characteristic and is described in equation 3.7. All transistors have a thermal noise due to the channel resistance, the thermal noise created by a device is described by equation 3.8.

$$I_n = \sqrt{2qI_{Gss}} \tag{3.6}$$

$$I_f^2 = \frac{K_F I_{DQ}^{A_F}}{f C_{OX} L_{eff}^2} \tag{3.7}$$

$$V_n^2 = 4kT\gamma g_m r_0^2 \tag{3.8}$$

Where I_n is the shot noise, q is the electronic charge (1.602×10^{-19}Coulombs), I_{Gss} is the DC reverse saturation gate current, I_f is the flicker noise current in the drain-source channel, K_F is the flicker noise coefficient, I_{DQ} is the quiescent drain current, A_F is a constant, f is the frequency in Hz, C_{OX} is the gate oxide capacitance, L_{eff} is the effective channel length, V_n is the thermal noise voltage, k is Boltzmann's constant, T is the temperature in Kelvins, γ is the constant relative to the channel length described by Razavi to become larger as the technology develops [21], g_m is the transconductance and r_0 is the channel resistance.

An other important expression is noise bandwidth, that describes the noise relative to the input gain bandwidth, and not signal bandwidth. Which implies that the input stage gain bandwidth should be as equal as possible to the signal bandwidth. The flicker noise with its $\frac{1}{f}$ characteristics should not be an issue due to the high frequency operation, neither is the thermal noise since it is frequency independent, though it can be reduced by designing longer transistors. The largest noise source from the devices should be the shot noise, which increases linearly from a certain threshold frequency. The contribution from all noise sources included noise at the input, makes up the total equivalent input noise, which is multiplied with the LNA gain to make up the noise on the output of the LNA. Thus making low noise considerations through out the design of the LNA is important.

Eric A. Vittoz also address noise in amplifiers, in the chapter "micropower techniques" from the book [22], where he compares transconductance and noise from gain cells. He indicates that when the values

of a inverter is normalized to 1, the differential pair has $\frac{1}{4}$ the transconductance and more than 8 the equivalent noise resistance, and where the equivalent input noise is more than 9 times larger. This implies that a simple design like the inverter is less noisy than a design like the differential pair, which consists of more transistors contributing to the total noise, and is designed in such a way that the equivalent noise resistance is large.

3.7 Matching

In traditional RF technology source and load impedances of a transmission line are matched to the characteristic impedance of the transmission line to achieve maximum power transfer and minimize reflections. However this may not be optimal for a pulse based UWB signal [23, 24]. Using a common source configuration, which is a voltage controlled current source as a LNA, implies that maximizing the input voltage rather than power, generates the largest output current. Thus a infinite input impedance would be ideal to achieve this. The input reflection coefficient would thus be 1, which implies that reflections appear. But the reflections would not introduce any problems as long as the electrical delay between the antenna and LNA is longer than a pulse duration. It would on the contrary introduce more reflections of a pulse to be used constructively in symbol detection [7, 8]. An other problem is standing waves from known interference sources affecting the sinusoidal interference ratio (SIR). By co-designing the LNA and antenna the SIR can be improved at frequencies where there are known interfering sinusoids. This can be done by placing the antenna close enough to the LNA that transmission line theory can be ignored, thus avoiding SIR fluctuations [24].

3.8 Design dimensions

The design was performed in Cadence schematic Composer and Virtuoso layout editor and simulated in analog environments using Spectre and Spectre RF. Achieving the optimal balance in dimensions of the transistors in the different LNA topologies was not precisely calculated in advance. The design procedure was more in the fashion of optimizing sizes through simulation. The balance between the transistor sizes was roughly estimated. The input transistors which is the major contributor to gain was selected with a channel width of approximately $100\mu m$, and a channel length larger than minimum in order to reduce short channel effects. The transistor regulating the tail current of the differential

pair was designed as wide as both input transistors put together. The transistors sizes for the current mirror, active load and cascode in the different topologies were given an initial value of approximately 10 μm - 20 μm, and further optimized through simulations of each topology to give the best performance. The resulting sizes of the simulated and compared topologies are given in appendix A, and with layout of the telescopic cascode in appendix B.

3.9 Summary

Different amplifier approaches was compared and discussed. The telescopic cascode design were the one that applied most to the requirements needed. It gives high frequency and gain performance as required for the application. The transistor mismatch and parasitics is hard to predict in fine pitch processes. The parasitic capacitances of the interconnections in particular seem to have major impact on the overall performance of implementations designed in such technology [25]. By using large transistors and simulating with large capacitive loads, and by making the design compact with short interconnections, the impact of parasitic capacitors and mismatch is reduced. Even if the gain of the LNA is sufficient in most corners during Monte Carlo simulation, there are corners where it can not cope. The input of the common source amplifier is high impedance and does not seem to need any additional matching when used in UWB-IR applications. The input of the LNA is level-shifted by a voltage follower of the same design as the one described in section 4.2.1.

Chapter 4

Comparator/Quantizer

The input signal has now been amplified coming from the LNA, and is still shaped as a dual monocycle. To be able to do any post processing on the signal the pulse now has to be converted into a digital representation, containing the information on the shape of the pulse. This is usually done by sampling the pulse with a frequency > 2 x input frequency (Nyquist sampling theorem) where the sampling values are post-processed for signal detection. However in this thesis a solution with continuous integration and a threshold trigging is preferred for lower power consumption. The two techniques are briefly discussed and compared for cons. and pros. Different comparator configurations are compared for performance, where the major issue is high frequency operation. The first question is to what extend the incoming, noisy signal could be quantized by sampling compared to simple thresholding. The emitted pulse is mixed with significant noise, so looking for a fixed threshold might not be feasible, either too noisy (low threshold) or too lossy (high threshold).

4.1 Sampling vs. thresholding

Most receiver structures is based on a sampling scheme like the one presented in 2.3.2, regarding receiver efficiency. This brings on the obvious question, which is to what extend a thresholding solution can obtain sufficient signal detection compared to template mixing. Presented in this thesis is a signal detection scheme based on two level thresholding and dual slope verification. The two levels are thresholds triggered by the upper and lower part of the dual sloped pulse respectively. From this thresholding there is generated two rectangular pulses, each with a width relative to the width of the respective slope in the dual sloped

pulse. This is illustrated in figure 4.1. The relation in time between the two rectangular pulses is the same as the relation in time between the upper and lower slope of the original pulse.

By comparing this scheme to the template mixing scheme with a rectangular shaped template, the performance of the two could be roughly equalized. Since the mixing only gives an output within the duration of the rectangular pulse, and by assuming perfect timing, for the whole upper slope of a dual sloped pulse. As will the thresholding technique but independent of timing and the pre-generation of a template, which also consumes additional power. One could therefore draw a parallel to the receiver efficiency presented in sub-chapter 2.3.2 and indicate the thresholding solution to be an improvement in efficiency though under ideal conditions, and especially since it consist of two level thresholding a dual slope verification.

4.2 Threshold trigging

The comparators optimal approach would be a design which desirable has a property of two adjustable trigging levels, and of course high frequency capabilities. By focusing at high frequency operation the obvious topology is the inverter, which is one of the most high frequency capable circuit topologies. The drawback of the inverter is that its switching point is hardcoded and difficult to design accurate at the acquired level due to process variations. The implementation must therefore contain additional circuits allowing the signal level to be adjusted relative to the inverter switching point. This implies that the accuracy of the hardcoded switching point is not an issue anymore, since the level of switching is relative to the switching point. One way to do this is by adding a series connected capacitor which works as a blocking capacitor on the line before the input of the inverter, causing the line between to be isolated in respect to DC. Thus by adjusting the level of the line above and belove the level represented by the switching point of the inverter, as illustrated in figure 4.1.

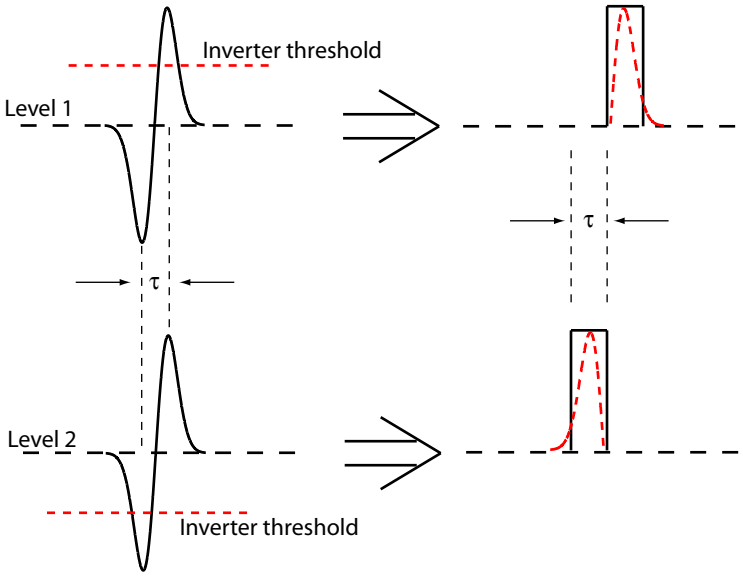

Figure 4.1: Illustrating the the parallel trigging scheme for positive and negative part of the dual sloped pulse, with its digital representations

This enables the possibility to use an inverter with a hardcoded switching point, hence keeping the high frequency capabilities at the same time as an adjustable level is acquired. Instead of adjusting the level of switching in itself, a level shifter approach would make it possible to adjust the signal offset relative to the hard coded switching level, hence adding the properties of an adjustable switching level. By using a balanced inverter the level of adjustment on each side of the switching point is equal.

4.2.1 Level-shifter

A simple level shifting solution would be to add a differential pair construction as the one in figure 3.4, but modified as a voltage follower, with its output connected to the isolated line illustrated in figure 4.2. The high frequency operation of the differential pair amplifier might not be sufficient to be used as a amplifier (sub-chapter 3.3.1), but its bandwidth is higher than 3.1 GHz, which implies that it will filter out the lower frequency content of the signal. The frequency response of the Voltage follower coupled differential pair configuration must therefore be limited to operate at a lower frequency than 3.1 GHz. This can be done by designing the input transistors smaller and/or slower than in a regular amplifier design, limiting their gain. An additional option is by

limiting the tail current of the device and thus limiting the total current through the device (equation 3.4 and equation 3.5).

4.2.2 Thresholding solution

By using the combined solution with a voltage follower as a level shifter on the input of the inverter which is DC isolated in respect to the signal, it is possible to achieve high frequency operation and adjustable level shifting.

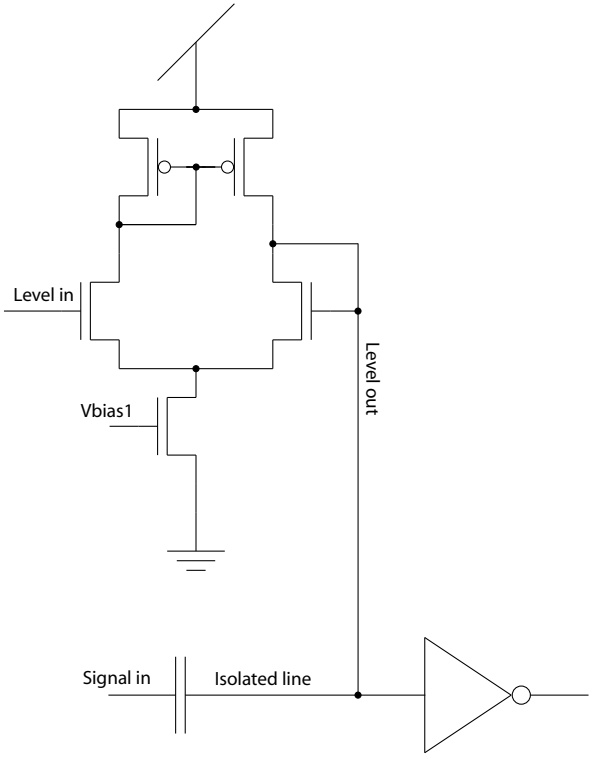

Figure 4.2: Showing the schematic of the differential pair amplifier coupled as a voltage follower and used for level shifting on the isolated line between the capacitor and inverter.

The proposed combination using a voltage follower introduces a high pass filter function, relative to the frequency performance of the level shifter. The high pass filter has an adjustable frequency range relative to the tail current and operating level. The filter should filter out noise in an adjustable frequency range up to a level relative to the tail current and design properties. Simulations of its performance is shown in the

simulation chapter. After the filtering and thresholding the signal can be represented as a rectangular shaped pulse. This shape is preserved by adding buffers or gain stages to an output.

4.2.3 Simulations

The following simulation shows the AC response of the level shifter with a stepped -3 dB frequency adjusted by tuning the tail current.

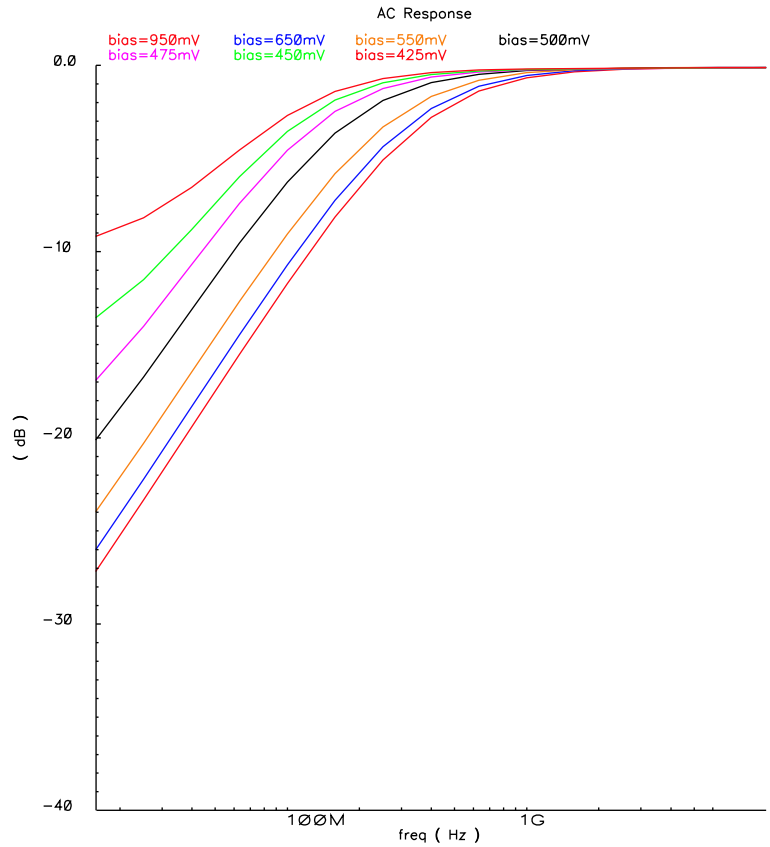

Figure 4.3: Simulation of the AC-response of the level shifter to verify filter function. The bias voltage adjusting the tail current was stepped.

The simulation shows the -3 dB frequency limit to be adjustable between 100 MHz and 500MHz, which is lower than what it should have been for optimal performance. Ideally it should have been adjustable up to 3 GHz.

The most important function of the level shifter is simulated in the following DC simulation, where the bias voltage adjusting the tail current is stepped to see if and how the tail current affects the linearity and/or offset relative to ideal dc level.

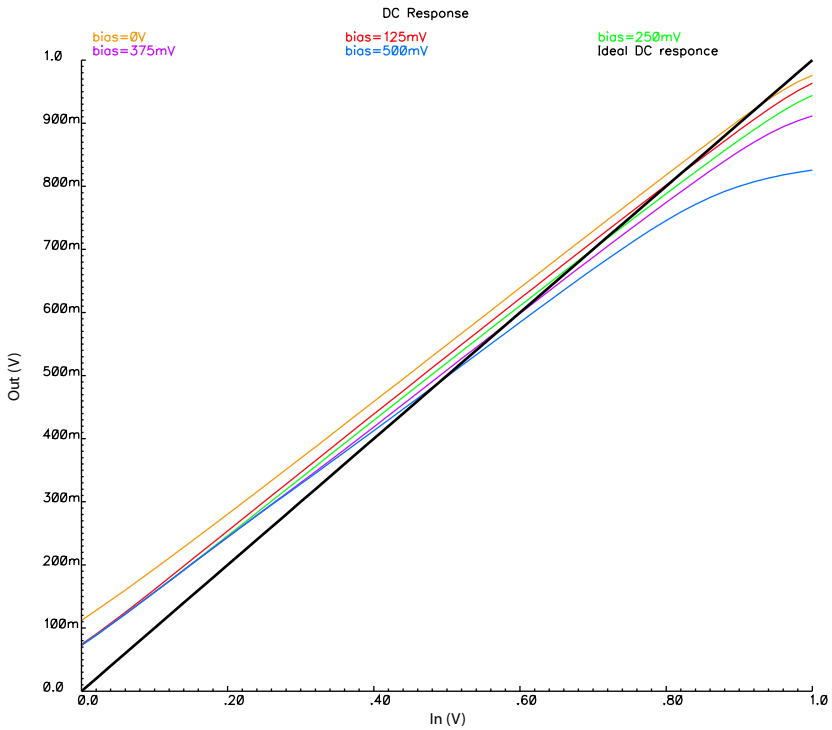

Figure 4.4: Simulation showing linearity and offset between the in and output of the level shifter, by stepping the bias.

The next simulation shows a simulation from a combination of the coupling capacitor, inverter trigger scheme with capacitive feedback and level shifter. Together making out the complete trigger scheme with adjustable level. Transistor sizes and layout of the different blocks can be found in appendix A and B.

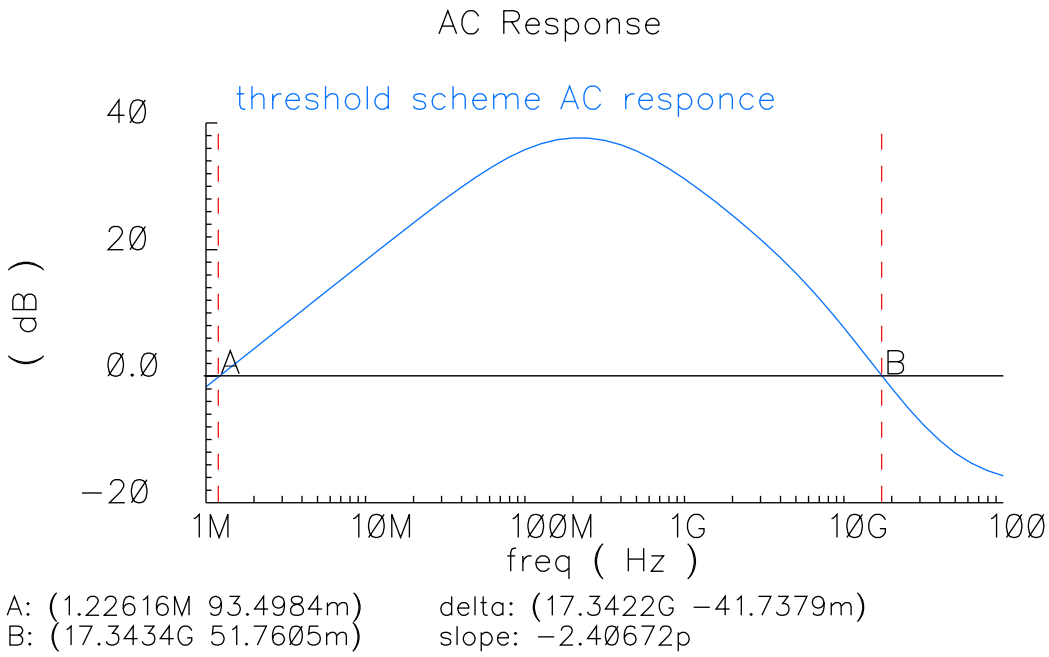

Figure 4.5: Simulation of the trigger schemes AC-response with a unity gain at approx. 17GHz.

4.3 Pre computation buffers and pulse shaping

The system from the LNA to the signal processing circuit was simulated to cope with an input amplitude of 10mV. At this level the LNA was operating at its limits, with a gain of approx. 35 dB. The output from the LNA was not going rail to rail and the combination with a short duration pulse represented a severe problem, since the signal could not make an inverter switch properly. This indicated that the signal would die out after a couple of inverters. The level set on the line was approx 30% from the rail, but even by adjusting the signal level closer to the switching point of the inverter to cope with the low gain, it seemed impossible to obtain sufficient gain from one inverter alone. Different sizes of transistors (balanced inverter) was tested, but by adding larger transistors a larger capacitive load is also added, hence it was not a good approach to make the transistors wider (larger gain) to cope with the issue. A solution to this was using two relatively small inverters connected in series, modified with a capacitive feedback from the output of the last inverter to the input of the first.

The AC coupling between the output and the input increases the dur-

ation of which the input crosses the inverter switching point, thus increasing the gain, illustrated in figure 4.6. This could cause the output pulse to be wider than the original pulse, but this is not an issue since it is the first edge of the pulse that is important for pulse phase recognition.

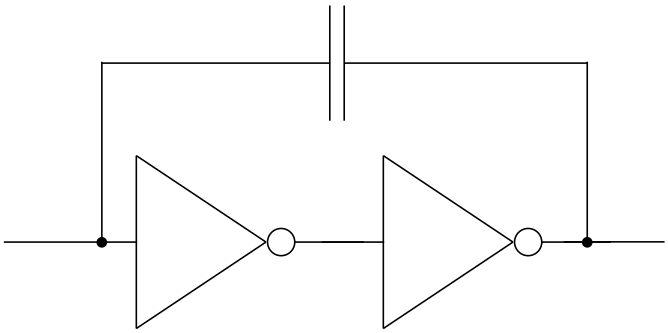

Figure 4.6: Showing the schematic of the topology used for additional gain in one trigger based on inverters

If the feedback was without a capacitor, hence DC coupled to the input, the trigger scheme would be hysteretic. Any input would have had to deliver an larger current than the output of the last inverter in order to shift the input node. This would have caused the level shifter approach to have a fairly large static current. Hence using the AC coupled approach seems feasible to this level shifted trigger scheme. The additional gain applied by the feedback gave the pulse enough duration and gain to be able to drive a inverter, but it was at the limit of not coping. Hence an additional trigger scheme with a level shifter was added i series, and with the same level and capacitive feedback as shown in figure 4.7. In case of any mismatch affecting the gain of the trigger topologies, this would ensure a sufficient gain.

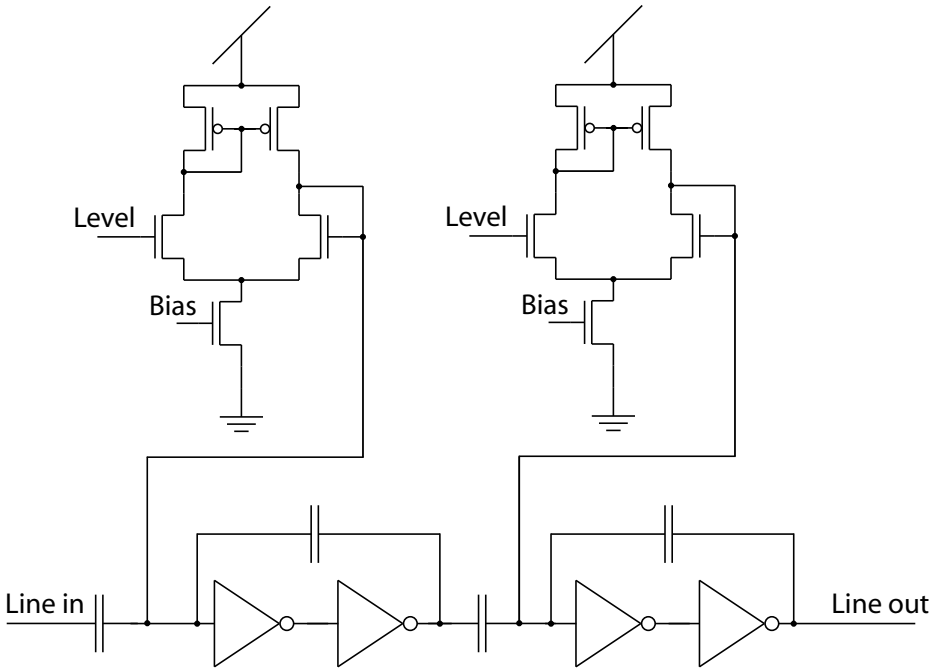

Figure 4.7: Showing the schematic of the topology used with dual trigging scheme for additional gain performance.

One issue is the node between the two series connected inverters with a capacitive feedback (figure 4.6). The node is driven hard and is static at the rails. This implies that the first inverter must drive the node all the way between the rails. If the dynamic voltage range on the node were limited to e.g. ± 200 mV in respect to $\frac{vdd}{2}$ which is the switching point of the second inverter, the delay from driving the node would bee reduced, thus the frequency capability of the switching scheme could be improved.

Further the pulse is shaped with a timed hysteretic function, which fabricates a rectangular pulse of a duration τ equal to the width of one monocycle (100 ps) for any input. The schematic of the timed hysteretic function is shown in figure 4.8, where the time is set by the delay through a chain of inverters. Transistor sizes and layout of the different blocks can be found in appendix A and B.

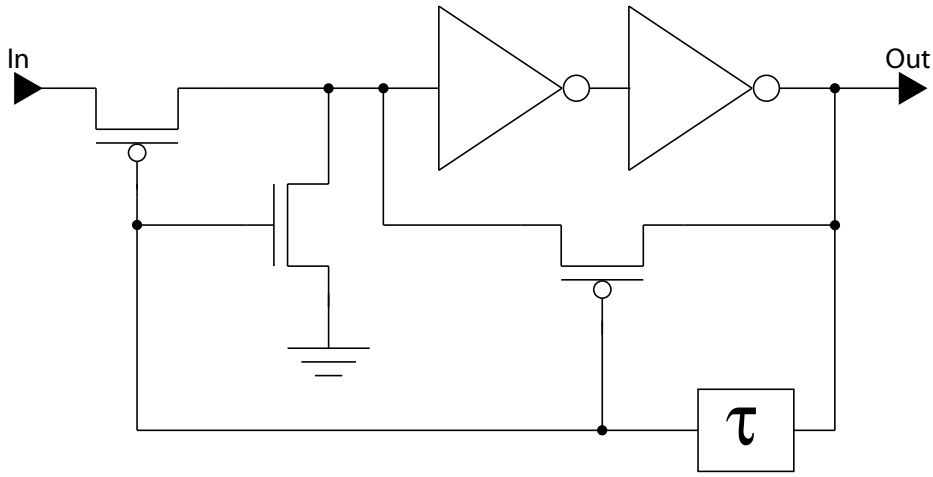

Figure 4.8: Schematic of the timed hysteretic pulse shaping circuitry, where τ is a chain of inverters.

The function of this circuit is to work as a hysteretic switch or a "one-shot", which gives a output pulse for any input crossing the inverter threshold, and at the same time starts its own timer (inverter chain) for resetting itself. This way the pulses constructed will have a duration relative to the delay in the inverter chain for any input. The pulses on the two lines is now pre-shaped and ready for the processing part of the system, where the dual slope is detected and more noise filtered out.

4.4 Summary

By comparing a thresholding circuit for signal detection to a template mixing scheme, it should be possible to directly relate it to the use of a rectangular shaped template for mixing. This would make a single thresholding scheme trigging on one level give the same output as a template mixing using a square shaped pulses as template. As the mixing technique is timing dependent, the thresholding technique is independent of timing and the pre-generation of a template. Thus it consumes less power, and is untouched by the issue of timing. The thresholding solution presented consists of two trigging levels and is combined with dual slope detection making out the rough shape of the pulse. Limited by the capability of the technology used for this implementation, the only possible solution for high frequency trigging on a threshold seems to be an inverter structure. By using a combination of inverters with feedback, an isolated line and a voltage follower, it seems possible to

build an high frequency trigging scheme with an adjustable level. The requirements for the system to cope with a 10 mV input (to the LNA) is fairly conservative. By designing a topology that can cope with inputs down to that level, it will be less vulnerable to mismatch affecting the gain in the LNA and the functionality of the trigging scheme.

Chapter 5

Pulse processing, dual slope phase detection and noise filtering

The dual slope Gaussian pulse and its phase is now represented by two rectangular pulses propagated on two parallel lines, where the phase information is represented by the time shift between the pulses. The triggering on the voltage level of the signal combined with a detection of the phase would combined make up a rough shape verification of the pulse. The remaining processing of the signal is phase detection, which by the representation of the pulse can be realized by using simple digital logic. A simple digital architecture for phase detection is presented and discussed with respect to performance.

5.1 Dual slope phase detection

The information on the phase of the pulse is being preserved in the time difference between the two square shaped pulses, on the two lines. A configuration for the phase detection mechanism has to be timing related, so that only one combination of pulses with the right time shift gives an output. The time shift between the two pulses are a representation of the Gaussian dual slope pulse, hence the time shift is given in advance and can be hard coded. One way to do this is by using a simple logical AND gate with a time delay on one of the inputs seen in figure 5.1, it should be possible to detect the right phase, and by using one more equal but mirrored solution in respect to the inputs, it is possible to detect both phases.

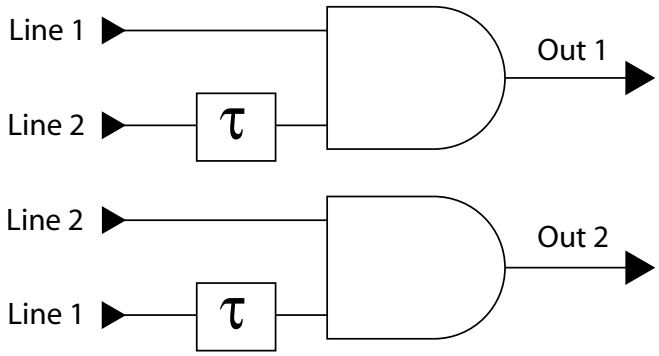

Figure 5.1: Showing the schematic of the digital logic needed for dual slope detection. Both phases are detected.

A simple AND gate is also a high frequency capable digital gate. And with a inverted output and one time shifted input it will give an output only for the right time shifted input. One obvious problem in this topology, is noise and how it will cope in noisy environments.

The thresholding and pulse processing combined indicate a rough shape filtering of the received pulse. This meaning that the shape of the noise signal must be roughly the same as for the pulse itself. If noise for any reason should make the two phase detectors give an output at the same time, the pulse detection would be compromised. But by inserting an logic XOR gate (exclusive-NOR gate with inverted output) it should be possible to discard the result if both phase detectors gave an output for positive phase detection at the same time, seen in figure 5.2.

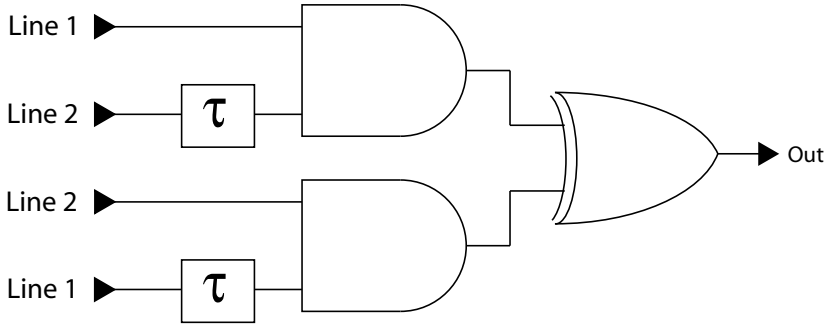

Figure 5.2: Showing the schematic of the digital logic needed for dual slope dual phase detection, with an added XOR to prevent noise from triggering both phases simultaneously.

The topology in figure 5.2 is the one implemented in the front-end presen-

ted in this thesis. The output is now a representation of a rough pulse shape recognition which at this time is represented by a digital output pulse from the XOR gate. The duration of this pulse is 200 ps and is to be relayed to the RAKE correlator, but prior to that the duration of the pulse needs to be shaped according to the properties of the delay line. This is presented in the following chapter. Transistor sizes and layout of the different blocks can be found in appendix A and appendix B.

5.1.1 Simulation

The following simulation shows the phase detection scheme with the noise discrimination in form of a XOR gate disabling the possibility of two phases to appear at the same time.

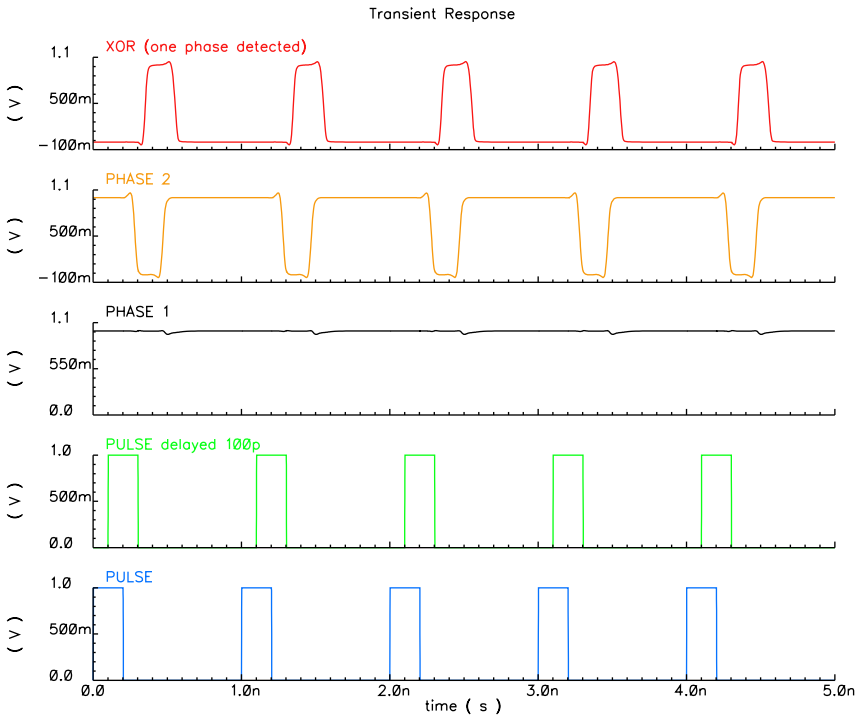

Figure 5.3: Simulation of the phase detection scheme where the two pulses (pulse and pulse delayed) are the two slope representations on the two lines, where one phase is detected due to the time shifted input on the AND gates. The possibility of two phase triggers giving output at the same time is disabled by the XOR gate. The simulation is performed with a bit duration of 2 ns.

5.2 Summary

The dual slope detection logic combined with the XOR logic in figure 5.2 is a novel and robust solution based on simple logic. The first stage correlates the pulse with a delayed version of the pulse on the parallel path, where the delay reflects the preset time delay between the slopes in the pulse, illustrated in figure 4.1. A symmetric solution is used for the opposite phase detection. The topology implements additional noise filtering by using an XOR gate to combine each slope-phase. By definition both phases may not occur at the same time, thus if so happen it must be due to noise and can be rejected by the XOR function.

Chapter 6

Delay line and pulse shaping

As mentioned earlier most approaches to UWB or impulse radio receiver front-ends are based on template mixing, where the signal is multiplied with a template, integrated and quantized. The symbol recovery processing is done by signal processing algorithms in the DSP. However, this architecture is hard to optimize for low power solutions due to very demanding timing constraints and the high sampling rate required to process GHz signals. Explored in this thesis is a continuous-time solution using early quantization and a sampled delay line architecture relaxing timing constraints, where the sampling rate is reduced to something less than 100 MHz. In this chapter the sampled delay line architecture is presented and related to the pulse shaping prior to the delay line. Also presented is a implementation which enables the possibility to select different outputs from the front-end.

6.1 Sampled delay line architecture

The incoming wide-band signal is amplified in a LNA and then immediately quantized. To be able to collect all information in one bin, the sequence of received impulses is delayed using cascaded inverters for a delay line, illustrated in figure 6.1. In this way the primary pulse and all its reflections are located within the delay line at the same time, storing the recent history of received pulses, making it possible through parallel sampling of the delay line to extract the signal with its reflections.

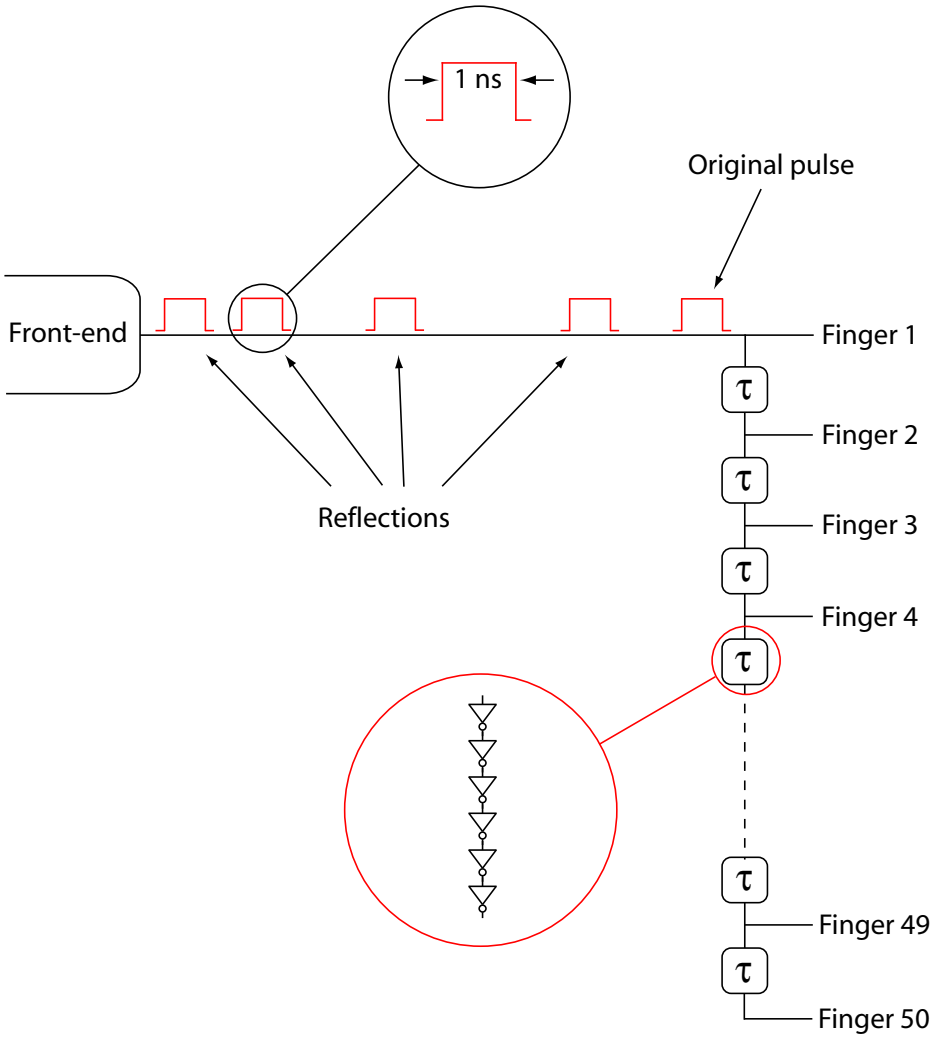

Figure 6.1: Illustrating the pulse and its reflections coming from the front-end and going through the delay line. The delay line is based on inverter structures as illustrated in the figure.

The delay line may now be sampled with a 20 MHz - 40 MHz clock and decoded using parallel correlators in a RAKE arrangement, [7, 8]. The sampling clock frequency must be directly related to the time between the emitted pulses, keeping the pulses making out one symbol in the same finger. An issue here is that keeping the pulses for one symbol within one finger is affected by frequency drifting between the transmitter and receiver. However the drifting relative to the symbol length is so insignificant that it can be ignored. This issue is also presented in the papers [7, 8].

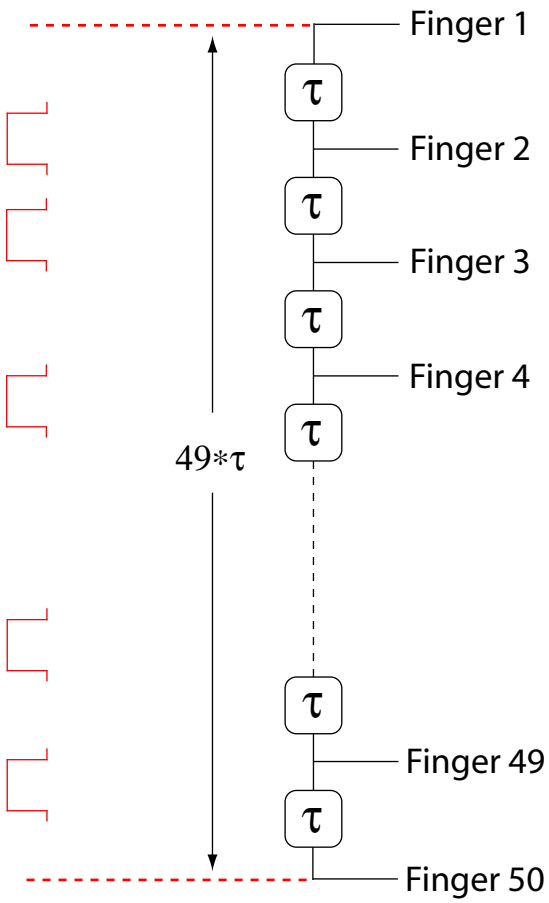

Figure 6.2: Illustrating the length of the delay line and its relation to the time between the pulse and the last possible reflection.

The length of the delay line and the duration of the constructed pulse is related to the total amount of fingers in the RAKE constellation and the time between the first and the last possible received reflection, illustrated in figure 6.2.

6.2 Pulse shaping

The duration of the shaped pulse must be matched to the unit-delay of the delay line shown in figure 6.1. A longer pulse implies a possible reduction of the sampling clock frequency of the delay line. A lower sampling clock will reduce power consumption. Then again longer pulses may mask information carrying reflections for parallel RAKE fin-

gers illustrated in figure 6.2. A reasonable pulse duration seem to be 1ns [7, 8] mostly avoiding masking of multipath components.

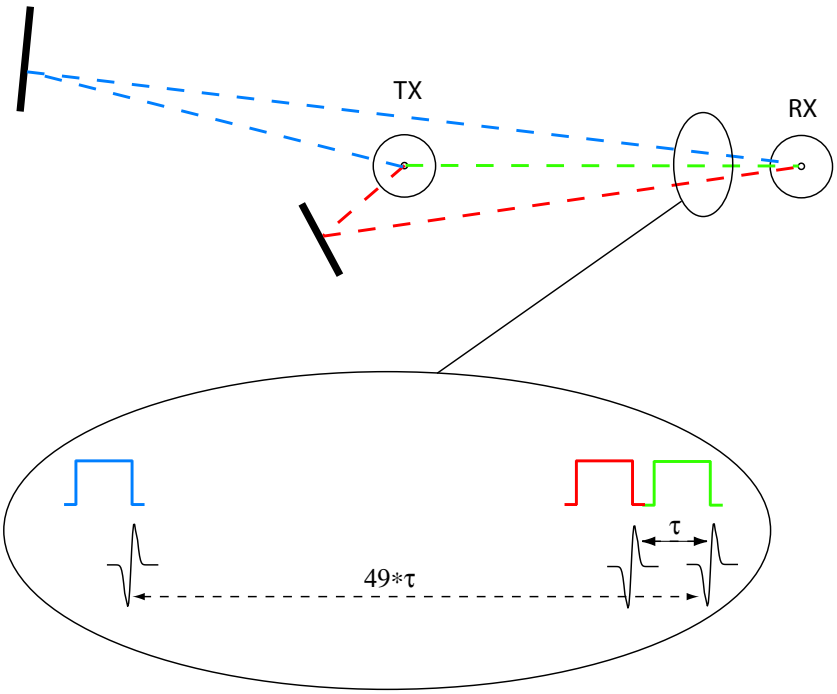

Figure 6.3: Illustrating the relation between the delay line and the first and last reflection in a transmission environment.

The duration of the pulse must be short enough not to mask out reflections at the same time as the total length of the delay line is proportional to the timespan between the first arriving pulse and the last possible reflection. The 1ns length of the constructed pulse and the 49 ns length of the delay line implicates that the reflections used are located within the timespan of approximately 30 cm to 15 m (in vacuum) apart from the original pulse, illustrated in figure 6.3.

6.3 Output buffers, pulse-shaping and output selection

The high frequency signal detection is now complete and the output is a result of the verification process, and the pulse is shaped in respect to the delay line. To be able to choose between different outputs from the front-end, such as only one of the phases, both, or even the signal before

phase detection, it is necessary to implement a switching possibility. This is not only feasible for testing a prototype, but could also be used as a possibility to filter out and use e.g only one of the phases. To apply this property a eight to one multiplexer (MUX) was implemented in the design. The MUX is a pre designed element available in the design kit. This enables a selection scheme of signal routing to the input of the rake receiver. The shaping of the pulse to 1ns which attends to a frequency of 1 GHz is a better frequency of operation for the MUX, thus making the operation of the MUX more reliable [26]. The load applied by the input of the MUX varies between 2.3 fF - 2.4 fF depending on which of the inputs that are used. To make sure there is no driving issues due to parasitic capacitors and load at the input of the MUX, a buffer is added in between the pulse shaping circuit and the MUX. The buffer is added prior to all inputs of the MUX. The buffer used is the same as the one used to drive the pads, thus capable of driving the load provided by the MUX. Details on the schematic and layout of the buffer is in appendix A and appendix B. The MUX is a 8 to 1 out configuration which makes it possible to choose 8 different outputs to the delay line and RAKE receiver configuration, as illustrated in figure 6.4.

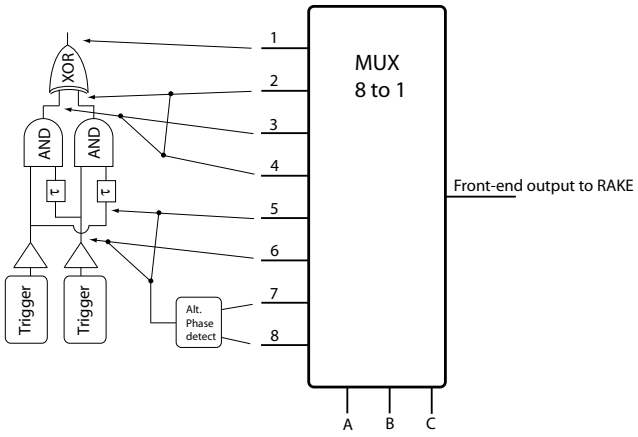

Figure 6.4: Illustrating the MUX and the input signals used in the implementation.

The signals chosen are the output from the phase detection after the XOR gate (nr 1), output from the phase detector for both phases (nr 2 and 3), output from both lines before the phase detection (nr 5 and 6), output from an alternative phase detection circuit (nr 7 and 8) and a output from an AND function between the two last mentioned outputs (nr 4). All signals are shaped with respect to the delay line (1 ns). The output from the MUX is then buffered up to be able to drive the load on

the input of the delay line.

In the next chapter all the different topologies priorly described are combined making out the front-end UWB-IR receiver.

6.4 Summary

By using a sampled delay line architecture with a fairly low sampling frequency compared to a template mixing scheme, the power dissipation is reduced. The issue of timing relative to synchronization is almost annulled due to the relative insignificant drifting in one symbol time period, described in the papers [7,8]. Using a sampled delay line enables the utilization of reflections constructively as signal gain. The use of a MUX to enable the selection of which signal to be sent to the RAKE is a implementation especially useful for testing purposes on a prototype chip, as this is.

Chapter 7

Complete system and chip I/O

Presented in this chapter is the implementation of a combination of topologies presented in former chapters. The combination makes up the complete front-end implementation, which is discussed and simulated to confirm its performance. The implementation is a prototype, which makes the implementation of test nodes important for the later measurement process for verification of the chip functionality. The test nodes used are presented.

7.1 System

This topology utilizes a simple level trigging, pulse shape and phase verification for signal detection and verification. The design can due to its pulse shape detection and XOR implementation be capable of filtering out a significant amount of noise. By assuming transmitted pulses to be a sequence of a charge of one polarity followed by the charge of a opposite polarity and by using pseudo random sequences and statistic symbol recovery in the RAKE constellation. The level of discrimination achieved by the front-end circuit can be sufficient to obtain an adequate SNR in an AWGN channel. The front-end approach uses no sampling clock for template mixing and should therefore consume less power than template mixing front-end approaches. The complete system to be designed on-chip is shown in figure 7.1, where the MUX prior to the delay line is not illustrated.

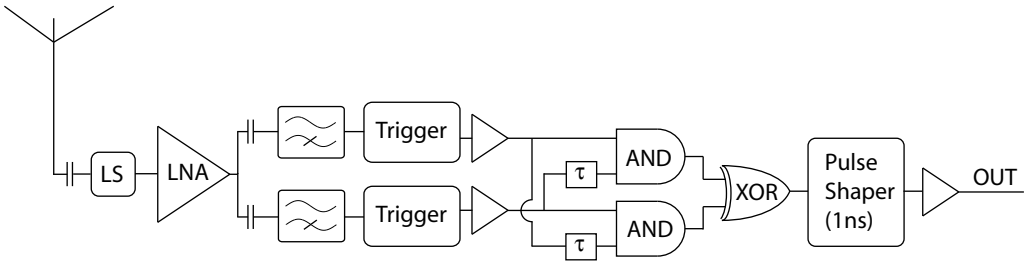

Figure 7.1: The system simulated to confirm functionality.

The input to the system is the level-shifted line to the LNA in figure 3.5, where the level-shifter (LS) will add a high pass filtering property to the signal suppressing low frequency noise. This filtering might not be sufficient and it can therefore be feasible to add an external filter outside the chip, removing noise outside the operating band of 3.1 GHz -> 10.6 GHz before the signal is amplified. The filter should also be designed to mask out the 5.8 GHz sinusoidal interferer. Transistor sizes and layout of the different blocks implemented in the system can be found in appendix A and appendix B.

7.1.1 Simulation

The system functionality was simulated with an input pulse amplitude of 10 mV. The results shown in figure 7.2 indicates a sufficient gain in the amplifier and the trigger buffer circuits to operate with an input signal of 10 mV in amplitude. The simulation results also show the signal processing scheme with dual slope detection and noise discrimination. This simulation was performed at the amplitude limit for the LNA to be capable of generating a rail to rail signal swing. The simulation is performed under ideal circumstances with no noise, but in a realistic environment with noise, the amplitude level of the input signal is increased up to a normal level for UWB impulse radio applications, which is 3 dB - 10 dB above the noise level. This means that the LNA gain is fairly high compared to the input signal, however, the LNA gain can easily be adjusted to the level which is required within the band of operation. By using a RAKE receiver for correlating a pseudo random sequence of pulses, the front-end seams to deliver a feasible level of noise discrimination for UWB impulse radio communication [7, 8].

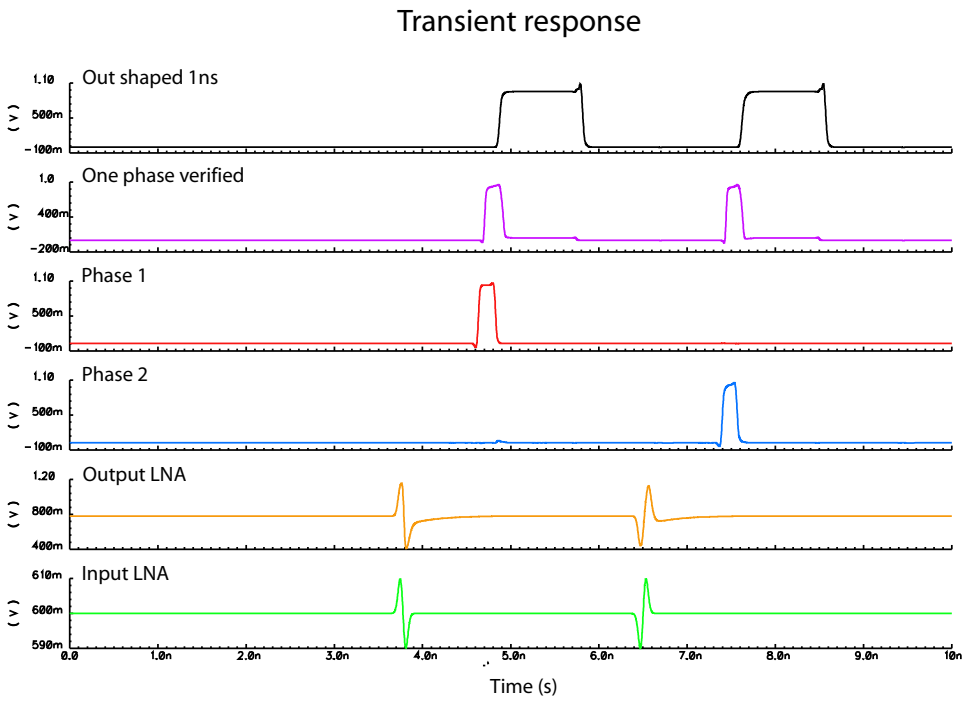

Figure 7.2: Shows a simulation of the processing where the green graph is the input to the LNA, the yellow is the output from the LNA, blue and red is the detection of the two phases (output from AND gates), purple is the output from the XOR and black is the output from the pulse shaper.

The simulation in figure 7.3 shows the complete circuit starting from the bottom trace. The lowest trace in black is input signals with complementary phases. The input dual monocycle has an amplitude of only 10 mV (modulated in MATLAB). The next trace is green and is the output from the LNA. As the signal is split, the next two traces exhibit the output from the complementary slope detectors each detecting the different slope phases. Where the “pre-trigg” trace is the level shifted signal at the input node of the threshold element. The “post-trigg” is the node after the first threshold element and “post trigg 2” is the signal after the second threshold element used as a gain stage. “High-slope” and “Low-slope” are the outputs on each line after additional buffers. The purple and yellow traces are the two phase detector outputs, and the green trace at the top is the output from the XOR gate where one phase is verified as detected. The black trace at the top is the output after shaping the pulse to 1 ns.

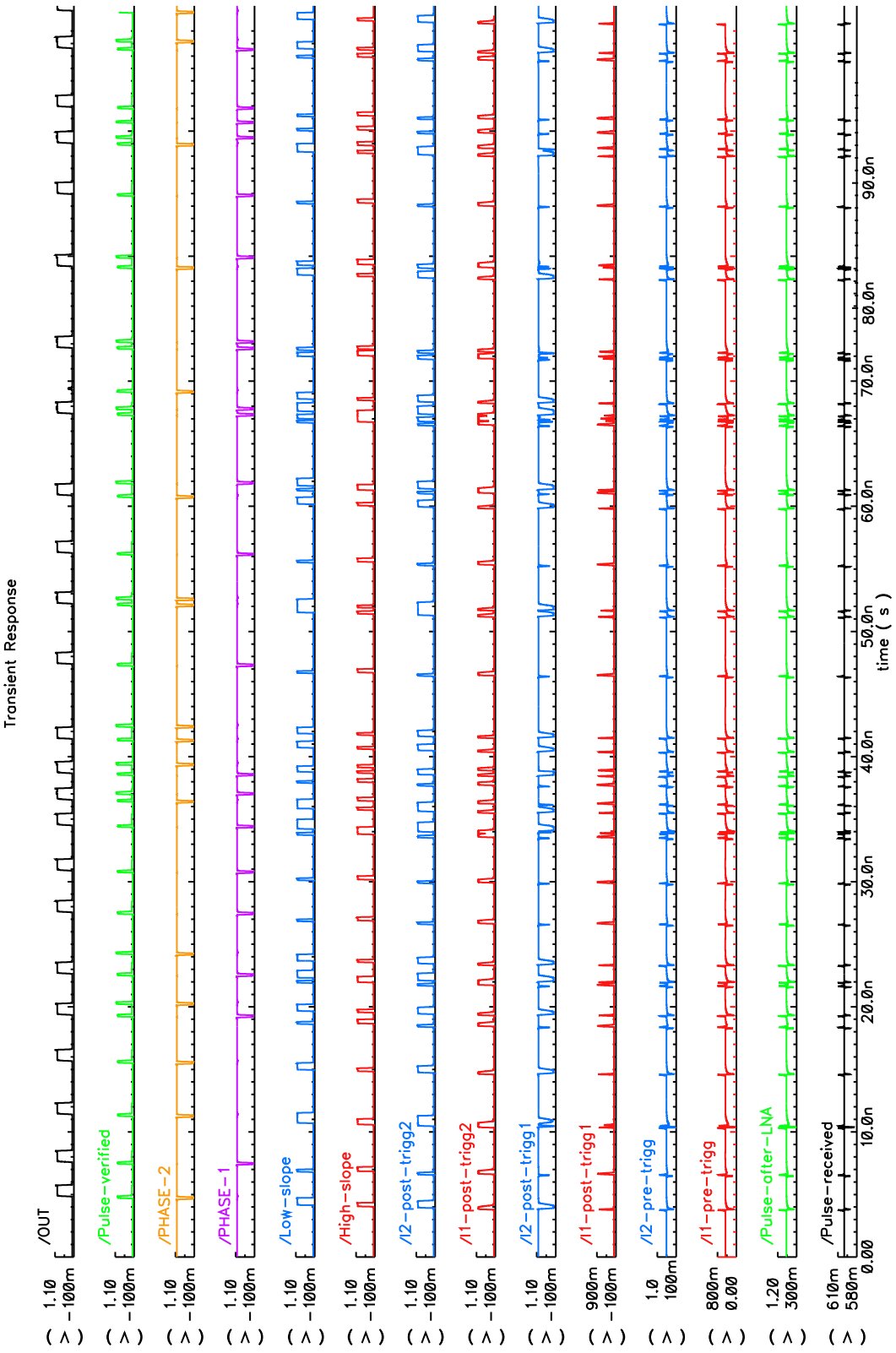

Figure 7.3: front-end processing simulation results

Power consumption is estimated for the dual monocycle input. If assumed three reflections for each pulse and 25 pulses (50%) for each symbol containing 50 bits sampled in the delay line at 20 MHz. The total power consumption adds up to 8.4 μw. Since it is assumed that 50% of the symbol contains pulses and they all are followed by three reflections each, it adds up to be a fairly conservative estimate, though under ideal circumstances.

7.2 Chip I/O

For a designer to be able to verify the design through measurement it is necessary to add testing points in the circuit. Enabling verification for functionality of isolated parts of the implementation. An easy way to add a variety of outputs and save pads is to use a MUX, adding the property to choose between a variety of signals as output. To apply this function an eight to one multiplexer (MUX) is implemented in the design, seen in figure 6.3. For the verification of the chip a total of 10 different outputs are selected which is two apart from the ones coming out from the MUX. The two additional outputs are in case the MUX does not work. The MUX and the two outputs are the ones referred to as number 5 and 6 connected to the MUX in section 6.3. These signals are buffered up and sent directly to two output pads. This means that there are three output pads. Adding the MUX also makes it possible to choose which signal to route to the delay line. The line after the last buffer is split-up in two lines, where one goes to the delay line and the other goes to another buffer. This buffer is for driving the load from a output pad so that the signals can be analyzed off chip.

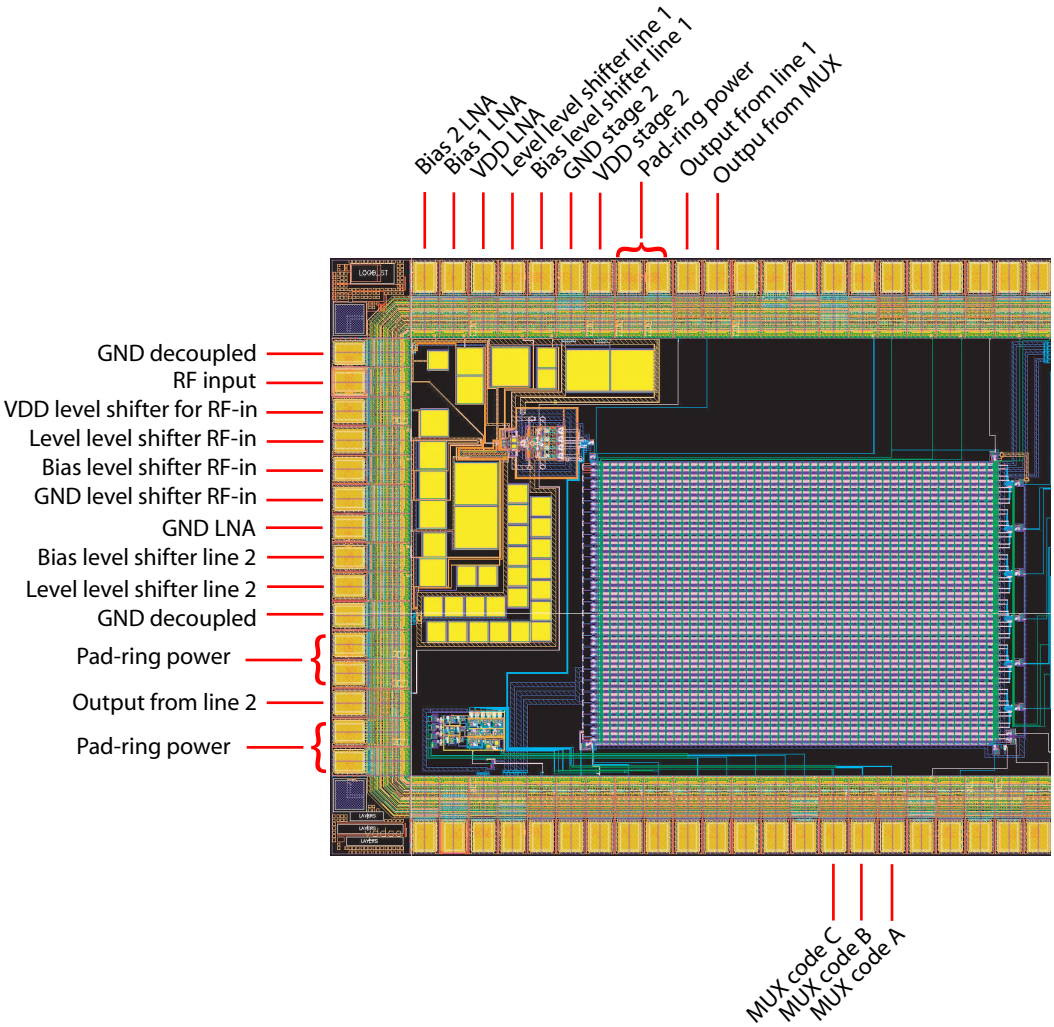

Figure 7.4: Shows the silicon implementation with inputs and outputs highlighted

7.3 Pads

The output pads needed are three, where one is for the MUX output and two are for the two separated output lines prior to the MUX. The required inputs are two (one pr line) because of the level for the level shifters, six because Vdd and Gnd are separated on the level shifter on the input, the LNA and the rest of the circuit. Three for the MUX code, one for the level shifter level on the input and two for the star connected ground and shielding. This is a total of seventeen pads. All I/O signals are labeled

in figure 7.4, where the decoupling capacitors on the DC signals also are visible. The schematics of the system in figure 7.4 were simulated with added capacitors, representing the parasitic capacitors gained due to interconnection lines and layout planning. Hence organizing the layout in such a way that interconnection lines reduce parasitic capacitors is essential.

7.4 Summary

The previously presented circuit topologies was combined in a system making up the front-end. The implementation of the complete front-end topology was simulated as a system to verify the functionality. By using a MUX in the design, several different testing points could be added without using a large number of output pads.

Chapter 8

Implementation

The front-end topology are to be implemented on the same piece of silicon as the RAKE receiver, together making up an UWB impulse radio receiver using a spatial RAKE for continuous symbol correlation. This implies a mixed mode implementation which implies a lot of precautions to be taken regarding noise. In this chapter different isolation techniques used in the implementation are presented. The organization of the different parts of the design on the silicon, and the location of the die in the package combined with package and bonding scheme is discussed.

8.1 Isolation techniques

Due to the high frequency operation, low power supply and sensitive circuit in a mixed mode design, on-chip isolation becomes an essential part of a design setting the limits of operation regarding noise [27]. On-chip isolation is a function of many independent variables, thus different isolation techniques is combined, adding up to the total level of isolation [27]. There are a variety of different isolation techniques available. High speed and low leakage technologies often add properties enabling additional isolation techniques such as substrate doping level and triple well isolation. Most fine pitch processes are triple well or so called “deep Nwell” processes. The technology used for this implementation is a 0.12 um process from STM distributed by CMP [28]. The process is a triple well process including properties of high speed switching and low leakage implementation. The triple well technology also provides an important isolation property making it possible to design isolated wells.

8.1.1 Applied isolation techniques

By using the triple well isolation the analog circuits are isolated from the digital switching circuits. The triple well enables the design of buried layers "NISO" which combined with surrounding deep Nwells isolates an area of p^-. Thus by placing a design in the isolated p^-area and in the Nwell, it is isolated from from the substrate noise as illustrated in figure 8.1.

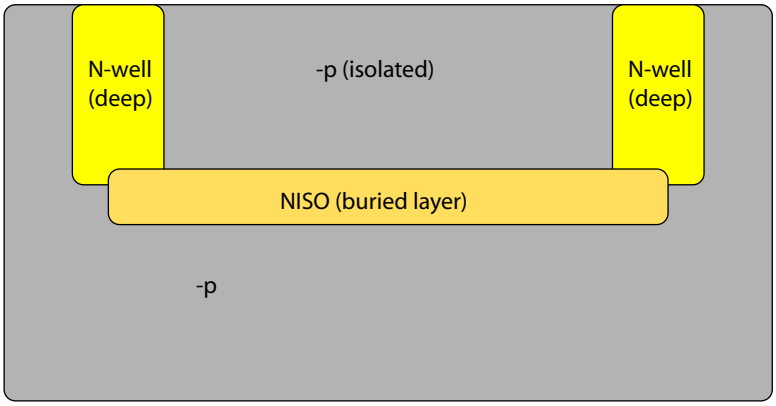

Figure 8.1: Illustration of how the deep n-wells and buried NISO layer creates an isolated section of p^-.

Examples of the effect from using triple well isolation reveals a gain of roughly 20 dB in isolation for a frequency of 10 GHz. The effect is increasing for lower frequencies [27]. The triple well is applied in two different places, one isolating the LNA from substrate, and second isolating the trigging and processing circuit with buffers from substrate. The analogue and digital circuits and isolated wells have separated power rails and power pads to ensure maximum isolation from noise on the power supply and from each other. Nearby generated noise from switching and noise generated externally can be reduced by applying decoupling capacitors, thus lowering the noisy peak currents. This essentially helps isolate sensitive circuits which no longer see the same noise levels. On-chip decoupling capacitors are added for all DC signals and power lines, separated decoupling for each signal. The size of the capacitors wary from 2 pF to 10 pF. Adding shielding for sensitive lines and passive components, providing isolation from on and off chip generated noise is a part of designing effective analog/RF IC layout. The challenge of using shielding is often to determine the layer and potential of the shield [27]. Added in the design is separated shields in metal6 above the LNA design, threshold trigging circuits and the rest of the front-end design.

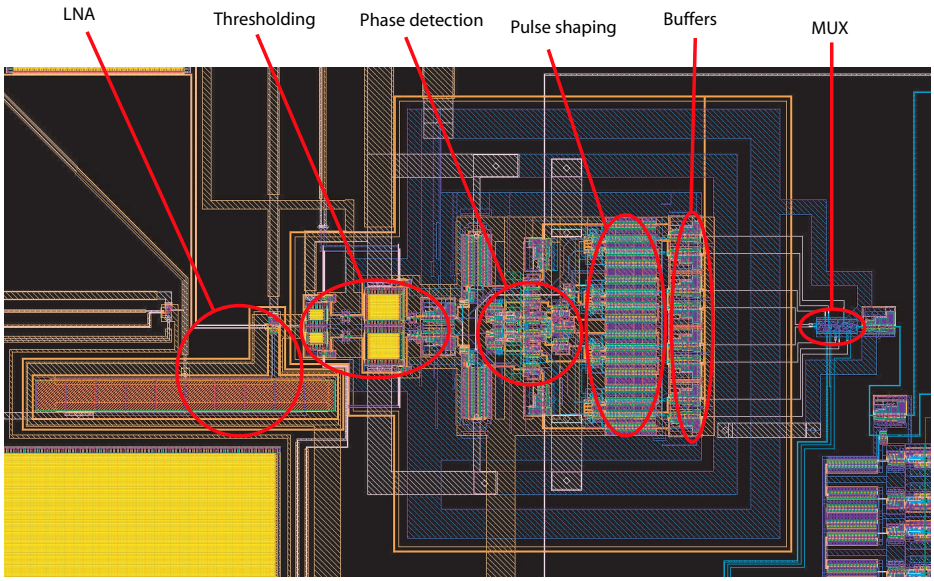

Figure 8.2: Showing the silicon implementation of the front-end with the LNA, thresholding, phase detection, pulse shaping(1ns), buffer and MUX circuitry highlighted.

All analogue lines and power lines are also shielded, this is done using horizontal parallel lines in metal 6 which is up to two times wider than the line its shielding. All the shielding and the ground references from the decoupling capacitors are star coupled in a few separated ground pads. Adding a shield necessarily also means adding parasitic capacitors, which in the case with the analogue, and power lines is a positive contribution adding up as a decoupling capacitor.

The few pads used as star-coupled ground from shielding and decoupling is off-chip star coupled together on the PCB with the other ground pads. Star coupling ground is a technique commonly used to reduce noise due to large ground currents [29]. The separated supplies and ground for the different circuits are all coupled into separated pads. As mentioned earlier the level shifting circuit also adds in as an isolation/noise reduction factor in the design by high pass filtering the signal, presented in chapter 4.2. One of the most critical parts of the design regarding noise is the LNA which is located at the input of the front-end therefor contributing with amplified noise to the rest of the system [20].

8.1.2 LNA isolation and noise reduction

The main contributions of noise from an amplifier design as proposed in chapter 3.5 is discussed in the same chapter, but noise contributions from the power source can also be a problem in a LNA design. Noise contributions from all analog inputs are reduced by adding shielding and decoupling capacitors, the input to the LNA is shielded and should have a filter added externally. When addressing a LNA and noise from power, a commonly used expression is Power Supply Rejection Ratio PSRR. PSRR defines the amplifiers sensitivity to noise in the power supply, represented as the level of noise contributed on the output of the amplifier. The noise contribution from the power supply is reduced by adding decoupling and shielding to the power, where the Vdd and Gnd are assigned separate pads from other supplies. Noise reduction from substrate is reduced by placing the design inside an isolated well, presented in the sub-chapter 8.1.1. The degree of isolation this provides together with a shielding in metal 6 on top of the LNA, separated from other circuits, should reduce the impact of noise on the amplifier.

8.2 System implementation

The complete design and implementation were based on a technology from STM, which is the 0.12um CMOS process distributed by CMP [28]. The pad and packages discussed are also the ones provided in the design kit from CMP. Implementing any system on silicon requires planning, and since this design is implemented on the same piece of silicon as the RAKE receiver created by an other designer, it is important that trade offs are discussed so the final solution can be in everyones favor. The one major question is how to in a best possible way organize the different designs on the silicon utilizing the area in a best possible way. This is of course dependent of the number of pads used in the design, and the total size of the design implemented, but by effectively utilizing the silicon area the production cost is reduced. And since producing prototypes in silicon is not cheap, it makes cost an important issue.

The area available for implementation is set by the number of pads in the pad-frame, which in this case is 74 pads. In the implementation the size of the RAKE structure was dominating the placement on the silicon, limiting the possibilities to organize the structures inside the pad-frame. This is also because the input on the RAKE and the output of the front-end had to be located close to each other. In figure 8.3 the different designs and placement is highlighted together with the critical signal paths, which together limited the options of organizing the designs on

the silicon. It is worth mentioning that the unused space at the top and bottom left could have been better utilized, for instance by placing larger decoupling capacitors there.

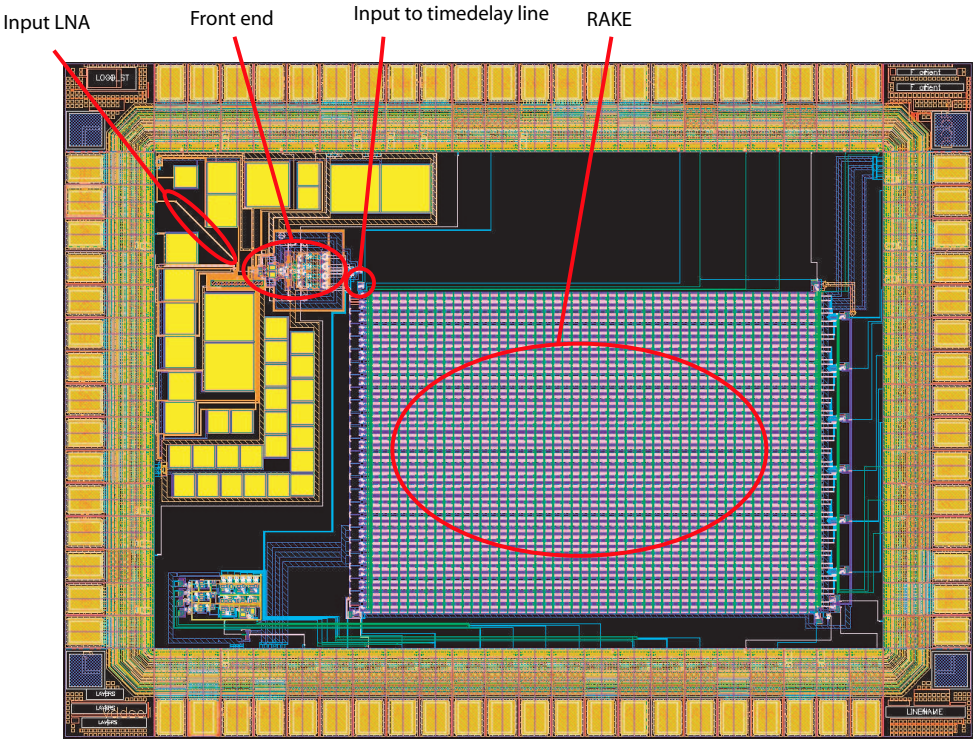

Figure 8.3: Showing the silicon implementation with highlighted areas as front-end, RAKE, input to LNA and input to delay line.

The highlighted signal paths are the input from the antenna, the path between the front-end and the delay line on the RAKE receiver. The output of the front-end is located at the upper left corner of the RAKE receiver, which is where the input of the delay line is located. There is of course a trade off to place the front-end design that close to the RAKE, where the signal path is short.

The switching noise from the transistors in the RAKE can be significant and raise the level of noise substantially compared to having the two designs more separated. Placing the designs in near proximity of each other helps in making the implementation compact and smaller in size, and thus reducing the cost of production. Using the noise countermeasures presented in section 6.1. and by making a compact design placing the front-end close to the RAKE the cost is reduced, the length of the signal path is kept at a minimum and presumably the higher level of

noise will have little or no impact on the functionality on the design. The previously described capacitors used as decoupling capacitors are pre designed and a part of the design kit. This capacitor is designed as a finger capacitors using all 6 metal layers where the orientation of the fingers are rotated by 90° for every second layer, combined with poly and an active region at the bottom connected to ground makes the capacitor symmetric in operation and compact in design. The capacitors are quadratic in design and thus easy to implement as space fillers. The organizing of the capacitors is visible in figure 8.3 as the square shapes surrounding the front-end in the upper left corner. All the signals paths going in and out of the circuit is connected to a pad, which is organized in a pad-frame.

8.2.1 Pad and package selection

The I/O and power pads for the design need to be selected for their properties relative to the outputs and inputs to and from the circuit. All I/O pads and the necessary power pads for the frame makes up the pad-frame. The design rules for the pad-frame regarding power pads [30] for the frame in combination with the I/O pads, implies planning to obtain a short as possible path for critical signals. This applies especially for the input to the LNA, and the front-end outputs where the pulse width is 1ns implying 1 GHz, but also the eight outputs from the RAKE having a signal frequency of minimum 160 MHz [8]. The total I/O and power pads needed for the circuit inside the pad-frame were 56, leaving 18 pads used for power pads to the pad-frame itself. The pad-frame power pad scheme was described in pad-frame design rules from CMP [30]. The 56 pads is a mix of digital and analogue I/O pads, power pads for the circuit inside the frame and a specially designed RF-pad, seen in figure 8.4 where the parasitic capacitance is reduced, for use on the input to the LNA. This pad was specially provided to us from CMP on demand. The different available pads were compared and chosen due to noise properties, ESD protection, applied load and driving properties such as high frequency operation. Details on the different pads can be found in reference [31].

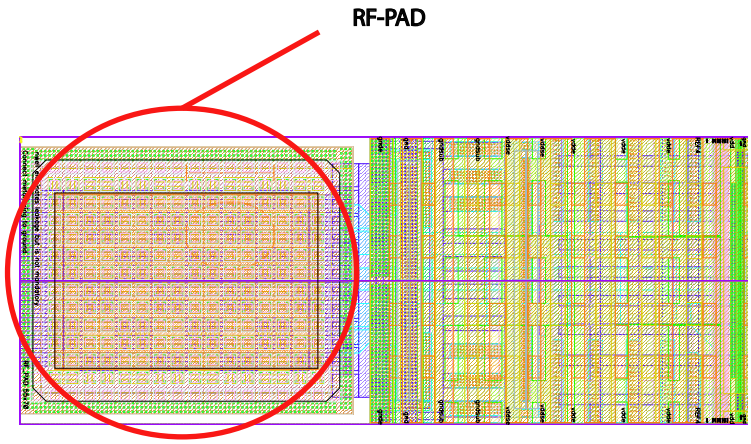

Figure 8.4: Showing the combination of the RF-pad and the pad rails used. The RF-pad is the connection point marked by the red circle.

All the pads used are of the type ISV which stands for Isolated substrate and Split Vdd. By using this type of pads the supply to the pad-frame and the circuits within is totally separated from each other. This way the effect of switching noise from the digital pads containing buffers is reduced. This especially applies to the analog signals and sensitive power lines as the one to the LNA. Assembling the pad-frame according to CMP rules and implementing the design inside the frame, finishes up the die part of the silicon. Remaining is the selection of a package, the placement of the die inside the cavity and the bonding scheme to be used. CMP have several different packages available, which can be combined with a variety of bonding schemes. Deciding which package to use mostly depend on two variables, one, the cost of the implementation and two, the frequency properties of the package. The package selected is not the only problem when operating at high frequency. By using bonding threads to interconnect the package with the pads on the die a fairly large inductor is applied, changing the frequency characteristics of the connection from the package to the pad.

Details on the compared bonding schemes and packages can be found in reference [30]. By comparing the different combinations it is clear that the flip-chip bonding scheme where the bonding threads is avoided, combined with the Plastic Ball Grid Array (PBGA) package is the best solution regarding high frequency performance. The only problem to this combination is the cost, which for this prototyping is totally unacceptable. The PBGA package could just be combined with the flip-chip bonding scheme, thus the PBGA package also had to be rejected. The die and the package have to be interconnected by bonding threads, making

it possible to use all other packaging options. The package LCC 84 was selected for its combination of frequency performance and acceptable implementing costs. The most sensitive signal line on the whole chip is the input from the antenna to the LNA, thus taking precautions when placing the die in the package is important. The best solution for die location inside the package is to place the die with the RF input to the LNA as close as possible to the respective package interconnection in the cavity, thus making the bonding thread short and reducing the inductor effect. This was rejected by CMP as a breach in their rules regarding die placement in the cavity.

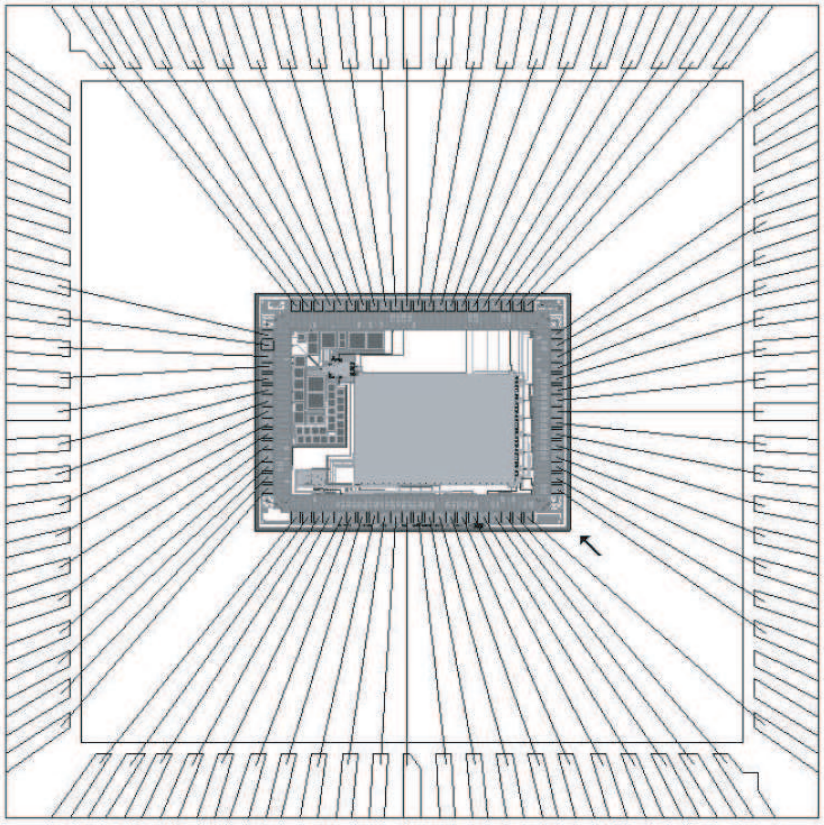

Figure 8.5: Shows the bonding scheme and die placement in cavity used in implementation.

The rules imposes the die to be placed in center of the cavity, leaving the only option to achieve a short bonding thread by using the cavity interconnection directly facing the RF input pad on the die. The package with the die and bonding threads implemented are shown in figure 8.5. The die implemented in the package is not quadratic like the cavity, so

using a package with 84 connections leaving 10 unconnected, makes it easier to achieve a reasonable bonding scheme combined with a short bonding thread to the RF input. While the pads, bonding threads and package introduces large inductors and capacitors, the circuit was not simulated in a test bench where these effects were accounted for. The simulations are presented in the next chapter.

8.3 Summary

The different isolation techniques used, and the location of the different designs on the silicon combined with the low noise design of the pad-frame should ensure low noise operation. Even if the best possible package and bonding scheme were not used, the utilization of the package and bonding scheme available relative to the die placement rules is probably optimal. By using a specially designed RF-pad for the input signal to the LNA, the parasitic capacitance distorting the input signal is reduced.

Chapter 9

Measurements and preparations

In this chapter the different measurement results are presented, briefly discussed and compared to theory and simulations. The design of the PCB used for measurements and the measurement setup is also presented.

9.1 PCB design

As most of the functions to be tested on the chip required additional high speed electronics for signal generation and IO, it proved necessary to design a print circuit board (PCB) especially to comply with the high frequency requirements. The design of the PCB was carried out with software from Cadence. It consists of a four layer print with epoxy resin laminate called FR4 described in reference [32]. As seen in appendix E additional antenna and filter structures were implemented on the PCB. The antennas and filters make it possible to test the front-end and rake receiver using a wireless link. Before using the antennas, the dual slope pulse will be shaped by a strip shaping PCB using a edge from a rectangular shaped pulse as input. Since this thesis does not consist of peripheral designs outside the chip, the antennas, filters and pulse shaping PCB designs have been copied from [33, 34, 35, 36, 37], and is thought used for testing purposes only.

9.2 Measurement setup

By designing a PCB a lot of different testing possibilities was made possible. A illustration in figure 9.1 shows the interconnections to the PCB

and some different lab equipment which can be utilized for analyzing signals coming from the PCB.

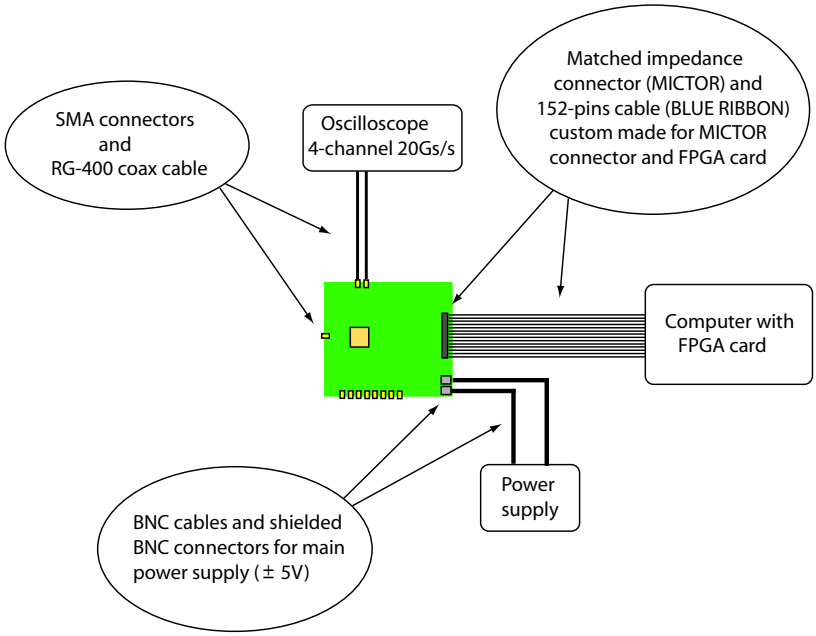

Figure 9.1: Illustration of PCB and interconnections with different available lab equipment.

The different interconnections in the illustrations show that the main power connections are well shielded reducing the amount of noise picked up by the power cables. By using SMA connectors and a dual shielded RG-400 coaxial cable for PCB readout, the signal integrity should be preserved. The 152-pins cable and matched impedance connector (MICTOR) enables readout of all fingers in the rake receiver (50 fingers) to a FPGA card which can collect the received information and enable the raw data to be post processed and analyzed in software.

The illustrations of the different measurement setups used and instrument lists can found in appendix D.

9.3 Measurements

The circuit should ideally be tested with input pulses of different phase, length and amplitude, and with different levels of added noise to verify the circuitries functionality. By using the available lab equipment it was

hard to generate the dual slope pulse, and could therefore not be used to generate measurement results. Even though, there were several other ways to test some of the functionality of the circuits implemented. The threshold and pulse shaping circuit can be tested by sending a signal through the level shifter, thus the signal affects the level on the isolated line in the thresholding inverter structure. By using a signal with square shaped pulses at a frequency of 10 MHz the thresholding circuit should give output for the levels above or belove the inverter threshold, depending on which of the lines is used.

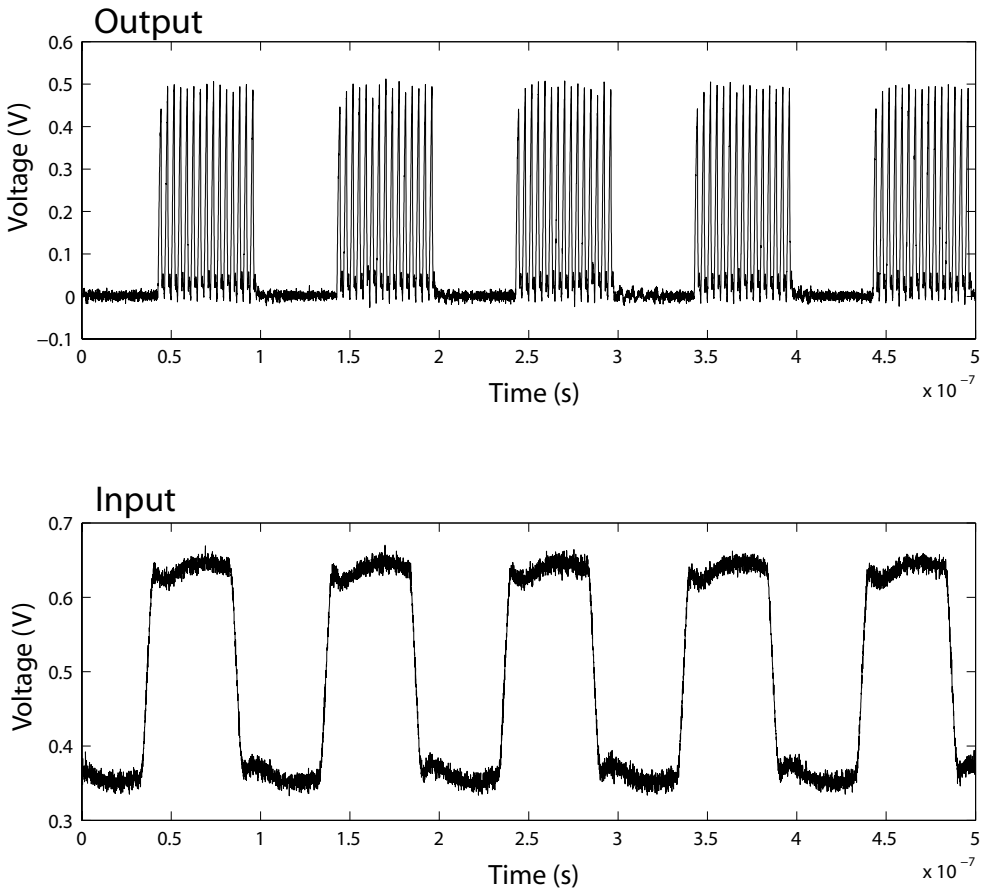

Figure 9.2: Measurement of a square shaped pulse at 10MHz trigging the inverter threshold through the level shifter, making the line1 pulse shaper generate pulses.

Figure 9.2 and 9.3 shows that the thresholding circuit give output for positive or negative part of the square shaped pulse depending on which line the output is from. As seen from the figures, the output is oscillat-

ing. This is caused by the pulse-shaping circuit, which generates output pulses continuously for a high DC input. The output pulses are not square shaped and does not go rail to rail, this is caused by insufficient driving properties in the output buffers, compared to the parasitic capacitors gained by interconnection lines, pads, package, PCB line and cable. It is worth mentioning that the output signal is approximately 200-300 mV higher by measuring it with a probe on the output pin on the chip.

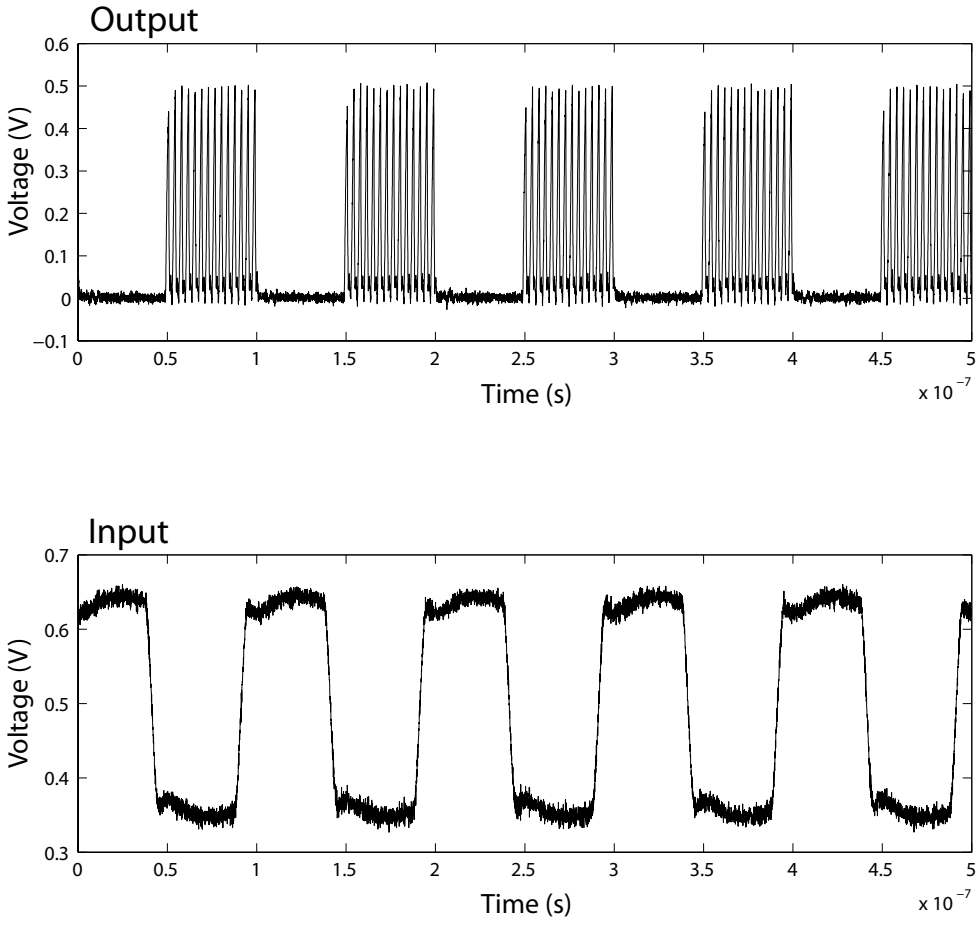

Figure 9.3: Measurement of a square shaped pulse at 10MHz trigging the inverter threshold through the level shifter, making the line2 pulse shaper generate pulses.

To be able to test whether the LNA and RF-pad works, it is necessary to emit a signal through air and receive it through the PCB antenna structures. A 1GHz sinusoidal wave is generated from a signal generator and emitted through an attached antenna.

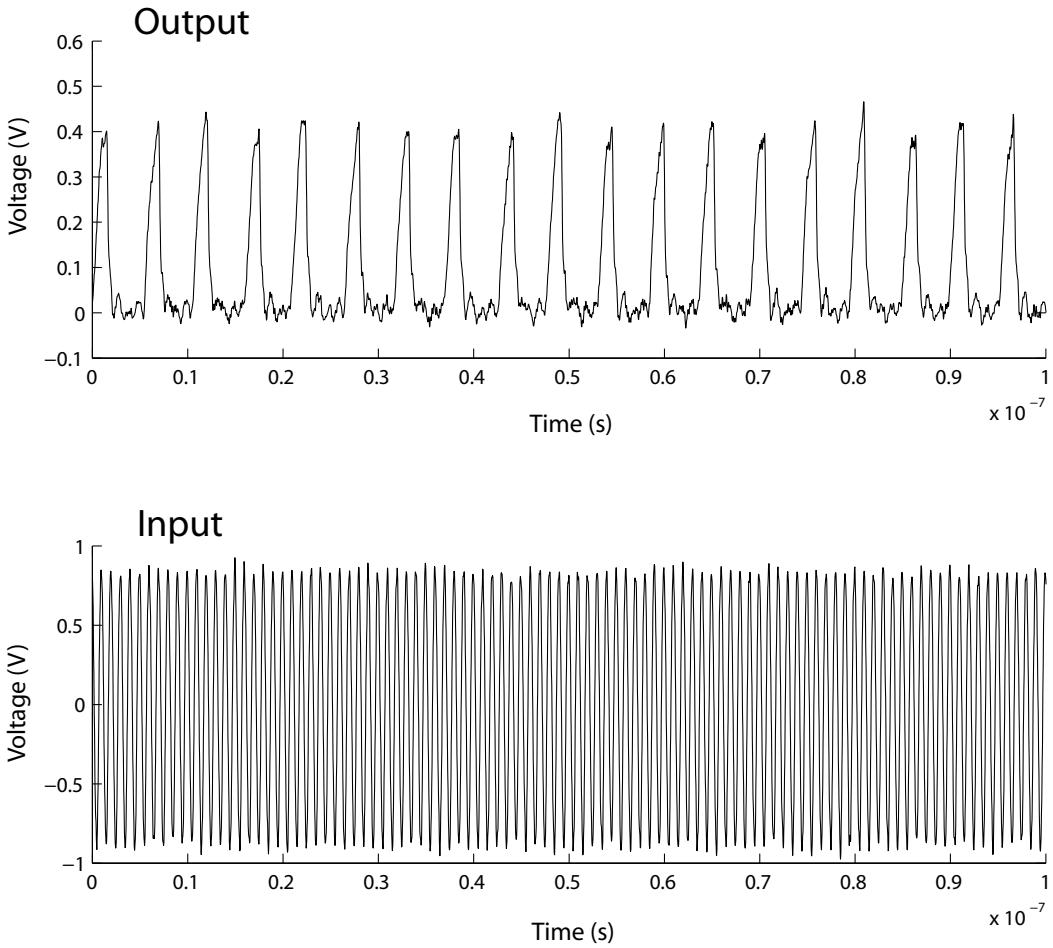

Figure 9.4: Measurement of a 1GHz sinusoidal wave emitted from an antenna attached to a signal generator, causing a continuous pulse generation from the line1 pulse shaper.

Figure 9.4 shows that the 1 GHz sinusoidal wave causes a continuous trigging on the line measured on. Worth mentioning is that the continuous sinusoidal wave generates no signal on the pulse verification output, which should give a output only if one phase is detected. This is because the time displacement between the pulses generated by the 1GHz input is larger than the one generated by a dual sloped monocycle. This implies that the noise discrimination added by the XOR-gate is functioning, but to test if it really is working, a dual sloped pulse should be received. When this was hard to do a different way to trigger the dual slope detection had to be used. By emitting a signal through the level shifter it was possible to test whether the thresholding elements were functioning. So

by using slightly different clocks on the two lines it should be possible to induce a pulse phase verification. By using two 10MHz clocks where one is inverted and slightly shifted in respect to the other, it was possible to induce the output from the dual slope one phase detection. the measurement results is shown in figure 9.5.

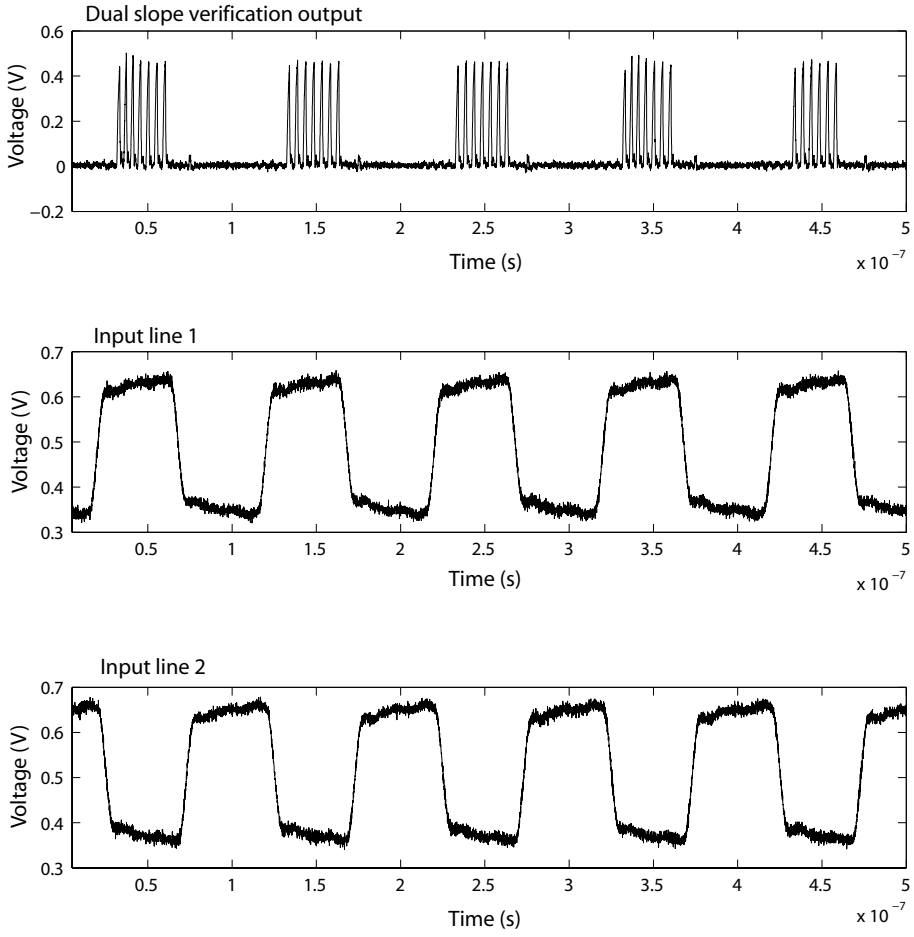

Figure 9.5: Shows the measurement of the induced dual slope detection and one phase verification using two clocks for trigging.

Though these measurement results only show the rough functionality of the front-end, it shows that the thresholding and pulse shaping works. It also gives an indication on the XOR discrimination, and the buffers insufficient driving properties.

In the next measurement, the threshold on one of the lines has been swept from 410mV to 490mV. The input signal is a 10MHz square shaped

waveform with an amplitude of 10mV. The signal is sent through the level-shifter.

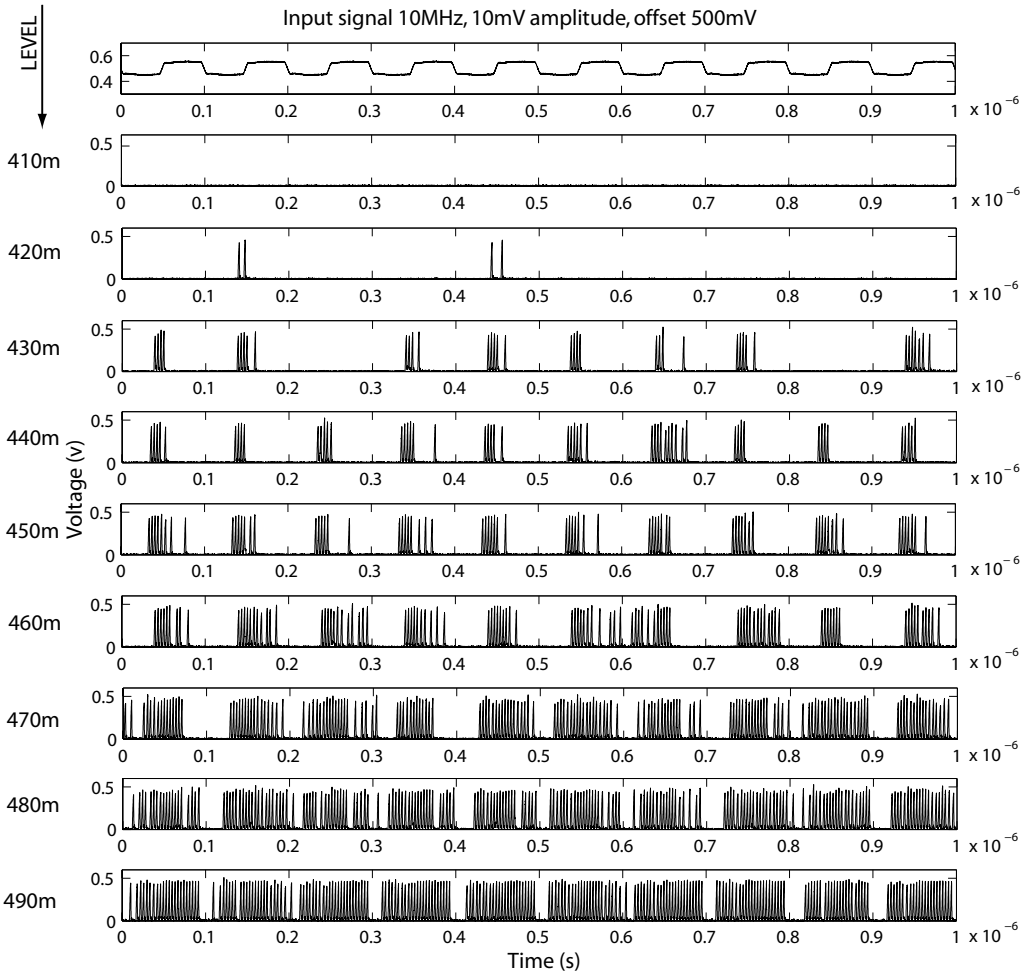

Figure 9.6: Shows the measurement of a threshold sweep from 410mV to 490mV.

This last measurement shows that there is a lot of noise triggering the signal in the first steps of the sweep, and as the threshold closes in on the inverter switching point, the noise dominates the trigging.

9.4 Summary

To be able to measure the chip and to reduce the effect from noise, a PCB was designed for this prototype chip. Though the lack of available

equipment for measurement, prevented the possibility to test the front-ends performance, it was possible to test some main functions. Through measurements different functions of the front-end was verified, and it was clear that the buffers lacked sufficient performance.

Chapter 10

Discussion and conclusion

10.1 Discussion

Through the complete thesis the template sampling scheme has been compared to the presented thresholding scheme, which also has been implemented. It is clear that the threshold scheme spends less energy on the symbol detection than the sampling scheme, since it is not waisting energy generating templates at high frequencies, neither does it utilize a DSP. The question is whether the thresholding is a more effective signal detection scheme than the template sampling. A comparison is done in section 4.1 where a single threshold level is compared to a perfectly timed template sampling using a rectangular shaped template. So by having a time independent thresholding, it alone can be an improvement to using rectangular shaped pulses for sampling. The signal detection scheme presented in this thesis is a combination of two thresholds (one for each slope) and a phase detection by using the time displacement between the slopes in a simple digital calculation. This combination results in the detection of a rough pulse shape, which is a rough approximation of template sampling with an analogue template equal to the shape of the received pulse, presented in section 2.3.2. The template sampling scheme using an analogue template have the advantage of getting an analogue mixing result, which for the thresholding scheme only gives a rough digital template representation, but with analogue time displacement representation. The thresholding scheme has an advantage on any template mixing scheme by being timing independent, thus synchronization is not an issue in signal detection.

The fact that the high frequency operation of this implementation is at the limit of what the technology used offers, implies it is very sensitive to mismatch and parasitic effects unaccounted for by the designer and

design tools. Due to the operation at the process limit a general problem in the complete implementation was getting sufficient gain.

The fact that the design process lacks parasitic extraction can be a serious problem. This can be roughly accounted for by the designer applying additional capacitors in the interconnections between the different blocks and transistors in the design. During the development of fine pitch processes the oxide layer has become thinner, and as a result of this development the parasitic capacitors in interconnection lines in the silicon implementation is increasing. This issue has been explored in a book published this year [25]. The tendency described in the book indicates a interconnection parasitic increasing exponentially from approx. 200nm and down, causing a larger delay than the gate delay. This depends on which metal that is used for wiring. With the missing parasitic extraction in combination with the absence of process parameters such as oxide thickness, it turned out to be a difficult task to make a qualified guess of parasitic effects.

The design process turned out to be a much longer and complicated process than first expected. This was due to lack of design-kit support from the distributors, a lot of software and design-kit compatibility problems and the fact that CMP demanded a design with no DRC errors what so ever.

In the chapter regarding the LNA a lot of important issues were addressed, but there is one in particular regarding matching and UWB-IR applications. The discussion on designing the antenna close enough to the chip, eliminating transmission line effects for the known interfering frequencies and at the same time longer than a pulse duration. For the 5.8 GHz WLAN carrier this can be problematic, since its wavelength is close to the duration of a Gaussian monocycle (dual sloped). Thus it must be preferable to design the antenna as close as possible to the chip to avoid standing waves, but at the same time loosing the property of reflections through a cable longer than a pulse duration. In addition to this it is preferable to add a filter to eliminate the 5.8GHz frequency and other frequencies outside the band, and since pulse reflections are always added from the environments, the loss from not getting reflections in the transmission line is probably insignificant.

The LNAs frequency response in figure 3.5 shows that the peak amplitude of more than 40dB in gain is at approximately 2 GHz. With a frequency response that low, noise as in other sinusoidal interferer's within the amplifiers frequency response will cause a lot of problems, and probably make the thresholding and pulse shaping circuit generate pulses continuously. Traditionally LNA design contains inductors and capacitors to improve the low noise and high frequency perform-

ance, but designing inductors and capacitors on chip demands a lot of area. In this thesis the LNA is designed without using capacitors and inductors, this is done on purpose to see what performance it is possible to obtain without using traditional design techniques. But there is probably a trade-off between area usage due to inductors and capacitors and performance in such designs. The simulation of the LNA in different corners reveals that the LNA performs poorly in some corners, especially for low temperatures and weak NMOS corners. This can partly be explained by the need to adjust the bias voltage as the temperature changes, but it is also a weakness in the design.

The thresholding and pulse-shaping circuit is designed to give an output on a broken threshold, where the output is a square shaped pulse with the duration equal to the duration of one slope of a dual monocycle. The implemented approach will probably only work in noise free environments, where the only signal braking the threshold is received pulses. It could probably cope with some level of noise, if the noise does not cause trigging with a duration larger than the duration for one slope of the dual sloped pulse.

As for the design of the output buffers, the parasitic estimation failed. This resulted in a output signal from the chip with an amplitude that is lower than Vdd, as seen in the measurement results.

The Idea of using single impulses and no carrier in signal emission is in itself a very interesting way to do radio communication. And though spark gap radio was among the first kind of radio technologies invented, it did not survive the competition from narrow-banded technologies. It is now interesting to see that the development of radio communication and regulation enables the use of broad banded impulse radio communication. As UWB-IR can be developed to effectively utilize the spectrum between 3.1 GHz to 10.6 GHz it seems possible to obtain low power high bandwidth communication links for short range communication, but there is also an other approach. As mentioned in the introduction the IEEE 802.15.4a standard addresses low power and low data rates in the size of hundreds kbps for short range communication. The proposed architecture in this thesis is a low power approach and can be a possible solution to a front-end used in such applications. There is of course a lot of improvements that need to be done, but the idea of using thresholding, pulse shape and phase detection for pulse verification utilizing no clock is a promising solution. The combination of a spatial RAKE receiver for statistical symbol correlation using reflections constructively, is an interesting low power approach where e.g. longer symbol length is a trade-off to bit rate, but also an improvement in SNR.

10.1.1 Proposal of improvement

The design presented in this thesis is the first prototype implemented in silicon, and as most other first prototypes there is much room for improvement. The most fundamental problem is that the CMOS technology used in this implementation seems to be too slow, so using a better or finer pitch process can facilitate the high frequency operation needed. Another fundamental improvement is to use design tools that are compatible with the design kit, thus making it possible to extract parasitic capacitors from layout.

Regarding the design there are also many major improvements that can be done, one is to add Automatic Gain Control (AGC) to the LNA and automatic level and biasing control to the thresholding circuit, reducing the amount of analogue control lines. This could also reduce the noise impact. One important issue in the LNA design is to add a current mirror controlling the active load, thus reducing the early effect. The LNA can also be improved by reducing its frequency response outside the band of operation. The ideal response would of course be located only within the 3.1 GHz to 10.6 GHz band. The input of the LNA could also be filtered through a band pass and band stop filter, reducing the effect of interference from outside the band with the band pass filter, and reducing the effect from the 5.8 GHz frequency with the band stop filter. There is probably a trade-off to pulse shape distortion by adding a band stop filter within the band. The design of the LNA should also be improved so that it provides sufficient gain in all corners during simulation, even if some of the poor corner results in low temperature probably is caused by the need of bias and probably input level adjustment.

Another improvement should be to design a threshold and pulse-shape generation scheme that generates a output pulse not only if the threshold is broken, but if the duration of the pulse crossing the threshold is equal to the duration a slope from a dual sloped pulse should have. A improvement to the pulse shape recognition can also be done by adding a multi threshold scheme using several separated threshold levels. And by using the different thresholding results to correlate for a rough analog shape of the pulse, a more accurate pulse shape verification can be done. This is possible to do without using sampling clocks. There could also probably be added more processing in the front-end, e.g. correlation against a ternary code (-1, 0, 1) to verify a received pulse sequence as a probable bit in a symbol, and it can all be done without using sampling clocks.

From the measurement results it is obvious that the output buffers in the design is to weak, but by designing the buffers with a few more stages, they should be able to cope with the parasitic capacitors gained from interconnection lines and pads.

To ensure the functionality and performance of the implementation it should be simulated not only with the correct parasitic capacitors gained by interconnections between building blocks and to pads. But it should be simulated with the parasitic effects from the pads, bonding thread and package, which all represent large inductors and capacitors in particular. Simulations should also include more excessive noise, corner and Monte-Carlo simulations to verify functionality within process variation and temperature.

When it comes to testing and measurement, the proposed receiver scheme should first of all be tested by receiving dual sloped pulses to verify the detection scheme. For a improved version of the receiver it needs to be tested in an AWGN channel and dense multipath channel, since it is more likely that the proposed receiver works in an AWGN channel. It may experience problems in a multipath channel as the shape of the pulse may not be ideal due to the inter-pulse interference. This also applies to interference from the 5.8 GHz WLAN carrier, which can mask out the signal and in worst case cause continuous trigging on one of the phases. This issue can be improved by implementing filtering masking out known “noisy” parts of the frequency spectrum, like the 5.8 GHz WLAN band.

10.2 Conclusion

The UWB-IR front-end presented in this thesis was found feasible for several reasons. First of all it is a pure CMOS implementation and low power approach enabling signal detection without utilizing a sampling template and/or high frequency clocks. The contribution of the rough pulse shape and phase recognition, which is a rough approach to the analogue template sampling scheme, though with respect to timing between pulses and pulse duration only. It is also unaffected by timing/synchronization issues. The front-end presented is a pre-conditioner for a sampled delay line RAKE receiver, which combined makes up a novel low-power UWB impulse radio receiver. The combination utilizes symbol transmission designed for lossy data using pseudo-random sequences and cross-correlation for statistical symbol recovery. The implementation of the rough pulse shape verification also enables the use of several modulation techniques like MBOK, PAM and dual slope coding. The complete front-end is a simple topology mostly based on inverter structures and simple logical gates. This makes it high frequency compatible and relatively simple to implement.

Though this UWB-IR front-end might seem feasible, simple and power saving, there are several possible improvements. One is that the de-

tection technique needs to be tested in a AWGN channel and multipath channel to see if it can cope with the disturbance from other transceivers causing inter symbol interference. It should also be tested in a noisy channel with narrow banded communication like the 5.8 GHz WLAN, which might be used in the same environment as an UWB-IR transceiver, used for short range communication. The implementation being the first prototype for testing and measurement, needed a lot of adjustable analogue inputs to be able to verify the functionality of the circuit, but for a functional receiver structure all the gain levels and thresholds should be adjusted automatically by implementing functions like AGC in the design.

In general the pulse verification function implemented in this prototype is probably not sufficient enough to obtain the required noise discrimination. However, improving the verification process by implementing a multi threshold scheme could result in a more analog verification process, which again implies a higher factor of discrimination. The level of discrimination can also be improved by adding more processing to the front-end.

The work on the UWB-IR front end presented in this thesis is combined with a spatial RAKE receiver to make up a UWB-IR receiver. During the work on the thesis, there has been three publications based on this receiver approach. One publication was at WOWCAS in 2004, one has been accepted for publication at ICU 2005 and one publication has been prepared and is pending publication at NORCHIP 2005. Through the publications it is verified that the UWB-IR receiver is a substantial contribution to the research on UWB-IR technology. All publications can be found in appendix F.

The implemented topology certainly needs improvements and further development in order to obtain the required functionality and performance. However the idea of using a front-end with thresholding elements which can detect and verify a rough pulse shape continuously at high speed without the use of a mixing template or a sampling clock. By using the front-end as a pre-conditioner for a spatial RAKE receiver for real-time symbol correlation and utilization of signal reflections, is certainly worth further investigation and research as it can be a promising approach for low power and short range communication.

Appendix A

Schematic with transistor sizes

In this chapter the different topologies transistor sizes are presented, including the transistor sizes for the compared and simulated LNA topologies.

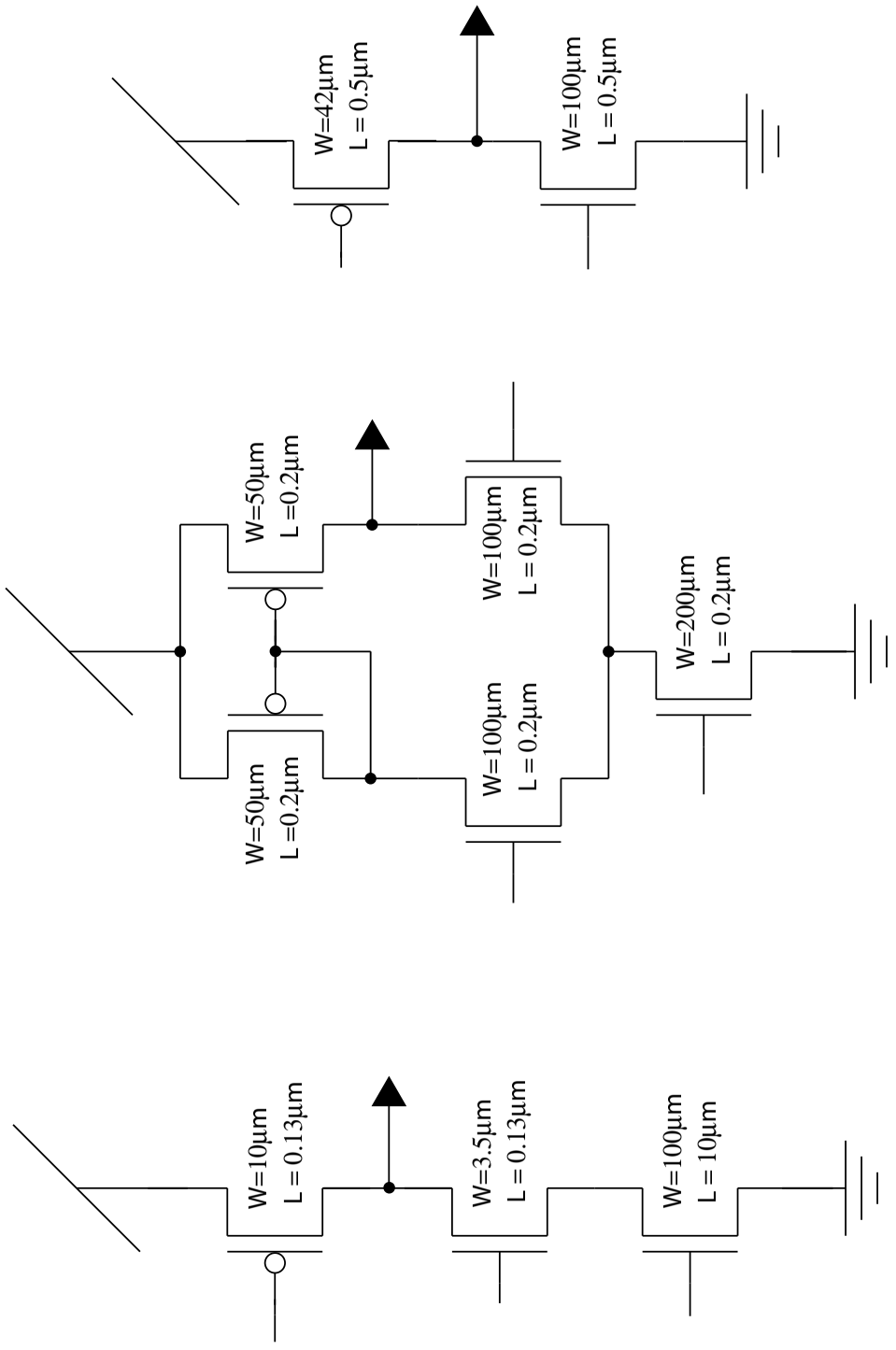

Figure A.1: Overview of the transistor sizes in the compared LNA topologies. The sizes of the telescopic cascode is the sizes on the implemented version.

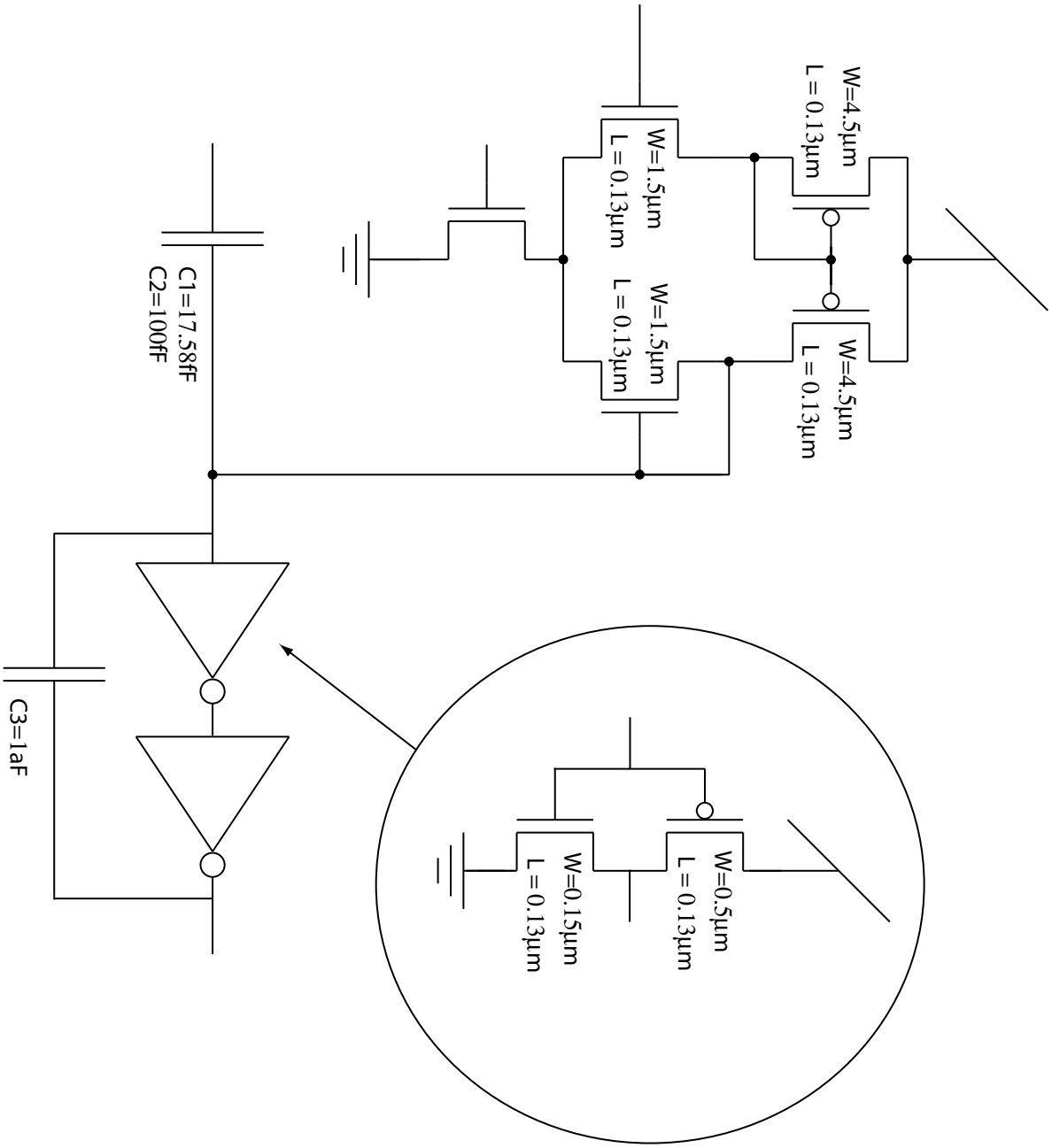

Figure A.2: Overview of the transistor sizes in the thresholding topologies implemented. The sizes of the transistors in the inverter is the size for all inverters in the design, except from the buffers. The values C1 and C2 is the size of the two blocking capacitors, where C1 is the one connected to the output of the LNA and C2 is the one in the additional gain stage. C3 is the feedback capacitor which has a size of 1aF

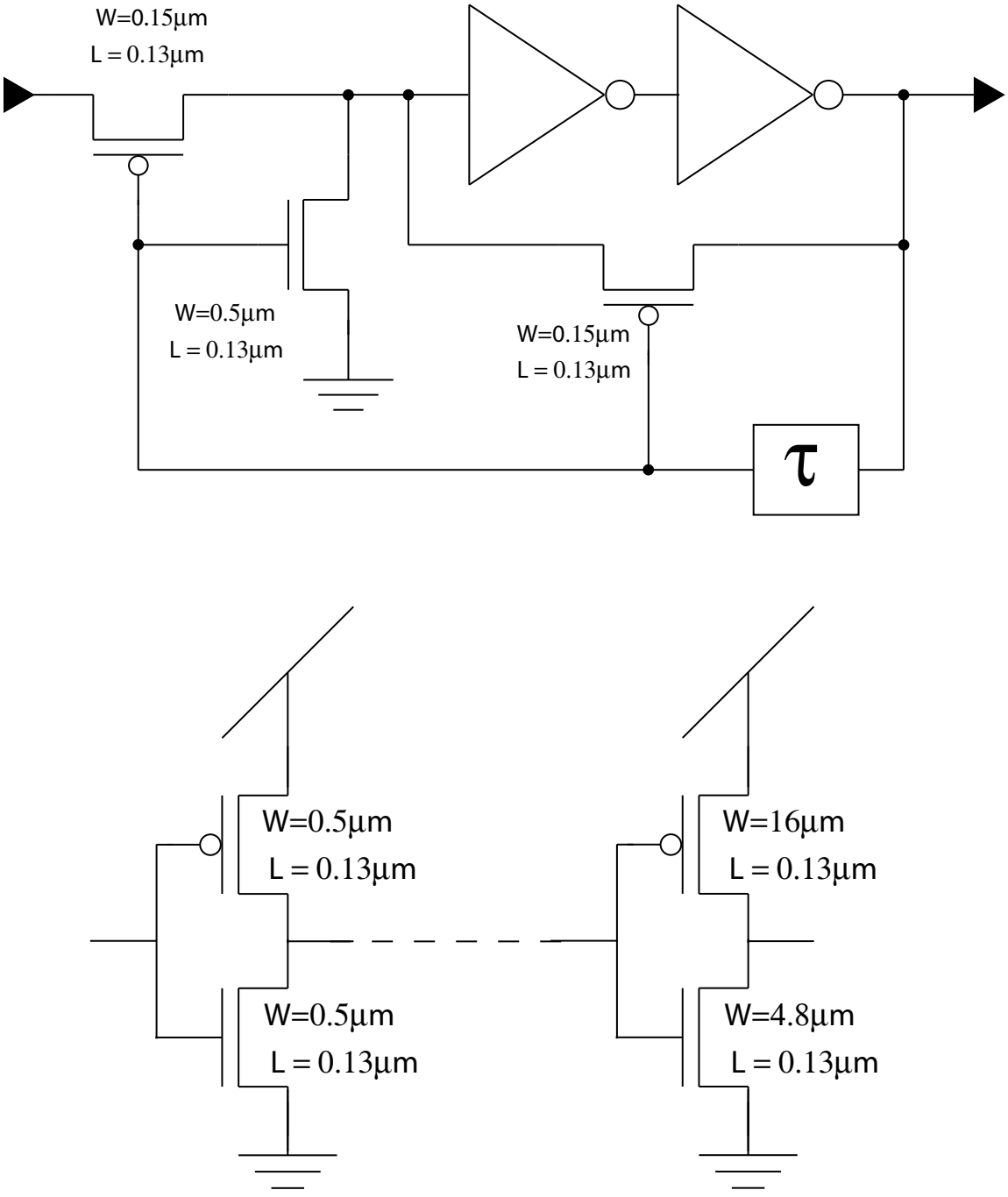

Figure A.3: Overview of the transistor sizes in the two pulse shaper topologies, where the only difference is the length of the element τ, which consists of a chain of inverters with sizes described in figure A.2. The buffer presented is designed with a fan out of 2, which makes up a total of 6 inverters.

Appendix B

Layout blocks

In this chapter the layout from all single blocks used in the design is shown. The layout pictures are exported from Cadence Virtuoso layout editor for each block.

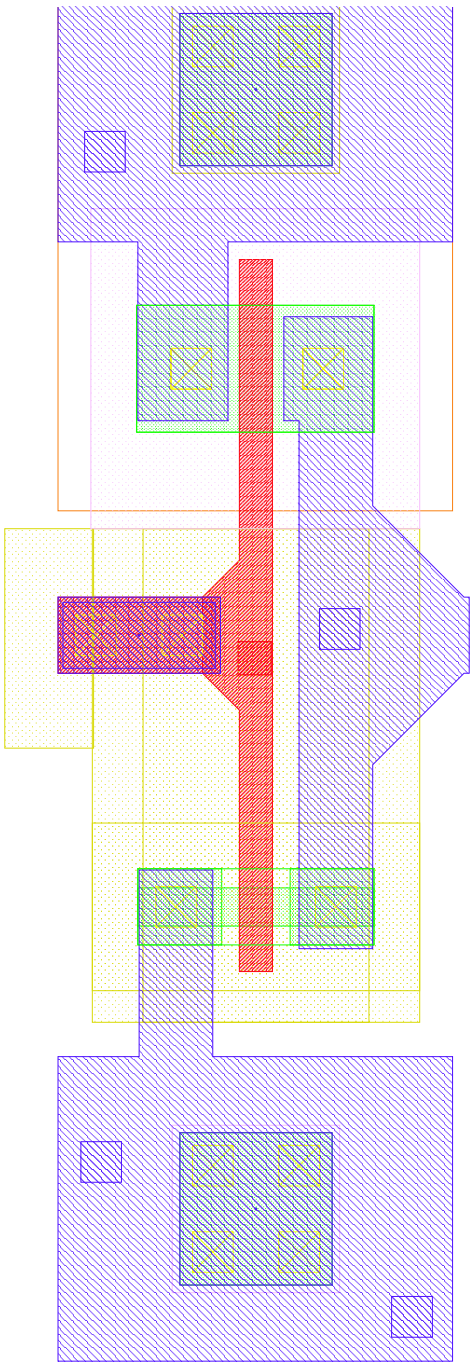

Figure B.1: Shows the layout of the inverter used in the design.

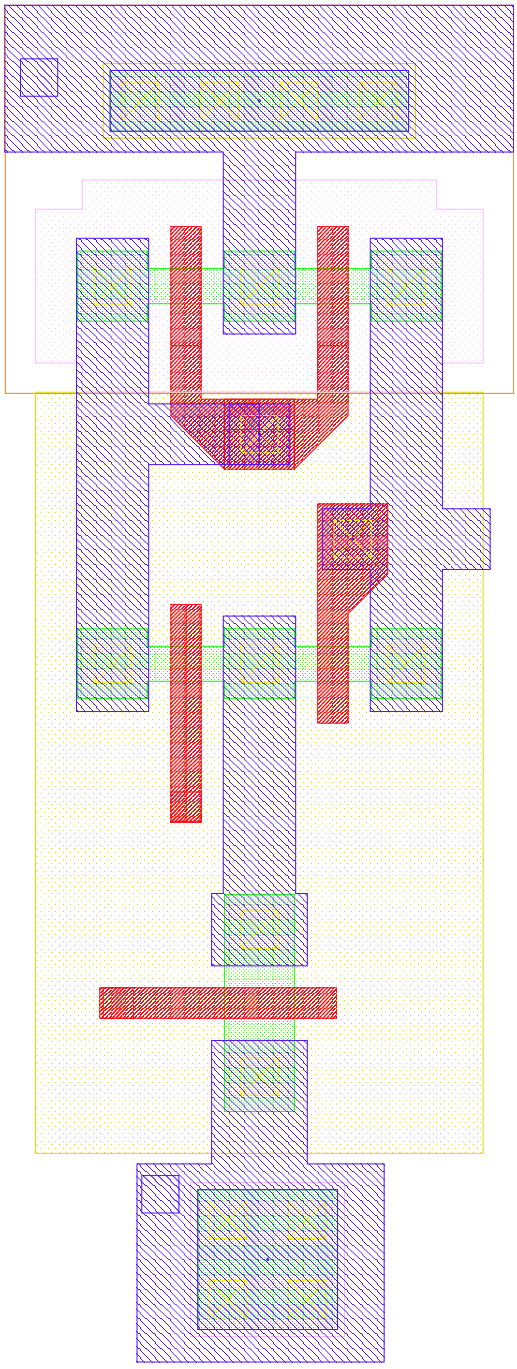

Figure B.2: Shows the layout of the voltage follower used in the design.

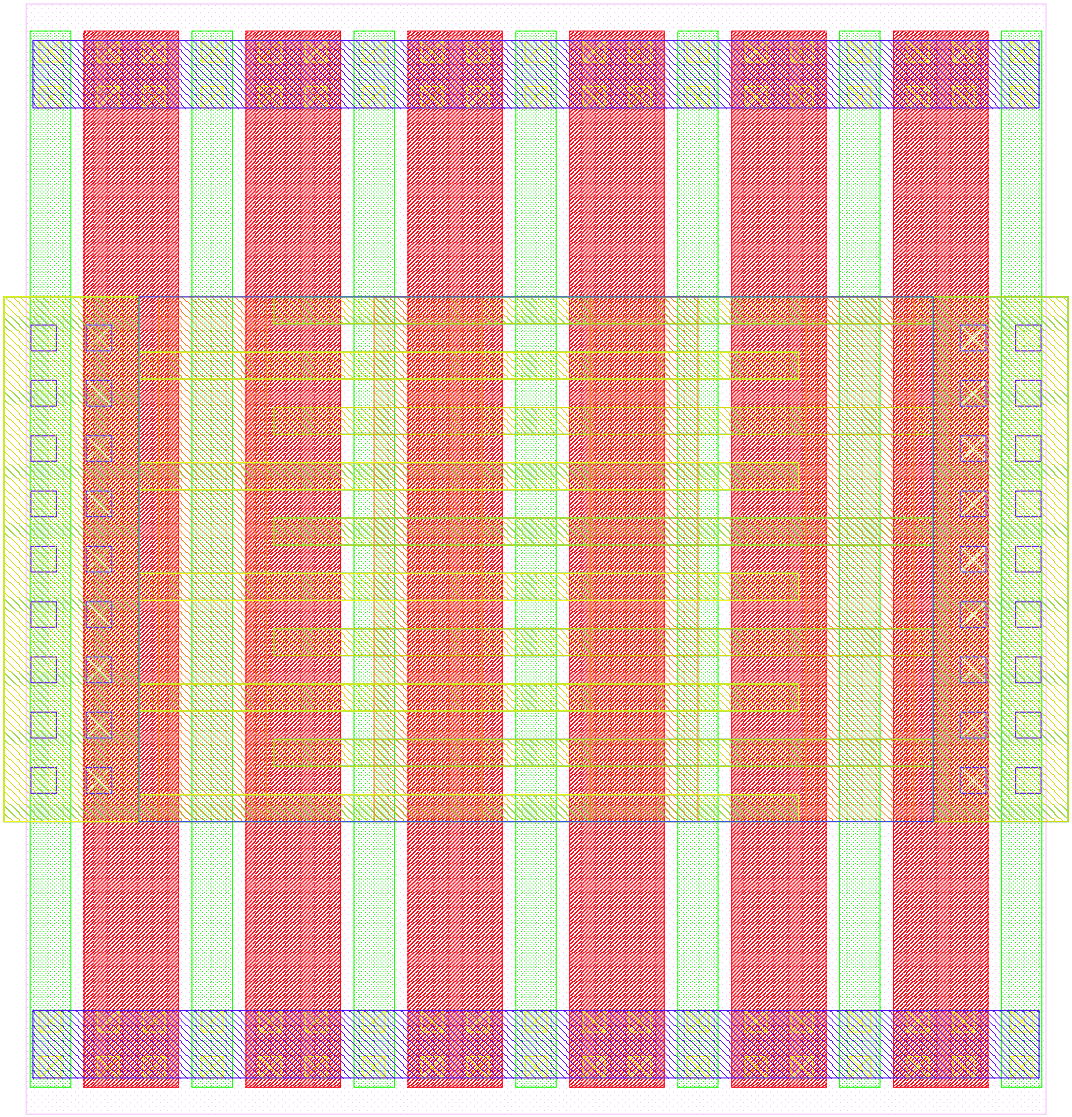

Figure B.3: Shows the layout of the capacitor used in different sizes the design.

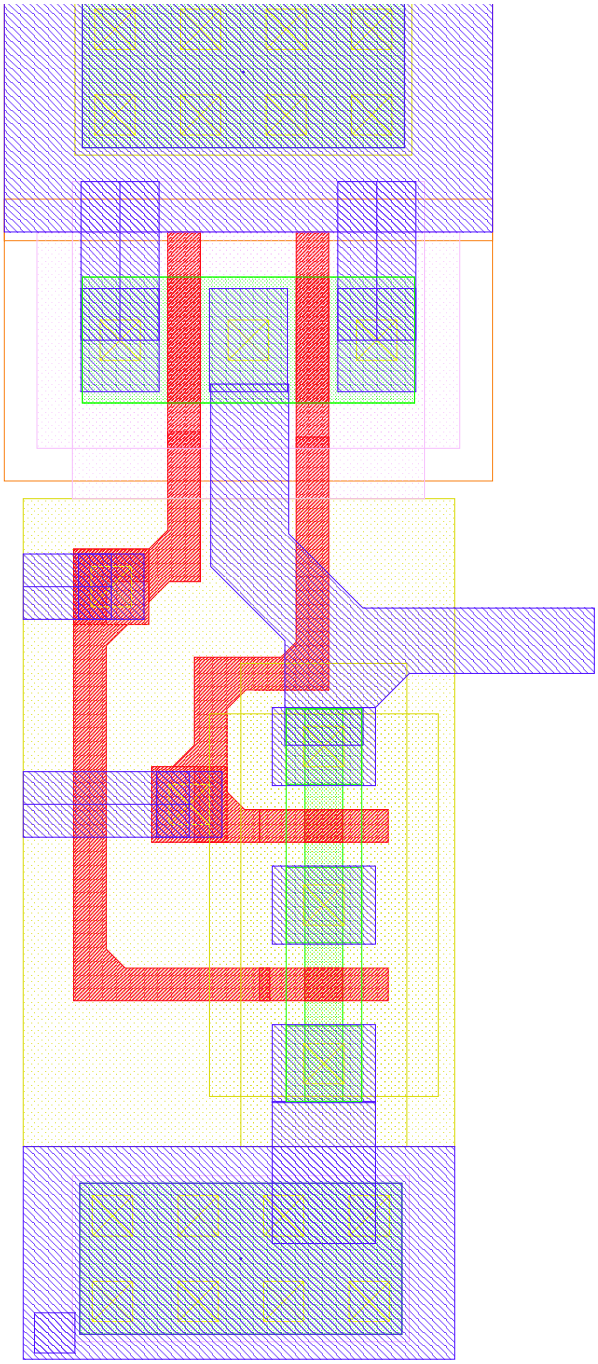

Figure B.4: Shows the layout of NAND gate used in design together with the inverter to make up the AND gate.

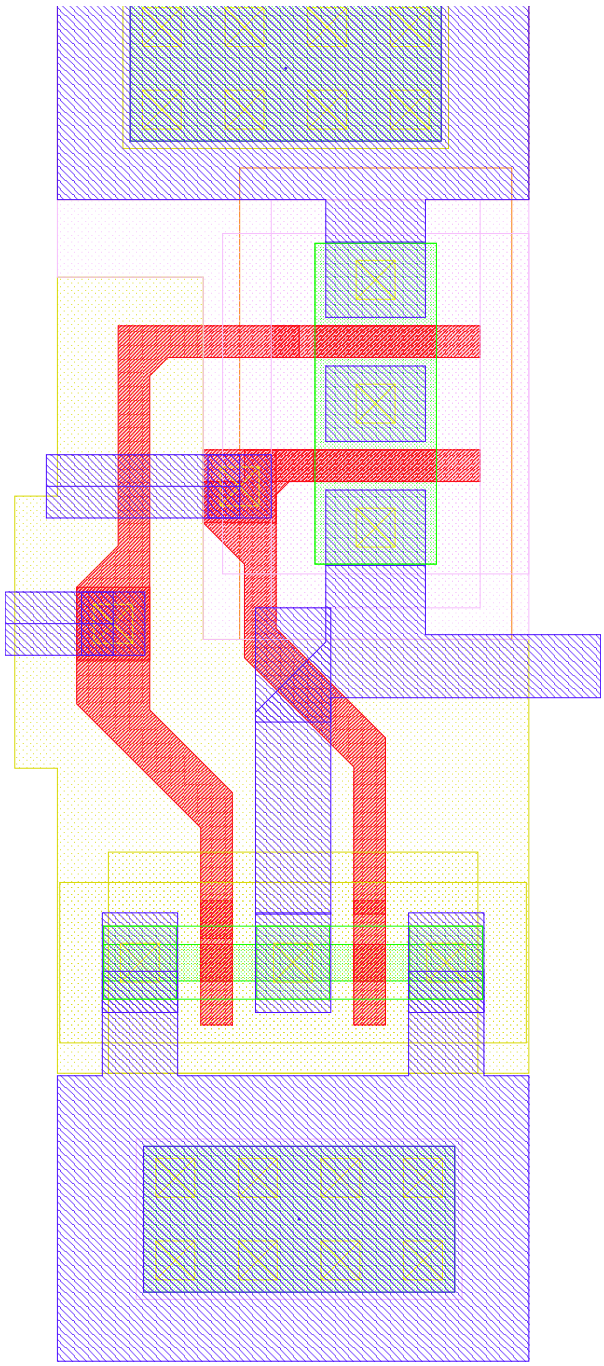

Figure B.5: Shows the layout of the NOR gate used in design together with the inverter to make up the OR gate.

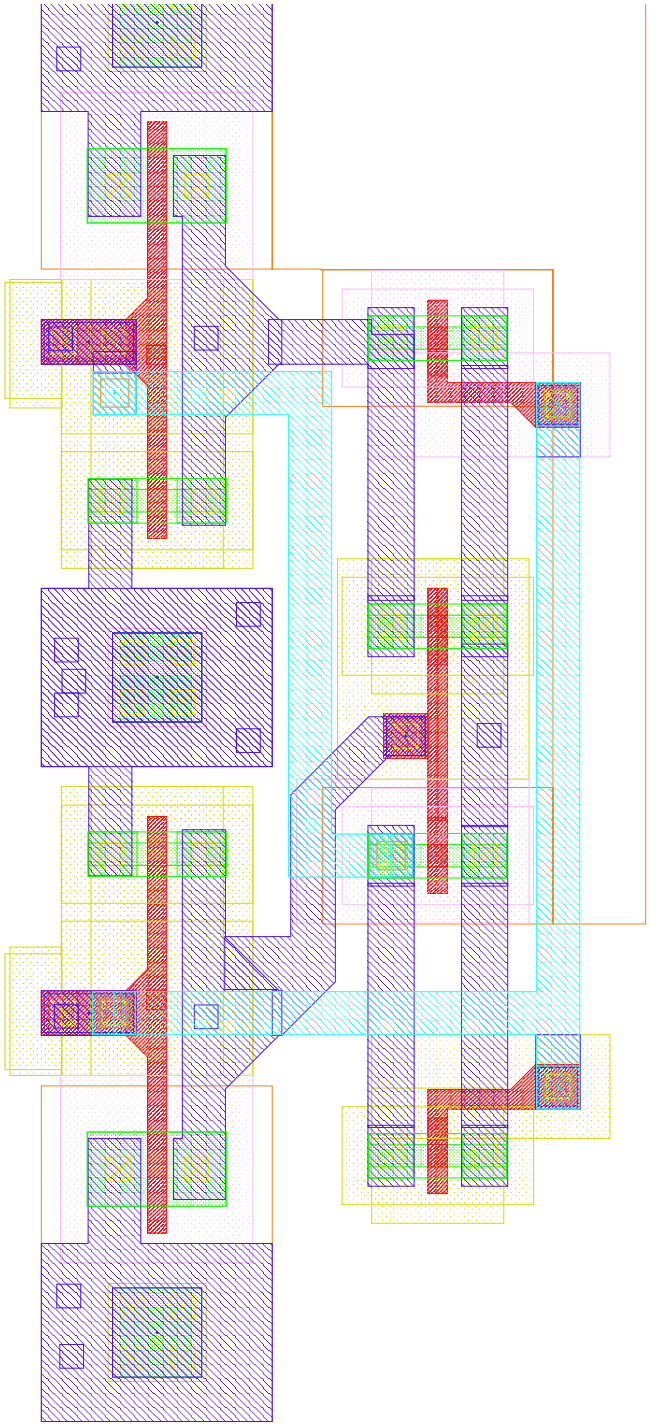

Figure B.6: Shows the layout of the XOR used in the design.

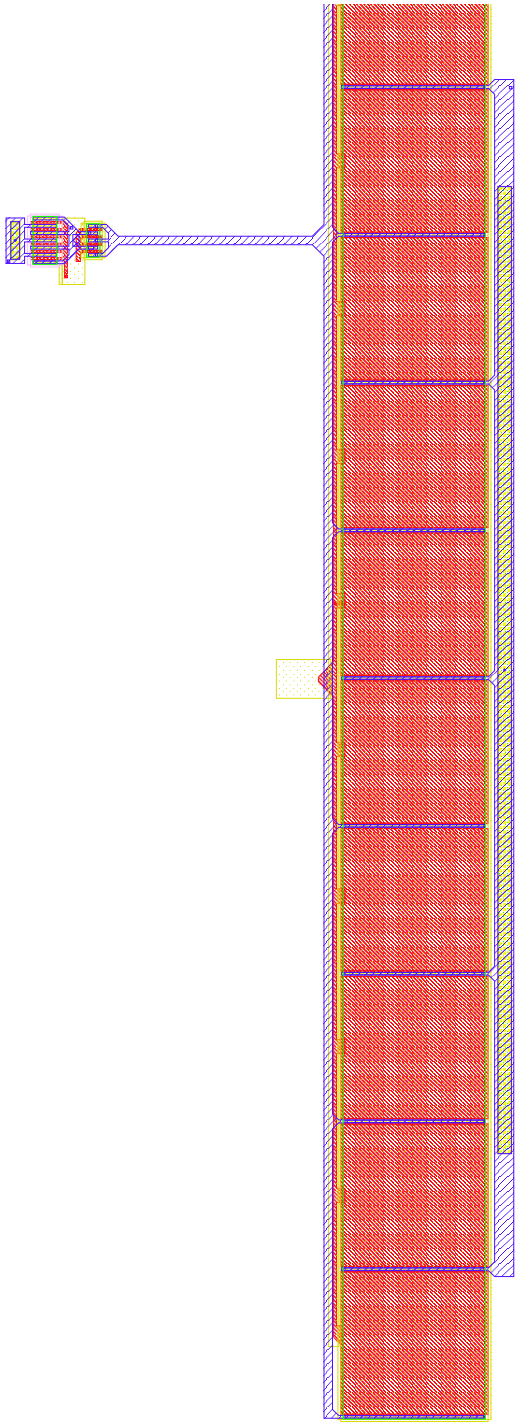

Figure B.7: Shows the layout of the LNA used in the design.

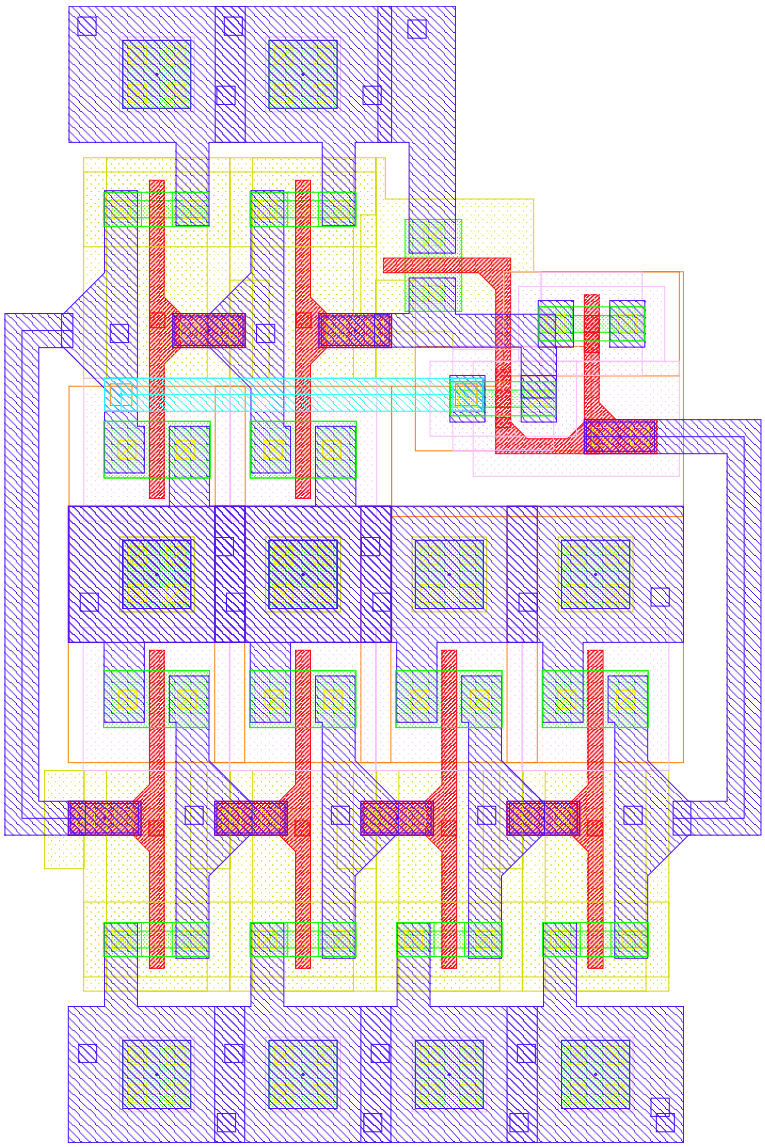

Figure B.8: Shows the layout of the pulse shaper which is implemented and used to shape pulses prior to the phase detection.

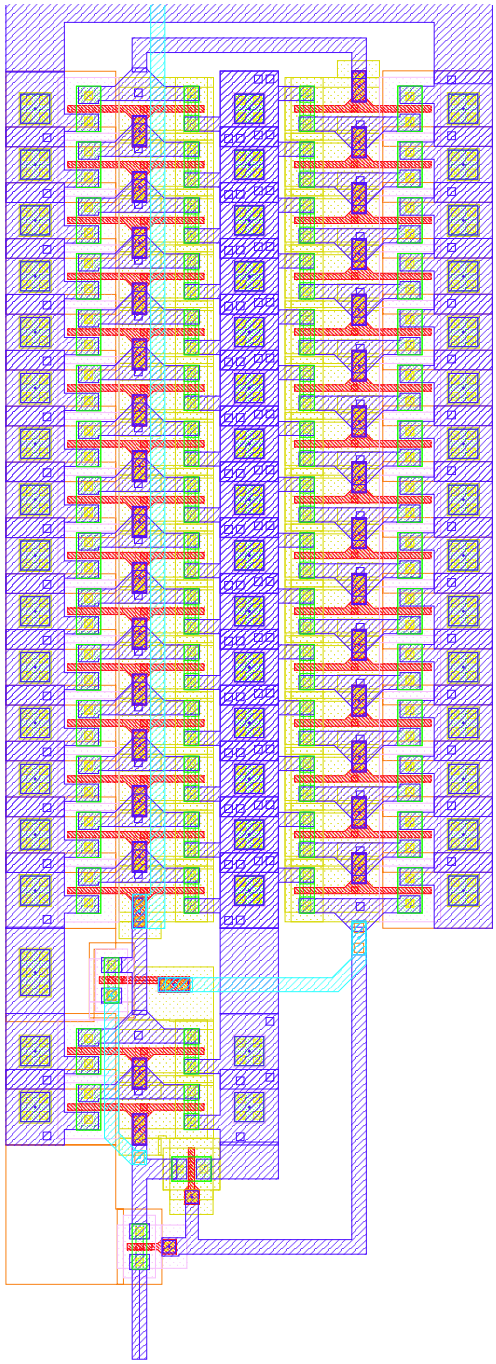

Figure B.9: Shows the layout of the pulse shaper which is implemented and used to shape pulses to 1ns prior to the output.

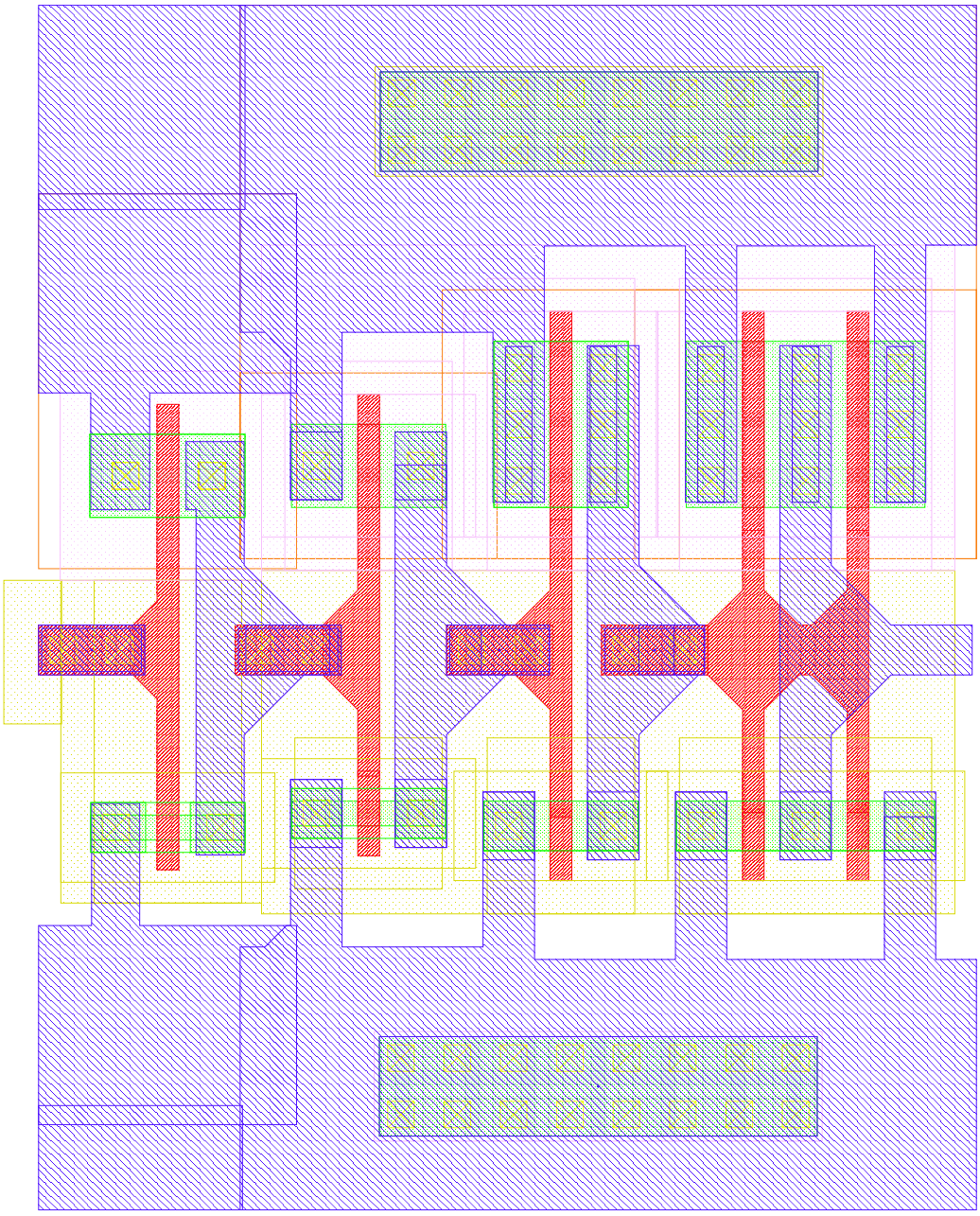

Figure B.10: Shows the layout of the small buffer which is implemented and used between some blocks internally in the front-end.

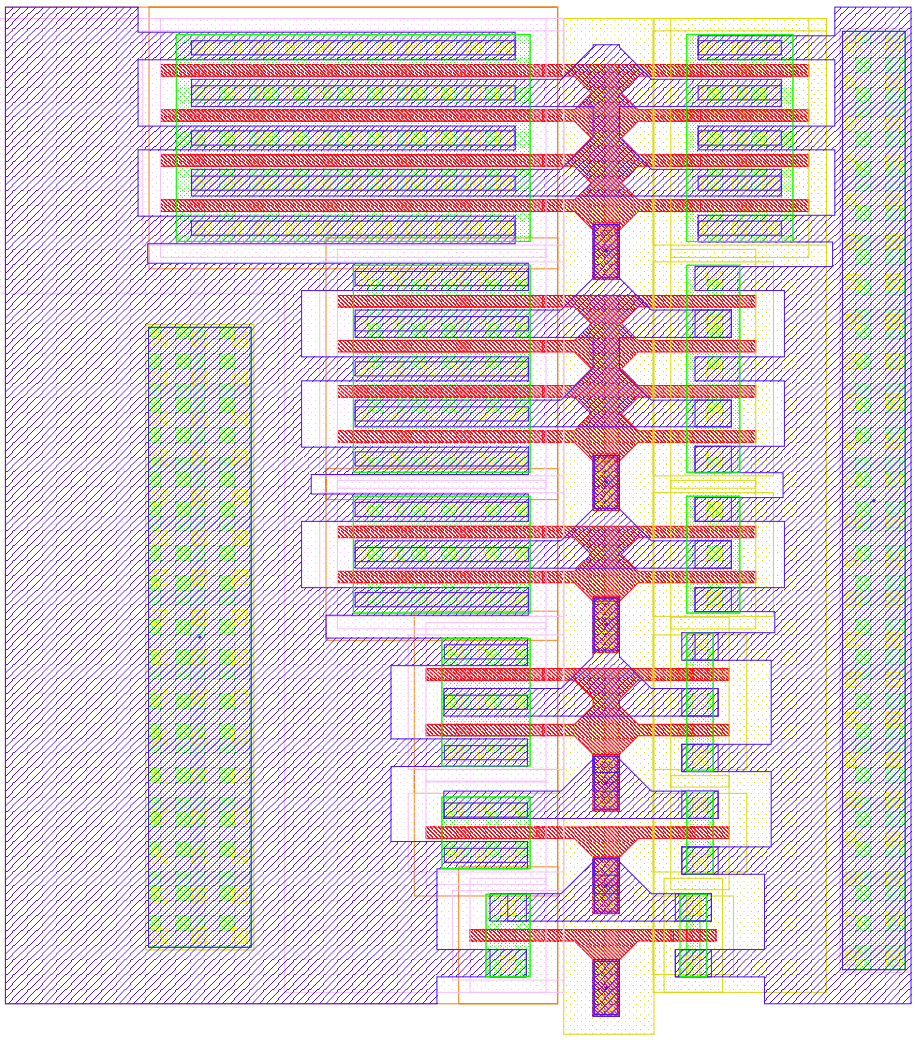

Figure B.11: Shows the layout of the output buffer used in the design.

Appendix C

Additional simulations

In this chapter all the additional simulation results are shown. The two first simulation results are simulations generated with the same testing environments as for the similar measurement results presented in section 9.3. The other simulations are Monte Carlo simulations on the five typical corners with temperatures of 0, 30 and 60 degrees Celsius for the LNA gain in the operating band.

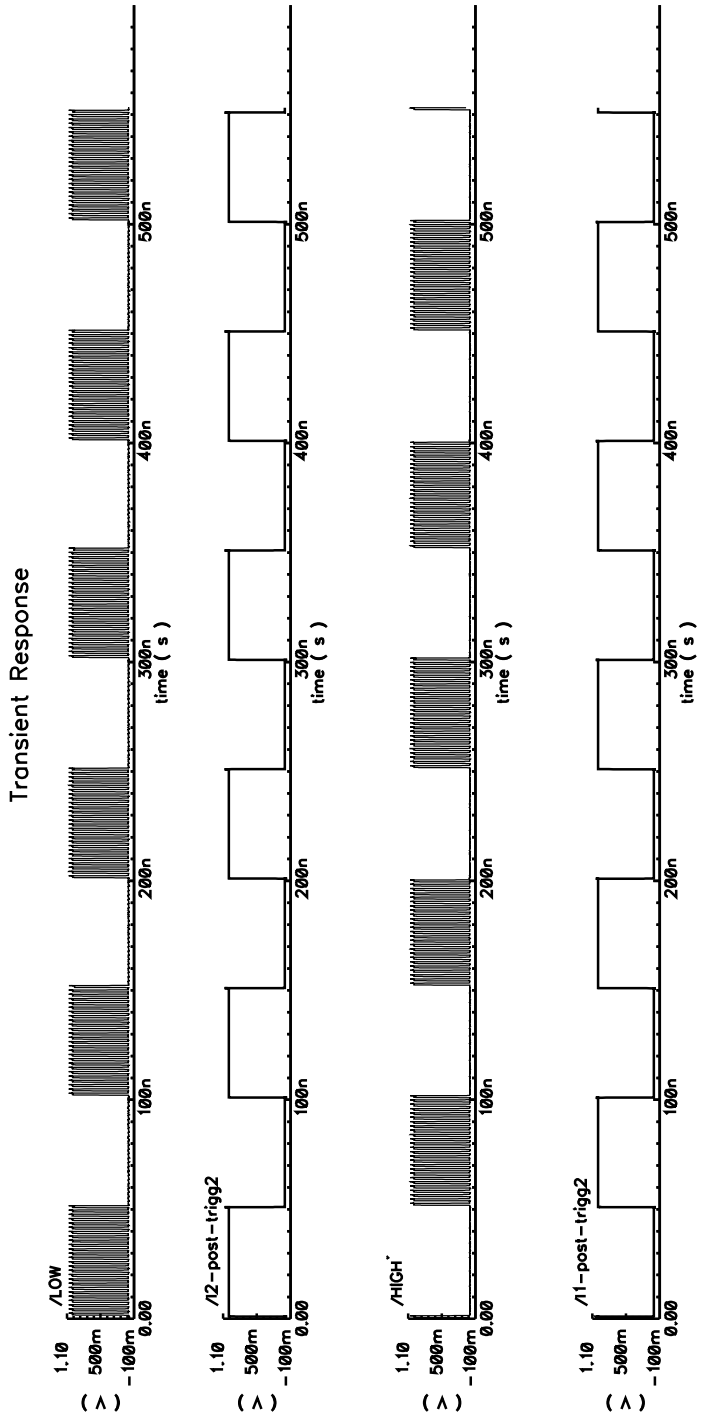

Figure C.1: Shows the simulation results from sending a square shaped waveform in through the level-shifter.

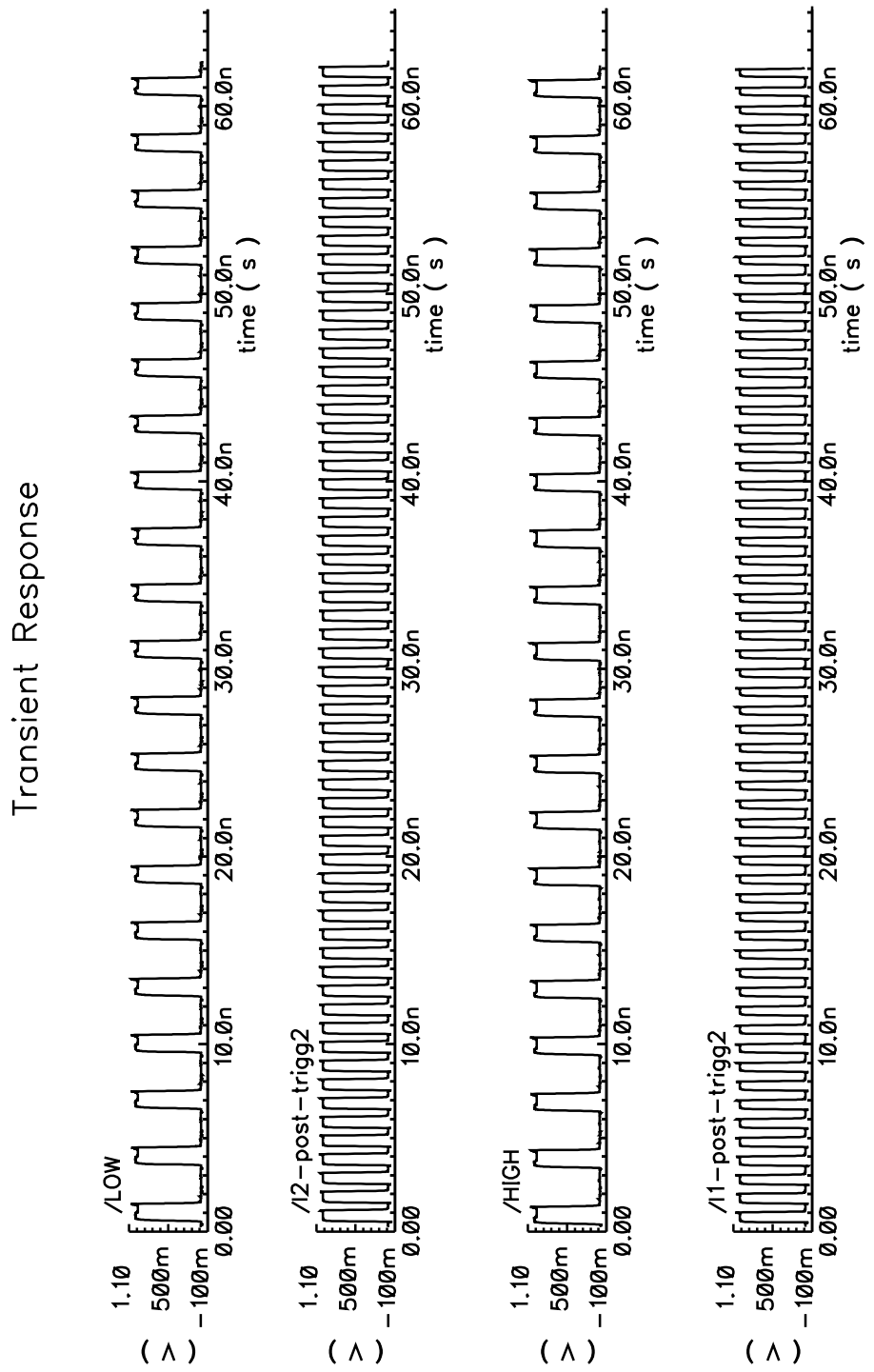

Figure C.2: Shows the simulation results from receiving a 1GHz sinusoidal waveform as input to the LNA.

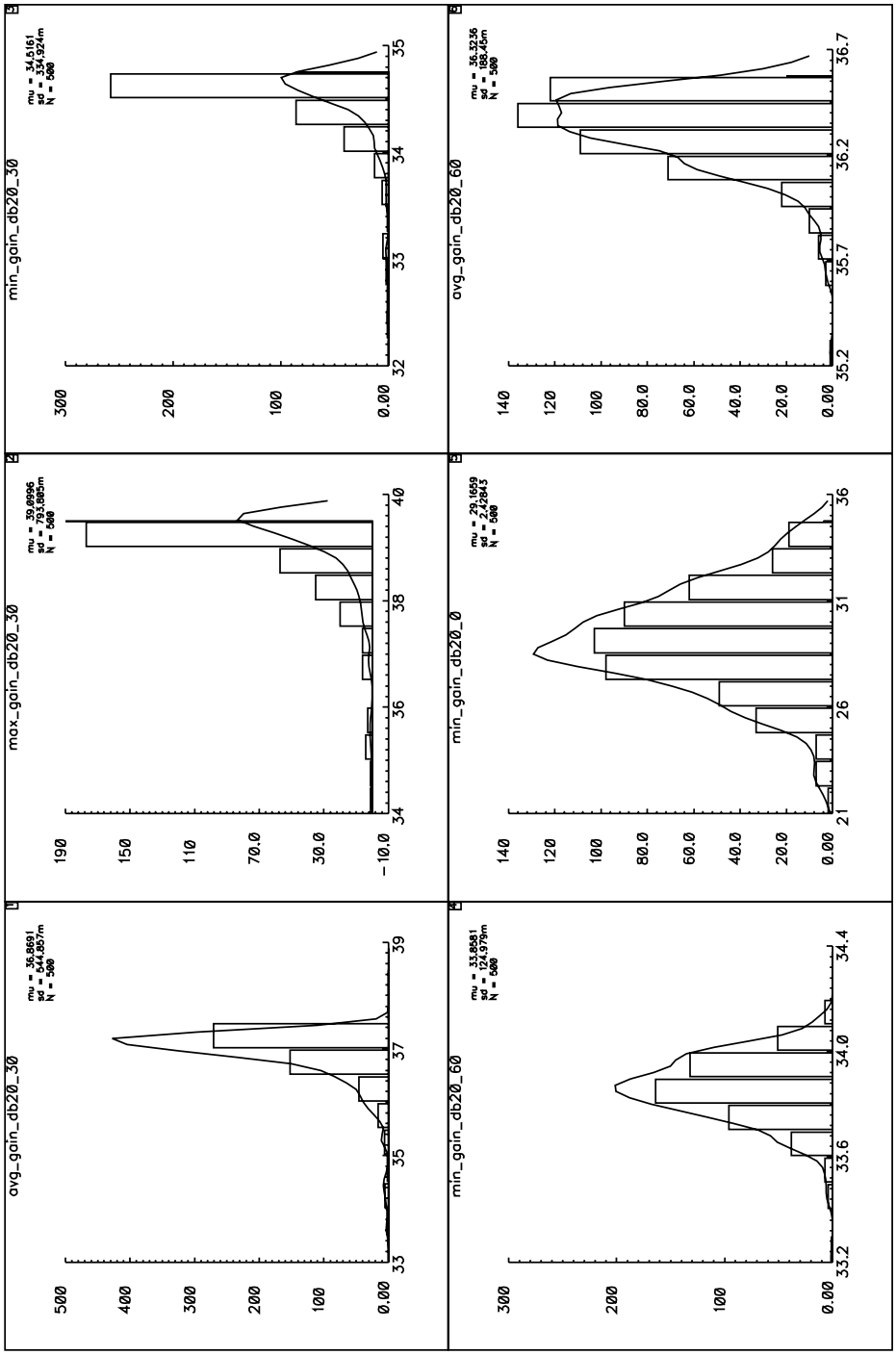

Figure C.3: Shows the Monte Carlo simulation results from an AC simulation run on the LNA with process, mismatch and temperature variations in the corner typical. The temperatures are 0, 30 and 60 degrees Celsius.

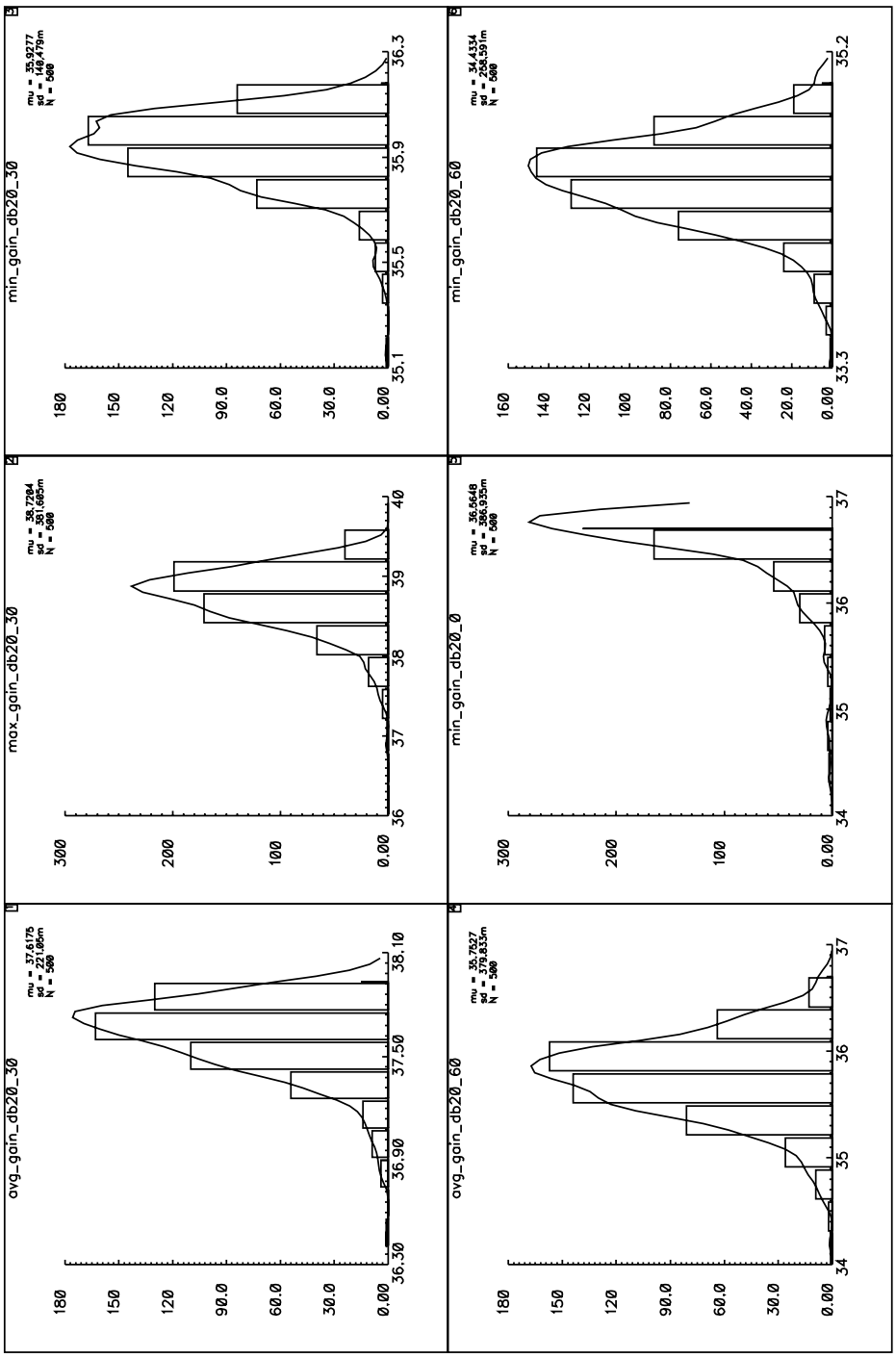

Figure C.4: Shows the Monte Carlo simulation results from an AC simulation run on the LNA with process, mismatch and temperature variations in the corner fast PMOS fast NMOS. The temperatures are 0, 30 and 60 degrees Celsius.

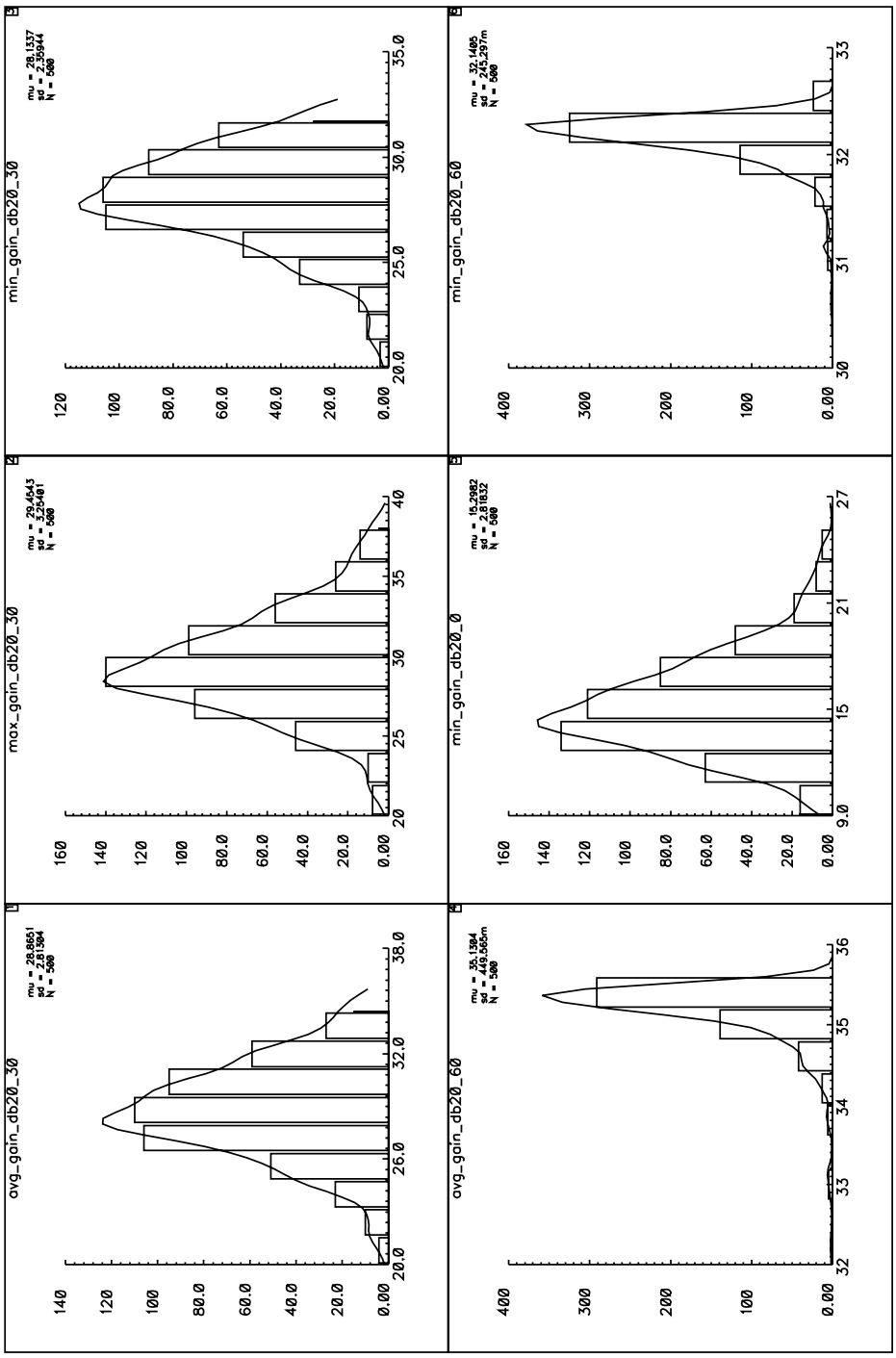

Figure C.5: Shows the Monte Carlo simulation results from an AC simulation run on the LNA with process, mismatch and temperature variations in the corner slow PMOS slow NMOS. The temperatures are 0, 30 and 60 degrees Celsius.

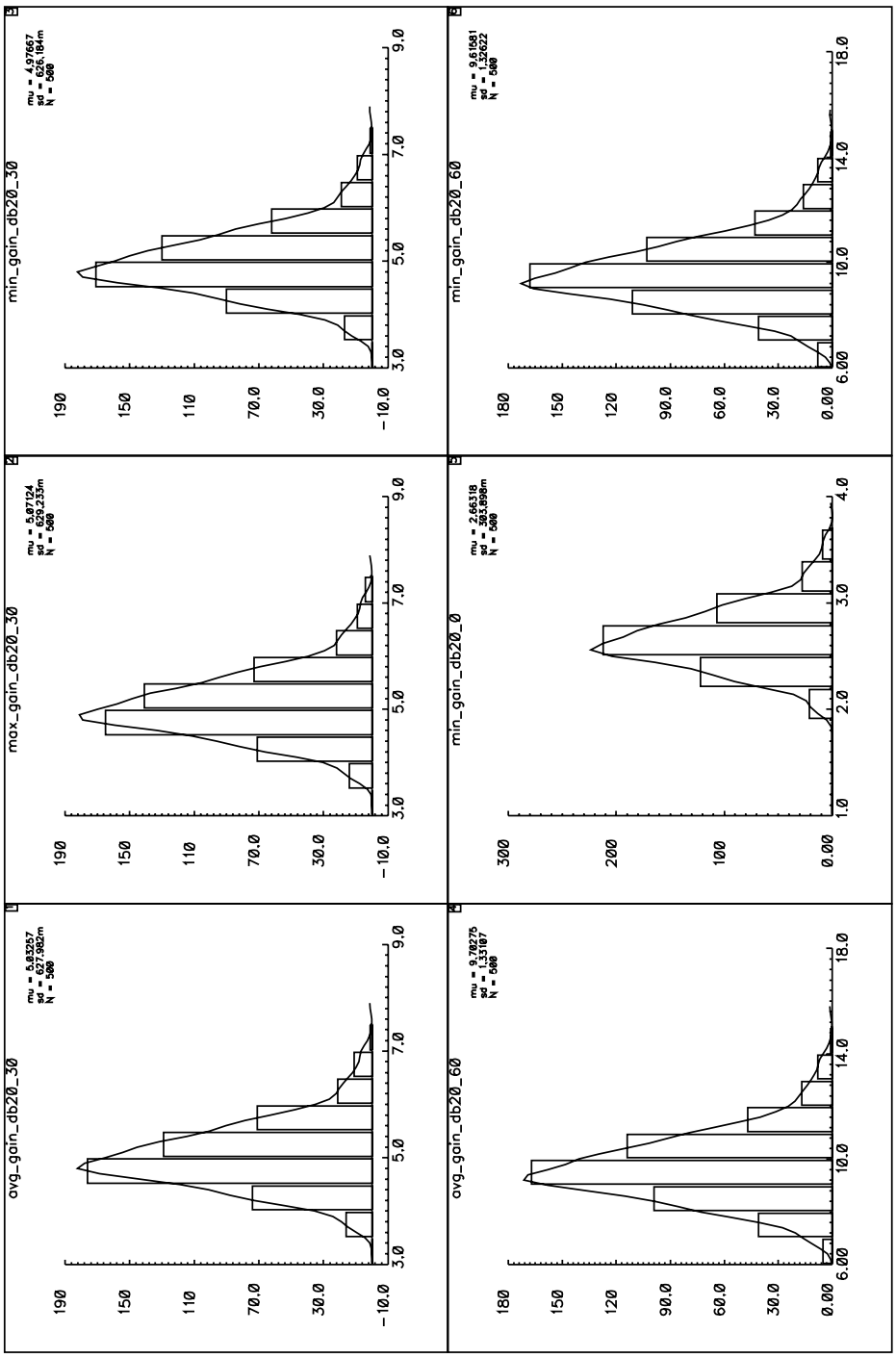

Figure C.6: Shows the Monte Carlo simulation results from an AC simulation run on the LNA with process, mismatch and temperature variations in the corner fast PMOS slow NMOS. The temperatures are 0, 30 and 60 degrees Celsius.

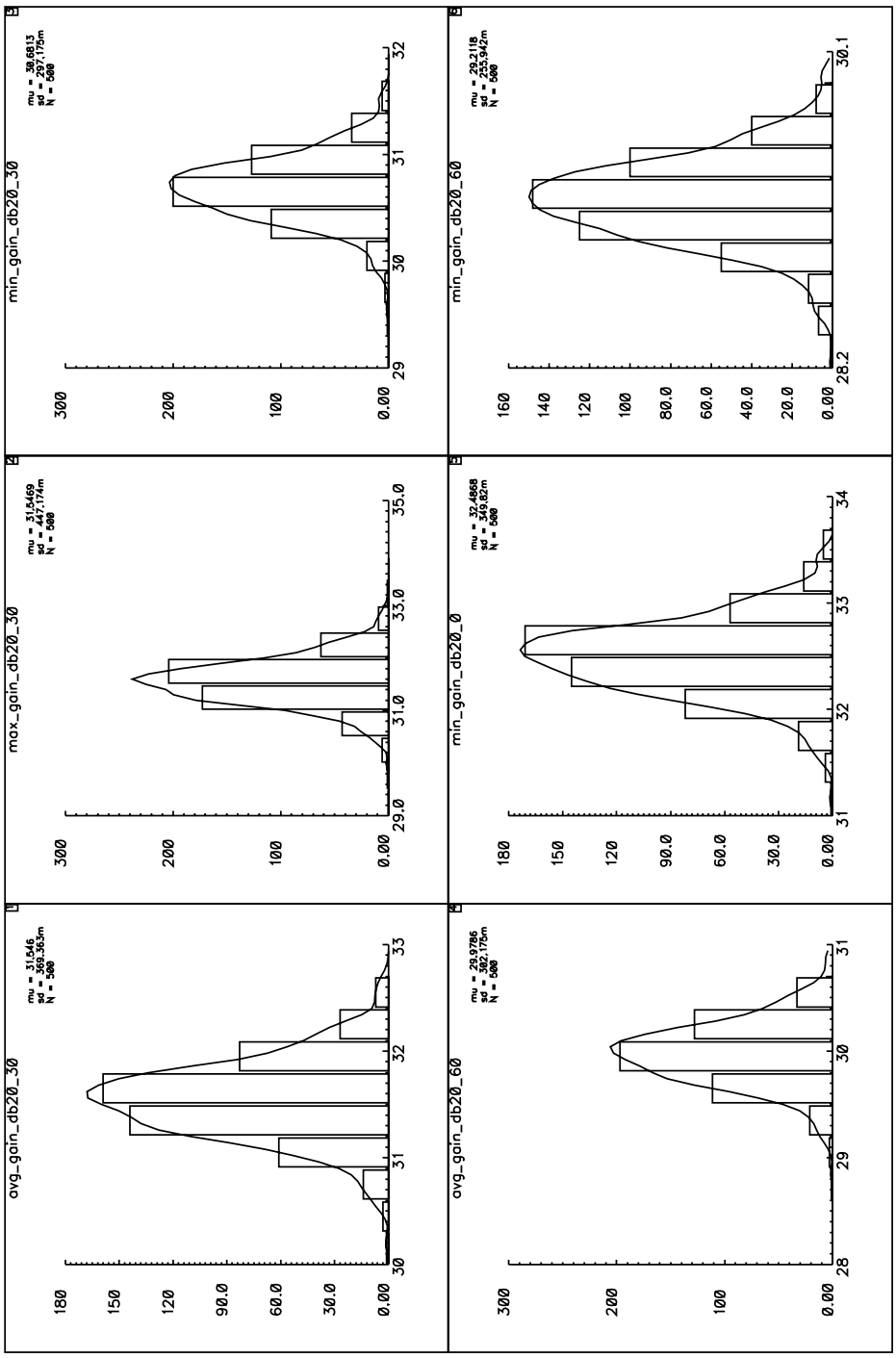

Figure C.7: Shows the Monte Carlo simulation results from an AC simulation run on the LNA with process, mismatch and temperature variations in the corner slow PMOS fast NMOS. The temperatures are 0, 30 and 60 degrees Celsius.

Appendix D

Instrument list

Measurement setup

Pin-chart for chip

Instrument list

The following table is an inventory list of the instruments used during measurement.

Measurement setups

Some different measurement setups are illustrated below, using the instruments from the inventory list. Two pictures of typical measurement setups and a lab environment picture are also added.

Pin-chart for chip

Presented here is the overview of the pins on the chip used by the design presented in this thesis.

Table D.1: Inventory of instruments used in the measurement setups.

Type of instrument	Producer/Name	Name	Specs.
Triple output DC Power supply	Hewlett Packard	E3631A	0-6, 5A / ±25V, 1A
Triple output DC Power supply	Hewlett Packard	E3631A	0-6, 5A / ±25V, 1A
Oscilloscope	Agilent	Infiniium 54855A DSO	6GHz 20GSa/s
Signal generator	Hewlett Packard	8648A	10kHz-1000MHz
Functional/Arbitrary Waveform generator	Agilent	33220A	20MHz
Functional/Arbitrary Waveform generator	Agilent	33250A	80MHz
Amplifier	Picosecond pulse labs	Linear Amplifier Model 5867	15GHz
Spectrum analyzer	Rohde & Schwarz	Signal Analyzer FSQ 26	20Hz-26.5GHz
Probe	Hewlett Packard	HF-Probe 85024A	300kHz-3GHz

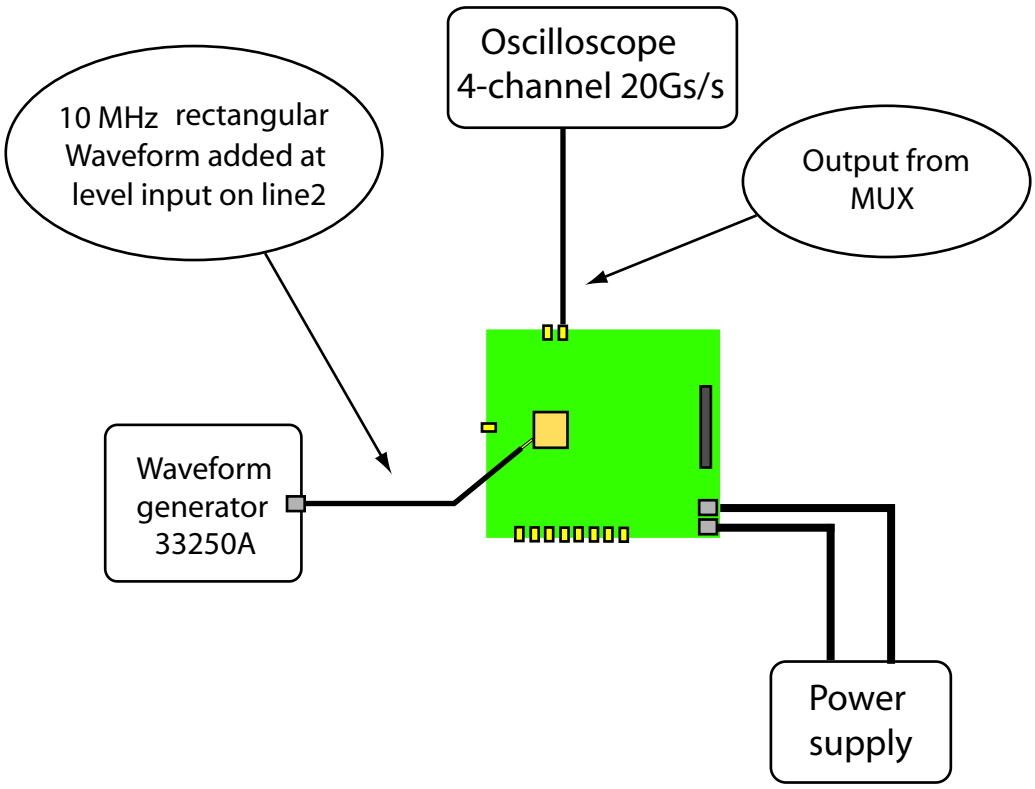

Figure D.1: Illustration of the measurement setup used where the level on one line is trigged by emitting a 10MHz square shaped waveform through the level-shifter.

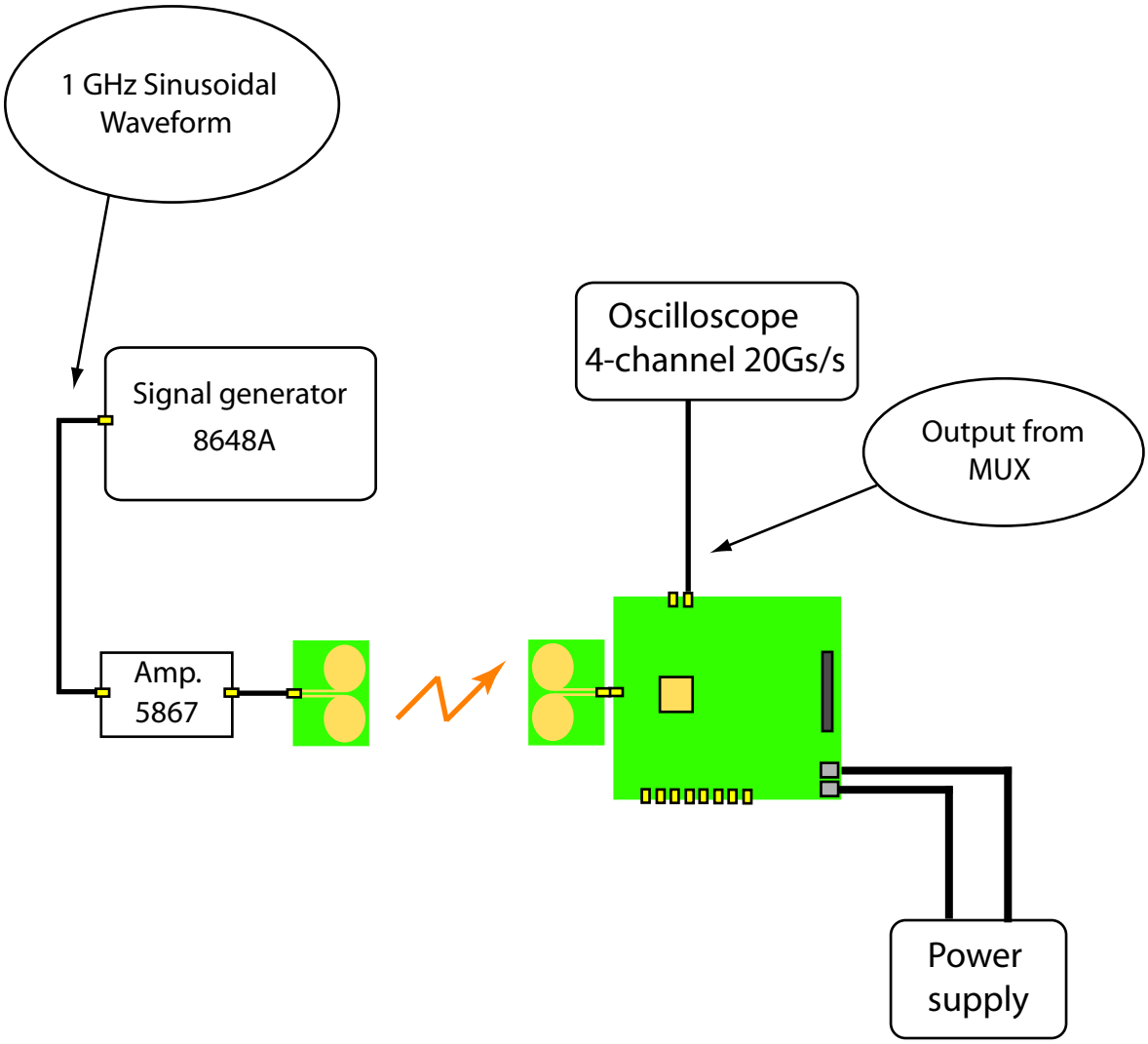

Figure D.2: Illustration of the measurement setup used where a 1 GHz sinusoidal waveform is amplified and emitted from an antenna. The signal is received by the antenna at the RF input pad.

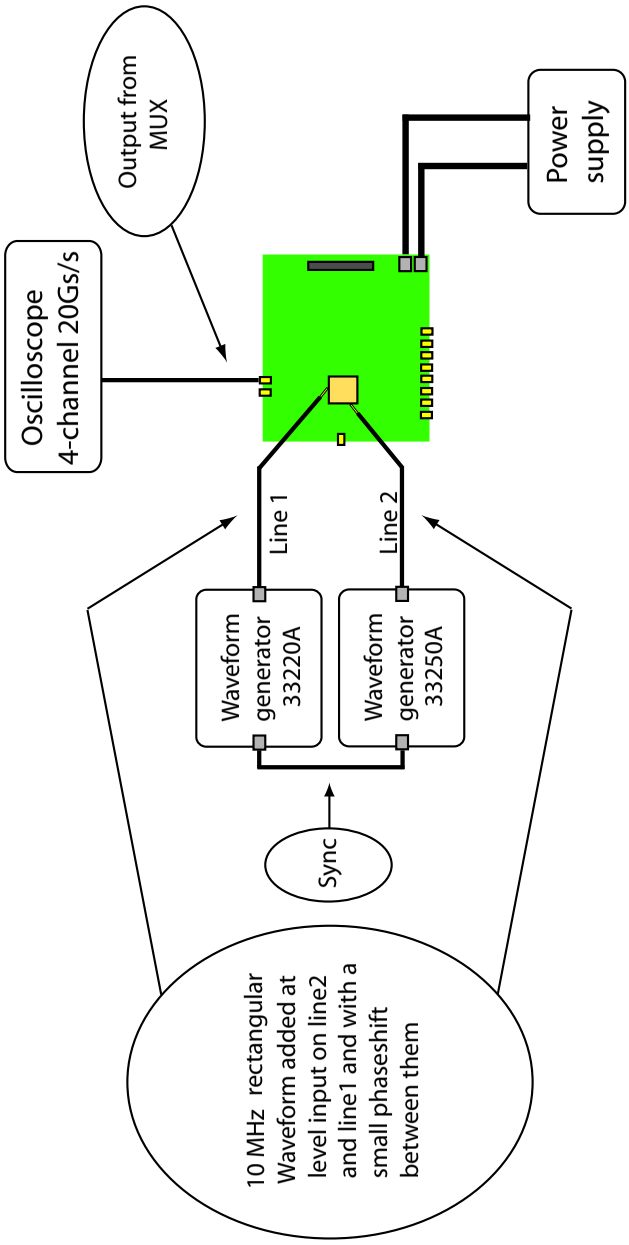

Figure D.3: Illustration of the measurement setup used where the level on both lines is trigged by emitting a 10MHz square shaped waveform through the level-shifter. One waveform is slightly phase shifted in respect to the other meant to cause a synthetic situation for triggering the dual slope detection.

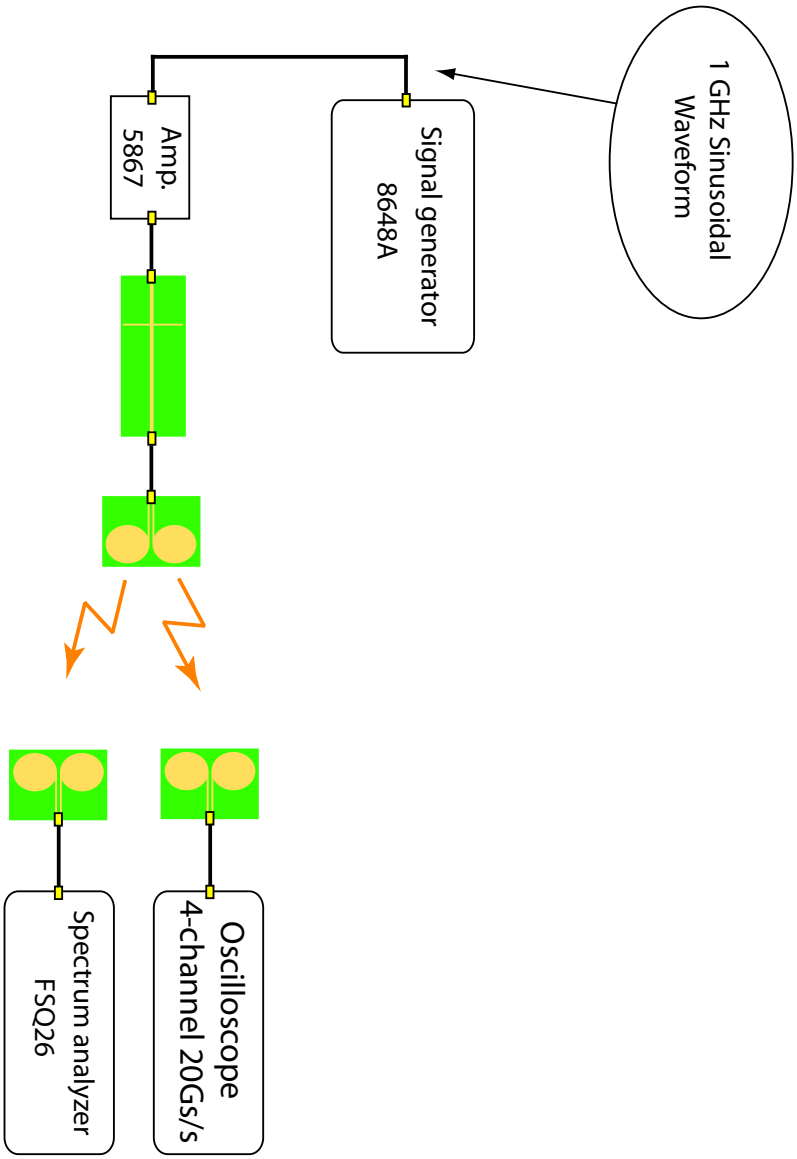

Figure D.4: Shows the measurement setup for testing if it was possible to generate dual slope pulses by using a pulse-shaping micro strip structure.

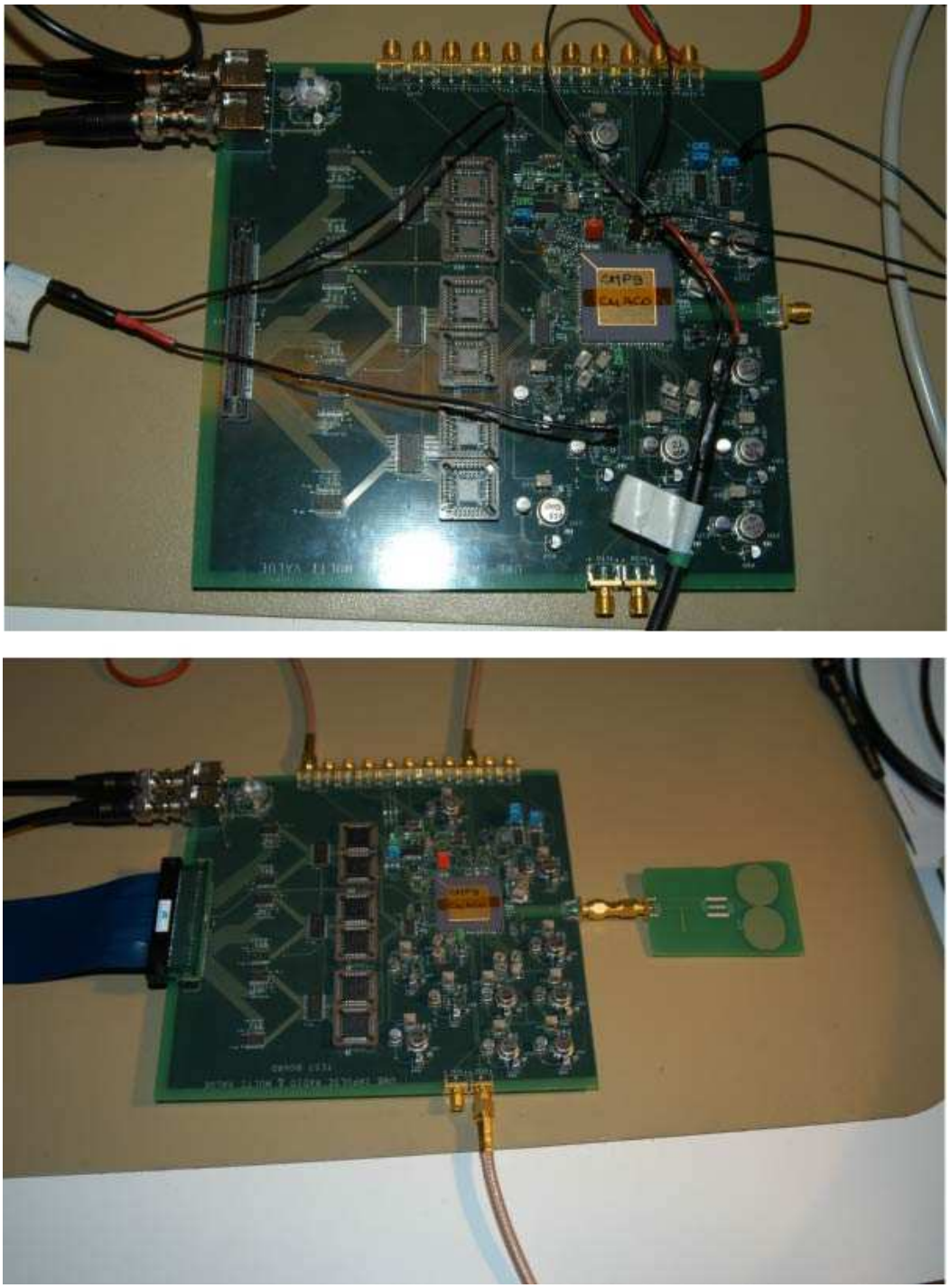

Figure D.5: Shows two typical measurement setups.

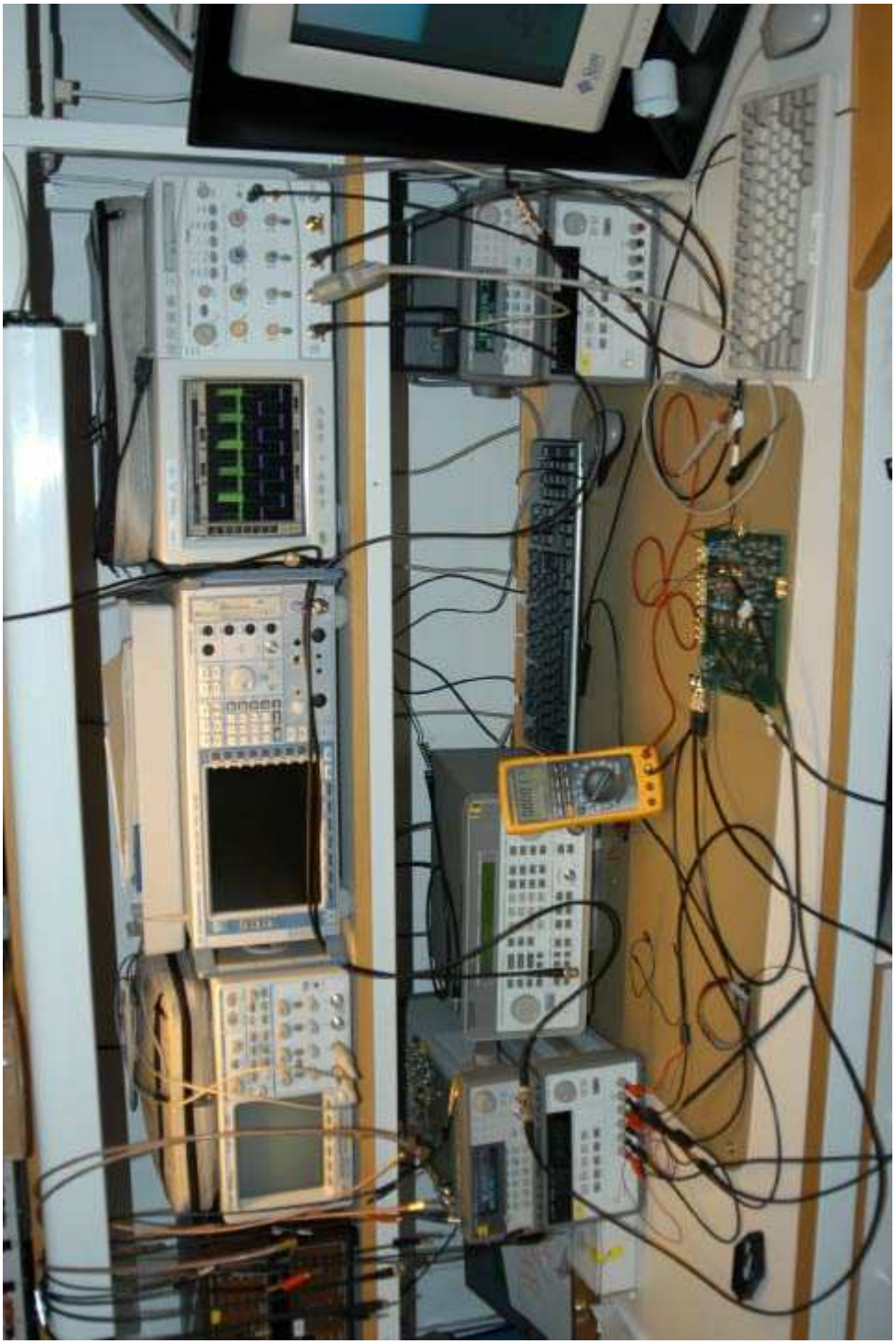

Figure D.6: Shows the lab environment.

Pin NR	Description	Pin NR	Description
5	MUX bit C	51	LNA VDD
6	MUX bit B	52	LNA Vbias 1
7	MUX bit A	53	LNA Vbias 2
10	Pad-frame VDDIO	60	Decoupling GND
11	Pad-frame GND	61	RF input pad
16	Pad-frame GND	62	VDD level-shifter RF-in
17	Pad-frame VDDSIO	63	Vlevel level-shifter RF-in
26	Pad-frame GND	64	Vbias level-shifter RF-in
27	Pad-frame VDDIO	65	GND level-shifter RF-in
39	Pad-frame GND	66	LNA GND
40	Pad-frame VDDSIO	67	Vbias level-shifter L2
41	Pad-frame GND	68	Vlevel level-shifter L2
42	Pad-frame VDDIO	69	Decoupling GND
43	Output from MUX	70	Pad-frame VDDIO
44	Output from Line 1	71	Pad-frame GND
45	Pad-frame VDDIO	72	Output from Line 2
46	Pad-frame GND	73	Pad-frame VDDIO
47	Stage 2 VDD	74	Pad-frame GND
48	Stage 2 GND	75	Pad-frame VDDSIO
49	Vbias level-shifter L1	76	Pad-frame GND
50	Vlevel level-shifter L1		

Table D.2: Shows the pins which is necessary to use for testing this design, the rest of the pins are used by different designs or not connected.

Appendix E

PCB details

In this chapter the different connection points and details on the PCB is presented by using a picture with numbers on each element, which are further explained in table E.1. A picture of the PCB with a minimum number of connection points needed to test the front-end presented in this thesis, together with some antenna structures used in measurement are also presented. The last picture also contains the strip-line attempted used for pulse shaping.

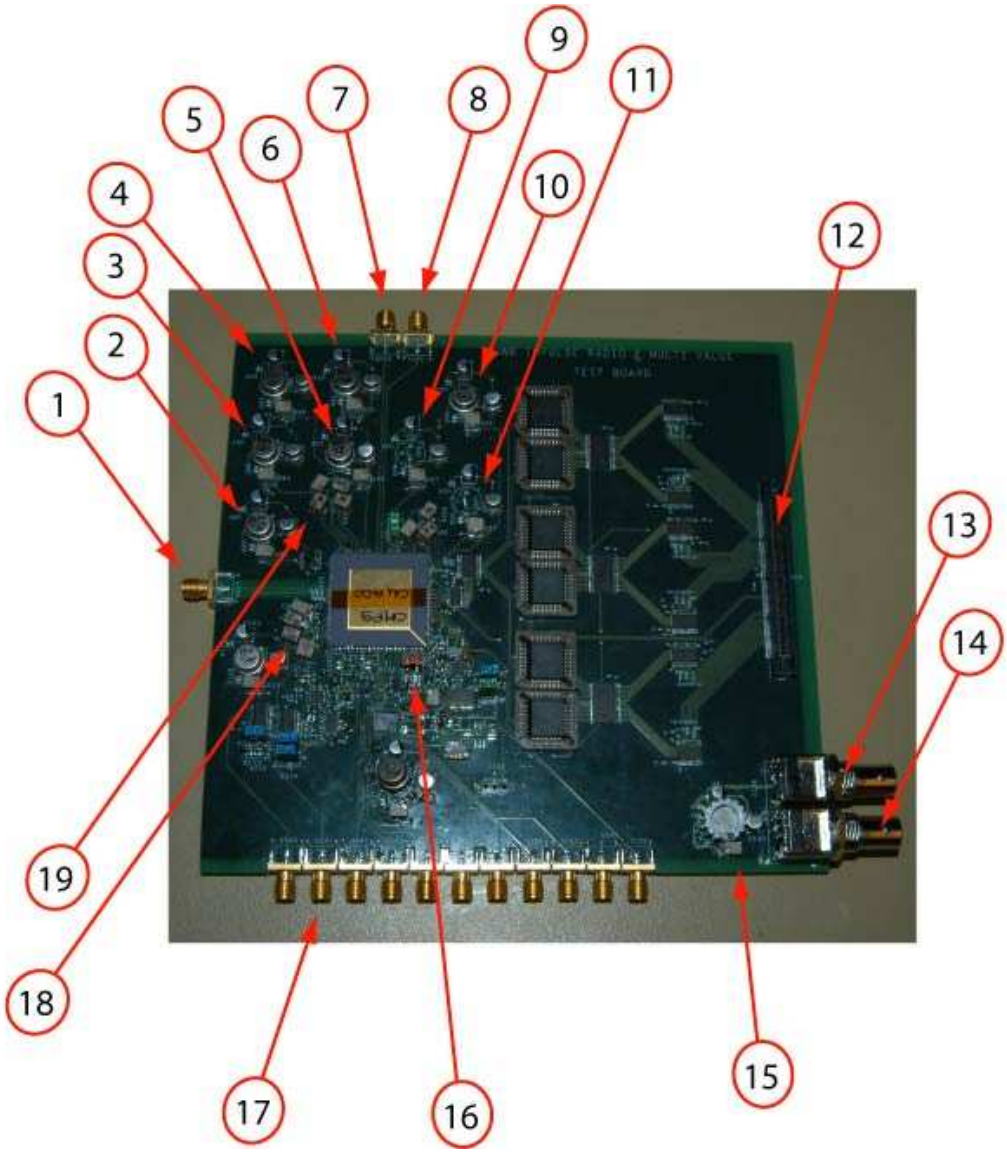

Figure E.1: Shows the PCB with index markings related to tableE.1.

index	description	index	description	index	description
1	RF-input SMA connector	8	MUX output (SMA)	15	VR for PCB 3.3V
2	VR for level and bias on LSs	9	VR for VDDSIO	16	MUX bit selection
3	VR for LNA biases	10	VR for VDD RAKE	17	Line 2 output (SMA)
4	VR for vdd level-shifter in	11	VR for VDDIO	18	Adj. LS in and line2
5	VR for VDD stage 2	12	MICTOR connector	19	Adj. LS line1 and LNA
6	VR for VDD LNA	13	POWER in +5V		
7	Line 1 output (SMA)	14	POWER in -5V		

Table E.1: Table of the connection points and voltage regulators (VR) on the PCB which is necessary to use mainly for testing the front-end design, the rest of the connection points are used by different designs on the chip.

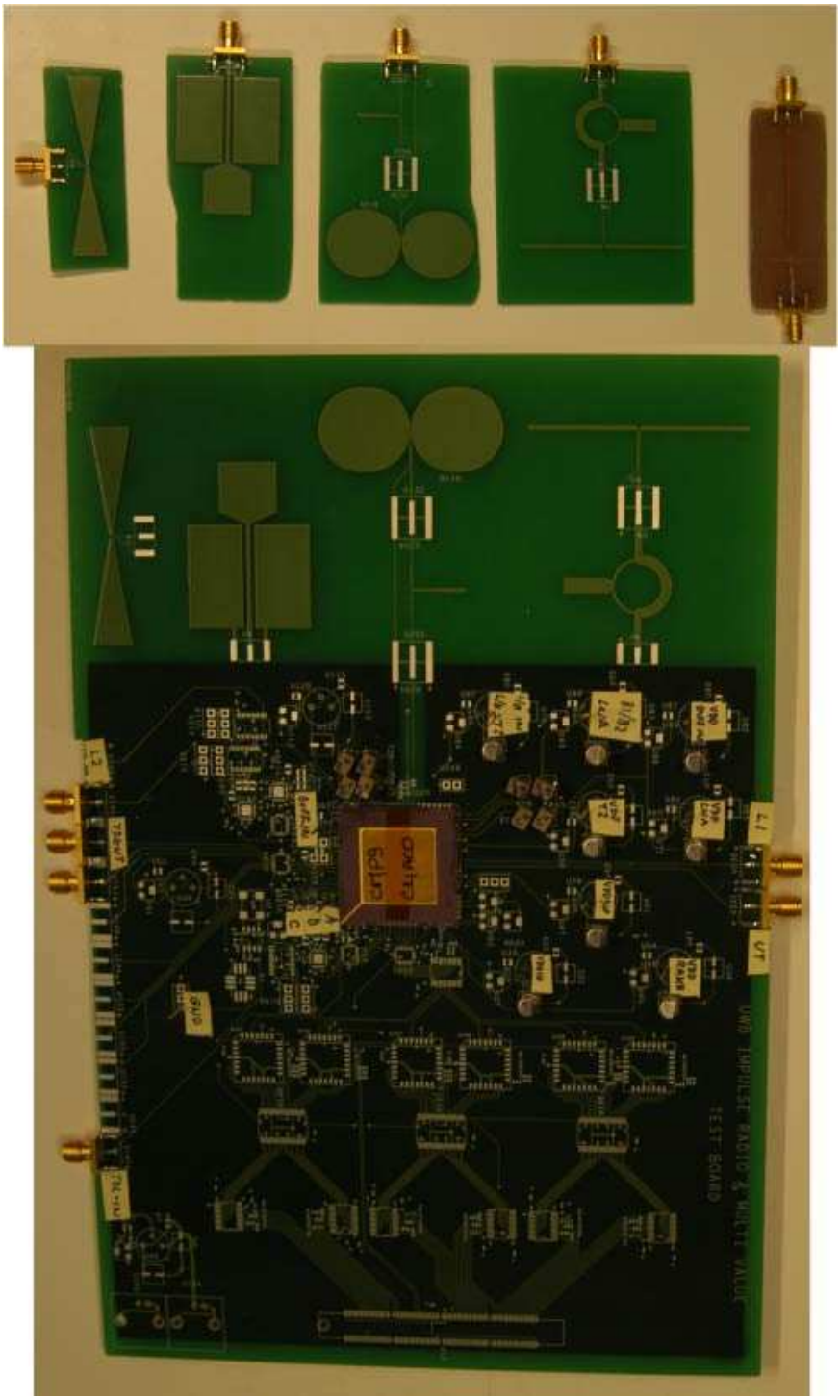

Figure E.2: Shows the PCB with minimum connection points and antenna structures used during measurement. Top left is the pulse shaping stripline tested for generating dual sloped monocycles.

Appendix F

Publications

In this chapter the publications related to this thesis are presented, where the first one is published, the second one is accepted for publication and the third one is prepared and pending for publication.

Tor Sverre Lande, Dag Wisland, Claus Limbodal and Kjetil Meisal.
CMOS UWB Receivers
Presented at the Workshop On Wireless Circuits And Systems WOWCAS at the University of British Colombia, Vancouver Canada 2004 May 21-22.

Claus Limbodal, Kjetil Meisal, Tor Sverre Lande and Dag Wisland.
A Spatial RAKE-Receiver for Real-Time UWB-IR Applications
Accepted for publication at the IEEE International Conference on Ultra-Wideband ICU2005 in Zurich Switzerland September 5-7.

Kjetil Meisal, Claus Limbodal, Tor Sverre Lande and Dag Wisland.
CMOS Impulse Radio Receiver Front-end
Prepared for submission at NORCHIP 2005 Oulu Finland November 21-22.

CMOS UWB Receivers

Tor Sverre Lande, Dag Wisland, Claus Limbodal and Kjetil Meisal

WOWCAS, Vancouver Canada, 21-22 May 2004

CMOS UWB receivers.

Tor Sverre Lande, *Member, IEEE,* Dag Wisland, Claus Limbodal, Kjetil Meisal
bassen@ifi.uio.no

***Abstract*—Ultra Wide Band systems are hard to implement in standard CMOS. In this paper we propose a spatial RAKE receiver using analog computation for symbol detection and inverter delay lines synchronization.**

I. Introduction

The purpose of this paper is to explore UWB techniques trading lower transmitted bandwidth for low power implementation. Mixed-mode practical structures are developed suitable for implementation in standard CMOS technology.

II. UWB power trade-offs.

In current UWB transceivers the major power consumption is the symbol recovery in the receiver. A typical UWB receiver is shown in Figure 1. The transmitted monocycle is received in a broadband antenna. After some course bandpass filtering (not shown) the monocycle is matched with a template. Since the emitted energy is severely restricted, the UWB signal is virtually buried in white noise. Through integration monocycles are recovered and quantized (ADC).

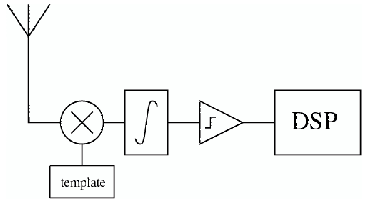

Figure 1 Generic UWB receiver

With significant noise present and interfering transmissions from other sources, several erroneous detections will occur. In order to transmit a symbol ('0' or '1') a number of monocycles must be combined for one symbol. Periodic repetition of emitted monocycles is impossible due to FCC regulations, so pseudo random sequences are used for symbol encoding.

The faint monocycle is also reflected by the surroundings giving delayed copies or reflections. In narrow band systems this kind of interference is destructive (fading). In UWB technology multipath pulses are explored constructively to reconstruct symbols. The pulse sequence is correlated in the time domain with the expected pseudo random pattern. With the presence of reflections, the pseudo random pattern will be repeated. If several parallel correlations are done on different delayed version of the received bit sequence, reflections may be used constructively to detect the transmitted symbol. (RAKE-receivers) [1].

Although a large number of multipath pulses are received for one emitted pulse [2], usually 2-3 "fingers" are used in the RAKE receiver. The main reason is the increased complexity with DSP-based RAKE implementation.

At the finest resolution a monocycle is typically integrated over a short timeslot like 1ns (Figure 2). With high energy pulses, several reflections or multipath components occur and a pulse window or bin of typically 10-50ns is used to "collect" all the emitted energy. Finally pulse detections of 50-100 bins are combined as a pseudorandom sequence to identify one symbol. A symbol encoding time is typically in the order of 500ns.

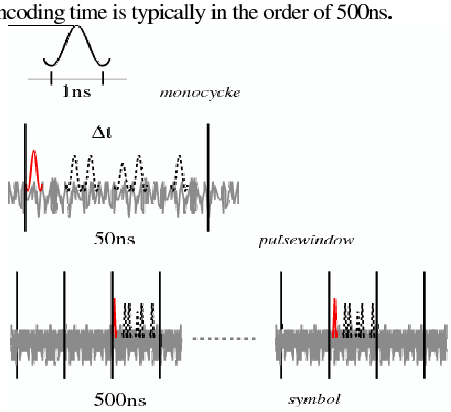

Figure 2 UWB timescales

Our aim is to explore mixed-mode circuits to implement a real-time RAKE correlation finger and digital delay lines to reduce clock frequency two orders of magnitude.

III. The spatial RAKE architecture

Each bin may contain a number of quantized monocycles. The maximum number of monocycles is varying significantly due to environmental conditions. According to [2] the strongest component usually occurs early in the observed bin. Although a significant number of reflections may occur, they tend to have damped energy.

The received signal is integrated with a short time constant reducing white noise. A simple threshold element like a comparator is used for pulse detection leaving us with a bit sequence with a rate of approximately $f_{mono}=1GHz$. Although GHz rate hardware is feasible in CMOS, great care and advanced (expensive) fine-pitch processes must be utilized. When a DSP is used, even higher clock frequencies is required to keep up with the arriving data.

Aiming at GHz operation the simplest, fastest and most compact element in CMOS is explored; *the CMOS inverter*. A cascade of 2-10 inverters should span the duration of a

monocycle (depending on technology) and the bit sequence of an observation bin may be "stored" with approximately 500 cascaded inverters. By "tapping" or sampling the inverter delay-line with a clock rate equal to the bit rate (f_{bin}) the detected monocycles within one bin is available simultaneously. The good news is that the bin rate is typically only 1/50 of the input bit rate giving a sampling clock of approximately only 20MHz.

The penalty of reduced clock rate is a number of parallel bit streams for each tap of the delay line. These bit streams are representing both the original monocycle and possible multipath reflections. Each bitstream should be inspected for occurrence of a pseudo random bitpattern encoding our symbols (usually only two: '0' and '1'). The number of bits in a pseudo random sequence is typically 50-100. These bit patterns are stored in a shift register connected to each tap on the delay line.

As suggested in Figure 3 the bit sequence stored in the shift registers is cross-correlated with a stored pseudo random sequence. As bits are shifted through the shift register, a running cross-correlation is done against the stored random sequence. Since we have two symbols, correlators and code registers must be duplicated. Since the fingers are holding the bitsequence of the different timeslots of the bin, we have synchronized the different delayed versions of the bitsequence. We are now able to compute the degree of combined match by simultaneously combine the correlation output from all the correlators. However, we need one combiner for each symbol.

By exploring spatial "maps" using delay-lines we are able to trade parallel correlation for lower clock frequency. The question is how this again may be implemented to achieve overall lower power consumption.

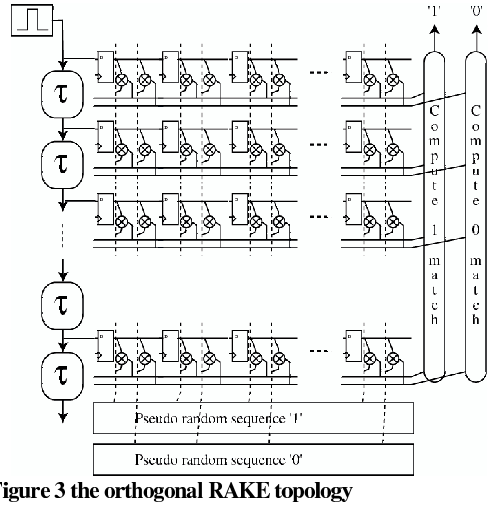

Figure 3 the orthogonal RAKE topology

IV. Implementation

The full RAKE receiver structure proposed in Figure 3 is after all a considerable matrix of correlators and shift registers. A typical number could be 50×50×2 which is something like 5000 correlators. The D-latches is just a handful of gates and 2500 is manageable.

The computation involved is statistical in the sense of finding a probability of symbol occurrence. Striving at lower power we may return to analog computation where a current-mode correlator may be implemented very simply using 3 nMOS transistors.

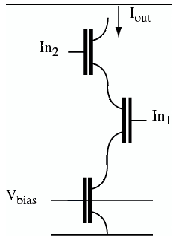

Figure 4 the correlator circuit

The current drawn by one finger is then

$$I_{finger} = \sum_{j=1}^{N} c_j I_j$$

N is the length of the pseudo random sequence, $c_j \in [0,1]$ and I_j is the unit current from each correlator. The finger current, I_{finger}, is directly proportional to the degree of match between the stored pseudo random pattern and the received bit sequence. Simply by matching the finger current with an appropriate pull-up current, the output will be low if and only if an appropriate degree of match is present.

The combiner may be implemented simply by OR-ing together the decisions from each finger. More elaborate procedures might also be implemented using some kind of weighting function. Some smoothing may also be necessary matching the maximum symbol rate.

V. Conclusions

The UWB receiver architecture presented in this paper is combining digital delay-lines with analog computation to implement a full RAKE receiver in CMOS. High speed clocks are avoided with estimated maximum clock-rate at 20MHz. This is enabling power efficient implementation in standard CMOS. Real time correlation is implemented with simple analog correlator circuit and symbol probability matching is computed using Kirchoff's current law. Initial simulations are promising and silicon implementations are underway.

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[1] R.Price and P.Green, "A Communication technique for multipath channels", Proceedings of the IRE, 1958

[2] Newhall, W.G.; Mostafa, R.; Dietze, K.; Reed, J.H.; Stutzmad, W.L.; "Measurement of multipath signal component amplitude correlation coefficients versus propagation delay" Radio and Wireless Conference, 2002. RAWCON 2002. IEEE , 11-14 Aug. 2002 Pages:133 - 136

A Spatial RAKE-Receiver for Real-Time UWB-IR Applications

Claus Limbodal, Kjetil Meisal, Tor Sverre Lande and Dag Wisland

ICU, Zurich Switzerland, 5-7 September 2005

A Spatial RAKE-Receiver for Real-Time UWB-IR Applications

Claus Limbodal, Kjetil Meisal, Tor Sverre Lande, *Member IEEE,* Dag Wisland, *Member IEEE*

Abstract— Ultra Wideband systems are hard to implement in standard CMOS technology. In this paper we present a novel spatial RAKE-receiver, exploring mixed-mode circuits for symbol detection and inverter delay lines for synchronization. The receiver is implemented as a RAKE structure combining digital shift registers with analog computation in a series of parallel taps of a synchronizing delay line. In each parallel bit stream the incoming signal is cross-correlated with a stored template. By combining a delay line and a mixed-mode correlator we can explore multipath reflections in a time domain statistical computation for symbol recovery.

Index Terms— UWB, Low-power, RAKE-receiver, Impulse radio

I. Introduction.

The concept of impulse radio (IR) has interesting properties. The wide transmission band makes penetration through different materials better than narrow band transmission. The lack of carrier may be traded for low power solutions provided a power efficient receiver may be implemented. Unlike narrow band radio, demanding statistical computation must be carried out. This is often done in a parallel (RAKE) architecture.

Although several portable applications are striving for higher bandwidth, there is however demands for short-range low bandwidth communication links like in wearable and implantable microelectronics. In several of these applications ultra low power is important. In addition other properties of impulse radio transmissions may be appreciated such as interference immunity and penetration.

The purpose of this paper is to explore low-power solutions for correlator-based impulse radio receivers. A mixed-mode RAKE-like structure is realized in a standard 0.12µm CMOS technology. Simulations are carried out and show promising results with regard to power consumption and overall functionality. Measured results are expected in short time.

II. UWB power trade-offs.

In current impulse radio receivers the major power consumption is the symbol recovery. A typical receiver is shown in Figure 1. The transmitted pulse is received in a broadband antenna. After some crude bandpass filtering (not shown) the impulse is matched with a template. Since the emitted energy is severely restricted, the UWB signal is virtually buried in white noise. Through integration pulses are recovered and quantized (ADC).

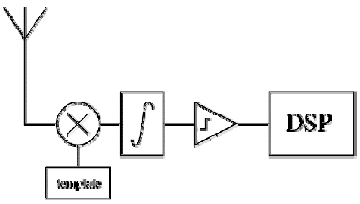

Figure 1 Generic UWB receiver

With significant noise present and interfering transmissions from other sources, several erroneous detections will occur. In order to transmit a symbol ('0' or '1') a number of pulses must be combined for one symbol. Periodic repetition of emitted pulses is impossible due to FCC regulations, so pseudo random sequences (PR) of pulses are used for symbol encoding. Typically 50-100 pulses are used for each symbol. Additional benefits with pseudo random coding is that both scrambling and canalization is achieved as well. PR sequences sparsely populated may enable a large number of simultaneous transmissions with minor interference (robust wireless link).

The faint monocycle buried in noise is also reflected by the surroundings giving delayed copies or reflections. In narrow band systems this kind of interference is destructive (fading). In impulse radio technology multipath pulses are explored constructively to reconstruct symbols. The pulse sequence is correlated in the time domain with the expected pseudo random pattern. With the presence of reflections, the pseudo random pattern will be repeated. If several parallel correlations are done on different delayed version of the received bit sequence, reflections may be used constructively to detect the transmitted symbol. These receivers are called RAKE [1] receivers and are usually implemented with a number of "fingers", one finger for each correlation.

Although a large number of multipath pulses are reported for one emitted pulse [2], only 2-3 fingers are used in the RAKE receiver. The main reason is the increased computational demand when implemented on a DSP.

Aiming at lower power consumption in UWB systems, the DSP implemented RAKE receiver structure is certainly an obvious candidate for power reduction. Current solutions depend on DSP hardware running at several GHz.

In order to understand the trade-offs three different time scales may be identified (Figure 2). At the finest resolution a monocycle is typically in the order of 200ps. With high-energy pulses, several reflections or multipath components occur and a pulse window or bin of typically 10-50ns is used to "collect" all the emitted energy. Finally pulse

detection in 50-100 bins is combined as a PR sequence to identify one symbol. A symbol encoding time is typically in the order of 500ns.

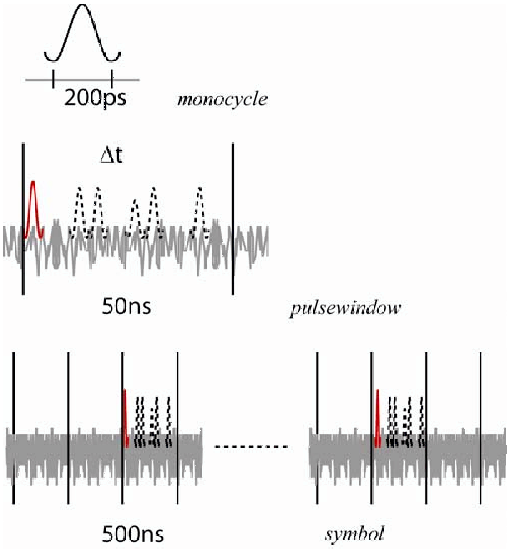

Figure 2 Impulse radio timescales

With pulse duration <1ns processing rates of several GHz must be used in order to combine a number of RAKE fingers and figure out the probability of a transmitted symbol with a DSP approach.

Our aim is to explore mixed-mode circuits to implement a real-time RAKE structure reducing clock frequency two orders of magnitude [5].

III. The Orthogonal RAKE Architecture

As shown in Figure 3 the incoming pulse is detected and quantized [4] in real time without any synchronization or clocking. The received and quantized pulse sequence is "stored" in a delay line using standard inverters. The delay is spanning one bin (typically 50ns) possibly containing the received pulse with reflections. The delay line is sampled with a clock reflecting the transmitting pulse repetition rate. For low bandwidth transmissions this may be in the order of some MHz.

The samples from the delay line are clocked into shift registers making up the RAKE fingers. Some finger will contain the PR sequence of the transmitted symbol. Depending on the number of reflections, symbol recovery is possible in several fingers. As suggested in Figure 3 the PR sequence stored in the shift registers is cross-correlated with a stored PR sequence. As bits are shifted through the shift register, a running cross-correlation is done against the stored PR sequence. With more than one symbol, correlators and code registers must be duplicated. The different fingers are not only correlating the PR sequences, but the PR sequences are also synchronized. We are now able to compute the degree of combined match by simultaneously combine the correlation output from all the correlators. However, we need one combiner for each symbol.

By exploring spatial "maps" using delay-lines we are able to trade parallel correlation for lower clock frequency. The question is how this again may be implemented to achieve overall lower power consumption [5].

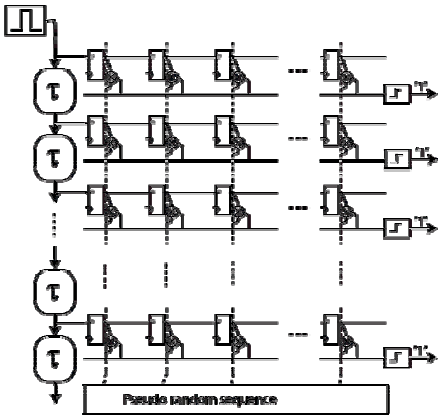

Figure 3 the orthogonal RAKE topology

IV. Implementation

The full RAKE receiver structure in Figure 3 is after all a considerable matrix of correlators and shift registers. It is built up as a 50x50 matrix of cells in a finger structure each consisting of one D-latch and one correlator, with a total of 2500 correlators and D-latches.

The arriving pulses have been shaped by a front-end, and are distributed as 1ns pulses through the delay line [4]. No delay is needed for the first finger so the delay line consists of 49 elements with 30 standard minimum sized inverters in each element, which adds up to a number of 1450 inverters. Aiming at a unit-delay of approximately 1ns, 30 inverters should match this requirement with the process used.

The computation involved is statistical in the sense of finding a probability of symbol occurrence. Striving at lower power we return to analog computation, as a correlator may be implemented very simply using three transistors.

However it is interesting to investigate the property of canalization. For PR-sequences of a given length there is a trade-off between canalization and bit error rate (BER). An increasing number of channels result in a higher BER. Increasing the length of the PR-sequence will improve both.

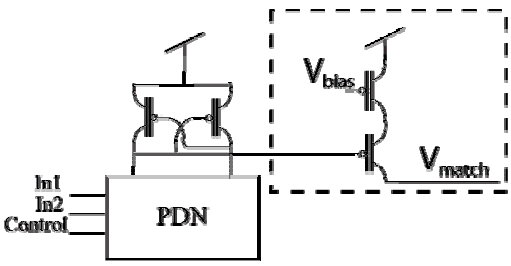

Figure 4 the implemented correlator circuit

By including simple digital logic, two different detection

modes are available. Detecting only matching of '1' is effective in a noisy environment while correlation of both '1' and '0' may be more efficient enabling shorter symbol sequences. Thus we needed the possibility to set the operation mode of the correlator between correlation on only ones and both ones and zeroes, which gives a combined XOR- and AND-gate. Extra logic had to be included in the correlator circuit in order to achieve the desired functionality as depicted conceptually in Figure 4.

The correlator consists of two parts. Two pMOS transistors controls the correlation current in case of a match, and a differential cascode coupled circuit performs in this case the actual comparing between the two inputs in a pull down network (PDN). The PDN consists of 13 nMOS transistors implementing the required combinatorial function. This kind of logic combines two concepts: differential logic and positive feedback, and requires that each input is provided in complementary format [6]. In order to meet this requirement three inverters, one for each input, are embedded in the PDN. The Control input decides whether the correlator matches only ones or both binary levels, while the two other inputs are the stored template and the output of the D-latch in each cell. The Vbias input controls the current flowing to the output line which contributes to pull the voltage level on the output line up to threshold level. Vmatch is the actual connection to the output line.

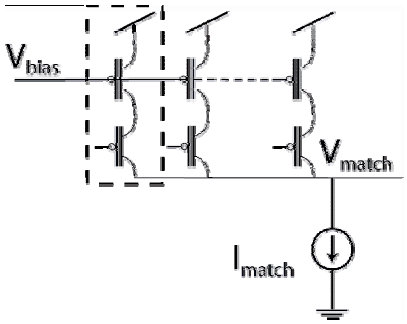

Figure 5 the principle of the current mode correlation

The circuit drawn in Figure 5 is like wired current-limited AND-gates. When the inputs are low, a unit current I_{out} is delivered as set by the bias voltage. The correlation currents from all correlators of each finger are summed on a single wire by interconnection. The current drawn by one finger is then

$$I_{finger} = \sum_{J=1}^{N} c_j I_j .$$

N is the length of the pseudo random sequence, $c_j \in [0,1]$ and I_j is the unit current from each correlator. The finger current, I_{finger}, is directly proportional to the degree of match between the stored pseudo random pattern and the received bit sequence. Simply by matching the finger current with an appropriate pull-down current, the output will be high if and only if an appropriate degree of match is present. The pull-down current provides a simple pre-charging to the output line. This pre-charging is performed by two nMOS transistors in series like a current-mode AND-gate. One transistor is running on inverted clock to pull down the output line between sampling, while the other transistor is for current limitation.

The comparator at the output of each finger (Figure 6) is a simple structure chosen because of its low power consumption and self-biasing properties in addition to a fairly good range of adjustment [3]. With some additional pulse shaping and driving capability in the output inverters this should be sufficient.

In order to reduce the number of output pads required for the output signals, six pre-designed 8-to-1 multiplexers were used. These will operate on a 160MHz clock frequency in order to keep up with the streaming data from all outputs.

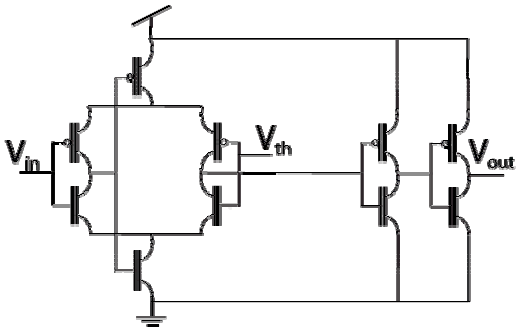

Figure 6 the comparator circuit

The RAKE-receiver is realized in a standard 0.12µm process on the same silicon as a front-end circuit [4]. The size of the complete receiver structure is 993µm by 682µm and contains just over 103000 transistors. Figure 7 show a picture of the RAKE-receiver. On the left side the delay line can be seen, while on the right side the six multiplexers and the output from the comparators are easily observed.

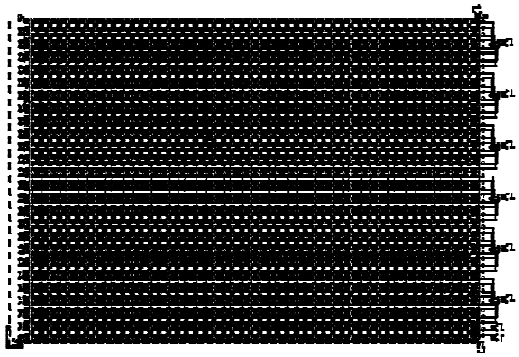

Figure 7 a picture of the RAKE-receiver

Figure 8 show the complete chip with pads. The RAKE-receiver is easily observed. The front-end is seen in the upper left corner with its decoupling capacitors as black squares. The total size of the chip is 1792µm by 1333µm.

So far simulations show promising result with regard to power consumption. Based on simulations estimated idle

power consumption of the receiver is about 50nW. An estimate of a fully correlating finger, with a sampling frequency of 20MHz is about 100µW. Similar hard wired receiver topologies for comparison are hard to find.

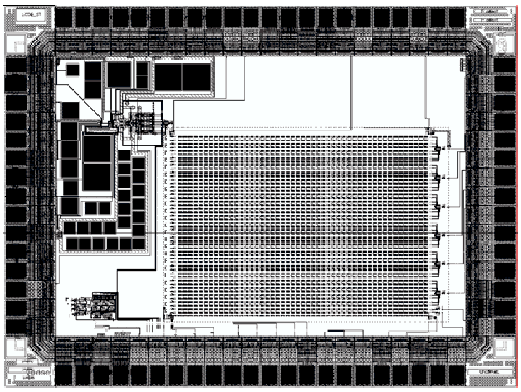

Figure 8 a picture of the chip with the RAKE receiver and front-end

V. Partial RAKE receiver

The proposed structure in Figure 3 is often called a full RAKE receiver with a finger for all available taps of the delay-line. It is however possible to reduce the number of fingers if the interesting bits are occurring repeatedly in the same position of the delay line. This may be possible if the clock is locked to some property of the bit stream. It is reasonable to assume some clustering [2] since reflections is a consequence of an initial emitted pulse. A possible approach could be to measure the "energy" of the lower part of the delay-line. Provided some clustering around the emitted pulse exists, the clock could be tuned to achieve the highest energy at that location. We may again turn to a current-mode approach. If digitally controlled current sources are attached to the lower taps and summed on a wire, the total summed current should be proportional to the number of '1' in the lower part of the delay line. This again may be used to synchronize the clock with a PLL. Due to the pseudo random occurrence of the clusters, clock adjustments must be slow.

The clock adjustment must however cope with the high frequency bit stream and significant current must be used to keep up. Based on simulations done on one finger, an increase in sampling frequency from 20 MHz to 40 MHz cause an estimated increase in power consumption of about 30%.

The upside is that the number of fingers may be reduced to taps at the lower part of the delay line. When earlier taps are not used, we may simply remove them and reduce the power consumption.

Another important consequence is that we may reduce the transmitted data rate by increasing bin length and still use the same receiver topology.

VI. Simulations

Figure 9 shows the result of a simulation of a delay element. The delay is just a few picoseconds less than 1ns.

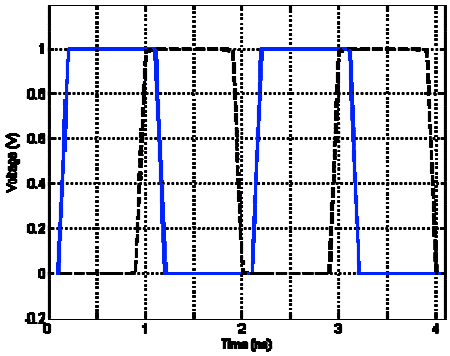

Figure 9 the time delay of one delay element

In Figure 10 the comparator functionality is shown. The dotted line is the input signal, which is a voltage going linearly up from zero to one volt in 50 ns, and then down to zero at 100ns.

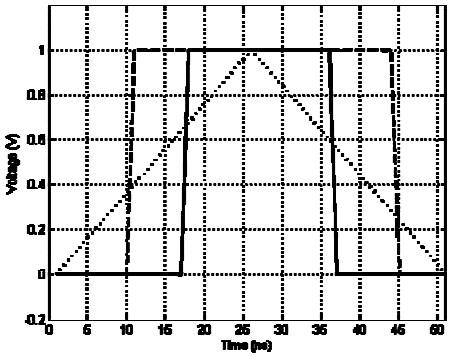

Figure 10 range of operation of the comparator

The dashed line show how the output responds to the changes in input voltage when the threshold voltage is set to 310mV. The solid line show the output voltage response when the threshold is set to 690mV. These two voltages determine the range of operation of this comparator.

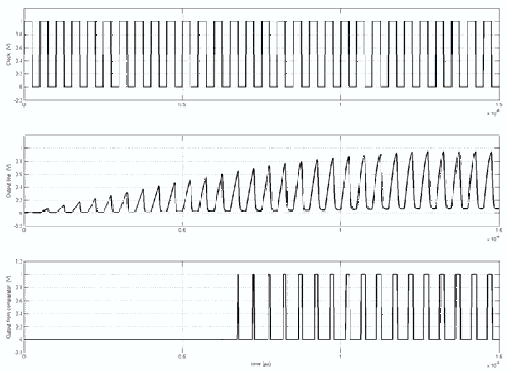

Figure 11 simulation results of one RAKE finger

Figure 11 shows the output from a simulation of a RAKE finger. The threshold voltage of the comparator is here set to 600mV. The top curve is the clock, while the curve in the middle shows the voltage level at the output line. The bottom curve shows the output from the comparator. The shift register with the template has been filled with only ones, the correlator is set to correlate on only ones and the input of the finger is set to the positive power rail. By doing this we get a signal of only ones traveling one step in the RAKE finger shift register each clock period. For each period we then get an increment in the number of correlators contributing to pull up the output line. In the simulation presented in … the correlation threshold is reached after 14 clock pulses corresponding to a match on 14 correlators. As expected the mixed-mode circuits presented are handling the modest frequency requirement of the spatial RAKE receiver.

Measured results are expected in short time; if possible they will be included in the final paper.

VII. Conclusions

The power efficient UWB receiver presented in this paper is combining digital delay-lines with analog computation to implement a full RAKE receiver. High-speed clocks are avoided with estimated maximum clock-rate at 20MHz. This is enabling power efficient implementation. Real time correlation is implemented with simple analog correlator circuit and symbol probability matching is computed using Kirchoff's current law. The receiver is realized in a standard 0.12µm CMOS process, with simulations showing promising results.

References

[1] R.Price and P.Green, "A Communication technique for multipath channels", Proceedings of the IRE, 1958

[2] Newhall, W.G.; Mostafa, R.; Dietze, K.; Reed, J.H.; Stutzmad, W.L.; "Measurement of multipath signal component amplitude correlation coefficients versus propagation delay" Radio and Wireless Conference, 2002. RAWCON 2002. IEEE , 11-14 Aug. 2002 Pages:133 – 136

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CMOS Impulse Radio Receiver Front-end

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Abstract — Low power impulse radio receiver front ends are hard to implement in standard CMOS. In this paper we present a simple thresholding solution exploring simple inverter structures. The ultra wide band impulse radio receiver front end consists of a LNA, integrator and thresholding pulse shaper all in standard digital CMOS technology. The continuous time front-end is designed to work with a RAKE receiver for low power ultra wide band applications.

Index Terms— UWB, Low-power, Impulse radio

I. Introduction

The focus on short range wireless communication technology is increasing. Although standards like Bluetooth should address such demands, there seem to be intense development of increased bandwidth using lower power. An interesting technology is Ultra Wide Band (UWB) or Impulse Radio. With the recent FCC approval of wide-band transmission between 3.1GHz-10.6GHz with a EIRP emission level at -41.6 dB several efforts have emerged achieving in excess of 100Mbit/s data rates for short range communication.

The concept of base band radio using very short pulses has other interesting advantages. The wide transmission band makes penetration through different materials better than narrow band transmission [6][7]. The lack of carrier may be traded for low power solutions. Traditionally narrow-band based transmissions are wasting energy on a HF carrier which in itself is transferring no information.

There is, however, another interesting development of short-range low bandwidth communication links like in wearable and implantable microelectronics (Personal Area Networks) [10]. In several of these applications like implantable devices ultra low power is important. Exploring impulse radio for robust wireless communication in medical applications is also interesting.

In this paper we propose a novel front-end for impulse radio receivers suitable for implementation in standard CMOS technology. The novel architecture is exploring continuous time delay lines avoiding high speed sampling clocks. The proposed solution is implemented in STM 120nm CMOS process.

II. Sampled Delay-line Architecture

There are several approaches to UWB or impulse radio receiver front-ends [9][10].

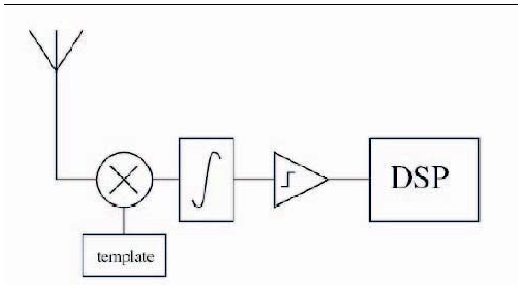

Figure 1: Generic UWB receiver

As shown in Figure 1 in a typical UWB receiver the incoming signal is multiplied with a template, integrated and quantized. The symbol recovery processing is done by signal processing algorithms in the DSP. However, this architecture is hard to optimize for low power solutions due to very demanding timing constraints and the high sampling rate required to process GHz signals.

We are exploring a continuous time solution using early quantization and a sampled delay-line architecture relaxing timing constraints. The sampling rate is reduced to something less than 100MHz.

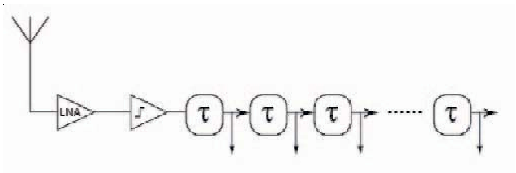

Figure 2: Sampled delay-line architecture.

In Figure 2 the sampled delay-line architecture is shown. The incoming wideband signal is amplified in a LNA and then immediately quantized. The sequence of received impulses is delayed using cascaded inverters. The delay-line may now be sampled with a 20-40MHz clock and decoded using parallel correlators in a RAKE arrangement [4][5]. Although sampling rate is reduced, the sampled delay-line architecture must handle the bandwidth of UWB signals (10GHz) making a straight CMOS implementation quite demanding. Our UWB front-end is implemented using 120nm technology from ST Microelectronics with a ft around 90GHz.

The length of the time delay line and the duration of the fabricated pulse is a representation of the total amount of fingers in the RAKE constellation and the last possible received reflection. The 1ns length of the fabricated pulse

and the 50ns length of the time delay line implicates that the reflections used are located 30cm to 15m apart from the original pulse.

III. LNA DESIGN

The wideband LNA amplifies the input signal with a gain of 25-30dB. With an extremely weak input signal, low noise structures are required. Our approach is to reduce the number of active elements to a minimum. As most fine pitch processes are triple well careful design may reduce substrate noise. The degree of isolation this provides together with decoupling and shielding should reduce the impact of noise on the amplifier. The proposed LNA is a simple cascode amplifier with a serial conductive load [Figure 3].

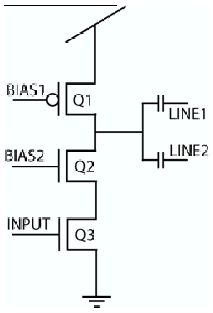

Figure 3: LNA architecture

The topology consists of an input transistor (Q3), and two biasing transistors (Q1 and Q2). The cascoding transistor (Q2) is improving LNA gain, and transistor Q1 is controlling the load current. This design is giving high frequency and driving performance in the required UWB band (Figure 8).

The transistor mismatch and parasitics is hard to predict in advanced processes. Especially the parasitic capacitances of the wires seem to have major impact [7]. By using large transistors and capacitors, and by making the design compact with short interconnections, the impact of parasitic capacitors is reduced.

The input of the LNA is level shifted by a voltage follower of the same design as the one described in section V.

IV. COMPARATOR/QUANTIZER

The first question is to what extend the incoming, noisy signal could be quantized by simple thresholding. The emitted pulse is mixed with significant noise, so looking for a fixed threshold might not be feasible, either too noisy (low threshold) or too lossy (high threshold). We still find this approach feasible for two reasons: 1) Symbol transmission is designed for lossy data using pseudo-random sequences and cross-correlation for statistical symbol recovery. 2) We have added dual-slope detection. By assuming transmitted pulses to be a sequence of a charge of one polarity followed by a charge of opposite polarity (figure 4), we expect to achieve sufficient discrimination.

The high frequency and low amplitude of the incoming signal makes it difficult to use a standard differential comparator for thresholding. In order to achieve high frequency performance our topology is based mostly on inverters, which sometimes is combined with a capacitive feedback to improve high frequency gain. The idea of pulse shape recognition is quite simple and is a combination of thresholding and logical gates. As shown in Figure 4 we are thresholding both slopes of an emitted impulse. By construction, the inter-slope time is fixed and set to τ. In order to detect both slope polarities (positive followed by negative and negative followed by positive) we feed the amplified signal through two different signal paths.

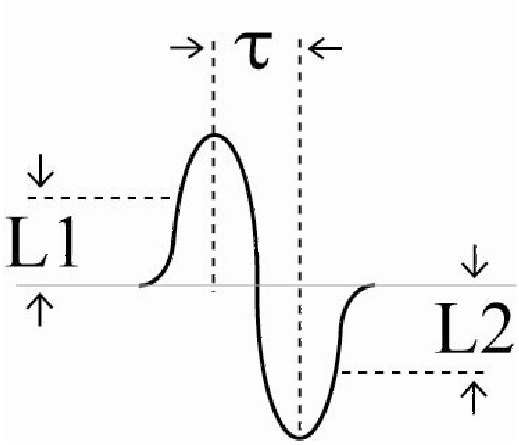

Figure 4: Dual slope monocycle (positive followed by negative)

In both signal paths the signal is level shifted to a suitable level depending on slope polarity. The detected pulses are shaped to pulses with the same duration (approx. 1ns). After thresholding the early pulse is delayed by τ and the final impulse is detected by simple digital logic.

The circuit implemented is shown in Figure 5 and has one path for each slope polarity. For details about the level shifting and thresholding circuit, see section V.

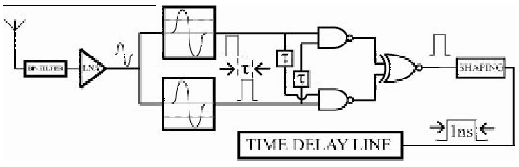

Figure 5: Pulse shape detection schematics

A following stage correlates the pulse with a delayed version of the pulse on the parallel path, where the delay reflects the preset, fixed τ between the slopes (figure 4). A symmetric solution is used for the opposite phase detection. An additional noise improvement is added by using an XNOR gate for combining each slope-phase. By definition both phases may not occur at the same time and must be due to noisy signals.

V. LEVEL SHIFTING AND THRESHOLDING

The level shifter and thresholding scheme (Figure 6) consists of a "slow" tailed pair differential amplifier used as a voltage follower, combined with two inverters and a capacitive feedback. The thresholding level is fixed in the inverters, but by combining the inverter structure with a level shifter it will have the functionality of a adjustable threshold circuit. The tailed pair topology of the level shifter makes up as a high pass filter due to the voltage followers frequency response. This can be adjusted by regulating the tail current, and shows through simulations to have an upper 3dB limit just above 2GHz.

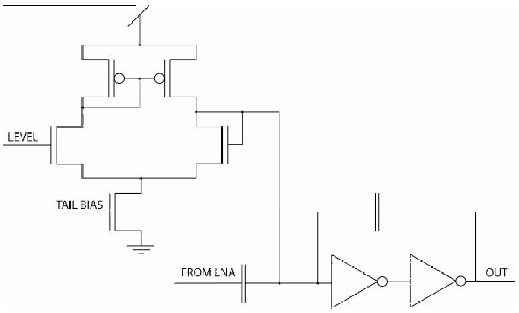

Figure 6: Levelshifting and thresholding circuitry

VI. DELAY LINE & PULSE SHAPING

The duration of the shaped pulse must be matched to the unit-delay of the delay line (τ in Figure 2). A longer pulse may reduce the sampling clock of the delayline. Lower sampling clock will reduce power consumption. Then again longer pulses may mask information carrying reflections for parallel RAKE fingers. A reasonable pulse duration seem to be 1ns [4][5] mostly avoiding masking of multipath components. The duration of the pulse must be short enough not to mask out wanted reflections at the same time as the total length of the time delay line is proportional to the timespan between the first arriving pulse and the last possible reflection.

VII. ISOLATION TECHNIQUES

Due to the high frequency demands, low power supply and the sensitive circuitry in this design, on-chip isolation is important [3]. The analog circuits are all isolated from the digital switching circuits. This is done by using P-wells for circuit separation and isolation. The different circuits and isolated wells have separated power rails and power pads to insure maximum cross-talk isolation. The shielding used is providing isolation from electric fields generated by other circuitry on or off chip, and the on-chip decoupling provides an AC connection to isolated ground. A shield was added in the top metal layer for analog circuits and wires together with decoupling to isolated ground on all analog signals and supplies. The isolated ground from decoupling and shielding are star-coupled into several separated pads for isolated ground, which again is star coupled together close to the power supply rail on the PCB off chip. The separated supplies and ground for the different circuits are all coupled into separated pads. As mentioned earlier the level shifting circuit also adds in as an isolation/noise reduction factor in the design by high pass filtering the signal. As it is the combination of all the different isolation techniques used in a design that determines the final results, we are confident that the combined techniques that were used will provide sufficient isolation and noise reduction.

VIII. IMPLEMENTATION

The front end circuit topology is implemented on the same silicon as the RAKE receiver (Figure 7). The front end radio receiver is located at the upper left corner of the RAKE (large square matrix). The black squares located around the front end are the decoupling capacitors. The total silicon size is 1.8mm x 1.35mm equaling 2.43mm2.

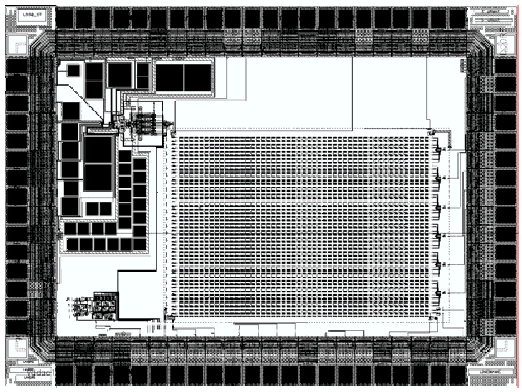

Figure 7: Circuit layout

IX. SIMULATIONS

Simulations of the circuit is divided into simulations of the LNA separate, the complete system with the LNA, level shifters, triggered high speed processing for pulse shape detection and pulse shapers and the level shifter.

The first simulation (Figure 8) shows the AC response of the LNA simulated between 100MHz and 50GHz.

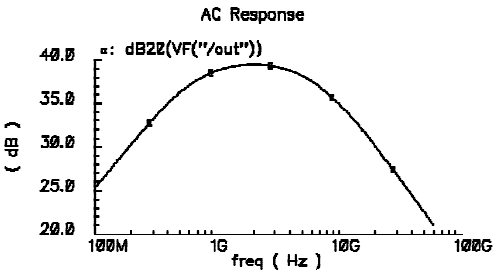

Figure 8: LNA AC response

The simulation shows that the gain stays above 30dB in the area between 3.1- 10.6GHz.

The second simulation (Figure 9) shows the complete circuit starting from the bottom trace. The lowest trace is input signals with complementary phases. The input dual monocycle has a amplitude of only 10mV (modulated in MATLAB). The next trace is the output from the LNA. As the signal is split, the next to traces exhibit the output from the complementary slope detectors each detecting the different slope phases. These signals are then combined by the XNOR gate and finally shaped to a 1ns pulse.

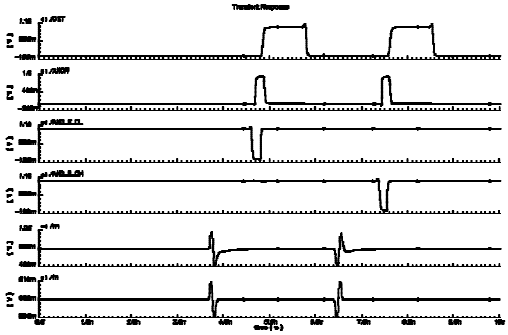

Figure 9: Front end processing simulation results

Power consumption is estimated for the dual monocycles input up to he levelshifter. If we assume three reflections for each pulse and 25 pulses (50%) for each symbol containing 50 bits sampled in the delay line at 20 MHz. The total power consumption adds up to 8.4 µw. Since we assume that 50% of the symbol contains pulses and they all are followed by three reflections each, it adds up to be a fairly conservative estimate.

An AC simulations of the levelshifter is shown in Figure 10 and a DC analysis in Figure 11 to indicate the performance. The AC response (Figure 10) shows that we have a cut-off frequency at 2GHz. The simulation was performed with a tail bias at 90%.

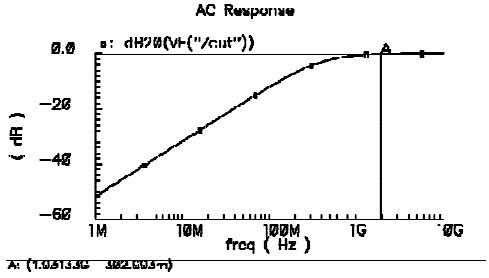

Figure 10: Voltage follower frequency response

The DC response (Figure 11) indicates the linearity of the voltage follower and the different offsets at tail bias voltages from 100-450mV.

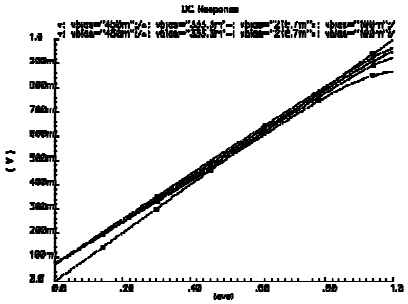

Figure 11: Voltage follower linearity

X. Measurements

The circuit will be tested with input pulses of different phase and amplitude, and with different levels of added noise. We are expecting the chip to arrive shortly, and measurements will start momentarily.

Figures of different measurement results and comments are therefore pending and will be added for the final version.

XI. Conclusions

The ultra wide band impulse radio receiver front end architecture presented in this paper is implemented in a 120nm CMOS process. The front-end is exploring dual-slope impulses and thresholding. The continuous time pure CMOS front-end is a pre-conditioner for a sampled delayline RAKE receiver, making up a novel low-power UWB impulse radio receiver.

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Glossary

Glossary

AGC	Automatic Gain Control
AWGN	Additive White Gaussian Noise
Bi-CMOS	Bipolar Complementary Metal Oxide Silicon
BPSK	Binary Phase Shift Keying
CMOS	Complementary Metal Oxide Silicon
DSP	Digital Signal Processing
EIRP	Effective Isotropically Radiated Power
ESD	Electro Static Discharge
ETSI	European Telecommunications Standards Institute
FCC	Federal Communications Commission
GPS	Global Positioning System
HF	High Frequency
LNA	Low Noise Amplifier
MBOK	M-ary Bi-Orthogonal Keying modulation
MOSFET	Metal Oxide Silicon Field Effect Transistor
MUX	Multiplexer
OFDM	Orthogonally Frequency Division Multiplexing
PAM	Pulse Amplitude Modulation
PAN	Personal Area Network

PBGA	Plastic Ball Grid Array
PCB	Printed Circuit Board
PN	Pseudo Noise
PPM	Pulse Position Modulation
PSD	Power Spectral Density
PSRR	Power Supply Rejection Ratio
RF	Radio Frequency
RMS	Root Mean Square
Si-Ge	Silicon Germanium
SNR	Signal to Noise Ratio
UWB	Ultra Wide Band
UWB-IR	Ultra WideBand Impulse Radio
WLAN	Wireless Local Area Network
WPAN	Wireless Personal Area Network

List of Figures

List of Tables

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