UNIVERSITY OF OSLO
Department of Physics

Novel silicon solar cell fabrication process

Thesis submitted for the degree of master of science in materials, energy and nanotechnology

Per Lindberg

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Abstract

A frame for fabrication of novel Si solar cells at the micro and nanotechnology laboratory (MiNaLab) at the University of Oslo (UiO) has been established. The focus has been on reproducibility and the possibility to modulate the steps in the process. The process incorporates random pyramidization by KOH-etch for increased light absorption, thermally grown dry-oxide for passivation and anti reflective coating and fabrication of both thin and standard emitters. For emitter formation both ion implantation and spin on diffusant (SOD) were tested. Rapid thermal activation was utilized for low diffusion and high activation fraction. Back side contacts were formed by evaporation of aluminium. Front side contacts were photo lithography defined, featuring titanium, palladium and silver stack. A total of nine different front side metalization patterns were made, optimized for three different sheet resistances and three finger widths. The cells have been electrically, structurally and optically characterized.

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Part I

Introduction

The world primary energy demand rose with 200M ton oil equivalents annually from 2005, through 2010. The international Energy Agency (IEA) predicts the world energy demand will continue to rise with almost the same rate for several decades, equaling an increase of 36% from 2008 to 2035 [1]. The increase in energy demands in addition to soaring oil prices is case for concern [2]. The energy situation in conjunction with increasing global temperature sets the stage for renewable energy sources, such as photovoltaic (PV) solar cells. The market share for PV solar energy is by comparison with coal, oil, gas, nuclear and hydro power vanishingly small, but the PV market has grown significantly [3].

The reason for the small market share is because of the relative high costs of PV energy. PV solar energy has not yet reached grid parity, meaning that it is not yet competitive with the general electricity prices on the grid today. With increasing energy prices [2] and decreasing manufacturing costs, convergence is predicted by the IEA by 2020 in many regions [4]. Also stated by IEA, a lot more research will be needed in order to reach the goal of 11% of world electricity production stemming from PV solar power by 2050 which is needed for sustainable development.

The aim of this work is to establish a frame for research on crystalline silicon solar cells at the MiNaLab at the University of Oslo (UiO). Therefore this process must be rigid enough to produce reliable result and versatile enough so that new concepts can be implemented. All the steps needed to produce, characterize and test a solar cell at the MiNaLab has been examined. Versatility and rigidity are coupled entities and are therefore difficult to satisfy simultaniously. Proceeding process steps will direct the following steps in a certain direction and impede the following choices. Regarding the applicability of this work for others, it may be regarded as a tool box analyzing the different steps, high lighting pitfalls and suggesting standardized operation procedures. Several different processing steps, techniques and simulations tools have been investigated and the results are presented below in such a form that they can be useful in other work.

This thesis is divided in three sections plus appendix. The first chapter introduces the basic theory needed for solar cell fabrication and characterization. The second chapter introduces two very useful simulation program, PC1D and Sentaurus TCAD and how they have been used in this work, followed by processing and characterizations details. The third and final chapter presents the results. The results are discussed and conclusions are made.

All sections begins with stating the main references. Any fact specific references are written in the bulk of the text.

0.1 History of the solar cell

This sub section is based on references [5, 6, 7, 8]. PV solar energy has developed from being an effect that could be observed in a lab and thought to be of academic interest only, via toys and calculators, niche applications such as of grid power sources to space industry. Today PV solar energy is on the verge of competing with traditional energy sources and might very well be of major importance as a contributor to the sustainable energy of the society of tomorrow.

In 1839 the French physicist Antoine-César Becquerel observed the photovoltaic effect in a conductive liquid, but it was not until 1883 that the first solar cell was was fabricated. The American inventor Charles Fritts constructed a solar cell based on selenium covered by a thin layer of gold, featuring a conversion efficiency of about 1%. In 1905 Albert Einstein published a paper explaining the photovoltaic effect and introducing the particle-wave duality of light for which he received the Nobel price in 1921. The researcher Calvin Fuller and Gerald Pearson, working at the AT&T Bell lab manufacture the first silicon solar cell. The conversion efficiency was a lot better than previous models and pioneered the modern phosphorus and boron doped silicon solar cell concept. Space industry rescued PV solar energy from obscurity. Vanguard 1 was the fourth man made earth satellite and the very first to be powered by PV solar cells, in addition to batteries. It was launched in 1958. The experiment was a success and space industry became the main driving force of PV industry. The reason for why space industry showed interest in solar cell energy production was based on the fact that PV solar cells showed a very good power to weight ratio. Cost was not an issue. This resulted in that all research was focused on improving conversion efficiency, not on price reduction, which did not necessarily help development of terrestrial PV solar. In the late 1960:s the Linden, New Jersey Exxon lab, Solar Power Corporation started looking in to means of producing cheaper electrical energy. They thought that solar power could be the next power source. Several cost reducing innovation were done and over a course two years, reducing the price of PV solar to a fifth of what is was before (100 $\$/W_p$ to 20 $\$/W_p$). One of the biggest discoveries was that solar grade silicon did not have to be of the same quality as silicon for the integrated circuit industry. Scrap silicon from the electronics industry could be bought by the PV industry contributing to a major cost reduction.

Several inventions followed in the decades to come, such as thin film solar cell, amorphous silicon and hetero structures. With increasing availability and efficiency many different applications came to light, such as solar power aircrafts and cars. The conversion efficiency continued to grow and the price per W_p decreased further. The world record for multi junction solar cell is today held by Solar junction at 43.5 %.

The next big market for PV solar power is grid power production. As soon as grid parity is reached the PV solar energy market will grow explosively.

1 Theory

The theory chapter is divided in two sections. Section 1.1 gives the reader a quick resume of the theory needed to understand the concepts discussed in this thesis. In this section some keywords will be introduced that are used through out this thesis. Section 1.2 discusses how the principles work in the context of a solar cell. The reader is assumed to have some knowledge of solid state physics and semiconductor physics.

1.1 Physical principles

This section starts with presenting the crystallographics of silicon which is fundamental for understanding the physics of both defects, electronic properties such as energy band and band gap formation, among other things. In order to have band gaps one must have energy bands, which is explained as the solution of the Schrödinger equation of many linearly coupled atomic orbitals. A few other fundamental concepts are introduced, such as 'density of states', the 'Fermi Dirac distribution function', insulator, semiconductors and metals. The concept of doping is introduced. By then it is time to see how these concepts together describe how charge carriers distribute in a solid. When it has been motivated how and why charge carriers distribute in a solid, the physics of the pn-junctions can be approached.

The principles behind anti reflective coatings (ARC) are described. In this work the ARC is made by growing an oxide, therefore the fundamental physics behind oxidation is explained. Afterward the fundamentals of implantation and activation is presented followed be a brief discussion of thermal processing.

1.1.1 Crystallographics of C- silicon

This subsection is mainly based on references [9], [10] and [11]. Many of the electronic and mechanical effects of solids are due to the crystallographics of the material. Therefore the crystallography of almost all materials have been thoroughly mapped. Imagine the atoms as spheres of the same size that are packed together in more or less dense configurations. The densest packed layers are differentiated in the following way; Picture one layer of closely packed spheres topped with another layer. The configuration of lowest energy would be if the atoms would lay in the pits were three bottom-layer atoms meet. The thirds layer has then the option between occupying the same lateral spots as the first layer, or choosing the only spot that has so far not been covered. This gives two types of stacking; ABA and ABC. If lines are drawn between the centers of the spheres the ABA stacking would produce a hexagonal arrangement, ABC a cubic one. These arrangements are examples of two of the in total seven Bravais lattices. Some elements repel each other enough to prefer a not so close packed symmetry. For instance if the second layer of atoms are placed directly on top of the first layer a so called simple cubic lattice is formed. The filling factor is the volume that is occupied by the spheres divided by the size of an infinite

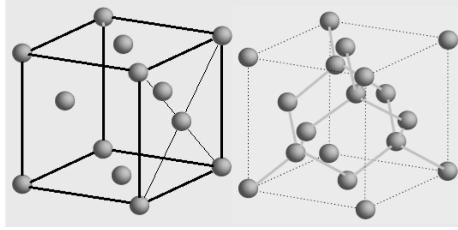


Figure 1: The picture to the left is the fcc lattice structure. If every point is assigned a primitive unit cell with two coordinates at (000) and $(\frac{1}{2},\frac{1}{2},\frac{1}{2})$ one gets the diamond structure, which is the structure of silicon, pictured to the right.

crystal, and obviously the close packed arrangements are denser than all other configurations. For instance the ABC and ABA has a filling factor of 0.740, the simple cubic; 0.524 and the arrangement with one sphere sandwiched between two planes that would have produced a simple cubic, a so called body centered cubic has a fill factor of 0.680.

Silicon has a diamond crystal structure 1, meaning that silicon adopts a face centered cubic Bravais lattice. At each point in the lattice two atoms are placed. These two atoms make up the Basis of the crystal. The coordinates of the basis atoms are 000 and $\frac{1}{4}\frac{1}{4}\frac{1}{4}$. Arranging atoms in crystals gives rise to many artifacts such as energy bands, Bragg reflection of both photons and electrons, in the latter case causing band gaps, which is all topics of the sub section "electrons in solids" 1.1.2.

All variations of the lattice are referred to as defects. The surface of a crystal is seen as a defect since it breaks the regularity of the lattice. In the bulk all bindings were tidily arranged were at the surface there is no obvious way of arranging the bonds, leaving the surface full of disorder. These defects are often electrically active causing recombination at the surface and other detrimental effects [12]. The termination of a crystal does not have to be at the very surface but can also be between crystal grains within the sample, such as in the case of multi crystalline silicon. Another important type of defects in solar cells is point defects, either as interstitial or substitutional defects. For example a by purpose introduced substitutional point defect is phosphorus in silicon. A common but not intended point defect in silicon is Fe, substitutional or interstitial [13].

1.1.2 Electrons in Solids

This sub section is mainly based on references [9] and [14].

Energy bands in solids are extended region of closely packed energy levels. Energy levels that are packed closely enough so that the thermal energy $k_B T$, where k_B is Boltzmann's constant and T is the absolute temperature, easily can excite an electron from one energy level to the neighboring one is called a band.

Later in this text it is motivated why there tends to be gaps between bands, so called band gaps.

Single atoms have clearly defined energy levels, i.e. not bands. When two atoms are brought close together their electron wave functions will start to interact and what was two atoms with separated energy levels at the same value will interact to cause two energy levels, one with higher energy then the other. The solution of the Schrödinger equation (SE) for the combined system will, for a linear combination of two electron wave functions, be two energy levels. When more atoms are added to the system there will be one more solutions/energy level, for every electron. In a solid, that in this case can be assumed to have infinitely many atoms, there will be infinitely many levels closely packed. These closely packed energy levels make up the energy band.

The free electron model is a simplified way of describing how an electron moves in a solid. The free electron model assumes that the electrons do not interact with either the lattice or each other, but propagate freely. In spite of the models simplicity it predicts surprisingly many characteristics of the electron gas accurately, such as electrical and thermal conductivity's, temperature dependency of the heat capacity and the shape of the density of states. Most important in this case is that it gives a frame for explaining energy band gaps in the so called nearly free electron model. When one solves the SE for the case of a free electron the energy dispersion will have a parabolic form with all energy level available.

$$\mathrm{E} = -\frac{\hbar^2 k^2}{2m*} \tag{1}$$

where m* is the effective mass of a free electron, k is the wave number for either one or all crystallographic directions and $\hbar$ is the reduced Planck constant.

Density of states (dos) in the free electron model is the value that describes for instance how many energy states there are per unit energy interval. In the free electron model the restriction of the k values induced by the boundary conditions limits the k-values to $k = 2\pi m/Na$. m is an integer, N is the number of atoms in the crystal and a is the inter atomic distance. The volume one k-value occupies in reciprocal space, assuming a quadratic crystal, is $(\frac{2\pi}{L})^3$, since $Na = L$ where L is the length of the crystal. The density of k-states is

$$\mathrm{dos}(k) = \frac{d(N)}{d(\vec{k})} = \frac{\text{number of k-values}}{\text{unit volume}} = \left(\frac{L}{2\pi}\right)^3 . \tag{2}$$

The density of energy states $dos(E) = \frac{d(N)}{d(E)}$. Solving the dispersion relation 1 for k and differentiating with respect to the energy is

$$\frac{d(k)}{d(E)} = \frac{1}{\hbar}\sqrt{\frac{m}{2E}} . \tag{3}$$

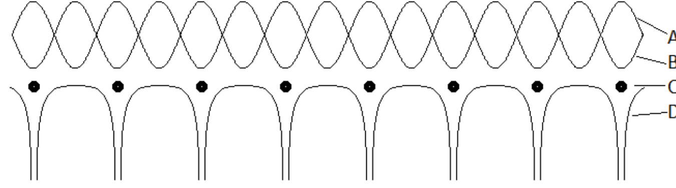


Figure 2: A and B illustrates the probability densities of the two solutions to the one dimensional S.E. perturbed weakly by the ion cores. C indicates the positions of the atom cores and D illustrates the potential landscape.

The derivative of k with respect to E multiplied with the density of of k-states gives the $dos(E)$ for free electrons;

$$\mathrm{dos}(E) = \frac{d(k)}{d(E)}\frac{d(N)}{d(k)} = \left(\frac{L^3 m^{\frac{3}{2}}}{\sqrt{2}\pi^2\hbar^3}\right)\sqrt{E}\,. \tag{4}$$

Notice that the $dos(E)$ is for free electrons is a continuous function that is proportional to the square root of the energy. Real materials have much more complex $dos(E)$ than presented here. This model will be used to give an understanding of how temperature and the Fermi level, a concept introduced below, leads to population and depopulation of the conduction- and valence band.

In the nearly free electron model one assumes that the propagating electron is slightly attracted by the ion cores every time it passes one. At certain k-values that coincide with the periodicity of the lattice the interactions between the electrons and cores will give a solutions to the SE on the form of a superposition of two sinusoidal functions propagating in opposite directions. The solution is therefore a standing wave, and the part of the solution that gathers electron density over the cores will have a lower potential than the solution that gather electron densities in between, and therefore there will be forbidden regions of energy 2. The free electron model fails at describing these forbidden regions.

Fermi Dirac (FD) statistics apply to identical, half integer spin particles such as electrons. The FD-distribution of electrons

$$f(E) = \frac{1}{1 + exp\,\{(E - E_f)/k_B T\}} \tag{5}$$

, describes the probability that a electron state is occupied. In FD-statistics electrons are assumed to occupy the lowest available energy level, filling the energy levels from the bottom and up. The last level to be occupied when adding electrons one by one is the so called Fermi energy level (E_f). E_f also represents the level with the probability 1/2 of being occupied, at any temperature, as long as the E_f lies within a band. If the E_f lies within a Band, only a minute energy

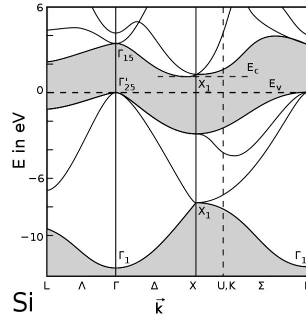


Figure 3: The energy diagram of pure silicon, from [15]. Notice that the smallest energy difference between the conduction band and the valence band is not at the same k-value meaning that a phonon has to be present in the excitation/deexitation of an electron from Ec to Ev, or vice verse. This is one of the reasons that silicon solar cells has to be relatively thick in order to absorb all the incoming light.

is needed to promote an electron to move, i.e. conduct electricity. If the E_f lies in a forbidden region, the E_g, a considerable amount of energy is required to promote an electron from the last filled level to the next available level.

Solids are commonly categorized by their ability to conduct an electrical current. Conductors are materials where the Fermi level lies within an energy band and therefore only an infinitesimal energy is needed to promote an electron in to a higher energy level, and will therefore conduct a current well. In the case of insulators the Fermi level lies withing the so called energy gap (E_g) between the valence band and conduction band. The valence band is the last band that contains electrons, while the conduction band is the first band that does not contain electrons, which is equivalent to the two bands neighboring the E_f, distanced by the E_g. An insurmountable energy is needed to promote electrons from the valence band to the conduction band, and will therefore, under normal circumstances, work as insulator. SiO_2 is an example is an insulator. The $E_g$of SiO_2 is about 9 eV.

If the E_g is small, on the order of one or a few eV, the material is said to be a semiconductor. Since a crystal appears different for electrons traveling in different crystallographic directions it is easy to see that the bands might have tops and bottoms at different k-values. If the top of the conduction band is at a different k-value than the bottom of the valence band the semiconductor is said to be an indirect semiconductor. Silicon is an example of an indirect semiconductor, see figure 3.

If the bottom of the conduction band (E_c) is located at the same k-value as the valence band maximum (E_v) the semiconductor is said to be a direct semiconductor, for instance GaAs. In the case of silicon a lattice vibration is needed in addition to a photon to promote an electron up in to the Conduction

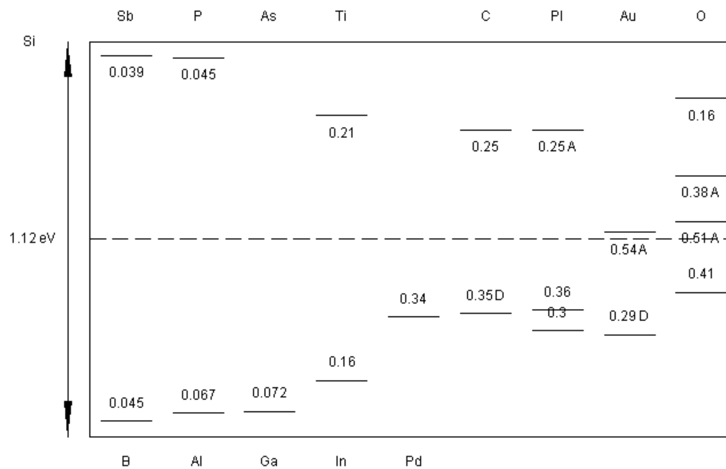


Figure 4: Image showing different energy levels of various impurities[16]. Not only the valence of an element has to be considered when choosing dopant. The energy level of the impurity indicates with which ease an electron is excited from the impurity to the conduction band, such as in the case of n-doping of silicon with phosphorus. Or as in the case of p-doping, when an electron is excited to the empty acceptor state close to the valence band, such as boron.

band. This makes silicon much more transparent for photons than most direct band gap materials, meaning that thicker layers of silicon is needed in order to capture all the incoming light.

Doping of a semiconductor is when a few atoms in the crystal is exchanged with atoms that have more or less electrons in it's valence band than the lattice atoms, such as phosphorus och boron in silicon, for instance. Phosphorus, for instance, has one electron more than silicon, and the energy level of this electron is right below the conduction band of silicon, see figure 4. Therefore only a little energy is needed to excite this extra electron in to the conduction band of silicon. Phosphorus, as an impurity in silicon, is called a donor since it donates an electron. If on the other hand a lattice atom is interchanged with an atom that has one electron less in it's valence band, then an electron could be excited from the valence band of the bulk in to the acceptor level of the impurity. Naturally the acceptor levels should be close to the valence band of the host, such as boron impurities in a silicon lattice. This type of dopant is called an acceptor. A material that is doped with donors are said to be negatively doped, and materials that are doped with acceptors are said to be positively doped, owing to the resulting free charge carriers. The lack of electrons in the valance band in a positively doped material can be thought of as positive charges that move when the electrons move in to take its place. Intuitively one can imagine the lacking piece in a sliding jigsaw puzzle as a positive charge moving along

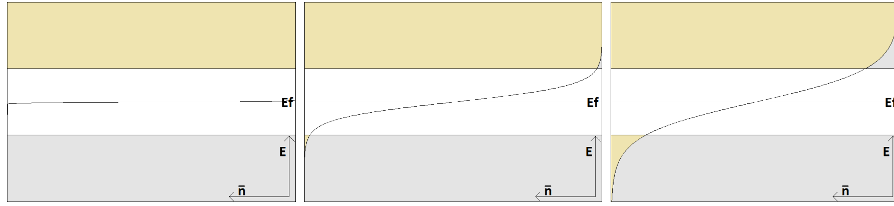


Figure 5: Intrinsic semiconductor. The first picture from the left illustrates the distribution between electrons (gray) and holes (beige) at very low temperatures ($k_BT = 0.01$ eV $\Rightarrow T = 116$ K). (At room temperature $k_BT = 0.0259$ eV) In the second picture it can bee seen that the Fermi-Dirac distribution function has tails stretching in to the valence and conduction band, ($k_BT = 0.25$ eV $\Rightarrow T = 2900$ K). This means that there is a non zero probability of electrons being excited in to the conduction band and holes in the valence band. In the third picture the Fermi-Dirac distribution is further smeared out and there is a large possibility of finding excited charge carriers ($k_BT = 0.5$ eV $\Rightarrow T = 5800$ K). Notice that the E_f is in the middle of the E_g and the increasing temperature increases the number of excited charge carriers at the same time maintaining charge neutrality.

as the other pieces move in to take its place. Negatively doped materials will at room temperature have electrons free to take part in conduction of electrical current, while positively doped materials will have electron holes free to conduct a current.

Intrinsic semiconductors are undoped. Thermal energy excites electrons from E_v to E_c leaving holes behind, meaning that the free charge in an intrinsic semiconductor will remain neutral, see figure**??**.

Distribution of charge carriers in semiconductors is due to all the above mentioned facts. Fermi-Dirac statistics gives the probability distribution. The Fermi level is the balance point between electrons and holes, meaning that an intrinsic material will have E_f in the middle of the band gap. If negatively doped the Fermi level will rise, closing in to E_c. On the other hand if an initially intrinsic material is positively doped E_f will close in to E_v, see figure 5 and 6.

1.1.3 pn-junction

This subsection is mainly based on reference [11]. In the very first part of this subsection a general expression for current will be derived, followed by an intuitive description of the physics of a pn-junction. Band diagrams will be introduced as a convenient tool for illustrating many of the phenomena of a pn-junction. After the intuitive descriptions of the physics behind pn-junctions an expression for the IV-characteristics of a pn-junction will be derived, the

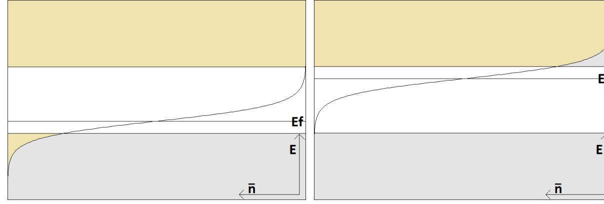


Figure 6: A doped semiconductor, i.e. extrinsic, does not have the same number of holes as electrons, and therefore it's E_f will not be in the middle of the valence band. This has the consequence that the distribution function will stretch further in to either the conduction band or the valence band, when at temperatures above absolute zero. The left picture illustrates a lightly doped p-type semiconductor at $k_b T = 0.25$ eV. The right picture is of a lightly doped n-type semiconductor at the same temperature.

so called diode equation, which is very central for understanding the power response of a solar cell.

So far no notion has been made about how an electric current is carried. It has been implied that is has something to do with both the number of charge carriers, their willingness to move; i.e. their mobility and their charge. The current in x-direction can be carried by both electrons and holes, and the two driving forces are called drift and diffusion. The general expression for drift current density in x direction (J_x) is

$$J_x = q(n\mu_n + p\mu_p)\varepsilon_x \tag{6}$$

where q equals the unit charge, μ_n and μ_p are the mobilities of electrons and holes, respectively, n is the number of excess electrons and p the number of excess holes and ε_x is the electrical field in x-direction. Drift current is the flow of charge carriers due to the electrostatic part of the Lorentz force. A potential difference, and hence an electrical field, will sweep charge carriers towards the pole with lower potential, i.e. electrons towards the plus pole and holes towards the minus pole. The effects of scattering from impurities, grain boundaries, phonons and other imperfections in the lattice are accounted for by the mobility.

The diffusion part of the current is due to the random movement of charge carriers and a concentration gradient. If there is a difference in concentration within a sample a random movement of the particles, or quasi particles such as holes, will even out the concentration difference. A general expression for flux due to diffusion is described by Fick's first law

$$J_x = -D_i \frac{d\phi}{dx} \tag{7}$$

where J_x is the diffusion flux, D the diffusion coefficient and ϕ is the concen-

tration. Combining the hole drift and diffusion currents equals

$$J_p(x) = q\left[\mu_p(x)\varepsilon(x) - D_p\frac{dp(x)}{dx}\right] , \quad (8)$$

where ϕ has been exchanged for p, the hole concentration. D_p is the hole specific diffusion constant. The expression for electron current is the same but with opposite sign.

Picture a n-doped semiconductor put in physical contact with a p-doped semiconductor. Since the p-doped semiconductor has plenty of free holes and the n-doped semiconductors plenty of electrons these will attract and recombine in the contact region. Each hole that recombines with an electron will leave a negatively charged ion core in the p-side, and each electron that recombines at the interface will leave a positively charged ion core. Since the ion cores are fixed to the lattice a charged region will form. Negative on the p-side, and positive on the n-side. This region is referred to as the depletion zone, since it is depleted of mobile charge carriers, see figure 7. The width of the depletion zone is, with bias $W = \left[\frac{2\epsilon(V_0-V)}{q}\left(\frac{N_a+N_d}{N_aN_d}\right)\right]^{1/2}$ were V is the built in voltage difference and V_0 is the applied bias. The electrical field in the depletion zone is what separates electrons from electron holes in a solar cell.

A way of illustrating the electrical field in a solar cell is by drawing band diagrams. Initially, before charge transfer both the p-and n-side have flat band diagrams. The Fermi level is close to the valence band on the p-side and on the n-side it is close to the conduction band, see figure 3. Since the Fermi level, at equilibrium, has to be at the same level through out the system charge carriers will diffuse in order to eliminate the imbalance, just as described in the previous section. At equilibrium the Fermi level will be the same at all spatial locations causing the valence band and conduction band to bend. From such band diagrams it is easy to see that electrons will drift from a high potential p-side to a lower potential n-side. In section 1.2 the band diagram of a pn-junction will extensively be used in order to illustrated how charge carriers are separated and how much energy the process consumes.

The diffusion current, as stated above, is due to a concentration gradient. In steady state the drift current will equal the diffusion current and for instance holes will diffuse down the slope in the same extent as holes are drifted up the potential slope.

$$J_p(x) = q\left[\mu_p p(x)\varepsilon(x) - D_p\frac{dp(x)}{dx}\right] = 0 \quad (9)$$

rearranging gives

$$\frac{\mu_p}{D_p}\varepsilon(x) = \frac{1}{p(x)}\frac{dp(x)}{dx} . \quad (10)$$

The electric field can be written as the derivative of the potential and $\frac{\mu_p}{D_p}$ can be expressed using Einsteins relation, se appendix 55. Integrating this

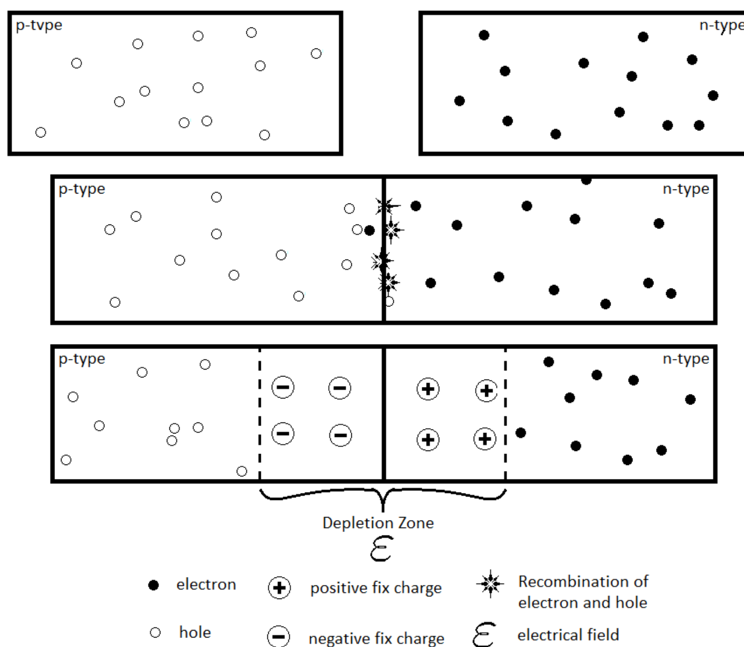


Figure 7: Three consecutive illustrations of how a diode is formed. When the p- and n-doped sides are not in contact free charge carriers diffuse randomly. No ε-field is present. When put in to contact the large charge carrier gradients will diffuse electrons and holes in to neighboring regions. A charge carrier that diffuses over the metallurgical junction will readily recombine with a majority carrier. Fixed charges are left behind after every recombination event; Positive fix charges on the n-side, and negative on the p-side. The sum of these fixed charges add up to form an ε-field that retards further diffusion.

expression from the potential at the p-side to the potential at the n-side, for the left side of equation 10 and from the hole concentration at the p-side to the hole concentration at the n-side one gets;

$$-\frac{q}{k_B T}\int_{v_p}^{v_n} dV = \int_{p_p}^{p_n} \frac{1}{p} dp \tag{11}$$

$$= -\frac{q}{k_B T}(V_n - V_p) = \ln(p_n) - \ln(p_p) = \ln\left\{\frac{p_n}{p_p}\right\} .$$

The difference in potential $(Vn - Vp)$ is called the contact potential, V_0, and is the difference in potential at the p-side and n-side. Later it will be claimed that V_0 is the same as open circuit voltage, the largest possible voltage that the cell can produce.

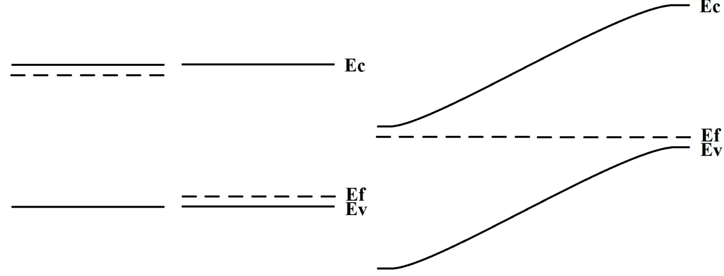


Figure 8: The left picture shows the band diagrams for n- and p-type semiconductor materials before charge transfer. The right picture is after charge transfer, equivalent to short circuit voltage conditions. Notice that the ε-field equals the derivative of the potential with respect to the distance; $\frac{dV}{dd}$. Under short circuit conditions the ε-field separates the charge carriers very effectively, but at the cost of lost potential difference.

$$V_0 = \frac{k_B T}{q} \ln \left\{ \frac{p_p}{p_n} \right\} \tag{12}$$

The contact potential can also be expressed in exponential form

$$\frac{p_p}{p_n} = \exp \left\{ \frac{qV_0}{k_B T} \right\} . \tag{13}$$

With bias this becomes

$$\frac{p(-x_{po})}{p(x_{n0})} = \exp \left\{ \frac{qV_0 - V}{k_B T} \right\} , \tag{14}$$

where $p(-x_{po})$ is the hole concentration at the edge of the space charge region at the p-side, and $p(x_{no})$ is the hole concentration at the edge of the space charge region at the n-side. V is the applied bias. The ratio of equation 13 and equation 14 is

$$\frac{p(x_{n0})}{p_n} = \exp \left\{ \frac{qv}{k_B T} \right\} . \tag{15}$$

Notice that $p(-x_{p0})$ has been exchanged with p_p. At $-x_{p0}$ a small part of the majority carriers will recombine with minority carriers injected in to the p-side, but the amount is small compared to the share number of holes, see figure 9. Therefore the ratio between $p(-x_{p0})$ and p_p said to be one. Also the n-side of the interface minority carriers are injected and will recombine with the large number of electrons. A small distance in to the n-side all access holes will have recombined and the minority carrier concentration will level out at the minority carrier concentration, p_n.

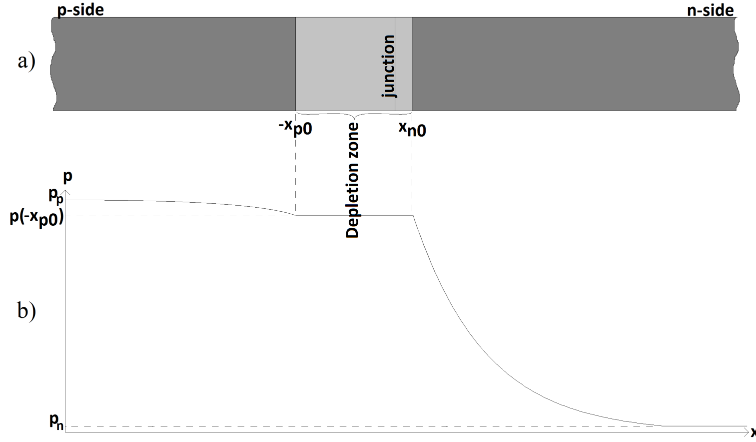


Figure 9: Steady state carrier injection in a long pn-junction. Part a shows the two semiconductors in contact forming a depletion zone. For clarity only the hole concentration is illustrated in part b. Notice that in order to be able to write equation 15 it is assumed that p_p equals $p(-x_{p0})$. In addition it is assumed that there is no recombination in the space charge region.

The injected amount of holes in to the n-side will therefore be

$$\Delta p_n = p(x_{n0}) - p_n = p_n \left(exp\left\{ \frac{qv}{k_B T} \right\} - 1 \right) \tag{16}$$

. The distribution is described by the steady state carrier injection. The steady state carrier injection is given by the continuity equation. See appendix 7.3. The flux of particles is driven by diffusion. The solution to the differential equation describes the hole concentration as a function of x.

$$\delta p(x) = \Delta p_n exp\left\{ \frac{-x_n}{L_p} \right\} = p_n \left(exp\left\{ \frac{qV}{k_B T} \right\} - 1 \right) exp\left\{ \frac{-x}{L_p} \right\} \tag{17}$$

The diffusion part of the general expression for electrical current, equation 8, with $p = \delta p$ describes the current. Evaluating the current at $x = x_{n0}$ gives

$$Ip(x = x_{n0}) = \frac{qAD_p}{L_p} p_n \Delta p_n = \frac{qAD_p}{L_p} p_n (\exp\left\{ \frac{qV}{k_B T} \right\} - 1) \tag{18}$$

A similar analysis can be done for the electron current injected in to the p-side. In the Schockley ideal diode model it is assumed that no recombination takes place in the space charge region, as is drawn in figure 9. The sum of both electron and hole current is

$$I = qA \left(\frac{D_p}{L_p} p_n + \frac{D_n}{L_n} n_p \right) \left(\exp\left\{ \frac{qV}{k_B T} \right\} - 1 \right) = I_0 \left(\exp\left\{ \frac{qV}{k_B T} \right\} - 1 \right) \tag{19}$$

which is known as the diode equation. The diode equation is essential for understanding how a solar cell works. The relevance of the diode equation will be accounted for in section 1.2.

A diode under illumination will produce a shifted IV-curve, see figure 10. At short circuit a certain current, hereafter referred to as the short circuit current, is the largest current a solar cell can produce. The IV-response of a solar cell is the super position of the short circuit current and the diode characteristics.

$$I_{PV} = I_{sc} - I_{diode} \tag{20}$$

. This approximation is called the superposition approximation. Regarding the diode plot only, one can see that at negative biases ideally no current will flow, and for a diode with good rectifying abilities the set on point will be abrupt and at a certain positive value, determined by the materiel used for the diode, the doping of base and emitter, the diode ideality factor and the potential loss at the contacts. Carefully engineering of the diode regarding these premisses the diode can be used as a power generating device when illuminated. At forward bias a potential difference at the contacts will force a current through the leads, and if the bias is small enough to let the current run in positive direction; Power is produced by the diode when illuminated. If the diode is run at a potential larger than open circuit potential (V_{oc}) the current will be traversing the diode in opposite direction, consuming power. The fed in current will recombine and at certain premisses can be used as a light emitting diode. In the case of a solar cell most of the power will be lost to heating, which could potentially destroy the cell. At reverse bias, in the ideal case no current will flow. If a photon excites a charge carrier it will effectively be captured by the E-field and a spike in the current can be detected. Such a device is called a photo detector.

The depletion zone is a central concept in solar cell design. In figure 7 it can be seen how the process of neutralization of free carriers creates a zone without mobile charges. Electrons and holes are attracted by the charge of the other, meet and recombine. For each electron that leaves the n-doped side a positively charged fix ion is left. The same goes for holes on the p-side. Each hole leaves a lattice ion core, but this time negatively charged. The build up of fix charges makes up an electrical field across the junction. It is this field that eventually stops further annihilation of charge carriers. In other words, the Fermi levels align when to semiconductors are brought in contact.

The ε-field is the derivative of the potential

$$\varepsilon(x) = \frac{dV(x)}{dx} \tag{21}$$

which gives the potential as

$$-V_0 = \int_{-xpo}^{xn0} \varepsilon(x)dx \ . \tag{22}$$

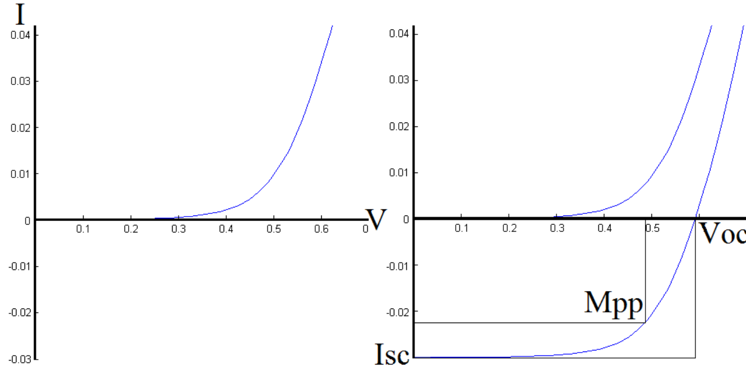


Figure 10: IV characteristics of a solar cell in dark ambient and illuminated. The plot to the left is what can be seen from any rectifying diode, what makes a diode in to a solar cell is its capability to capture light and shift the IV-curve, so that at positive biases can produce power, such as in the middle lower plot. At zero current the cell delivers largest voltage, the so called open circuit voltage (V_{oc}). At no potential the largest current will flow, the so called short circuit voltage (I_{sc}). The power, being the product of potential and current, peaks at the so called maximum power point (Mpp). The fill factor (ff) is a measure of merit for solar cell and is the quotient of $\frac{M_{pp}}{V_{oc}I_{sc}} = ff$. The plot to the right shows how a solar cell is expected to respond to light. The IV-curve is shifted towards a larger (drift) current, undistorted.

The ε-field is assumed to be linearly varying, and therefore the integral can be calculated as the area of a triangle

$$V_0 = -\frac{1}{2}\varepsilon_0 W \,, \tag{23}$$

where W is the width of the depletion zone and ε_0 is the maximum value of the ε-field. ε_0 can be calculated from the width of the depleted region and minority carrier density, on either side of the junction.

$$\varepsilon_0 = -\frac{q}{\epsilon}N_d X_{n0} = -\frac{q}{\epsilon}N_a x_{p0} \,. \tag{24}$$

Replacing for ε_0 in equation 22 gives

$$\frac{1}{2}\frac{q}{\epsilon}\frac{N_a N_d}{N_a + N_d}W^2 \,, \tag{25}$$

were X_{n0} has been replaced for $\frac{WNa}{Na+Nd}$ in equation 24, which solved for W is the expression for the width of the depletion zone.

The depletion zone is what separates holes from electrons in a solar cell.

In metal-semiconductor interfaces, such as when contacting a solar cell a depletion zone might form. The width of which will be governed by the doping level of the semiconductor and therefore altering the conductivity over the junction. A further discussion will follow in the metalization section 1.2.5.

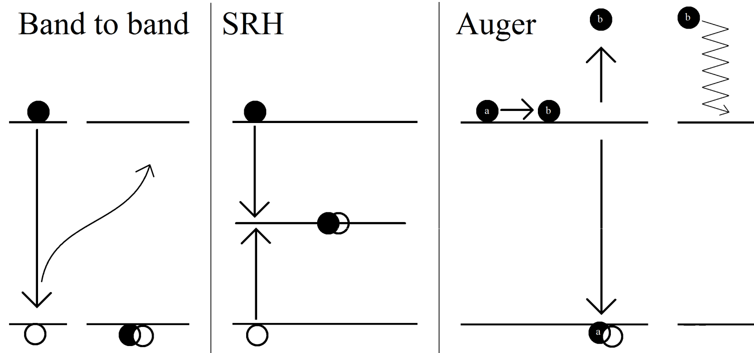


Figure 11: Figure illustrating three recombination mechanisms. Band to band, also referred to as radiative recombination, Schockley Reed Hall and Auger recombination. The filled dots represents electrons. Empty circles represents holes. A dot partially covering a circle illustrates a recombination event.

Recombination of charge carriers has so far only been mentioned briefly. The recombination processes are divided in three groups; Band to band, Auger and Schockley Read Hall recombination, see figure 11. Band to band is a radiative process were an excited charge carrier recombines with a hole. This is a process that can not be avoided by careful engineering, but will happen at high concentrations of charge carriers. Auger is another example of an unavoidable recombination process. A charge carrier interacts with another charge carrier exciting one of them while the other recombines over the band gap. The excited charge carrier will loose it's extra energy by inelastic scattering events, leading to heating of the sample. Schockley Read Hall effect is also referred to as trap-effect. Spatially localized defects can act as traps for electrons and holes. If a hole and electron are both captured by the trap they will recombine, leaving the trap emptied so that it can capture another charge carrier pair. If the energy level of the trap is close to the edges of the band gap there is a higher possibility of the charge carrier being thermally excited out of the trap again, not recombining. The thermal energy at room temperature is small compared to the band gap (0.0259 eV). This means that a defect with an energy level deeper in the band gap will act as a more efficient life time killer since the thermal energy available to free a trapped charge carrier is to small. Such defects are called deep level defects. Examples of such are Au, silver and Fe in silicon.

1.1.4 Anti reflective coating (ARC)

This section is mostly based on references [17] and [12]. The sun-power radiating earth varies with location, time and atmospheric conditions. Therefore a standard test condition has been agreed upon called the air mass 1.5 which resembles the solar spectrum after attenuated by one and a half atmosphere, resembling an incident angle of 48.2°. The spectrum is abbreviated a.m. 1.5. A

polished wafer will reflect about 34% of the the energy of the a.m. 1.5 spectrum. As-cut is a little better: 25-30% [18], but still a lot of the energy is lost. One of the measures taken to increase the absorption of light is by covering the front side of the solar cell with an anti reflective coating. The refractive index and thickness is scaled to minimize reflection, i.e. maximize absorption.

Fresnel's equations state that the reflection of an incident electromagnetic beam will depend on the angle of incidence, the polarization of the light and the refractive index. The refractive index is the relation between the velocity of the light in vacuum over the speed of light in the material of interest; $n = \frac{V_0}{V_i}$. For unpolarized light at normal incidence the amplitude of the reflected light becomes

$$r = \left(\frac{n_1 - n_2}{n_1 + n_2}\right)^2 . \tag{26}$$

This means that the optimal one layer ARC should have a refractive index of the geometric mean of the air and solar cell;

$$n_1 = \sqrt{n_0 n_2} . \tag{27}$$

With $n_2 = n_{Si} = 4$ and $n_0 = n_{air} = 1$, the optimal refractive index of the ARC should be 2.2 over the entire spectrum.

The refractive index of a material varies slightly with wavelength. For example, SiO_2 has a higher refractive index for shorter wavelengths.

Bragg's law governs the interference between the incident and reflected light. Rewritten for anti reflective coatings Bragg's law becomes:

$$m\lambda = 4d\cos(\theta) \tag{28}$$

. m is an integer, λ the wave length, d is the thickness of the ARC and θ the angle of incidence. As stated by Fresnel's equations the highest absorption is for an angle of incidence normal to the plane, i.e. $\theta = 0$. Therefore the thickness of the ARC should be $d = \frac{\lambda}{4}$. Obviously the optimal thickness depends on the wavelength, and therefore has to be optimized for maximal energy absorption with respect to the a.m. 1.5 spectrum.

1.1.5 Oxidation

The main reference for this subsection is [19]. Thermally grown oxide has been used in this work both as an anti reflective coating, optimized for absorption of the a.m. 1.5 spectrum, and for decreasing the number of surface trap states, i.e. a surface passivating layer. This subsection deals with the mechanisms of oxide growth, motivating why SiO_2 has become such a central material in semiconductor industry. Fick's first law will be used when deriving an expression for oxide growth rate, the Deal-Grove model. At the end of this subsection a short paragraph discusses what factors there are that drive the oxide growth.

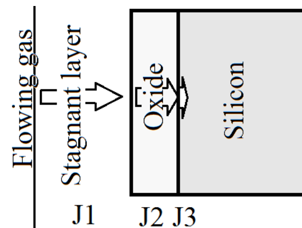
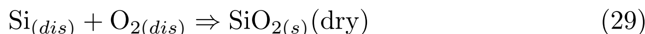
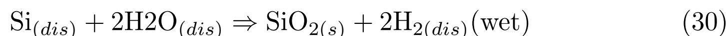


Figure 12: Illustration of fluxes of O_2 or H_2O through stagnant layer of ambient gas, SiO_2 and in to the interface between SiO_2 and silicon.

One of the reasons for the great success of silicon in the semiconductor industry is its ability to form high quality insulation (dielectric constant: 3.9), passivating oxide.



$$Si_{(dis)} + O_{2(dis)} \Rightarrow SiO_{2(s)}(\text{dry}) \tag{29}$$



$$Si_{(dis)} + 2H2O_{(dis)} \Rightarrow SiO_{2(s)} + 2H_{2(dis)}(\text{wet}) \tag{30}$$

A thermally grown oxide will not grow any further when exposed to room temperature and O_2 pressure. The oxide is resistant to dielectric breakdown ($> 10^7$ V/cm) [20, 21], and can therefore be used as a thin insulator in a field effect transistor. It is relatively easy to grow an oxide fairly free from impurities due to the nature of the formation of the oxide, which will be discussed below. SiO_2 has a high band gap (9 eV) and a small absorption coefficient.

In this work thermally grown SiO_2 was used as an ARC and passivating layer. The refractive index of SiO_2 (1.46) is not optimal for this purpose, see section 1.1.4, but the other aspects made it the material of choice.

SiO_2 can either be grown in oxygen environment or in water vapor i.e. dry and wet oxidation. Dry oxide is of a denser quality, with higher refractive index (1.46) and dielectric constant, while wet oxide grows faster. Wet oxides are primarily used as field oxides, where a thick, well passivating, highly non conducting film is needed. The reason for the good passivating effect is addressed to the hydrogen remnants after oxidizing. A native oxide forms quickly on any bare silicon surface at room temperature and in O_2 atmosphere, but does not grow thicker than one or a few nm [22]. For further oxidation either silicon has to dissolve and diffuse through the oxide to reach the surface and there react with O_2, or O_2 ($/H_2O_{(g)}$) has do diffuse to the surface of the silicon, to react. Comparing the diffusivity of silicon in SiO_2 and O_2 one sees that O_2 will much more likely diffuse through the oxide to the surface of the wafer, and not vice verse. This means that the oxide grown will never have been exposed to the atmosphere, always shielded from impurities.

The growth rate can be calculated using the Deal-Grove model. The Deal-Grove model divides the surface area in to three regions, see figure 12. The unreacted silicon at the bottom, an Oxide layer in the middle and a layer of gas at the surface. The oxygen is feed to the surface be a gas-flow over the wafer. Closing in to the wafer the flow will slow down and in the very vicinity of the

surface the flow will have stopped entirely. This is called a stagnant layer, and is a phenomenon found in any fluid flowing over a surface. The rate at which O_2 diffuses through the stagnant layer to the surface is described by Fick's first law

$$J_1 = D_{O_2} \frac{C_g - C_s}{t_{sl}}, \tag{31}$$

where C_g is the oxygen concentration in the gas, C_s concentration at the surface, t_{sl} the thickness of the stagnant layer and D_{O_2} the diffusion constant of $\mathrm{O_2}$ in the stagnant layer. Using the ideal gas law the concentration in the gas can be calculated from the partial pressure, and from there the flux can be calculated. Even though this approach works, it tends to underestimate the flux, J_1, therefore the flux is usually postulated directly by

$$J_1 = J_{gas} = h_g(C_g - C_s) \,, \tag{32}$$

where h_g is the mass transport coefficient.

The second flux is the transport of oxygen through the oxide layer. The driving forces is the gradient between the concentration of oxygen in the layer at the very surface; C_o, and the concentration at the interface between oxide and silicon; C_i.

$$J_2 = D_{O_2} \frac{C_O - C_i}{t_{ox}} \,, \tag{33}$$

where t_{ox} is the thickness of the oxide and D_{O_2} in this case the diffusion constant of oxygen in the oxide.

The third flux is the consumption of oxygen at the surface in the reaction of Oxygen and silicon. Since silicon is in abundance the limiting factor is the concentration of oxygen; C_i.

$$J_3 = k_s C_i \tag{34}$$

, where k_s is the chemical rate constant. In equilibrium the three fluxes must equal;

$$J_1 = J_2 = J_3 \tag{35}$$

. Equating J1 (equ.32), J2 (equ.33) and J3 (equ.34) leaves us with one equation short of solving for the three concentrations C_s, C_o and C_i. Henrys law states that the concentration of an absorbed species is proportional to the partial pressure of the element at the surface.

$$Co = Hp_g = HkTC_s \,, \tag{36}$$

where H is Henry's constant and $p_g$is the partial pressure in the gas. The ideal gas law is used to express the partial pressure, and gives the third relation to uniformly describe the three concentrations. The concentration at the interface is

$$C_i = \frac{Hp_g}{1 + \frac{k_s}{h} + \frac{k_s t_{ox}}{D}} \,. \tag{37}$$

The growth rate is the the flux at the interface divided by the number of Oxygen atoms per unit volume of the SiO_2 molecule; N1. For a given flux, the growth rate is determined by the number of oxygen atoms needed for one unit volume oxide. A lower concentration oxygen per unit volume oxide would give a higher growth rate, and vice verse.

$$R = \frac{J}{N1} = \frac{Hk_s p_g}{N1 \left[1 + \frac{k_s}{h} + \frac{k_s t_{ox}}{D}\right]} \tag{38}$$

The solution for this second degree differential equation can be written as

$$t_{ox}^2 + At_{ox} = B(t + \tau) , \tag{39}$$

where $A = 2D\left(\frac{1}{k_s} + \frac{1}{h}\right)$, $B = \frac{2DHp_g}{N1}$ and $\tau = \frac{t_0^2 + At_o}{B}$ and t_0 is the initial thickness of the oxide. The parameters A and B make up the linear and parabolic rate coefficients. For a thin oxide the square of the thickness, t_{ox}, is neglect able, hence the solution is

$$t_{ox} = \frac{B}{A}(t + \tau) . \tag{40}$$

On the other hand, if the oxide is thick enough the linear part is negligible and the solution becomes

$$t_{ox}^2 = B(t + \tau) . \tag{41}$$

The oxidation rate is obviously driven by several factors. The activation energy for diffusing of the oxidizing agent in the oxide is one. The activation energy of both water and oxygen in fused silica agrees reasonably well with the activation energy of B. The concentration at the surface is the solid solubility of oxidizing agent in SiO_2. Water is far more solvable then oxygen in SiO_2 hence a larger concentration gradient and a faster growth rate. For thin oxides the reaction limiting step is the dissolution of solid silicon and not the diffusivity of O_2

1.1.6 Implantation

This section is based on [19]. A common method of doping a surface layer is by ion implantation. Ion implantation is both reproducible and versatile, which makes the method interesting for investigating novel concepts.

Ions are accelerated towards the sample using high voltage and collide with the sample target atoms. The penetration depth is dependent on the energy of the accelerated ion, among other things. The ions charge the sample, hence a current equalizing the charge, will flow between the sample and ground. This current is integrated over time and knowing the ions charge state and the implanted area the total dose is deduced. The dose can therefore be chosen with great accuracy. Altering the energy the implant depth can also be tuned. The impinging ions have a tendency to cause emission of electrons from the sample, which would distort the determination of the implanted dose. This effect is suppressed by keeping the sample under a certain potential, hence increasing the energy needed to expel electrons from the sample.

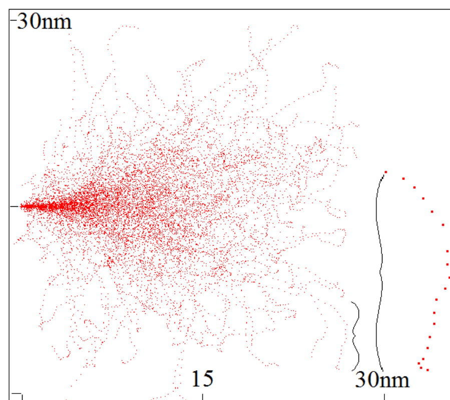


Figure 13: SRIM simulation of phosphorus implanted in silicon. The implant energy was 4 keV. Each implanted ion will feel both electron drag and ionic stopping. The electronic drag retards the speed of the ion, while target atoms can also cause the incident ion to change path. Both effects can be seen above. The distance between consecutive spots indicates the velocity of the ion. Notice that the speed slows down without the ion changing direction, evidently due to electronic stopping. The end of one of the trajectory are enlarged to visualize the stopping effects mentioned above.

The implanted ions moving through the sample will scatter off from lattice atoms and penetrate electron-clouds, see figure 13. The kinetic energy will be given off as heat and disorder to the lattice. An incoming ion will scatter against a great number of electrons. The weight of the electron is several orders of magnitude smaller than the incoming ion and therefore each scattering event will not redirect the path of the ion significantly. Considering this fact and that most of a material is filled with electron clouds, the scattering resembles a viscous flow more than individual scattering events. A particle traveling through a fluid experiences a drag in the opposite direction of the movement. The drag is proportional to the velocity hence proportional to the square root of the energy; $F_D \propto v \propto \sqrt{E}$. This drag is referred to as electronic stopping. Higher implant energies yield stronger electronic stopping.

The scatting events of a single ion can not be seen as a continuous flow. The number of interactions is not that great, and regarding the weight and charge of the ion, each event could deflect the incident ion by a great amount. If the incoming ion has energy enough to knock out a lattice atom, part of the energy will have been transferred. On the other side, if the incoming ion does not have enough energy to knock a target atom out of its position almost no energy will be lost in the collision. The faster the ion is traveling the shorter time the Coulombic interaction will take place, hence lesser energy transferred. Considering these two opposing effects there will be maximum energy transfer at a certain implant energy. All implanted ions will have an individual path

and stopping depth. Calculating the predicted range is done via Monte Carlo simulations, which gives a distribution profile, see figure 23. The shape of this distribution curve is of great interest in semiconductor engineering. The width, concentration and sharpness will have impact on solar cell performance, hence both the 'as implanted' and post annealed profiles will be analyzed by SIMS (see section 4.6), simulated in SRIM (see section 3.2), process simulated in Sentaurus TCAD (see section 5.4) and operation simulated in PC1D (see section 2.2).

The straggling increases with higher implant energies, which must be considered when implanting through a thermal oxide. An ion traveling further through a solid will have more optional paths, and therefore resulting in an wider distribution.

The skewness is a measure of how much back scattering an implanted profile displays, see figure23. A negative value means that the profile has a center of gravity closer to the surface. This is usually an effect of the weight of the implanted ion in comparison to the lattice atoms. A lighter implanted ion will experience a great deal of back scattering, such as boron implanted in silicon. Skewness is enhanced at high implant energy.

The kurtosis of the profile is a measure of how likely extreme values are. A normal Gaussian has a kurtosis of three. Larger values means that it is likely to get extreme values, in this setting that means a larger distribution of ions far from the predicted range.

In most cases an undesirable effect, called channeling, is when the implanted ions are funneled by the hollow channels in certain crystallographic directions, as for instance the [011] direction in silicon. By tilting the sample a few degrees this can be minimized.

1.1.7 Thermal processing

This subsection is based on references [19, 23, 24, 11]. The basics of activation and diffusion of dopants are very briefly introduced. The mechanism of phosphorus diffusion is described, motivating why different diffusion mechanisms have different activations energies. The concepts of activation energy will be used in order to explain why phosphorus diffuses faster with higher temperatures. The diffused profile will be discussed in context of activation degree and P-gettering, laying out the arguments for rapid thermal processing (RTP) versus standard thermal processing (STP). The differences of activating implanted dopants and driving in a spin on diffusant (SOD) will be discussed.

The lattice of a sample that has been doped by ion implantation will be distorted to a large degree, as mentioned in the previous section 1.1.6.

The aim when activating a sample is to substitute lattice atoms with implanted ions. Recrystallization of a a sample that has been made amorphous will cause the impurity atoms to be incorporated in the lattice on substitutional places, hence activating the dopants. Recrystallization is done by thermal processing. The undamaged underlying layers will work as a template for solid phase epitaxy recrystallization.

Point defects have a high formation energy in a crystal, and will therefore

tend to cluster in order to decrease the energy. At lower annealing temperatures the activation energy of many point defects are overcome and they can gather in clusters. At higher temperatures, above 900 °C, extended defects are annealed out. It can therefore be beneficial for the life time of minority charge carriers to anneal at moderate temperatures over a longer time, but evidently this might also lead to further detrimental diffusion of dopants.

Samples were also doped using a SOD. SOD is a, for instance phosphorus containing liquid that is either spun on to a wafer or spay coated on a wafer followed by hot plate prebake and annealing. The dopant has to be diffused in to the sample, and reside predominately in substitutional places. The driving force is the mixing of materials. Regions with high concentration phosphorus will diffuse in to region of lower phosphorus concentrations, reducing the gradient.

The mechanism of P-diffusion is a widely researched field. The general conception is that phosphorus diffuses mostly by interaction with lattice vacancies and/or self interstitial i.e. mobile impurity pairs. The reason for phosphorus diffusing mainly by impurity-pair exchange can be visualized in the following manner: For any form of diffusion some energy is needed to overcome the barriers surrounding the potential well experienced by the phosphorus atoms. In order to diffuse to a neighboring lattice site a total of six bonds have to be broken if the neighboring lattice site is occupied. If the phosphorus atom is neighbored by a vacancy only three bindings need to be broken, which motivates why vacancies are a major contributor to the overall diffusivity of phosphorus in silicon.

Lattice atoms will be vibrating at a frequency dependent on the temperature. The exchange of a substitutional phosphorus with a vacancy can be described by a hopping probability. The rate such interchanges occurs will be related to the vibrational frequency, and therefore the temperature. At higher temperature the trial rate will be higher and therefore the diffusivity will increase.

The aim in this work has been to produce a P-profile in shape as square as possible, so that the pn-junction is abrupt. At low temperatures long diffusion times will be needed to achieve a high enough dose. The consequence will be a wider phosphorus profile, later referred to as the emitter of a solar cell, see section 1.2.4. At high temperatures a high dose can be driven in to the sample at a short time, not allowing the profile to diffuse as far. For fabrication of narrow P-profiles temperatures higher than that of conventional thermal processes (CTP) are utilized. High power tungsten-halogen lamps are often used, in opposition to IR heating of STP.

The most common way of emitter formation used by industry today is a drive-in process utilizing a gas phase phosphor precursor ($POCl_{3(g)}$). The gas is condensed on the surface and driven in by CTP [24]. The CTP is usually a belt oven, radiating mostly in the IR-regime. The wafer temperature tends towards the inside temperature of the oven. The process cycle is long, compared to RTP.

Heat treatment at a lower temperature could getter the impurities and therefore increase the lifetime of minority charge carriers. On the other hand, a longer diffusion time would result in a wider emitter. Both RTP and CTP were investigated in this thesis work.

On lab scale RTP offers a fast and versatile method for testing a range of different parameters.

1.1.8 KOH etching of silicon

This subsection is based essentially on references [25, 26, 27]. In order to increase light absorption the surface was textured using a KOH-solution. The reason for choosing KOH was the potential for a very good light absorption. For good reproducible result using KOH-etch the process has to be handed carefully[28].

It is well known that a high concentration of KOH will etch silicon isotropically and that a lower concentration will give a more anisotropic etch. A lower concentration KOH will attack the lesser dense (100), and (110) planes faster, revealing the (111)-planes. This will, due to the crystallinity of silicon, result in pyramids in a (100)-cut mono-silicon wafer, with (111)-surfaces. A well textured wafer should be fully covered with small pyramids. The difference in etching nature of low and high concentration solutions is probably due to the different rate limiting factors. At high concentration of KOH the rate limiting factor is probably the supply of silicon, and therefore all planes etch equally fast. At lower concentrations there will be enough silicon while the KOH is limiting the reaction, and therefore only the fastest reacting planes will etch.

The etching process is commonly described as dissolving of silicon via

$$Si + 2OH^- + 2H_2O \Rightarrow Si(OH_4)^- + H_2 \quad (42)$$

The process can be described as a two step reaction. First the hydroxides from the KOH-solution bind to the dangling bonds of the silicon at the surface. Secondly an electron transfer from the silicon in to the conduction band takes place followed by addition of further OH-groups. The first step has a low activation energy (0.35eV) and takes place rapidly. The breaking of silicon-silicon bonds determines the rate of the second step which is influenced by the rest of the nature of the other bonds to the atom [29].

isopropanol (IPA) was added to the etchant as a wetting agent. The main purpose of IPA is thought to be reducing the surface tension [30]. It has been claimed that IPA is used for controlling the rate [31]. Without IPA, H_2 bubbles would form and stick to the surface of the sample, partially masking it, which would give a mottled result. It has been claimed that IPA as an additive gives nucleating sites for the reactants to attack, and that a higher concentration of IPA gives more such reactions spots and smaller pyramids, and therefore higher absorption.

1.2 Solar cell theory

This section is essentially based on references [24, 32, 12, 33, 23, 34, 35]. The aim is to string together the physical principles from the preceding chapter, showing how they work in the context of a solar cell. Challenges that might be encountered during solar cell fabrication will be highlighted.

1.2.1 Outline

Incident light will have to make two transitions in order to enter the active region of the cell. One at the very surface when entering the ARC, and one when leaving the ARC and entering the cell. Following Fresnel's equations, see equation 1.1.4 a small part of the incident light will be reflected from the surface of the ARC. The reflected part is lost, but the transmitted light might enter the cell. When the transmitted beam hits the top of the cell another reflection/transmission event occurs. The reflected beam will travel back through the ARC and add to the initially reflected beam. The adding of a wave to another wave is called the super position of two waves, and the effect of super positioning two waves is governed by Bragg's law, see part 1.1.4. If the sum of the waves is a positive value the reflection in enhanced. In a solar cell the ARC is designed to produce an extinction. Obviously each and every wave will reflect many times back and fourth within the ARC making the super position a complex function. The result is easy to interpret, though. For monochromatic light, the ARC must be one quarter of the of the wave length thick. For terrestrial utilization the A.M. 1.5 is used as the template values of the abundance of the different wave lengths. In addition the energy of the different frequencies ($h\nu$) must be accounted for when designing an ARC.

Entering the cell the light will interact with either the lattice atoms or the electrons of the material. If the photons interact directly with the lattice, vibrations are forced, heating the cell. Heat is detrimental for solar cell performance, as can be seen in the diode equation 19. Photons can interact with either free or bound charge carriers. If the energy of the incoming phonon is big enough an electron might get exited from the valence band in to the conduction band contributing to the photocurrent.

The incoming light might also interact with free charge carrier, such as electrons or holes, exciting them further in to the conduction/valence band causing hot carriers. The transparency of a semiconductor is therefore dependent on the abundance of free charge carriers, i.e. band gap, doping level and temperature. Today there is no industrially feasible way of utilizing the energy of hot charge carriers, therefore all the extra energy over the band gap will be lost to lattice heating. The band gap of silicon (1.11 eV) equals a wave length of 1100 nm. For wave lengths shorter than 1100 nm only 1.11 eV at the most, can be utilized. The spectrum above 1100 nm does not posses enough energy for band to band excitations, and is therefore lost to heating or simply the photons penetrate through the cell.

1.2.2 Absorption coefficient

Quantitatively the absorption is described by Beer's law

$$I(z) = I(0)\exp\{-i\alpha z\} \ , \tag{43}$$

where I is the intensity as a function of depth; z. α is the absorption coefficient, which is a function of wave length and ideally should be written $\alpha(\lambda)$. As indicated above, both the temperature and the excitation level are also factors that alter the absorption coefficient. The intensity of a ray of light is a exponentially decaying function, meaning that most of the energy will be absorbed in the area closest to the surface of the solar cell. Some of the low energy light will penetrate through the cell, and must therefore be reflected back in to the cell, diverged at the surface to promote an effectively thicker cell, or construct the cell out of thick enough silicon layers. Since silicon is an indirect semiconductor the absorption coefficient is smaller than for direct semiconductors, and therefore requires an optically thicker cell.

1.2.3 Separating mechanism

An electron in the conduction band is free to diffuse in any direction, likewise a hole in the valence band. If there would not have been any mechanism separating them they would diffuse around until they recombine. The separating mechanism is the band bending at the pn-junction. The electrical field is the derivative of the voltage potential with respect to the distance, and since the potential for an electron is high at the p-side and low at the n-side there will be a gradient forcing electrons to the n-side. The potential of a hole is the opposite of the electrons. Therefore a hole will be forced towards the p-side, the back of the solar cell.

1.2.4 Emitter design

The emitter of a solar cell is the highly doped thin top layer. The thickness and doping level of the emitter has a direct effect on the conversion efficiency of the solar cell, see subsection 2.2. Several factor need to be considered when designing the emitter. The main factors effecting the design will be discussed in this subsection

Silicon is a indirect band gap material and up to several hundred µm in thickness might be needed to get full utilization of the sunlight. Charge carriers might recombine when randomly diffusing in the bulk of the cell. That's why the space charge region should envelope as much as possible of the cell. Say that the cell was designed with a lightly doped emitter, just as wide as the base. Then only a small part of the center of the cell would be covered by the space charge region. With table values for all parameters, zero bias and referring to equation 25 the width of the space charge region would for a sample with $p = n = 5e16\,cm^{-3}$ be 0.2 µm, a mere fraction of the width of the cell mentioned above. The first drawback with this design is the high contact resistance at the front due to the lightly doped emitter. In order to gain a good Ohmic contact the emitter has to be highly doped, see subsection 1.2.5. Secondly, charge carriers being far from the space charge region would not necessarily find their way to the contacts, which especially goes for the region closest to the front side of the cell were all the high energy light is absorbed. Electrons have a longer diffusion

length than holes. The minority charge carrier in p-type material is obviously electrons. Therefore less current would be lost to recombination if most of the cell was made of p-type material. The emitter is hence made thin and highly doped. Obviously the emitter resistance will be a function of not only the doping concentration, but also the thickness of the emitter. A thinner emitter would inevitable lead to more resistive losses. The lateral distance an electron will have to drift in the emitter in order to get to the contacts is fairly large, up to a millimeter for most grid designs. This distance can be compared to the distance holes have to travel to reach the back side contact. The back side of the solar cell is usually entirely covered by a metal contact, therefore the width of the cell becomes the distance for holes to traverse. The emitter is also highly doped in order to make the space charge region stretch furthest in to the base.

A consequence of the emitter being highly doped is that it will be an area of high recombination. Especially if there is a so called dead layer at the very top of the cell, where the space charge region does not reach. The blue, high energy portion of the light will be mostly affected by this type of losses, hence the "blue response" is value of merit when fabricating thin emitters.

Industrially emitters are usually made by letting a phosphorus containing steam condensate on a lightly boron doped wafer. Thereafter the wafer is feed in to a furnace and the phosphorus diffuses in to the wafer, not deeper than one µm. Because of the low cost and high scalability of this method it has been the choice of many producers of solar cells. It has also affected the perception of what a thin emitter is. Emitters thinner than these (~0.2 µm) are often referred to as thin emitters. Ion implantation as a mean of emitter formation was also investigated.

1.2.5 Front side metalization

The front side contacts must have a low contact resistance, good adhesion and industrially they must also be easy to solder. In the section of pn-junctions the concepts of aligning Fermi levels were introduced, see section 1.1.3 . The same will happen between the emitter, or base, and the contact metal. The metal can be thought of as a sink of great size for both holes and electrons. Just like in the case of a pn-junction the charge carriers from both sides will recombine in order to equalize the Fermi level leaving a space charge region. Depending on how well the metal and semiconductor contains their electrons either an Ohmic or a Schottky contact is formed. The measure for how much energy is needed to move an electron from the Fermi level in to the vacuum level is called work function. If the metals work function is smaller than the semiconductors work function the contact is Ohmic. The current as a function of voltage over an Ohmic contact is linear and symmetric. The other case would be if the work function of the metal was larger than the work function of the semiconductor. The resulting band diagram would show a potential barrier for a current from the semiconductor to the metal, which is not desirable in this context. Such a contact is called a Schottky contact. n^+-type silicon has a work function of 4.1 eV[36] while silver has a work function of about 4.3 eV. That

means that the metal-semiconductor interface between silver and silicon would be slightly rectifying and therefore not Ohmic. In spite of that silver is today the most common conduction metal for screen printing pastes. What has not bee mentioned so far is that when the space charge region becomes thin enough the current rather tunnels through than overcomes the potential barrier. As mentioned above, one of the reasons for highly doping the emitter is reducing the contact potential. For sufficiently high doping levels the emitter becomes thin enough for quantum tunneling to occur. Again referring to equation 25 one can see that for an emitter doping of $1e19\,cm^{-3}$ and a proximate hole concentration in the contact metal of $1e22\,cm^{-3}$ the depletion width becomes approximately 10 nm at zero bias.

1.2.6 Back side metalization

The back side contacts of a solar cell is often covered entirely by aluminium. At the metallurgical interface between silicon and the aluminium back side contact one can assume that all compositions ranging from 100 % silicon to 100 % aluminium exists, see figure 14, if the interface has been annealed at a temperature high enough. The region with a mixture close to the eutectic composition will melt and when cooled solidify with different compositions. The hypo eutectic region, the region closer to the Al-side of the eutectic point, will solidify with grains of alpha-phase precipitating out, while the liquid increases its silicon concentration until the eutectic point is reached. If the solution containes more silicon than the eutectic composition, the so called hyper eutectic region, silicon will precipitate out giving an increasing aluminium concentration in the liquid as the temperature is lowered. At the eutectic point grains with a mixed structure will form, featuring alpha and aluminium regions. This means that there will be a transition from a region with pure aluminium, alpha grains, alpha grains interwoven with a few mixed grains, only mixed grains, mostly silicon grains and a few mixed grain, only silicon grains and at last pure silicon. There are several good reasons for utilizing this process. The eutectoid gives a good electrical and mechanical contact with low contact resistance. Aluminium has an energy level close to the valence band of silicon, see figure 4, and will therefore work as acceptor when substituting for silicon. The back side of the solar cell will therefore be increasingly p^+-doped. This back side $\varepsilon-$field will attract holes and repel electron and make a good Ohmic contact for holes. In addition a shiny metal on the back of the cell will to some extent reflect photons that have traversed the whole cell. Keeping in mind, though, that the photons reaching the back side of the cell are of low energy. The back side coating has to some extent be passivating as well.

1.2.7 IV characteristics

This sub section describes the power response of solar cells. The origin of the IV-characteristics will be motivated by band diagram theory, which leads to an explanation of how the diode model describes the IV-response.

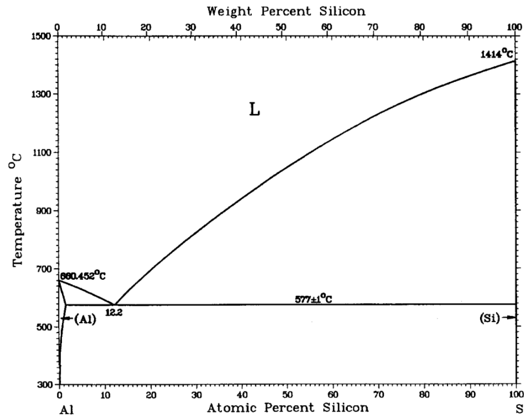


Figure 14: Phase diagram of aluminium and silicon from [37].

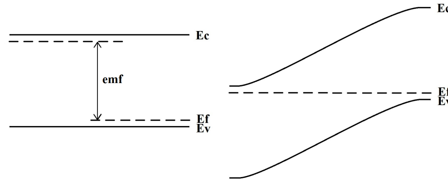


Figure 15: Band diagram for np-junction under open circuit conditions to the left. The maximum potential difference between the poles of the cell is produced at open circuit condition, but there won't be an ε-field drifting a current. To the right is an illustration of short circuit voltage-conditions. There is a big ε-field drifting charge carriers to their respective pole, but at the cost of lost potential.

The potential of a solar cell is due to the difference in quasi Fermi levels, see figures 15 and16. The quasi Fermi level is affected by the width of the band gap, the applied potential, doping levels and contact potential, not regarding Fermi level pinning and band gap narrowing. When the cell is illuminated and the circuit is open the potential over the cell is at it's highest. However, no current will be flowing, and there is no ε-field separating the charge carriers, see figure 15 to the left. The other extreme is short circuit condition, were there is no potential-difference over the cell, see figure 15 to the right, but all charge carriers, that do not recombine, are drifted through the circuit. The maximum power point is obviously some where between these extremes. The current voltage response of a solar cell can be approximated as the short circuit current minus the dark current,

$$I = I_{sc} - I_{dark} \tag{44}$$

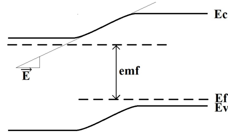


Figure 16: Maximum power (MP) is produced under a specific load, the so called maximum power point. At MP there will be an $\varepsilon-$field big enough to drive the current but not scarifying to much of the potential.

$$I = I_{sc} - I_0(\exp\left\{\frac{qV}{k_B T}\right\} - 1) \tag{45}$$

which is referred to as the superposition approximation. The super position approximation assumes that there is a maximum current that can be delivered by the cell given by $I_{sc} - I_{dark}$.

It is desirable to be able to utilize a power source at different potentials without the current dropping. Unfortunately a solar cell does not work in that way, see figure 17. The diode part of the one diode model shows that at higher potentials the current will not stay the same but drop off, rather drastically after some certain potential. The current voltage curve is in other words a lot different from a battery. A battery is usually thought off as a current source, meaning that a battery is expected to deliver the same potential at different currents, which to some extent is true. A solar cell, on the other hand is not a current source but at a given illumination works as a potential source. This is not how a solar cell is operated, though. Usually one is more interested in producing the highest possible power, and therefore a converter is needed for applying the module to a system.

A solar cells current response to bias is referred to as the IV-characteristics of the cell. Under illumination and reverse bias the current will reach saturation. Increasing the reverse bias even further will not increase the current, in the ideal case. The current under reverse conditions is called the saturation current. The ε-field separating charge carriers will be large. The factor limiting the current will not be the separating mechanism, therefore increasing the reverse bias even further will not increase the current. At extreme biases the reverse current will increase again due to break down mechanisms.

At forward bias, under illumination, the cell will be producing power. Initially the current will not drop significantly with increasing bias. Obviously the separating mechanism is not the limiting factor. The diode response is dampened by the small prefactor I_0. Increasing the bias even more will eventually lead to loss current due to recombination and leakage current. The exponential part of the diode equation will outweigh the small prefactor. Obviously the separating mechanism is the limiting factor at large biases. If the voltage is increased even further the power will switch sign. The current will be running in the opposite direction, from p to n side. What was a solar cell could start working as a light emitting diode. A large part of the charge carriers will re-

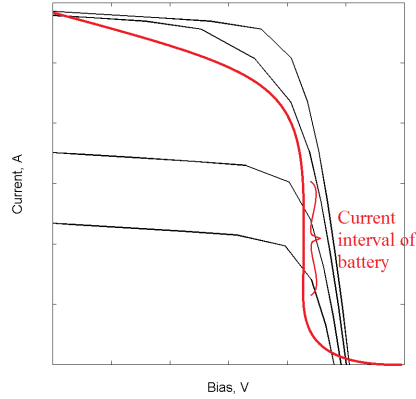


Figure 17: Illustration of typical IV-plot of a battery and a solar cell under different illuminations. Idealized one can say that a battery can deliver the same potential over a range of different currents, while a solar cell delivers the same current over a range of potentials. The maximum power point is shifted to higher currents and higher potentials with increasing illumination, which must bee accounted for when optimizing the use of PV solar cells.

combine in the junction, and a part of the recombination will occur as radiative recombination making a light emitting diode out of the cell, which is commonly used as a solar cell characterization method.

The prefactor I_0 is the so called leakage current. Physically it determines how much current that will diffuse over the potential barrier. I_0 should be as small as possible for good power output at large forward biases. I_0 determines how soon the diode part of the one diode model, see equation 45 starts to decrease the power output.

Part II
Processing, characterization methods and simulation details

The solar cell design simulation tool PC1D[38] is introduced below. It is used for showing a few important trends and for adding weight to claims. In the same section it is explained how a front side metalization grid can be designed and optimized using the numerical computing environment MATLAB. Section3 begins with a quick description of the process flow, followed by a detailed description of all process steps. Section 4 introduces some essential methods for solar cell characterization.

2 PC1D simulations and other numerical calculation

Subsection 2.1 describes how the front metalization patterns was designed. Based on the laws of Ohmic losses the total power produced as a function of finger width and spacing, among other variables the optimal one busbar standard grid was designed.

The next section2.2 regards the optimal emitter designed and investigated using PC1D. PC1D is a tool for simulating different solar cell compositions. As can be seen in the name of the program it models the process in one dimension, meaning that it could not simulate front contact patters for instance. The program can be set for the parameter interested for the user, such as ARC, texture, doping levels and so on. PC1D has been used as a guide to approximate appropriate parameters and to showing trends. One of the biggest advantages in using a simulation tool is that a guideline is given, before conducting experiments which saves time and resources.

2.1 Front metalization patterning

The front side contact pattern has to be made dense enough to conduct the current without too much Ohmic losses while at the same time sparse enough to let light pass. Considering these aspects gives the ground for optimizing the front contact. A simple iterative MATLAB code was written to sum up the Ohmic losses and the losses due to shading. See appendix for the code. The assumptions were that the fingers were 1µm thick, conversion efficiency: 10%, solar intensity: $1000\,\mathrm{W/m^2}$, potential at maximum power point: $0.7\,V$, and the resistivity of the conductor: $1.63e-6\,\Omega\mathrm{cm}$. In addition the current was assumed to flow perpendicularly to the nearest conductor. The simulation was done for finger widths of $1, 10$ and 100 µm and sheet resistances of $50, 100$ and $150\,\Omega/\square$ for the emitter. The dimensions of the solar cell were1x1 cm^2. See figure 18.

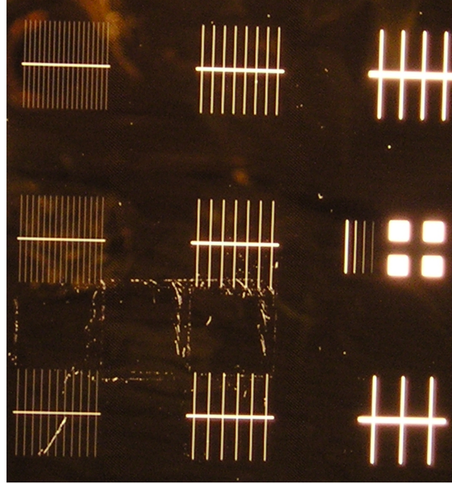


Figure 18: Photography of photo lithography mask used in this work. The upper row is three masks optimized for a sheet resistance of 150 $\Omega/\square$. The middle row is of masks optimized for sheet resistances of 100 $\Omega/\square$, and the bottom row for 50 $\Omega/\square$. From left to right, the finger widths are1, 10, and 100 µm. The optimal mask for 100 $\Omega/\square$, with a finger finger width of 100 µm is the same as the one for 50 $\Omega/\square$ with the same finger width. Therefore this mask was not duplicated, but the place was used for a technical tool, which is seen in the picture. The dimensions of all masks were 1x1 cm^2.

Ohmic losses have to be calculated in both the lateral current in the emitter, and conduction in the finger. Ohmic losses in the busbar was assumed small enough not to be taken in to account. The power lost due to Ohmic resistance is $W_{lost} = I^2R$, were I is the current. The solar cells front was divided in to small square pixels. Each pixel having the sheet resistivity of $\rho_\square$. The resistance of the pixels, because of it being square, is the same as it's sheet resistance. $R = \frac{\rho_\square l}{w}$ with $l = w$ equals $R = \rho_\square$. The pixel is illuminated, of which 10% is assumed to be converted to electrical power. The power is conducted to the next pixel, and the remaining power after resistive losses is added to the power produced in the next pixel. The power adds up, and if the line of pixels was infinitely long, it would converge to a positive value. The line of pixels is defined as half the length between fingers minus half the width of a finger. In this way the shading of the fingers is accounted for. A wider finger would result in a shorter line of pixels, and a smaller sum. A similar argumentation is done regarding the Ohmic losses in the finger. The only difference is that the added entity of power to each segment of finger is the total sum of the power from the sides, i.e. the emitter. The full summation is conducted for different finger spacing in order to find the distance giving the smallest losses, see figure 19.

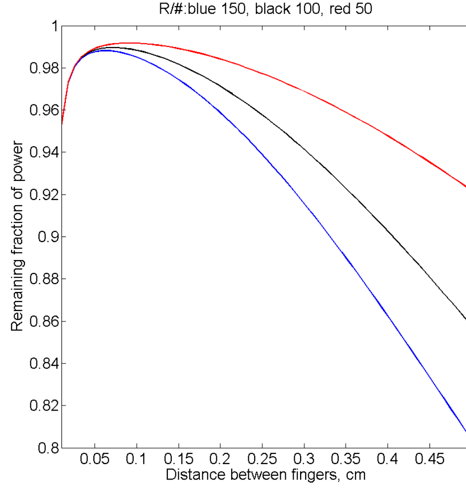


Figure 19: Simulation of relative power loss due to Ohmic losses in the emitter and the front side contact. The figure shows the power not lost as a function of spacing between fingers. Theses calculations were done with the parameters mentioned in the introduction of subsection 2.1. One can see that the optimal finger spacing is 0.059 0.06717and 0.09767 cm for sheet resistances of 150, 100 and $50\Omega/\square$. Wider finger spacing leads to Ohmic losses in the emitter, while narrower spacing causes too much shadowing.

Choosing the right metalization pattern can make all the difference between proving a novel concept or having the entire effect lost in Ohmic losses. Comparing the metalization patterns for critical dimensions of 1, 10 and 100 µm for a sample with a sheet resistance of $50\,\Omega/\square$ the unavoidable Ohmic losses would be 0.18, 0.83 and 3.74 %. Obviously a pattern with thinner fingers closer spaced would give a better result. If a mask is chosen that is optimized for a sheet resistance other than the resistance of the sample a significant part of the power can be lost. For instance if a mask optimized for $50\ \Omega/\square$ with a finger width of 100 µm is used for a sample that has a sheet resistance of $100\,\Omega/\square$ $0.29\,_{abs}\%$ will be lost. The effects is smaller for smaller finger widths because the absolute value of the spacing between the fingers are not altered to the same degree when optimizing for different sheet resistances.

For optimizing the process one would have to draw a line when finger breakage reaches an unacceptable level. In this study 100 µm was considered narrow enough. With a finger width of 100 µm one could expect no finger breakage caused by the photo lithography step. With a finger width of 10 µm about a third of the samples were damaged because of particles causing finger breakage during photo lithography.

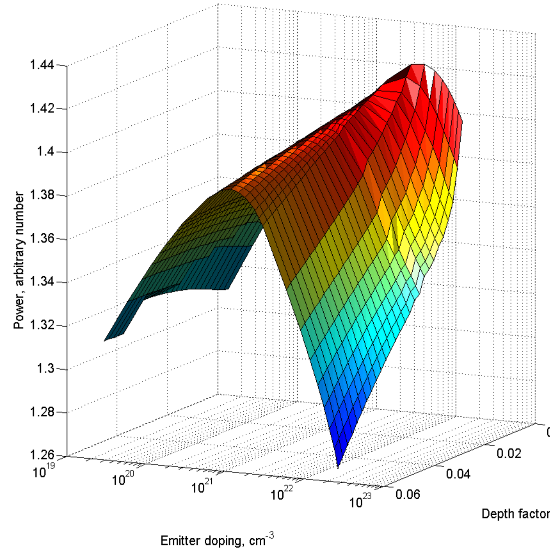


Figure 20: Power output as a function of emitter doping level and depth factor. It can be seen from this PC1D simulation that solar cells with highly doped emitters deliver higher Power. In addition it can be seen that a highly doped emitter has to be thin, which is not the case for lighter doped emitters.

2.2 Doping considerations

This section is based on [39], [40], [34] and [12]. PC1D simulations confirmed what the literature says regarding doping concentration and emitter thickness. The efficiency of the cell increases up to a certain point with increasing doping and thickness where recombination losses start to dominate. An emitter doping level has to be matched with an appropriate emitter thickness, meaning that a highly doped emitter should be narrow to keep recombination to a minimum. A lighter doped emitter should ideally be a little wider, as can be seen from figure 20. PC1D does not consider the lateral conductivity of the emitter, and novel concepts can therefore be a little harder to make reliable models of, for instance solar cells contacted with transparent conducting oxides or solar cells with extremely thin emitters. With decreasing emitter thickness the lateral conductivity will decrease giving larger Ohmic losses.

The base doping must also be matched with the emitter doping, se figure 21. PC1D simulations show where the junction between p- and n-side will be located, as a function of both the emitter doping and base doping. A higher base doping gives better transverse conductivity, but more recombination.

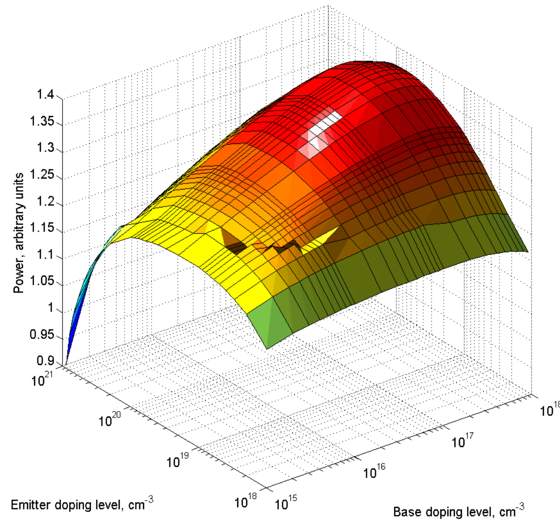


Figure 21: PC1D simulations varying the base doping and the emitter doping levels.

3 Experimental procedures

This chapter describes the details of the conducted experiments. All processing steps were tested out one at the time in order to not let former steps influence the results. The experiments conducted were:

- Sample were textured for increasing light absorption.
- Samples were oxidized for increasing light absorption, both textured and untextured.
- Samples were oxidized for passivation. Both undoped and implanted samples.
- A P-getterering experiments was conducted of a textured, oxidized and implanted sample.
- Samples were implanted and RTP at different temperatures and times. The sheet resistance was measured and the diffused profiles were measured.
- Samples were spin coated with SOD and annealed by RTP at different temperatures and times. The sheet resistance was measured.
- Samples were metalized, both by resistive and e-beam thermal evaporation. Metals tested were aluminium, silver, titanium and paladium.

<table>
<tr><th>Stp nr</th><th>Step goal</th><th>By which means</th><th>key parameters</th><th>Contamination precautions</th></tr>
<tr><td>1</td><td>Cleaning wafer</td><td>RCA 1,2 and 3+HFdipp</td><td>80 °C, 15 min</td><td>RCA-tweezers</td></tr>
<tr><td>2</td><td>Light absorption</td><td>Texturing</td><td>1 $_w$%KOH, 6 $_w$%IPA, 80 °C 24 min</td><td>KOH-tweezers</td></tr>
<tr><td>3</td><td rowspan="3">Emitter formation</td><td>SOD</td><td>4000 rpm 30 s</td><td>SOD-tweezers</td></tr>
<tr><td>4</td><td>Prebake, hot plate</td><td>200 °C 4 min</td><td>-||-, on dummy wafer</td></tr>
<tr><td>5</td><td>In diffusion</td><td>STP/RTP</td><td>-||-, on dummy in SOD susceptor</td></tr>
<tr><td>6</td><td>Cleaning</td><td>RCA1,2 and 3 +HF</td><td>80 °C,15 min</td><td>-||-,</td></tr>
<tr><td>7</td><td>ARC/Passivation</td><td>STP oxidation</td><td>1000 °C 90 min O_2ambient</td><td>Metallization-tweezers, On dummy</td></tr>
<tr><td>8</td><td>Clearing backside</td><td>Etching oxide</td><td>BOE, Front masked with PR</td><td>-||-</td></tr>
<tr><td>9</td><td>Back contact</td><td>Evaporation of aluminium</td><td>E-beam,200 nm</td><td>-||-, on dummy</td></tr>
<tr><td>10</td><td rowspan="4">Front contact</td><td>PL definition of contacts</td><td>Soft bake,100 °C 4 min 240 W 10 s</td><td>-||-</td></tr>
<tr><td>11</td><td>Etching Oxide under fingers and Busbar</td><td>BOE, floating on surface</td><td>-||-</td></tr>
<tr><td>12</td><td>Evap. of Ti, Pd and Ag</td><td>E-beam, 10 nm, 10 nm, 100 nm</td><td>-||-</td></tr>
<tr><td>13</td><td>Lift off</td><td>In ultra sound bath in acetone</td><td>-||-</td></tr>
<tr><td>14</td><td>Sintering</td><td>Forming gas Annealed</td><td>1:9 H_2:N_2, 375 °C, 30 min</td><td>-||-, on dummy wafer</td></tr>
<tr><td>15</td><td>Edge isolation</td><td>Laser scribing/diamond sawing</td><td></td><td>-||-, on dummy wafer</td></tr>
</table>

Table 1: Process flow chart showing step number, the goal of each step, how the goal is reached, a few important parameters and what precautions were used to guarantee not contaminating the samples from step to step. -||- means that the same tweezers follow with the sample to the next step. Dummy wafers were used as a bed in step 4, 5, 7, 9, 14 and 15.

- The full process was conducted and characterized.

The full process started with a p-type wafer (Czochralski-silicon (Cz-silicon), Boron doped, (100), $525 \pm 25\,\mu m$) cleaned, textured and spun with SOD. After drying on hotplate the wafer was scribed with a diamond pen and broken in to smaller pieces, each piece large enough for one cell. The emitter was diffused with RTP at 990 °C for 30 s. One batch was post annealed in a STP in O_2 environment to grow a thermal oxide thick enough to both work as a passivating layer and anti reflective coating. After heat treatment the samples were contacted by evaporation of metals using e-beam thermal evaporation. The back side was contacted with aluminium, and the front with a titanium, palladium and Ag-stack. The pattern was defined by photo lithography.

3.1 Texturization

The samples were prepared with a full RCA123-clean, and left to soak in water, never allowed to dry. A KOH solution with a final concentration of $1\,_{\mathrm{W}}\%$ was prepared and heated to 80 °C on a hotplate. When the target temperature was reached $6\,_{\mathrm{W}}\%$ IPA was added. Before adding the samples the solution was left to heat again to within one degree from 80 °C. The samples were moved from the water beaker in to the solution quickly so that there would be no chance for water droplet to dry at the surfaces. The samples were placed directly at the bottom of the beaker with the front side up. The solution was constantly mixed using a magnet stirrer held in a basket elevated above the sample. Every sixth minute $2\,_{\mathrm{W}}\%$ IPA was added. The samples were etched for 24 min, see figure 22.

Both small samples (1x1 cm^2) and full wafers were textured. The size of the beaker was chosen to fit the sample at hand.

3.2 Implantation

Emitters were implanted with different doses and energies. In general a high dose at a low energy was used in order to get an emitter with high doping and narrow profile. When a passivating oxide had been grown on top of the sample a higher energy was needed to drive the P-ions all the way though in to the silicon, which in inevitable would lead to a higher straggling and therefore a wider emitter. The width of the emitter has a direct relation to the blue response of the final solar cell, as was discussed above1.2. In addition, a larger straggling would also call for a higher dose, in order to reach the desired concentration.

The ion-stopping simulation program SRIM was used to simulate the energy and doses of implanted phosphorus [41], see figure 23. The implant energy was chosen so that the mean penetration range would be at the interface between SiO_2 and silicon.

A textured sample will effectively be implanted at an angle of 144.74°, measured from the incident beam. This means that the P-ions will experience an effective thickness of the SiO_2 that is 1.733 times thicker than the thickness

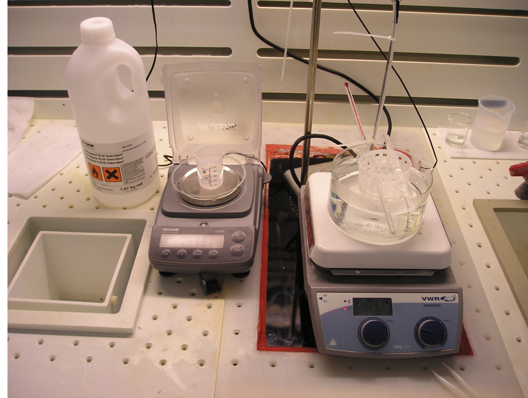


Figure 22: Picture of etching setup. The sample were placed at the bottom of the glass beaker, see to the right of the picture. The basket holding the magnet stirrer is clearly visible. The temperature was monitored with a thermocouple submerged in the bath. IPA was scaled and added every sixth minute.

measured at a normal angle from the surface of the pyramids. Therefore even higher energies are needed in order to get the doping peak at the surface of the silicon wafer.

3.3 Annealing

The section is based on references [19],[24] and [42].

RTP was used to anneal both implanted- and SOD samples. AnnealSys RTP system AS-micro was was used for RTP in this work. The oven was heated with high temperature tungsten halogen lamps, causing the radiation spectrum to be further in to the ultra violet range, in contrast to CTP.

The sample was placed in a silicon carbide susceptor, covered by a silicon lid. The purposes of the susceptor is two fold: The susceptor will have an inherent ability to convert high energy electromagnetic radiation to IR-radiation. Silicon carbide has a direct band gap at 2 to 3 eV which means that it is opaque to high energy electromagnetic radiation. Incident short wavelength radiating will heat the susceptor which in its turn re emits a Planck spectrum according to the susceptors temperature. The sample will not be exposed to short wavelength radiation but IR. The susceptor also doubles as a guard against contamination of sample/chamber. Historically a lot of work has been done to show weather or not RTP has a diffusion enhancing effect. The idea stems from that the larger portion of high energy light might in some way enhance the diffusion of impurities. Any possible form of diffusion enhancing effects due to high energy radiation is eliminated by the setup used in this work.

The chamber is evacuated and thereafter filled with N_2 to atmospheric pres-

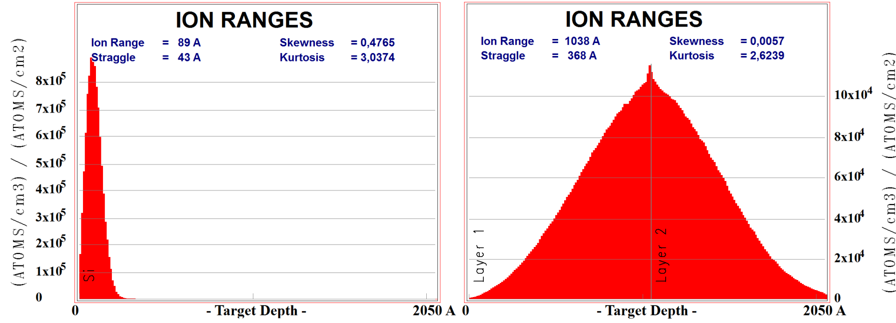


Figure 23: SRIM simulations of P-ion implantation. The y-axis shows concentration divided by dose as a function of depth, the x-axis. Both a structure with no oxide (left) and a bi layer structure with $105nm$ thick SiO_2 at the surface with a density of $2.2\,\mathrm{g}/cm^3$ (right) is pictured. The implant energies were 4 and 72 keV. The right plot corresponds to the situation when implanting through an ARC. The left plot illustrates how thin an emitter could have been achieved for implantation without an ARC. Obviously if the scope is a thin emitter, it can not be implanted through an ARC.

sure. Both the ceiling and bottom of the chamber is equipped with tungsten halogen lamps, that can be heated to several thousand degrees. The temperature is measured by a pyranometer. The pyranometer responds to temperatures above 400 °C. It was placed facing the susceptor. Therefore one would have to assume that the susceptor and the samples would have the same temperature.

The temperature was ramped up at 50 °C/s, held at the desired temperature for a chosen time and ramped down. The cooling rate was calculated to about −50 °C/s the first few seconds. The annealing time and temperature given in the result section refers to the plateau time and temperature.

STP was used for growing a passivating oxide and P-gettering. Thermco model 4104 oven for general thermal oxide was used. It was showed that a lot of contamination was introduced and the minority carrier life time was significantly shortened. Therefore a quartz tube dedicated for growing thermal oxide was cleaned in three parts HNO_3 and one part HCl for 24 h. The mixture, often referred to as aqua regia, is often used to clean lab-room quartz. The dedicated tube was inserted in to a bench size oven, Gero HTRH 40 250/18. In both cases the oxidation was done in a O_2 atmosphere. In both the first and second experiment the samples were oxidized at 1000 °C, for different times.

3.4 Metalization

3.4.1 Backside

The back side contact was formed by thermal evaporation of aluminium by e-beam evaporation. The samples were at this stage textured, doped and activated. The samples were mounted in a e-beam evaporator with the back side facing the crucible. The chamber was evacuated to a pressure between $5e-7$ mbar and $10e-7$ mbar. A high energy electron beam is focused in to a crucible containing aluminium, which melts and evaporates. Aluminium atoms are expelled from the melt and condenses on any surface in the trajectory path. The samples are covered by a layer of aluminium at a rate of about 1 Å/s. The thickness is monitored by a in situ thickness monitor. The thickness monitor is a crystal driven by AC at it's eigen frequency. When matter is deposited on the crystal the weight increases and the eigen frequency drops. Knowing the density of the matter the thickness can be execrated from the eigen frequency data.

Aluminium was chosen for backside contacting. Aluminium forms a good contact to silicon, has a low resistivity ($2.8e-6\,\Omega$cm), reflects photons that has traversed the thickness of the sample and acts as an acceptor in silicon.

The first batches of cells were heavily shunted. To cope with this the sides were masked during metal deposition. At a first stage aluminium tape was used for this purpose, while later a mask was machined out of a thick plate aluminum. The rim holding the sample in place, while exposing the backside to the source would double as a mask for the sides. Some shunting was still evident leading to the next resort. The finalized process comprised producing cells on wafers larger than the final cell size. Leaving it to the very last step to cut of the sides and therefore make a very good edge isolation. A draw back with this method is that the edges themselves will be areas were large recombination can occur, since the surfaces of the edges will be bare.

200 nm aluminium was evaporated on the backside of the solar cell. As mentioned above, aluminium will act as an acceptor in silicon and therefore could be used to make aback surface ε-field (BSF). The samples would have to be heated to temperatures above the eutectic point of silicon-Al. After annealing at 600 °C the contact showed a very good mechanical adhesion but were also mottled. With respect to the small gain in conversion efficient this step was not investigated further. The samples were produced on fairly thick wafer (450 µm) rendering the effect of BSF small. PC1D simulation showed that one could expect an increase in conversion efficiency of 0.08 % for a cell 450 µm thick. A thinner cell does have a significant increase. For a 180 µm thick cell the increase is 2.6 %, which would have granted further investigation of the matter.

3.4.2 Front side metalization

The front side metalization pattern has to been optimized with respect to shading- and resistive losses. A photo lithography mask was produced for three different sheet resistances, $50, 100$ and $150\,\Omega/\square$, and with three different finger

widths; 1, 10 and 100 µm, giving a total of nine different masks. For robustness of processing the mask with a finger width of 100 µm was used in the following experiments.

A primer can be used to enhance the adhesion of the photo resist (PR). In this work it was chosen not to use primer, since it caused sever problems in the lift off step, following metal evaporation. It was proven much more reliable to be sure to use dry wafer, directly from e-beam evaporation, than risking a far to good adhesion and hindered lift off. Romb Haas photo resist, S1813, was spun on at 3500 rpm for 30 s. In order to avoid unnecessary contaminating equipment no pipette was used. The PR was poured from a beaker directly on to the spinning sample. The sample was soft baked on a hotplate for four minutes at 100 °C. The pattern was exposed for 10 s at an intensity of 290 ± 10 W, and thereafter developed in a 1 : 5 mixture of Romb Haas developer for 90 s.

The next step was deposition of metal. Both silver and a stack of titanium, palladium and silver were tested. Aluminium was not used for a front side contact due to its tendency to form spikes in to the emitter, which might shunt the cell. In addition, as mentioned in the section 2 aluminium in silicon works as an acceptor, which causes the very opposite ε-field needed for extraction of electrons. Titanium is readily used as a getter in vacuum systems and when turning on the e-beam, while the shutter is closed one can observe how the pressure slightly decreases. Titanium was used for its great ability for mechanical adhesive. A10 nm titanium layer was followed by a 10 nm layer of palladium before 100 nm silver was deposited. Palladium was used as a diffusion stop for silver. Silver was chosen as the conducting metal because of it's low resistivity ($1.63e-6\ \Omega$cm). For a good, clean adhesion the stack has to be deposited without breaking the vacuum.

After metal deposition the samples were submerged in to acetone in an ultrasonic bath. The PR was dissolved, lifting off the excess metal. Only the metal in the the fingers and busbar was left intact.

4 Characterization methods

Section four reports which Characterization methods were used, briefly how they work and what information they can give.

4.1 Scanning electron microscopy (SEM)

This section is based on reference [10]. SEM was used to visually observe the quality of the textured surface. Using a SEM instrument it was possible to see to what degree the texturization covered the front. In addition the size and shape of the pyramids could be observed.

In a traditional optical microscope light is used as the probing medium. The resolution is limited by the optics of the microscope but also to the wavelength of light. The resolution limit, d, is coupled to the refractive index of the medium surrounding the sample N, the apparatus diameter A and the wavelength via$d =$

$\frac{\lambda}{2NA}$. Usually an optical microscope can distinguish objects down to a couple of hundred nanometers. If the depth resolution had been better an optical microscope would have been enough for observing the result of texturing, but since it has very limited depth resolution, especially at larger magnifications levels SEM is preferred.

SEM uses electrons as probing medium. The de Broglie wavelength of an electron accelerated to for instance 5 keV is $1.73e^{-23}$ m, which means that the wave length alone is not the liming factor of an SEM. Limitations are rather how well the spot can be focused on to the sample via electromagnetically lenses and the interaction volume.

A filament emits electrons that are accelerated over a potential difference. The electron beam is focused via lenses on to a small spot on the sample. The electrons interact either elastically or in elastically with the sample. Secondary electrons emitted from close to the spot where the incident electron entered the sample are attracted with a potential, and accelerated to be given enough energy to be registered. The image from secondary electrons gives a good view of the topography of the sample. Incident electrons that do not knock out secondary electrons travel deeper in to the sample and scatter elastically with sample atom cores. Heavier cores will deflect the path of the incident electrons more than lighter ones. If the path of the incident electron is deflected enough to expel the electron from the sample it can be detected as a back scattered electron. Areas of the sample with a higher density of heavier atoms will appear lighter in the image, and the energy of the back scattered electron can be used to determine the composition of the sample.

The signals, either secondary of back scattered, are detected as a function of position over the sample, giving one pixel of information. The incident beam is thereafter moved a little and a new measurement is done, and that is why the method is called *scanning* electron microscopy.

4.2 Photo spectrometry

This section is based on [43]. Photo spectrometry can be used to gather information on how much of a certain wavelength that is transmitted through a sample or reflected off the surface. The instrument features light sources of different spectra. The light is refracted through a prism in order to get monochromatic light. The light is directed on to the sample, the reflectivity is measured, one wave length at a time, and the result is plotted as the reflectivity as a function of wavelength. The reflectance of all wavelengths are investigated, from ultra violet to near infrared. The integral of the product of reflectance and A.M. 1.5 spectrum gives the total weighted reflectance. The limiting factor at the long wavelength end of the spectrum is the band gap of silicon, equaling to 1117 µm, meaning that at wavelengths longer than that there is not enough energy to promote an electronic excitation. Silicon does not become entirely transparent above 1117 µm, which means that the energy is lost to heating of free charge carriers and lattice vibrations. On the short wavelength end of the spectrum the limiting factor is the black body radiation from the sun. There is basically no

sunlight at wavelength shorter than 250:nm and therefore the product of light flux and absorption goes to zero.

4.3 Ellipsometry

The non destructive light optical analysis technique ellipsometry was used to measure the thickness of the ARC. With ellipsometry one measures the complex dielectric function $\tilde{\varepsilon} = \varepsilon + i\varepsilon$, which is coupled to the complex refractive index $\tilde{n} = n + ik$ via $\tilde{\varepsilon} = \tilde{n}^2$. Ellipsometry utilizes linearly polarized light exposed on to a sample, such as a film grown on a wafer, and measures the change in polarization of the reflected light. Linearly and circular polarization are the extremes of polarization, any other polarization is elliptical hence the name of the measurements technique. A beam of light that strikes a junction between two optically different material will partly be reflected, transmitted and refracted described by Fresnel's equations. The reflection from the surface of the ARC will add to the light that has traveled through the ARC and reflected off from the emitter. A part of the reflected beam will be reflected back towards the emitter again, while the emitted part will interfere with the light primarily reflected from the surface. The interference will either be constructive or destructive following Bragg's law. In ellipsometry the phase difference is measured and not only the intensity of the reflected light and accordingly the thickness of the film can be deduced.

4.4 Life time measurements

This section is mainly based on references [44], [45], [46] and [47]. Life time (τ) is the average time it takes for a charge carrier to recombine. A longer life time increases the probability for a charge carrier to drift or diffuse to the contacts of a solar cell, meaning that the maximum power point can be at a higher potential. Since the lifetime is a characteristic that effects the efficiency so directly the PV solar cell community has develop several ways of measuring it. Generally there are three different approaches; Steady state, transient decay or Quasi Steady State. Steady state is when a constant excitation gives a constant level of charge carriers. Since life time is dependent on charge carrier density the two following methods account for that. Transient life time measuring is when the excitation is very short compared to the life time which means that the charge carrier levels will decrease during the subsequent measurement. The third approach is life time measurements with the excitation intensity varying slowly enough so that the sample always is in equilibrium.

The continuity equation states

$$\frac{d\Delta n}{dt} = G - U + \frac{1}{q}\nabla J\,, \tag{46}$$

where G is the photo generation rate and U is the recombination rate. Since the sample is electrically isolated the derivative of the current density is zero.

If the recombination rate

$$U = \frac{\Delta n}{\tau} , \tag{47}$$

the continuity equation can be solved for the life time

$$\tau(\triangle n) = \frac{\Delta n(t)}{G(t) - d\Delta n(t)/dt} . \tag{48}$$

If the light pulse is terminated abruptly $G \ll d\Delta n(t)/dt$ and equation 48 becomes

$$\tau(\Delta n) = -\frac{\Delta n(t)}{d\Delta n(t)/dt} , \tag{49}$$

which describes the transient mode. If on the other hand the sample is illuminated under a steady light $G \gg d\Delta n(t)/dt$ and equation 48 becomes

$$\tau(\Delta n) = \frac{\Delta n(t)}{G} , \tag{50}$$

which is the steady state mode, while equation 48 refers to the generalized case, i.e. quasi steady state.

The charge carrier life time was measured using a Sinton WCT 100 quasi steady state photo conduction (QSSPC) measuring device. The working principle is that a light pulse excites charge carriers and the time for the charge carriers to recombine is measured. This is done by electromagnetical coupling between the sample and a coil.

A sample is placed on a stage with an integrated coil and light sensitive diode. A flash of light excites the charge carriers in the sample. Ideally the light from the flash should be of the a.m. 1.5 spectrum, but that is seldom the case. The flash of light is long enough so that it can be assume that the sample is illuminated steadily under a specific light intensity. This means that the generation rate will balance the recombination rate. The conductivity of the sample is measured inductively by the coil. Since the coil is driven by an oscillating potential the resulting oscillating magnetic field will make the charge carriers in the sample move in so called eddie currents. The movement is so that the Lorentz force due to the magnetic field counteracts the magnetic field from the coil, stated by Lenz's law. This is measured as an increased resistance in the coil. The light intensity is slowly decreased and the charge carriers for a lower level of illumination is measured. The extremes are steady state, where the sample is steadily illuminated, and transient, where the excitation is continuously changed and the derivative of the life time is measured. In QSSPC a region in between is used.

4.5 Four point probe measurements

This section is based on references [48, 49]. A common and convenient way to evaluate the effect of doping and annealing is to determine the sheet resistance of the emitter layer. The sheet resistance is resistivity per layer thickness. The

resistance of the emitter is $R = \frac{\rho l}{tw} = \frac{\rho_{\Box} l}{w}$, were ρ is the resistivity, l the length, t thickness, w the width and $\rho_{\Box}$ is the sheet resistance. However, the resistance of an emitter is rarely quoted. Sheet resistance is usually enough.

To eliminate the resistance in the leads and contacts from the measured values a four point probe is used. A current is run via two outer needles and the potential drop is measured with two inner needles placed close to the outer needles in a line. The resistance is high in the circuit measuring the voltage drop and therefore only a miniscule current runs through it.

In this work a Jandel RM3-AR Test unit was used in combination with a Jandel Microposit probe.

4.6 Secondary Ion Mass Spectrometry (SIMS)

This section is based on reference [50]. In this work SIMS has been used to determine depth profiles of implanted and thermally diffused samples.

In SIMS a primary ion beam is accelerated and focused on to a small area on the sample where target atoms are sputtered. A small fraction of the emitted particles ($\lesssim 1$ %) are ionized and these so-called secondary ions are collected into a mass spectrometer. The intensity of the secondary ions can be used for quantification by employing reference samples with a known concentration of specific impurities, for example phosphorus in silicon.

In this work, a Cameca IMS 7F instrument has been used and a detection limit of phosphorus in silicon of about $\backsim e15\, cm^{-3}$ was obtained.

4.7 IV-testing

This section is mainly based on references [35], [49] and [12]. The electrical characteristics and performance of a solar cell are determined by measuring the output power under different potentials. The cell is contacted, illuminated and put under a potential difference. The current flowing at the potential is registered and the potential is changed. The cells quality can be determined and some of the background for power loss can be seen, such as shunting or series resistance.

Shunting is when a cell is in some aspect short circuited. Industrially it is often a matter of contact paste lapping the distance from front contact to back contact, over the edge of a solar cell. Experiments showed that even e-beam evaporation, which is a highly directional deposition technique, leads to shunting if not special care is taken to avoid metal depositing on the sides of the cell. Another common form of shunting is when front side metalization paste is driven to deep in to the cell, through the total thickness of the emitter. Care must therefore be taken when optimizing the firing step after front side metalization. Series resistance is when too much of the power is lost to Ohmic resistance. The resistance can be in the emitter or base, fingers, busbar or the contacting of the cell. Combining shunt and series resistance in the diode model gives the following diagram 24.

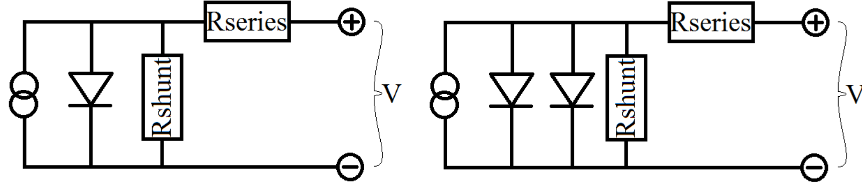


Figure 24: One diode model shoring both series resistance and Shunt. Obviously the Shunt resistance should be as large as possible while the series resistance should be small.

The equivalent one diode model is

$$I = I_{sc} - I_0 \left(exp \left\{ \frac{q(V + IR_s)}{k_B T} \right\} - 1 \right) - \frac{V + IR_S}{R_{sh}} \tag{51}$$

were R_s is the series resistance and R_{sh} shunt resistance.

Regarding the IV characteristics of the solar cell of figure 10 , one can see two things. Considering the illuminated case, right most picture, both the curve close to the I_{sc} and V_{oc} point are sloping. Ideally the curve close to the I_{sc} should be perfectly flat, resembling the picture to the left more, but in this example it is not. This is because of shunting. At larger potentials more current is forced through the shunt, and not fed through the external leads contributing to the produced power. Solar cell described by the ideal diode equation will be able to deliver almost the same current with increasing potential up to a couple tenth of a volt from the V_{oc}, where after the current drops until V_{oc} is reached. The IV plot should look more like the left most plot of figure 10. With decreasing shunt resistance the fill factor is reduced, and at extreme values the open circuit voltage is reduced as well, reducing the diode to a mere conductor.

A cell that suffers from series resistance will be affected in the high voltage end of the IV plot. The open circuit voltage is obviously not effected since there is no current flowing, but as soon as a current starts to flow through the cell power is lost to Ohmic heating. Therefore the slope close to the V_{oc} will be lesser steep. For moderate series resistance the same current can pass as if the cell was not subjected to series resistance at smaller voltages, meaning that the IV plot will merge in to the ideal IV plot at smaller potentials. The fill factor will be reduced, though. In the extreme case the I_{sc} is reduced and all the ideal diode behavior is lost.

IV characterization is therefore commonly used to diagnose solar cells with respect to resistive losses.

When performing an IV-test a solar cell must be contacted. Tests showed that the way of contacting the solar cell can have severe consequences for the result. Usually the cell is placed on a copper bed and the front side grid is contacted with a probe. If the front side metalization pattern is optimized for current transport vs thickness the point of contact will be a bottleneck for the current. The front side metalization pattern has in this work been deposited

via thermal evaporation followed by a lift off step. In order not to deposit unnecessarily thick layers in the e-beam and to make sure the lift off step is not hindered by the thickness of the metal, the front side contacts were kept fairly thin, compared to for example screen printing. If then the busbar was to be contacted by a pointy needle the area around the needle point would be the bottle neck causing series resistance. Soldering leads proved to give low Ohmic resistance, but were impractical to make on small cells, with narrow busbars. Instead a wider probe was used, that would create a larger area of contact.

The fabricated cell was illuminated by light with a.m. 1.5 spectrum of $1000\,\mathrm{W}/m^2$ and a potential source (Keithley 2440 5A, Source Meter) stepping the voltage from a few tenth of a volt below zero beyond V_{oc}. The current was measured by the same instrument.

The IV-characteristics are affected by temperature, as can be seen directly from the equation 51. Therefore the temperature has to be kept the same for all measurements. The standard temperature for measuring solar cells are $25\,^{\circ}\mathrm{C}$.

As stated above, the current through a solar cell is the short circuit current minus the dark saturation current. The dark saturation current is in turn a function of bias, obviously. To which degree the saturation current responds to voltage changes is quantified by the so called ideality factor. The ideality factor scales how fast the dark current grows with increasing bias. The ideality factor usually ranges from one, for the ideal case, to two, for non ideal cases. The ideal diode equation is derived considering only band to band recombination and SRH recombination, and that all recombination occurs in the bulk of the cell or in the bulk of the emitter, i.e. no recombination in the depletion zone. For a non ideal diode the ideality factor is tuned in order to account for the recombination in the depletion zone, and recombination in the depletion zone gives ideality factors close to 2.

The ideality factor can be derived from the IV characteristics of a solar cell. Using the simple ideal diode equation 19, assuming a small bias, the factor -1 following the exponent can be ignored. Solving for the natural logarithm of the current

$$\ln\{I\} = \ln\{I_o\} + \left(\frac{q}{nkT}\right) V \tag{52}$$

the slope of the plot is $\frac{q}{nkT}$, which can be solved for the ideality factor n.

For positive biases there will be less recombination in the depletion zone. For negative biases, when the depletion zone is large, there will be a larger portion of recombination in the depletion zone. The ideality factor will therefore change as a function of bias. To account for this effect a two diode model is invoked, see figure 24. In the two diode model two diodes are coupled in parallel with different ideality factors, normally one and two. In the one diode model it is assumed that there is no recombination in the depletion zone, as mentioned in section 1.1.3.

Part III
Results and discussion

5 Results

The experimental results are presented in this section. The reflection data of textured and oxidized samples were confirmed by Anna Malou Petersson at Northen Research Institute. For a discussion of the results please see section 6.1.

5.1 Results of Texturization

Before texturing the polished wafer had a reflectance of 39.3 $_W$%, meaning that 39.3 % of the energy in the entire air mass 1.5 spectrum will be reflected. The results from several experiments showed that a low concentration KOH, at high temperature and a fairly high concentration IPA (6 $_W$%) gives a well textured surface that reflects 9.5 $_W$%, see picture 25.

The biggest challenge was to obtain a homogeneously etched surface. The procedure described in subsection 3.1 had to be carefully followed. Etching using a dipper was proven to not work very well, since all plastic/teflon surfaces will attract H_2 bubbles, which would partially mask the sample. It was also evident that the extra heat from lying on the bottom of a hotplate-heated beaker had a positive effect on the etch rate. A word of caution regarding laying the sample in the bottom of the beaker is to notice that the heat conductivity through bottom of the beaker is not necessarily spatially homogeneously distributed. The glass is not perfectly flat causing localized contact points. Varying thickness of the glass might also vary the heat radiating/conducting through. Since the etching process is so heat sensitive, it might be a good idea to let a stirrer lightly move the sample over the floor of the beaker.

Any form of surface contaminations would act as reaction sites, meaning that a dust particle on the surface would give a visible spot on the sample after etching.

IPA has a boiling point at 82.5 °C which means that at 80 °C there will be a lot IPA evaporating, which had to be compensated for in some manner. In this work IPA was refilled every sixth minute during the entire etch.

5.2 Results of Oxidation

Thermally growing SiO_2 layers for light capturing show good reproducibility and low values of reflection. However, obtaining a good passivation by growing thermal oxide proved difficult. A slight passivating effect has been proved, when using equipment dedicated for SiO_2-growth, see table 2.

The samples were also optically characterized. Weighted reflectance showed a smallest value at 110 nm thick oxide, see figure 26. This thickness coincided

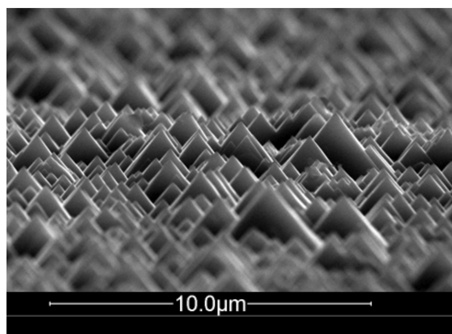


Figure 25: SEM-picture of (100)-grown CZ-silicon, detected with Everheart Thornley detector, 15 kV, spot 4.0, WD 10.5 mm, Magnification 5000X, etched for 24 min at 80 °C with 6 $_W$% IPA.

minutes annealed	12	21	80	140
lifetime before oxidation, µs	1.89	1.88	1.86	1.88
lifetime after oxidation, μs	2.88	2.67	0	2.86
oxide thickness, nm (refracting index 1.43)	73	110	136	161
Weighted reflectance	20.55	17.28	20.39	23.68

Table 2: Lifetime measurements for samples oxidized in O_2 environment at 1000 °C. The samples were CZ (100)-grown silicon, P-type. Resistance $10 - 20\,\Omega$cm. Four 4x4 cm^2 pieces were cut from the same wafer. The lifetime was measured at an injection level of $2e14\,cm^{-3}$. The sample annealed for 80 min did not give a measurable life time after annealing, presumably due to contamination from the furnace tube.

very well with PC1D simulations, which predicted the same optimal thickness.

Reflectance measurements were conducted after texturing and oxidation as well. It was expected that the optimum thickness should be a factor of 0.577 smaller, meaning that if the optimum effective thickness of the ARC is 110 nm, the actual thickness should be 63.5nm. As stated in the texturing theory section, an alkaline etch will leave the surface covered with pyramids. The angle between the pyramid side and the normal to the surface is 54.74°, so that a light ray that strikes the surface at a normal angle will travel though the ARC a longer distance if the surface is textured, than if flat. Therefore, the ARC was expected to be optimized at a smaller thickness, but it was not. The lowest reflection was found to still be at 110 nm.

It can be seen in both the textured and non textured case that the minimum reflectance is moved towards shorter wavelengths with decreasing ARC thickness, see 27.

SEM results show that the sharpness of the pyramids does not get effected by oxidizing the sample, see figure 28.

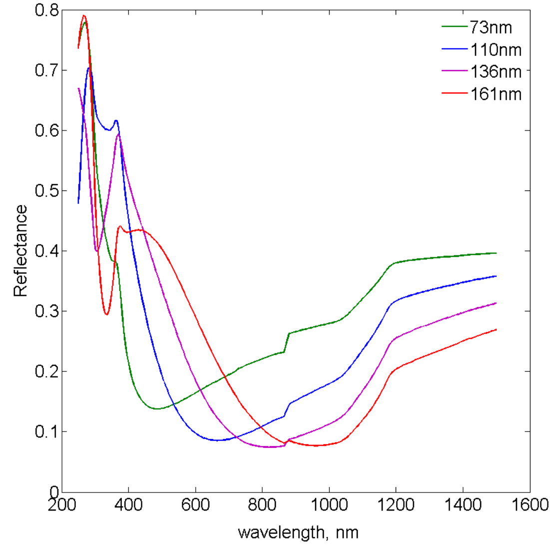


Figure 26: Plot of reflectance of samples with thermally grown oxide of thicknesses 73, 110, 136 and 161 nm. The weighted reflectance were 20.55, 17.28, 20.39 and 23.68 $_{\mathrm{w}}$%.

5.3 Results of P-implantation and activation

It proved to be difficult to achieve a shallow emitter with the use of Ion implantation. The samples were designed with a screening oxide optimized for light absorption. This meant that a fairly thick oxide covered the surface (110 nm). Therefore a rather high energy was needed in order to get the implantation peak at the surface of the silicon (73 keV). A high energy causes a large straggling. SRIM simulations shows that with a sample not textured but passivated with a thermal oxide the straggling was 36.8 nm, while for a sample that is textured, and therefore has effectively a thicker oxide, results in a straggling of 57.9 nm.

Seven samples were implanted with phosphorus at an energy of 73 keV to a dose of $1e14\ cm^{-2}$. The samples were of CZ-silicon, $505 - 545$ µm thick with a resistivity of $25.5 - 42.5\ \Omega$cm with no ARC.

It can be seen from four point probe measurements that at temperatures of 1100°C no further activation could be accomplished, see table 3. The only effect is further diffusion of the emitter and, what will be discussed later, gettering. At the other extreme end of the scale one can see that at 600 °C the sheet resistance has increased a lot. An explanation to that could be that only a P-concentration enough to cancel out the background doping of the sample has been activated.

From the SIMS measurements 29 it can be seen that for longer annealing times the emitter will have diffused further in to the bulk. With an annealing

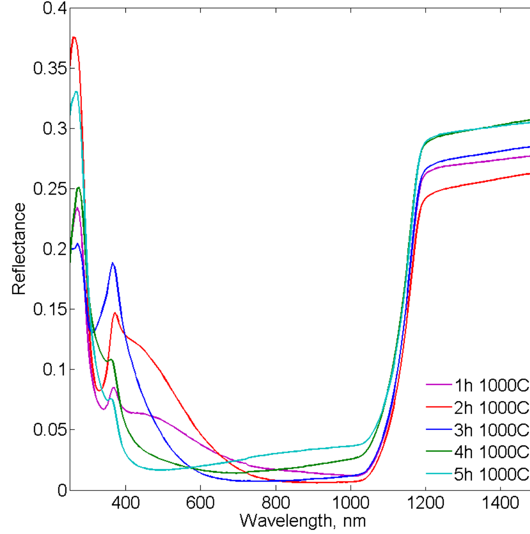


Figure 27: Plot of reflectance of textured samples with thermally grown oxides of thicknesses (purple), (red), (blue), (green) and nm (turquoise). The weighted reflectance is 3.55, 4.65, 3.07, 2.62 and 2.84 $_{\mathrm{W}}\%$.

time of 30s and temperature of 1100 °C the pn-junction for a sample with background doping of $1e16\,cm^{-3}$ will be at approximately 450 nm, a fairly wide emitter. A strange happening is that at the same temperature, at one second annealing the diffusion seems to have gone even further. This fact is hard to explain by annealing only. Perhaps the second sample has not been placed at the same angle in the implanter, causing channeling.

The difference between expected and measured temperature can be seen in this plot30.

The red line is the measured temperature and the narrow black line is the recipe temperature. From this plot it can be seen that the peak temperature is barely within 30 °C of the recipe temperature. Another observation done

Color in fig29	$R/\#$ before RTP	peak temp	time	$R/\#$ after RTP
green	$273\Omega/\#$	$1100°C$	30s	$168\Omega/\#$
black	$287\Omega/\#$	$1100°C$	5s	$153\Omega/\#$
blue	$284\Omega/\#$	$1100°C$	1s	$129\Omega/\#$
brown	$292\Omega/\#$	$800°C$	1s	$111\Omega/\#$
purple	$301\Omega/\#$	$600°C$	1s	$3300\Omega/\#$

Table 3: Four point probe results of RTP implanted samples.

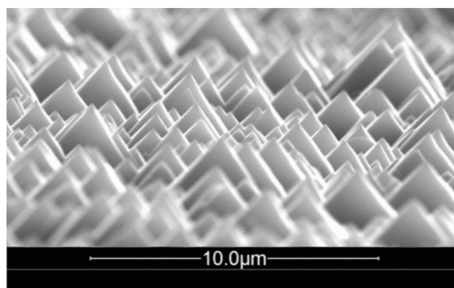


Figure 28: SEM picture of textured and oxidized sample. Magnification 5000X, Everheard Thornley detector, HV 15keV, Spot 4.0, WD 10.5 mm

after analyzing historicals is that the rounded corners of the plateau will make it difficult to see any difference between 1 and 5 s treatment.

One important conclusion from SIMS-analysis is that at 800 °C the peak concentration is not altered considerably. In this measurement it looks as if it increases, which could be explained by variations within measurements. A thin, highly doped emitter is not thermodynamically stable. Therefore quite a lot of attention has to be given the activation of the dopant in order to minimize diffusion.

An effect that has a tendency to decrease with decreasing annealing time is gettering. A 4x4 cm^2 sample was textured, oxidized and implanted to a dose of $2e14\,cm^{-3}$ at an energy of 124 keV. With an oxide thickness of 105 nm, SRIM simulations predict that the peak doping level would reside at the junction between SiO_2 and silicon. QSSPC measurements showed that the life time dropped from 3 µs for a wafer directly from the box to almost nothing after growing the "passivating" oxide. After 20 min annealing in a thoroughly cleaned tube, under N_2-gas flow at 900 °C the lifetime increased to 2 μs. After yet another 20 min gettering the lifetime increased to 4 µs. The third and forth gettering period not increase the gettering any further but killed the lifetime again.

This experiment indicates that the impurities introduced when growing a passivating oxide can to some extent be annealed out. If given enough time the ε-field from the P-gradient will gather electrically active impurities. Since single impurities have relatively high energy they will cluster, lowering the energy and therefore the overall cross section, and by that increasing the minority lifetime.

5.4 Results of SOD doping

The handling of SOD, as an alternative too ion implantation is first discussed. Measures to gain a homogenous result, and imminent pitfalls are highlighted. Relying on TCAD simulations and four point probe-measurements it is claimed that the homogeneity of the diffused P-profile is not affected by wavelets in the coating. A method for simulating SOD processing in Sentaurus TCAD has

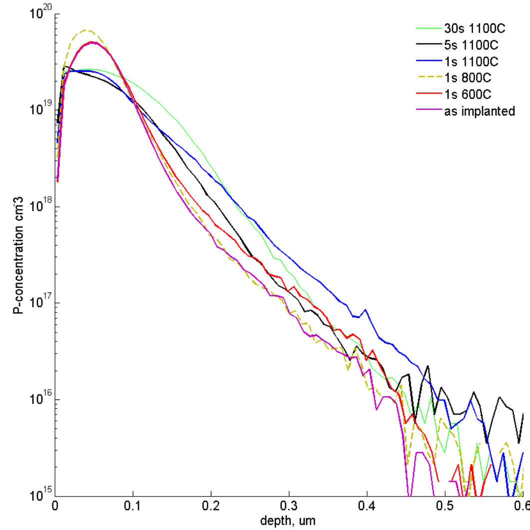


Figure 29: SIMS results of implanted and annealed samples.

been developed and is presented. The resulting emitter sheet resistance of wafers doped by SOD is thereafter presented.

SOD proved to be a reliable and handable way to fabricate the emitter. Applying and annealing SOD is much faster processing than ion implantation. Some care had to be taken not to accidentally dope the back side of the wafer, since the SOD had a tendency to wet around the edge of the sample. Textured samples were specially sensitive to this effect. The capillary effects of the texture distributed the SOD readily. In order to avoid this effect the samples were rotating on the spinner when SOD was added to the surface. Excess SOD would be wicked off, not contaminating the backside of the wafer. Further the wafer was moved directly from spinner to hotplate without any delay.

If the SOD soaked wafer was cut in several pieces they could be annealed under different circumstances investigating different concepts, such as RTP, STP, P-diffusion and thermal oxide growth.

One consideration was that different thicknesses in the SOD would result in spatially different sheet resistances. Different thickness could arise because of edge- and spinning effects. However, four point probe measurements done at different places on the same sample showed no such effects. Another concern was that even though the doping seemed spatially homogenous, there might be very small spots that are not doped to the same degree, to small too be observable with four point probe. Spinning the SOD does not cover the surface with a homogeneously flat surface, but will form small ripples stretching out from the center of the wafer, see figure 31. The concern was that the valleys

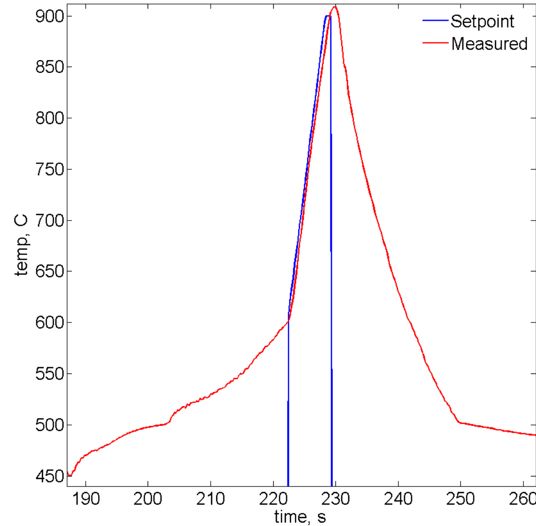


Figure 30: Temperature versus time for a RTP process with a peak plateau time of one second and a peak temperature of 900 °C. The annealing process is set to ramp up to 600 °C before peaking begins. The peak temperature i held for one second before cooling. The difference between peak time and temperature can be significant for very short annealing processes.

of these regions might not be doped to the same level as the hilltops between. The four point probe being to large to differentiate between valley and hilltop. Trying to avoid this samples, both textured and untextured, were drop coated and the surface covered by only letting the surface tension distribute the SOD, see figure 32. After drying in room temperature over night the samples were still covered by a smooth film of SOD, but upon annealing the SOD cracked up and exposed channels of bare silicon tens of micrometers wide. The conclusion was that the SOD had to be spun on, to make a thinner film. Sentaurus TCAD showed that to be able to see a difference in doping level the SOD had to be thinner than10 nm, so therefore one can rest assure that as long as there is a film covering the sample it will be homogeneously doped.

Work done by [51] reinforces this claim. Investigating two different techniques, spray coating and spin coating samples with both diluted and concentrated SOD showed that the thickness of the deposited SOD layer does not affect the doping level. Five samples were prepared, which of two were spin coated with Emulsitone solution, and two were spincoated with Filmtronics SOD. The final sample was spray coated with diluted SOD (1:4 part in volume SOD:ethanol). The spincoated samples were doped with either diluted or concentrated SOD. All samples were annealed at 900 °C for 40 s. The SIMS measurements are

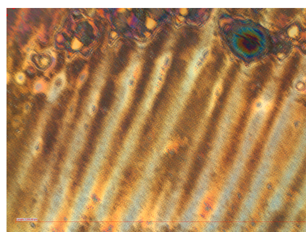


Figure 31: Spun, dried and annealed SOD on an untextured wafer. The width of the picture is 1.3 mm.

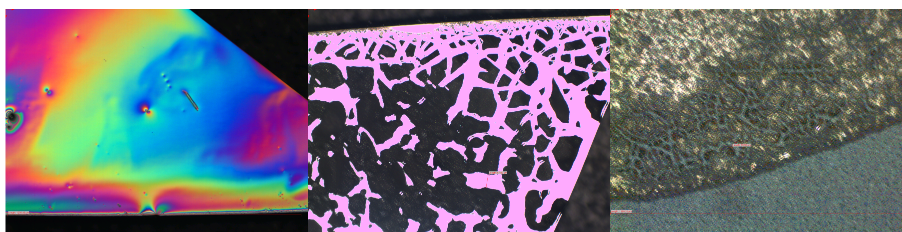


Figure 32: Dropcoated SOD. Dried over night and thereafter annealed in $990°C$ $30s$. The two pictures to the left are of the same sample, before and after thermal processing. The cracks after annealing, picture in the middle, are about half a mm wide. The right most picture is of a textured sample with the upper 2/3 covered by SOD after heat treatment. The cracks in the SOD are smaller and therefore more difficult to observe, but still large enough to leave areas undoped. If an undoped region is covered by a finger or busbar the area will short circuit the cell, i.e. a shunt. The width of the area in all three pictures is 1.3 mm.

presented in figure 33.

The depth of the emitter is a factor of great interest for solar cell production, see figure 20. P-diffusion was simulated in Sentaurus. Accurately simulating drive in by SOD required equating simulations with SIMS measurements. A method for simulating spin on diffusion of phosphorus in to silicon in Sentaurus TCAD was developed for this study, but it is not applicable to any arbitrary system. A SOD formed a glass similar to SiO_2 when annealed. Simulating depositing a highly doped SiO_2 and running the program with the oxide as SOD proved to be difficult. Phosphorus does not diffuse in SiO_2 fast enough to resemble SOD. Therefore the SiO_2 was replaced by a highly doped Si-layer. The simulations produced a diffusion profile resembling a drive in, with the characteristic kink for the change over between vacancy- and kickout dominated diffusion [19], but most noticeable was the width of the emitter. Simulations gave a far to wide emitter. SIMS-plot showed rather a restricted in diffusion impeded by the increasing difficulty for phosphorus to reach the substrate, without any obvious kink. Therefore a thinner layer of silicon was deposited, to assign for the abating phosphorus flux in to the sample. The kink effect became less obvious and the

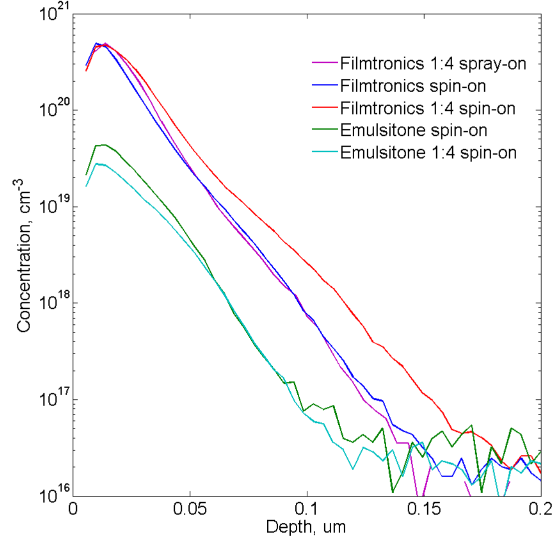


Figure 33: SIMS measurements of samples spincoated with different techniques, solution and concentrations from[51]. The most obvious result is that Filmtronics P509 gives a much higher doping level than Emulsintone. Secondly the concentration of the solution, i.e. the thickness of the deposited layer effects the doping profile less.

concentration dropped off more or less at the same rate as the measured values. SIMS measurements shows that the region closest to the surface has to some extent come to equilibrium. The concentration gradient is fairly small, meaning that even though the phosphorus concentration in the SOD is much larger no more phosphorus is dissolved in the sample. The solid solubility was assumed to be unaffected by time. Therefore the phosphorus concentration was assumed to be the same for all annealing times. The first 0.015 µm from the surface of the sample were assumed to have been saturated with phosphorus, meaning that the phosphorus concentration will start to decrease first after 0.015 µm. The SOD is described by a 0.1 µm thick silicon layer, doped to $4e20\,cm^{-3}$. The first 0.015 µm are set to a constant value., see figure 34

This method was used to initiate the simulation of emitter diffusion during growth of SiO_2. As mentioned above, thermally grown oxide was used as anti reflective coating, and possibly as passivating layer. The simulation was done for sample that was to be treated with RTP (900°C 30s) to drive in phosphorus, followed by thermal oxide growth (900 °C 90 min in O_2 atmosphere). Se figure 35. The emitter was assumed to be about 0.5 µm wide, when using a substrate doped to a concentration of $1e17\,cm^{-3}$.

Two batches a' four sample of polished CZ (100) p-type $10 - 20\,\Omega$cm silicon

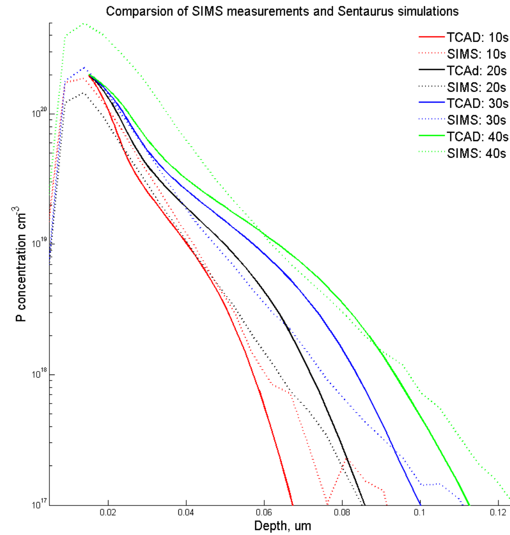


Figure 34: Plot of Sentaurus TCAD simulation and SIMS analysis of samples spraycoated with Filmtronics P509, Annealed at $900°C$ for 10, 20, 30 and 40 s. The SIMS data from [51].

wafer were spun with Emulsitone 5e20 PSOD and Filmtronics p509 SOD. The samples were dried on a hotplate and Annealed at 890, 940, 990 and 1040 °C for 30 s for one batch and the other at 950 °C for 10, 20, 30 and 40 s. The sheet resistance was measured at three different places on the wafer at three different currents. The foremost to assure homogenous doping, the latter to assure that the measurements are conducted in a linear regime. The result is presented as a plot of sheet resistance over annealing temperature or time 36. With increasing annealing temperature or time the sheet resistance declines. There are two mayor contributing factors to the reduction in sheet resistance. The doping level and the emitter thickness. The doping of the emitter will continue to increase until solid state solubility is reached. The emitter thickness will continue to grow until the SOD is depleted. The SOD was probably not depleted in these experiments, and the data over not detailed enough to resolve these to regions.

5.5 Metalization

Silver was deposited on both textured and untextured samples. For the untextured case silicon did not adhere and was washed away in the lift off process. On a textured sample the fingers could stick, if a finger width of more than 100 µm was used. The conclusion is that silver is not recommended as a front side

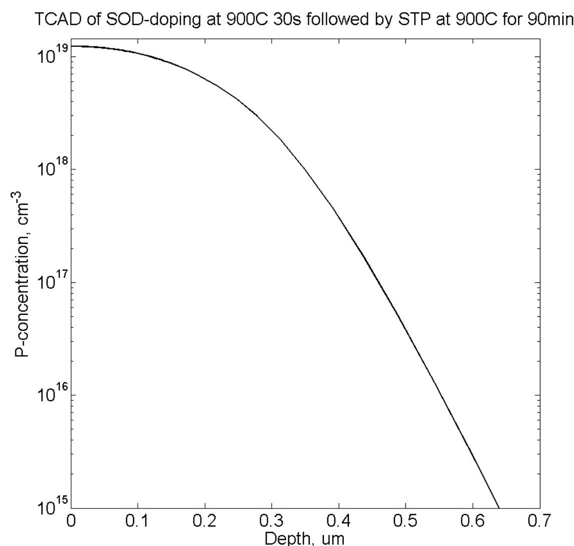


Figure 35: Sentaurus simulation of the two step process of SOD phosphorus drive in followed by thermal oxidation.

contact material for thermal evaporation deposition directly on to the sample.

The total thickness of the fingers were about 120 nm. Both fabrication technical and series resistance issues had to be considered when choosing thickness of front side contacts. On one end, a thicker front side contact would lead to better conductivity, both because of a larger cross section of the conductor, but also for bridging the valleys between texturization pyramids. A thin metal finger will drape the pyramids resulting in an effectively longer path. On the other hand, if the deposited metal is thick enough to cover the slot in the PR the solvent will not attack the PR, rendering the lift off step impossible.

The back side was coated with aluminium. After heat treatment the Al-back coating had a better mechanical bonding. IV measurements showed a good Ohmic contact. In order to test the back surface field the aluminium was etched away and the samples minority charge carrier life time was tested by QSSPC. The results were not homogenous enough to say for sure how the life time was improved by the back surface field. All four tests showed an increase in lifetime after Al-diffusion of a few μs. A problem with this approach was that there is a limited selectivity of the etch of aluminium over silicon. This fact in combination with that the edges of the samples had been in contact with the furnace tube, and therefore not been homogeneously annealed made the experiment difficult to reproduce. Never the less, all four samples did show an increase in the minority charge carrier life time.

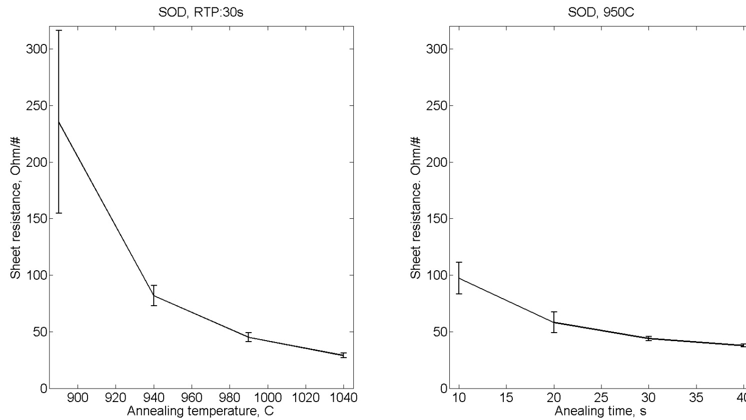


Figure 36: Sheet resistance as a function of annealing temperature to the left and as a function of annealing time to the right. The samples were untextured, spin coated with Emulsitone 5e20 SOD and annealed for 30 s, left. To the right untextured spraycoated with Filmtronics p509 and annealed at 950 °C.

5.6 Electrical characterization

Several batches of solar cells were produced with increasingly better conversion efficiency. Initially all cells were short circuited during metalization, which motivated the use of larger pieces of silicon to facilitate isolation. With out passivating layer and no anti reflective coating the the best cells had a conversion efficiency of 6 %. The IV data of a batch of three cells can be seen in figure37.

The batch shows fairly good diode characteristics in the dark, but under light the diode characteristics degrade. Ideally the IV-curve would have been shifted in to the power producing fourth quadrant of the IV diagram, while maintaing it's shape. What one can see here is that the generated current decreases faster than predicted when the forward bias is increased. The fill factor is therefore reduced significantly. The short circuit current and open circuit voltage are not affected to the same degree. In order to gain sharper diode characteristics several consideration had to be made.

The batch of tested cells were not passivated. A not passivated cell will suffer from large surface recombination rates. With increasing forward bias the space charge region will become smaller and surface effects will be more dominant. With a large ε-field the charge carriers will be effectively separated increasing the lifetime of the minority charge carriers. For a poorly passivated cell the surface recombination rate will be less dominant for lower concentrations of charge carriers. Therefore one would expect a sharper knee on the dark IV-curve, than the lighted one.

The data were fitted to both the one and the two diode model. The results are presented in table4.

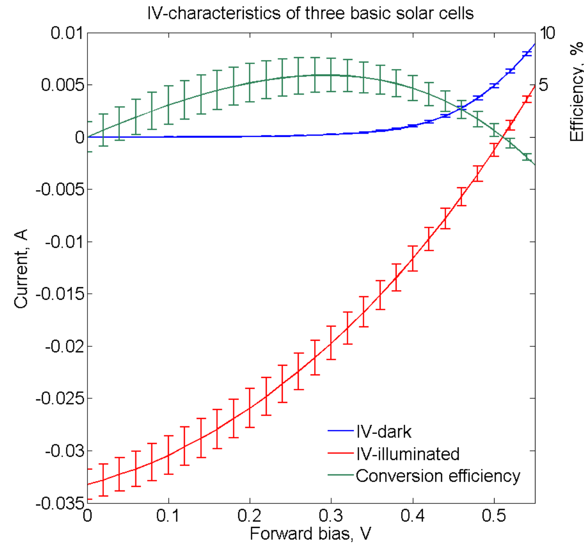


Figure 37: Electrical characteristics of fabricated solar cells. Random pyramidization, SOD, driven in at 990 °C for 30 s. 100 nm thick silver front contact, 200 nm thick back side contact. No passivating layer and no ARC. The blue line is IV-characteristics measured in dark ambient. Red line is measured under normal standard test conditions, a.m. 1.5 and room temperature. The green line is the conversion efficiency.

The closest fit for dark conditions was obtained by the two diode model while under illumination the one diode model gave a closer fit. In the first case, two obvious regions with very different recombination values were observed. The ideality factors of these regions were 2.6 and 12.0. The IV-response was also effected by shunt and series resistance. The samples shunt resistance decreased a lot when illuminated.

6 Summary

In this section the results are discussed in subsection 6.1, and concluded upon in subsection 6.2. Finally some suggestions for further work are made, see subsection 6.3.

6.1 Discussion

First in this section is the discussion regarding the processing steps. Afterwards follows the discussion of the IV-characterization results.

Ambient	R_{sh}	R_s	n	η	ff	V_{oc}	I_{sc}
Dark	$4.0e3\,\Omega$	$9.6\,\Omega$	2.6, 12.0	-	-	-	-
Light	$61.0\,\Omega$	$5.8\,\Omega$	8.3	$6.0\,\%$	0.34	0.52 V	33 mA

Table 4: Diode fit of samples annealed at 990 °C 30 s no ARC, textured. In dark condition the closest fit was $I = 2.36e{-}6{\cdot}exp\,\{14.94V\}{+}5.44e{-}5{\cdot}exp\,\{3.255V\}$, Root mean square error; $2.23e4$. Under illumination the closest fit was $I = 0.003exp\,\{4.68V\}$, root mean square error; $1.72e{-}4$. Series and shunt resistance and ideality factors were obtained from curve fittings. Conversion efficiency, V_{oc}, I_{sc} and fill factors were obtained from the IV-data.

6.1.1 Texturing

Texturing the sample with a low concentration KOH-etch at a high temperature was proven successful. The concentration of IPA in the solution was kept at a high level by periodically refilling. This method is not easily scalable, but it is not intended to be. The glass beaker might not conduct heat from the hotplate to the wafer homogeneously. Both spots or stripes of differently etched silicon might occur on the wafer, probable as an effect of 'hot spots' on the bottom of the beaker. Longer range order in the glass, such as crystal edges or one dimensional defects stretching through larger parts of the bottom of the beaker might conduct heat better than the average amorphous glass. Therefore a magnetic stirrer was suspended in a teflon basket a few cm above the wafer in the etch bath and set to a rpm fast enough to cause a flow in the etch bath that would slowly rotate the wafer. The wafer being cushioned by the constant formation of bubbles would easily rotate, leaving out eventual 'hot spots' on the bottom of the beaker.

6.1.2 Oxidation

Thermal growth SiO_2 showed to be a very sensitive step, regarding introduction of impurities. A fairly thick oxide is needed for light absorption, and therefore a long oxidation time at a high temperature. The possibility of introducing impurities is evident. For a reliable process a dedicated furnace tube is needed. It was showed that when oxidizing in a glass tube, that had been cleaned in aqua regia, the life time was enhanced, but not more than a few μs. For comparison samples passivated by HF-dipping were tested. The surface dangling bods would then be saturated by H and the lifetime would be dominated by bulk recombination, and not surface recombination. The values for those samples were much better, proving the quality of the substrate. Optically the oxide worked very well. Specially combined with texturing. SEM pictures showed that the topography of the samples were unaffected by the oxidization. The reason for that is probably a combination of the facts that all surfaces, both peaks and valleys, were predominantly oxidized at the same rate and that only a few percent of the height of a pyramid was needed to grow an oxide thick enough. In this context it might be pointed out that a grown film is not expected to alter

the surface texture, in contrast to that of a deposited film.

6.1.3 Emitter formation

Implanting a thin emitter through a 105 nm thick oxide was not feasible. The straggling was to large. In order to get a thin emitter other methods had to be implemented. One approach would be to implant the profile before oxidizing, which would be interesting as further work. In such a case the ARC would have to be applied after implantation, probably by deposition.

SOD as a dopant source for emitter formation was investigated. The conclusion is that SOD is a feasibly way of producing an emitter. The thickness of the emitter, and doping level can be engineered using different annealing conditions. In general a high temperature for a short time, with fast ramping up and down of the temperature gives a shallow, well activated and heavily doped emitter. For longer annealing times a P-gettering of impurities can be expected, just as was seen for the case of P-gettering with implanted samples, which would improve the charge carrier life time in the samples.

It was not straight forward to use SOD on textured samples. Tests were performed that indicated that pinholes in the emitter might occur when a SOD is spun on to randomly pyramidized sample. The reason for pinhole formation might be that the SOD is sucked down in to the valleys between texturization peaks by capillary force, leaving higher peaks undoped. The depletion width is not necessarily larger than the peaks are wide, which means that an undoped peak might leave a channel open from front to base. If an undoped peak is contacted be the front side metalization a small shunt will occur.

Both RTP and STP were investigated as means of electrically activating and diffusing the dopants. For STP a dedicated oven must be used, in order not to introduce life time killers. STP gives the opportunity to both grow a passivating, dry oxide, and perform a P-gettering step at the same time. RTP, on the other hand gave the possibility to drive in a thin emitter. Gettering and passivating/ARC had to be performed/added independently.

6.1.4 Metalization

The backside was successfully contacted with aluminium. A 200 nm thick layer was evaporated on to the sample. IV measurements showed a good Ohmic contact, in addition to a good mechanical contact.

For front side metalization both aluminium, silver and a stack of titanium, palladium and silver were tested. A single layer of silver would have been preferred, but it proved difficult to bond silver mechanically to the emitter. For thicker fingers (mm wide) on a textured surface the silver would stick sufficiently well. But for narrow, photographically defined fingers on both textured and non textured surfaces, the metal was washed away in the lift off step. Aluminium

would stick to the surface sufficiently well even without annealing. Heat treating the front surface would inevitable lead to a detrimental contact potential. To avoid this titanium was chosen as a contact layer. Titanium with it's 4.6 eV in work function [52] might be a little too high, for the use as an Ohmic contact to silicon which has a electron affinity of 4.05 eV [36]. One could have expected a Schottky contact if it was not for the high doping of the emitter, and as mentioned above, one of the reasons for a highly doped emitter is to make a good Ohmic contact. Calculating the width of the depletion region between the contact and the emitter one can see that the extension of the depleted region is small (nm). Therefore it is of great interest how well the metal adheres and functions together with the other metals. Palladium is added as a diffusion barrier. Last silver is deposited in a thicker layer as a conductor (100 nm). This also gives the possibility to electroplate thicker contacts. Ti-Pd-Ag would adhere very well to the surface. Lifting off µm thick films proved to be straight forward.

6.1.5 IV-characteristics

The large series resistance can be attributed to three reasons. The cells were never post annealed. Annealing at a moderate temperature for 10 min could have improved the contact adhesion and reduced the series resistance. Secondly, the method of measurement was not optimal. A large series resistance can probably rise from the way the sample was contacted when measured. The IV-response was measured using two point method, contacting the sample with narrow probes. Some further gain might be possible by depositing thicker contacts. Calculations showed that the contact thickness was not the limiting factor. But there might be a difference between theory and experiment that would call for thicker contacts.

To increase the shunt resistance several measures were taken, see section 3.4. The shunt resistance is good for a sample in dark, but deteriorates when the sample is illuminated. Apparently the general increase in conductivity when illuminated opens up for shunting. One explanation might be that the emitter contains pin holes. The base might be reaching through the emitter via narrow paths. Owing to the small cross section and poor conductivity of the base, these pinholes might not reduce the shunt resistance noticeable when not illuminated. Due to the photo conductivity of silicon the pinholes will conduct a lot better when illuminated and therefore shunt the cell.

Optical microscopy of the SOD did not reveal any pin holes. A possibility is that pinholes might form on the tops of especially high texturization pyramids, like snow caps the peak in a mountain range. Due to the natural limitations of focus depth of optical microscopy possible pin holes were not readily observed in this manner.

Curve fitting of the IV-characteristics in the dark reveled two regions with different recombination values, causing ideality factors of 2.6 and 12.0. An

ideality factor of 2.6 suggests high recombination. An ideality factor of 12.0 is very poor. For small positive biases the space charge region is wide and separates charge carriers readily. The recombination is probably mostly in edges and surfaces. For larger positive biases, when the space charge region decreases, the current deteriorates fast, and the life time of minority charge carriers becomes very small. The vast difference in recombination rate between low and high forward biases could possibly be explained by pin hole formation. The space charge region might envelope the texturization pyramid peaks when the bias is low, but increasing the bias might reveal the undoped peaks.

Under illumination the best fit was accomplished with the one diode model. The semi logarithmic plot of the current did not reveal any different regions, only a continually growing recombination current.

The scaling current found from the curve fit of the IV-data is another way of analyzing the recombination rate in the cells. The prefactor is the dark saturation current, which is the measure of the diffusion current over the potential barrier. The dark saturation current injects minority carriers in to the neighboring region, which will be lost to recombination. A small dark saturation current means low recombination values. For a sample with a high dark saturation current the diode current will cancel out the short circuit current already at a small forward bias. See table 4.

6.2 Conclusion

It has been proved that it is possible to make an unconventional and perhaps solar cell process at UiO in MiNaLab. It is not stream lined, and some adjustments have to be done, see chapter 6.3.

The uncertainty is mostly due to contamination issues. The most noticeable points are listed below:

- Particles in photo resist causing finger breakage.
- Contaminated furnaces, altering doping profiles or introducing foreign elements.
- Varying oxide growth due to inhomogeneous heating of sample in furnace tubes.
- Wafer contamination before texturization leading to areas with different texturization.

Measures have been taken against high series resistance, low shunt resistance and low life time.

Both thin emitters and wide, p-diffused emitter have been implemented and tested.

Issues concerning comparison of one concept against another have been addressed, such as effects due to convergence between sheet resistance and grid

pattern or what makes a wide but long lifetime cell better than a thin emitter one, without P-gettering step, in spite of its inherent superior quantum efficiency.

Sentaurus TCAD simulation tools has been used to model the emitter profile of the SOD process, highlighting pros and cons, and a MATLAB frame for calculating optimal finger spacing has been done.

6.3 Further work

A solar cell fabrication process is difficult to implement in a lab were other research is being done with the same equipment. In order to increase the reproducibility of the results a dedicated line is preferable. Placing all process equipment in a row and reducing the handling could potentially increase the efficiency of the cells and would definitely aid the reproducibility. A process line with very good reproducibility would make it easier to alter parameters to gain the perfect settings, knowing that nothing else affects the result.

All changes that lead to different conversion efficiency of the solar cell will call for new optimized front grid patterns. The importance of this optimizing step was discussed in the section covering front side metalization2.1. When deviating away from optimal finger spacing, due to differing sheet resistance, the overall conversion efficiency of the cell is reduced. If a batch of solar cells with a wide range of sheet resistances is made the result will be influenced by the congruity of the sheet resistance and the chosen metalization pattern. Any novel solar cell should therefore be designed and fine tuned before the finger spacing is chosen.

In this work a wafer was spin coated and thereafter broken in to a number of pieces. A more convenient path is to heat treat a whole wafer, metalized and at the very end laser scribe and cut in to small samples. The benefits are less sample handling, and that a larger number of solar cells are produced in every batch. On the other hand, one would have lost the opportunity to alter the thermal processing within the same batch.

Further deeper analysis of possible pin hole formation is a natural continuation of this work.

Part IV

Appendix

7 Attachments

This section consists of a list of keywords, the derivation of Einsteins relation, explanation of the continuity equation, the MATLAB code used for calculating optimal finger spacing, a list of settings used when simulating solar cell performance in PC1D and the TCAD code used for process simulation of emitter

formation.

7.1 Keywords

- Processing
  - RCA clean
  - KOH random pyramidization
  - Spin on dopant
  - Rapid thermal activation
  - Standard thermal processing
  - Thermal oxide
  - Front contact grid optimization
  - Metal evaporation
  - Ti, Pd, Ag stack
  - Photo lithography
- Characterization
  - IV-characterization
  - Lifetime measurements
  - Photo spectrometry
  - Secondary ion mass spectrometry
  - Four point probe
  - Ellipsometry
  - Scanning electron microscope
- Simulation
  - PC1D
  - Sentaurus TCAD

7.2 Einsteins relation

At equilibrium the general expression for hole current, see equation 8, equals zero. Solved for the ε-field gives

$$\varepsilon(x) = \frac{D_p}{\mu_p}\frac{1}{p(x)}\frac{dp(x)}{dx} \ . \tag{53}$$

Inserting $p_0 = n_i exp\left\{(E_f - E_i)/kT\right\}$ equals

$$\varepsilon(x) = \frac{D_p}{\mu_p}\frac{1}{kT}\left(\frac{dE_i}{dx} - \frac{dE_f}{dx}\right) . \tag{54}$$

Using $\varepsilon(x) = \frac{1}{q}\frac{dE_i}{dx}$ and the fact that the Fermi energy level does not change with x, the above equation can be solved for $\frac{D}{\mu}$

$$\frac{D}{\mu} = \frac{kT}{q} \tag{55}$$

which is the Einstein relation.

7.3 Continuity equation.

The continuity equation is the statement that the change in particle density must equal the flux of what goes in to a volume, minus the flux out. In addition in semiconductor physics recombination must also be calculated for.

$$\frac{dp}{dt} |_{x \to \triangle x} = \frac{\theta(x) - \theta(x + \triangle x)}{\triangle x} - \frac{\delta p}{\tau_p} , \tag{56}$$

whereθ is the flux, δp is the excess holes and τ_p is the lifetime of holes.

7.4 MATLAB code

The MATLAB code for calculating optimal finger spacing is hereby attached.

```
clear all
L=0.5; % Half the length of the finger, in cm
Xmax=800000; % integers integrated over
dl=L/ (Xmax-1); % length of one integer square, integer point along cond.
Psun=0.1; % Incident power from the sun, in W per square cm
netta=0.1; % conversion efficiency of cell
dP=Psun*dl^2*netta; % Power incoming per integration point
Vmp=0.7; % Vmp, optimal potential
dI=dP/Vmp; % integer incoming power
Rsheet=150; % Sheet resistance (change between 50,100 and 150)
RAg=1.63e-6; % Resistivity of finger metal ohm cm
ThF=1e-8; % Finger thickness in cm
Wf=5e-4; % Half the width of the fingers, cm
Prem=0; % Remaining power
X=1;
q=1;
Sfmin=1/100;
Sfmax=1/2;
dSf= (Sfmax-Sfmin)/ (60);
for Sf=Sfmin:dSf:Sfmax
Area=L* (Sf+Wf); % Area of cell integrated over.
Rcond=RAg*dl*ThF^-1*Wf; % Resistance of conductor
```

```
%————————————————————————————-
% calculating the power loss due to sheet resistance in the emitter, per
% point along the conductor.
for x=0:dl:Sf
Ploss= ( (Prem/Vmp)+dI)^2*Rsheet;
Prem=Prem+dP-Ploss;
X=X+1;
end
Psides=Prem;
X=1;
Ploss=0;
Prem=0;
%————————————————————————————-
% Calculating the power loss due to series resistance in the conductor.
for x=0:dl:L
Ploss= ( (Prem/Vmp)+ (Psides/Vmp))^2*Rcond;
Prem=Prem+Psides-Ploss;
X=X+1;
end
PowerOutPerArea (q)=Prem/ (Area*Psun*netta);
q=q+1;
Prem=0;
end
%————————————————————————————-
% Plotting the power produced of the cell as a function of finger spacing.
Sf=Sfmin:dSf:Sfmax;
plot (Sf,PowerOutPerArea)
axis ([Sfmin Sfmax 0.6 1])
xlabel ('Distance between fingers in cm')
ylabel ('Part of Power not consumed by resistive and shading losses')
title ('Rsheet=150ohm/\square, Finger width=100um, Finger thickness=1um')
PowerOutPerArea=PowerOutPerArea';
Sf=Sf';
%DS=dataset (Sf,PowerOutPerArea);
%export (DS,'file','100um_50ohmSquare.txt')
```

7.5 PC1D settings

The standard PC1D settings used when testing for different doping degrees and junction depths are listed below.

- Device area: 1 cm^2
- Front surface texture depth: 3 µm
- Exterior front reflectance: 10 %

- Base contact: 0.015 Ω
- Internal conductor: 0.3 S
- Thickness: 450 nm
- Material: .mat-file describing silicon
- Bulk end emitter doping: variated
- Bulk recombination life time: $\tau_n = \tau_p = 7.308$ µs
- Front surface recombination rate: $S_n = S_p = 1e6$ cm/s
- Back surface recombination rate: $S_n = S_p = 1e5$ cm/s
- Light source: am15g.spc, 0.1 W/cm^2
- Emitter depth: varied
- Emitter profile: error function
- Surface charge: neutral

7.6 Sentaurus TCAD

Code used for simulating emitter formation in Sentaurus TCAD.

```
\square— Declare Initial grid ——————————————
\square Note: x=0 is at anticipated top of the epi layer
line x location=0<um> tag=SubTop spacing= 0.1<nm>
line x location=0.02<um> spacing=10<nm>
line x location=0.3<um> tag=SubBottom spacing= 0.1<um>
\square— Declare substrate ————————————————
region silicon xlo=SubTop xhi=SubBottom
init concentration=1e+16<cm-3> field=Boron
\square— MGOALS settings for automatic meshing in newly generated layers -
mgoals on normal.growth.ratio=1.1 \
min.normal.size=0.1<nm> max.lateral.size=0.1<um>
\square— P-SOD——————————————————
deposit Si type=isotropic thickness=0.1<um> Phosphorus conc=4e20
grid remesh
\square— Activation ——————————————————
diffuse temperature=400<C> ramprate=50<C/s> time=10<s>
diffuse temperature=900<C> time=40<s>
diffuse temperature=900<C> ramprate=-50<C/s> time=10<s>
etch material=Si thickness=0.1<um>
grid remesh
select z=Boron layers
SetPlxList {PActive}
WritePlx PhosphorProfile.plx
```

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