UNIVERSITY OF OSLO

Department of Physics

Fabrication of SiGe/Ge core-shell nanowires by oxidation of SiGe

Master thesis

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Contents

Abstract

As Si technology is reaching its limits in solar cell and transistor applications, ways to improve these devices are being investigated. This study looks at the fabrication process of SiGe/Ge core-shell nanowires (NWs). Larger SiGe column structures can be oxidized to reduce their size and create a SiGe/Ge core-shell structure with a layer of SiO_2 on the outside.

Initially, SiGe dry oxidation was investigated in epitaxially grown SiGe films with 15% and 20% Ge, focusing on the Ge pileup region to be used as a "shell" when nanostructured. The Ge pileup region was found by RBS to have between 57 and 65% Ge for the SiGe sample with 20% Ge, and between 34 and 44% for the sample with 15% Ge. The thickness of the pileup region was found to be linearly dependent on the oxide thickness, and independent of the Ge concentration. Ge was found near the top of the SiO_2 layer in some of the oxidized SiGe samples.

Magnetron sputtering was used to get a supply of cheaper SiGe films, but these films were found to be amorphous and contaminated by oxygen. Further, the samples were patterned using photolithography, oxidized and characterized.

In addition, electrical characterization of Si nanocrystals embedded into a SiO_2 matrix, resembling the core of NW structures after longer oxidations, was done. The samples show diode characteristics, exhibiting, however, large leakage currents and poor ideality factors. CV measurements show a significant deviation from the ideal MOS capacitor.

"Worry not that no one knows of you;
seek to be worth knowing."

-Confucius

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To my colleague and girlfriend Anne - you are the greatest. I love you with all my heart, and I am eternally grateful for the love and support you keep showing me.

Frode Kløw, Oslo, May 2011

Chapter 1

Introduction

There is an increasing demand for renewable energy as the world adapts to a society with less fossil fuels. The renewable energy options are many, but photovoltaic solar cells was the fastest growing renewable technology in the world from 2000 to 2010. It still accounts for only a small amount compared to the traditional energy sources, but of the roughly 40 GW that have been installed to date, 17 GW were installed in 2010 [1].

The highest efficiency recorded of a single crystalline Si solar cell is 25% [2]. It is difficult to push this efficiency further, and for traditional solar cells the theoretical limit is 33% [3]. The third generation of solar cells uses new technology to surpass this limit. One way to increase the light absorption is with the use of nanowires. Because the surface-to-volume ratio of nanowires is high, more light is absorbed where the charges can be collected.

It is also possible to stack several solar cells on top of each other in a multijunction cell. For example, a solar cell with the three junctions a-Si, a-SiGe, and a-SiGe has achieved 10.4% [4]. It is difficult and expensive to put these materials together, but a possibly cheaper option is to have a layer with nanocrystals instead. Nanocrystals have the special property that the part of the light spectrum they absorb differs depending on their size. In the above example, the bottom a-SiGe layer has been replaced by

Si nanocrystals to achieve an efficiency of 13% [5].

When SiGe is oxidized, Si is oxidized preferentially and Ge piles up inbetween the oxide and SiGe layer. The ambition of this work is the formation of SiGe columns before oxidizing these to smaller sized SiGe/Ge core-shell nanowires. Oxidation is done on flat samples first because it is important to understand the process at a larger scale to apply it to the smaller scale.

A potential use for SiGe/Ge nanowires is to improve field-effect-transistors. The Ge shell keeps the SiGe core strained and enhances the mobility [6]. Also, if oxidized further, the original SiGe layer can be fully consumed and a core of Ge-rich SiGe will be surrounded by SiO_2. Other studies have shown that the oxidation of Ge-rich SiGe can cause the formation of Ge nanocrystals embedded in the oxide [7, 8, 9, 10], as shown in Figure 1.1. As a comparative study, Si nanocrystals embedded in a matrix of SiO_2 are electrically characterized. A layer of Ge or Si nanocrystals can be used in multijunction cells to increase the efficiency.

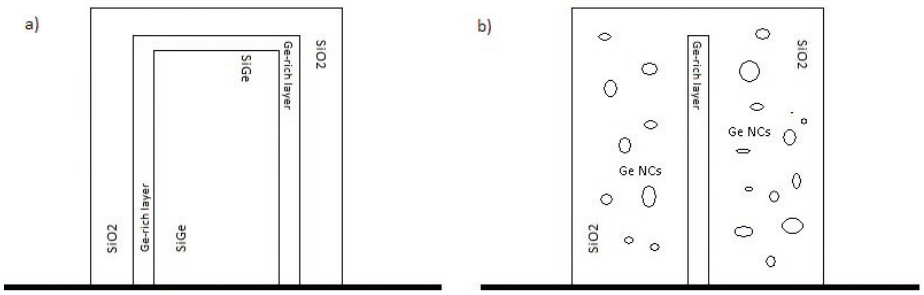


Figure 1.1: a) Schematic of a SiGe/Ge core-shell nanowire. b) After oxidation until only the Ge-rich layer remains, Ge nanocrystals can form in the SiO_2 layer.

The focus of the thesis is on the material science and the understanding of the processes involved in the experimental work. Magnetron sputtering is done to create an abundant and cheap supply of SiGe films on a Si substrate. The column structures are formed by photolithography and etching, but could be made smaller using electron beam lithography. Scanning capac-

itance microscopy is investigated as a way to characterize oxidized samples.

Chapter 2

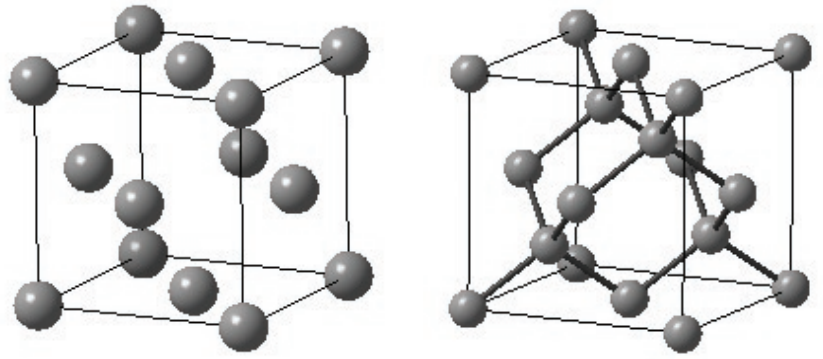
Background

This chapter gives an overview of the theory needed to understand the thesis. The first two sections are basic crystallography and semiconductor physics, and are based on the sources Understanding Solids: The Science of Materials by Tilley [11] and Introduction to Solid State Physics by Kittel [12]. After this there are two sections on semiconductor applications: solar cells and MOSFETs. The solar cell section is written based on Solid State Electronic Devices by Streetman and Banerjee [13], The Physics of Solar Cells by Nelson [3] and Solar Cells: Operating Principles, Technology and System Applications by Green [14]. The section on MOSFETs is based on Streetman [13].

2.1 Crystal Structure

Crystals are solids with a periodic arrangement of atoms or groups of atoms. This arrangement can be described by selecting one of the groups of atoms and repeating it indefinitely. Every such group can then be represented by a mathematical point, called a lattice point, which comprises a lattice. Taking symmetry into account, there are 14 possible ways of uniquely configuring the lattice points, and these configurations are called Bravais lattices. Si,

Ge and SiGe have a face-centered cubic lattice, shown in Figure 2.1(a). The crystal structure is acquired by adding atoms to each lattice point, and Si, Ge and SiGe all have the diamond cubic structure (Figure 2.1(b)).



(a) A face-centered cubic Bravais lattice.

(b) The diamond cubic structure.

Figure 2.1: The crystal structure of Si, Ge and SiGe. Created using Diamond 3.0.

With the basic repeating group of atoms you would know what to repeat, but not how. The unit cell contains the minimum amount of information to describe all the positions in a crystal. The lattice constant gives the distance between the repeating atoms, with one constant for each dimension, and the atoms themselves are represented by coordinates within the unit cell. Si, Ge and SiGe only have one lattice constant because their Bravais lattice is cubic, and thus equal in all three dimentions. For Si it is 5.431 Å, and for Ge it is 5.646 Å [15].

Whenever there is a change in the periodic arrangement of the atoms, the change is called a defect. All solids have defects because of the balance of enthalpy and entropy. A defect can appear in many ways. A point defect is a change in only one of the atoms. When an atom is absent from its normal position, the defect is a vacancy. When there is an extra atom in a non-lattice position inbetween the other atoms it is an interstitial. If this

atom is of the same kind as the atoms building the solid, the defect is called a self-interstitial. An impurity is an atom not normally belonging to the solid, either substituting another atom or staying in an interstitial position. Higher dimention defects also exist, and the most common are dislocations, grain boundaries and precipitates.

2.2 Semiconductor Theory

2.2.1 Energy Bands

Solids have various degrees of electrical conductivity and materials are divided into three groups based on this property. A metal has good conductivity, an insulator has no conductivity, and a semiconductor can only conduct when certain conditions are fulfilled. The reason for this difference is the electronic band structure of a material. When two atoms are bonded in a solid the Pauli exclusion principle forces the energy levels of the atoms to split into two parts: a bonding level and an antibonding level. When many atoms are joined, these levels turn into continuous bonding levels and continuous antibonding levels, called energy bands. The upper band is called the conduction band and the lower band is called the valence band.

The difference between metals, semiconductors and insulators is the alignment of the energy bands and thus the degree of which they are filled by electrons. When a band is filled, an electron does not have available states to move into, and there is no conduction. When a band is empty there are no electrons that can conduct. As shown in Figure 2.2, in a metal the two bands either overlap or the top band is partially filled, so that there can be conduction when an electric field is applied.

For both insulators and semiconductors there is an energy gap between the filled valence band and the unfilled conduction band. The difference between an insulator and a semiconductor is the size of the gap. When

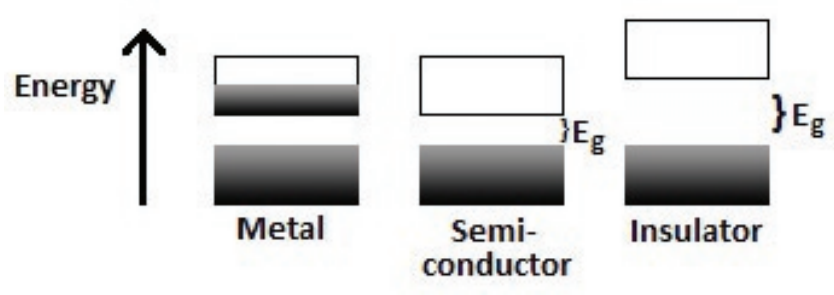


Figure 2.2: Simplified energy band structure of metals, semiconductors and insulator. For the semiconductor and insulator bands the only difference is the size of the energy gaps, E_g.

the band gap is small enough, electrons can be thermally excited from the valence band to the conduction band. Germanium and silicon have a band gap of 0.66 eV and 1.12 eV respectively [15], and are semiconductors, while diamond is an insulator with a band gap of about 5 eV. The difference is not clearly defined, however.

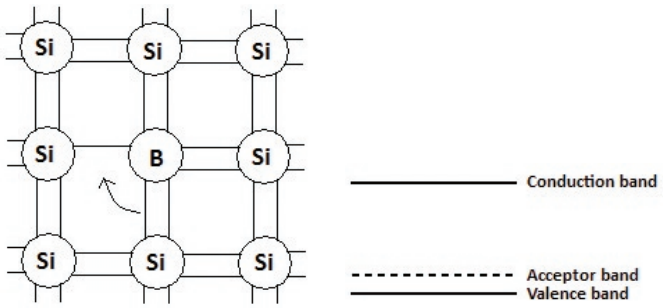
Because of asymmetry in the periodic lattice, the excitation of an electron may need extra momentum to reach the lowest point of the conduction band. This type of energy gap is called an indirect gap, and Si, Ge and SiGe are examples of this. The other type of band gap, where no extra momentum is needed, is called a direct gap.

2.2.2 Doping

To increase the conductivity in a semiconductor, foreign atoms can be introduced into the crystal by a process called doping. These atoms have generally one more or one less electron compared to the host material. The foreign atom can then easily be ionized by either losing the surplus electron to the conduction band or filling its extra hole with an electron from the valence band. The effect is that there will be more electrons and holes available for conduction.

The process can be explained using silicon as an example. Si has four valence electrons. When Si is doped with boron, B takes a place in the Si lattice. B has only three valence electrons, so the octet rule around the B atom is not fulfilled. The nearby bonding electrons can move to the available position, as shown by the arrow in Figure 2.3(a). B is called an acceptor because it can accept other electrons, and a material doped with acceptors is said to be p-doped or p-type. Because this process requires only a bit more energy, the band diagram will be as shown in Figure 2.3(b). The electrons can easily enter the new energy band, which is analogue to an electron moving into the new empty position.

When an electron is excited from the valence band it leaves an empty position. Rather than saying that there is one less electron, this position is called a hole and has a net positive charge. This hole can move around similarly to an electron in the conduction band. This can be visualized by looking at how the empty position in Figure 2.3(a) moves when an electron takes its place. The hole has moved a position, and the charge has been moved as well.



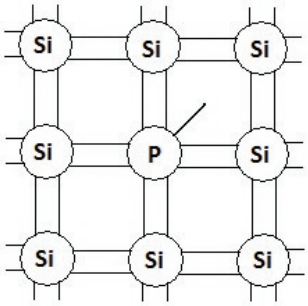
(a) Doping with B creates a hole, which can accept electrons.

(b) The acceptor band.

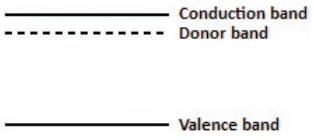
Figure 2.3: Acceptor doping of Si with B.

Similarly, when Si is doped with P, which has five valence electrons, the

extra electron is not necessary for bonding, as seen in Figure 2.4(a). It can be easily removed from its original atom to the conduction band, so that the band diagram will look as in Figure 2.4(b). P is called a donor because it gives away its electron, and this material is called n-doped or an n-type semiconductor.



(a) Doping with P gives an extra electron, which can move around more freely.



(b) The donor band.

Figure 2.4: Donor doping of Si with P.

Before doping, when the semiconductor is without any defects or impurities and is called an intrinsic semiconductor, there are as many holes p_i in the valence band as there are electrons n_i in the conduction band. At 0 K all the electrons are in the valence band and there are only empty states at higher energy levels. When the energy of the system is increased, some electrons will be excited into the conduction band, but they will always leave a hole behind. At 300 K, the number of conducting electrons in Si is 1.5 $\times$ 10^{10} cm^{-3}. It is normal to dope a material with 10^{15} - 10^{19} cm^{-3} atoms, and their electrons or holes are usually excited to the conduction band or valence band, respectively, at room temperature. This is an increase of five to nine orders of magnitude of charge carriers, which greatly increases the conductivity.

2.2.3 Fermi Level

To find the exact distribution of charge carriers it is necessary to use the Fermi-Dirac distribution, which gives the probability of an electron occupying an energy level E at thermal equilibrium

$$f(E) = \frac{1}{1 + e^{(E-E_F)/kT}} \tag{2.1}$$

where k is the Boltzmann constant and T is the temperature. E_F is called the Fermi level. At this level, when $E = E_F$, $f(E) = \frac{1}{2}$, meaning that the probability of there being an electron here, given that there are available energy levels, is exactly a half. In an intrinsic material the Fermi level is near the middle of the band gap, only altered by thermal excitations, because $p_i = n_i$.

When a material is doped there are not equal amounts of holes and electrons. The Fermi level moves close to the doping energy level because there are many more ionized donors or acceptors than there are intrinsic charge carriers. In a p-doped material the dominant charge carriers are holes, and in an n-doped material they are electrons. These are called majority carriers. The minority carriers are electrons in a p-doped material and holes in an n-doped material.

2.2.4 P-n Junction

A p-doped semiconductor and an n-doped semiconductor have a different overall energy level as shown by the Fermi level. When the two materials are brought together there is a flux of energy from the one to the other until the new material reaches energy equilibrium. The Fermi level can only have one value in a material at equilibrium, because electrons from the n-doped side will diffuse to the p-doped side and holes from the p-doped side will diffuse to the n-doped side. The electrons will leave positively charged donor ions and holes will leave negatively charged acceptor ions, which are fixed

in the lattice. These ions will create an electric field, which induces drift of charge carriers in the opposite direction to the diffusion, until there is no net charge transfer.

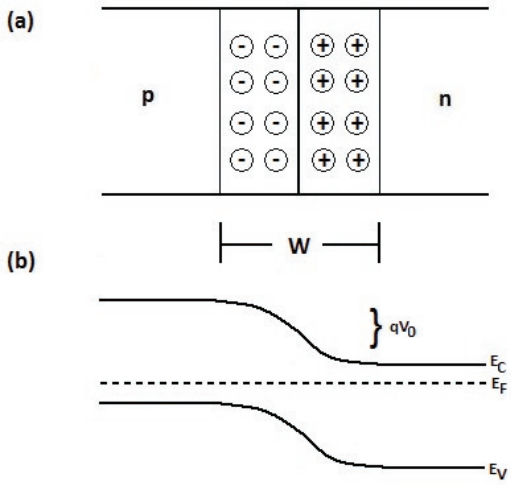


Figure 2.5: The p-n junction, showing the acceptor and donor ions (a). The schematic energy band diagram in (b) shows how the bands have changed to reach equilibrium with only one Fermi level.

The area with only ions is called the depletion region, the width of this region is called the depletion width W, and the potential difference created by the ions is called the contact potential V_0. The width of the region depends on the charge balance between the two materials. When one of the materials has a larger doping than the other, the depletion region on that side will be more narrow because there are as many charges in that small volume as there is in the larger volume on the other side.

Poisson's equation gives the gradient of the electric field as a function of the charges in the depletion region:

$$\frac{d\mathcal{E}(x)}{dx} = \frac{q}{\epsilon}(p - n + N_d^+ - N_a^+). \tag{2.2}$$

ϵ is the product of the relative dielectric constant of the semiconductor material and the dielectrical constant in vacuum, and q is the charge of an

electron. This is easier to solve without the free charge carriers p and n, and omitting these charges is called the depletion approximation. Because of this approximation, the electric field $\mathcal{E}(x)$ will be largest at the junction and linearly smaller towards zero at the edges of the junction. By assuming that all the doping atoms are ionized, the charged ions N_d^+ and N_a^+ can be replaced by the doping levels N_d and N_a, respectively. This can be written as

$$\begin{aligned} \frac{d\mathcal{E}(x)}{dx} &= \frac{q}{\epsilon} N_d \\ \frac{d\mathcal{E}(x)}{dx} &= -\frac{q}{\epsilon} N_a. \end{aligned} \tag{2.3}$$

Integrating Equations 2.3 across the respective parts of the depletion region gives the maximum value of the electric field

$$\mathcal{E}_0 = -\frac{q}{\epsilon} N_d x_{n0} = -\frac{q}{\epsilon} N_a x_{p0} \tag{2.4}$$

where x_{n0} is the part of the depletion region on the n-doped side and x_{p0} is the part of the depletion region on the p-doped side. The contact potential V_0 is the negative of the sum of all values of the electric field across the junction

$$V_0 = -\int_{-x_{p0}}^{x_{n0}} \mathcal{E}(x) dx \tag{2.5}$$

which because of the linearity of the electric field is simply

$$V_0 = -\frac{1}{2} \mathcal{E}_0 W = \frac{1}{2} \frac{q}{\epsilon} N_d x_{n0} W \tag{2.6}$$

where W is the width of the depletion region.

The total charge on each of the sides of the depletion region with a volume V is

$$q V x_{p0} N_a = q V x_{n0} N_d \tag{2.7}$$

and $W = x_{p0} + x_{n0}$, so V_0 can be rewritten as

$$V_0 = -\frac{1}{2} \frac{q}{\epsilon} \frac{N_a N_d}{N_a + N_d} W^2. \tag{2.8}$$

This gives an equation for the width of the depletion region as a function of the contact potential and the doping levels

$$W = \left[\frac{2\epsilon V_0}{q}\left(\frac{1}{N_a} + \frac{1}{N_d}\right)\right]^{1/2}. \tag{2.9}$$

2.2.5 Electrical Conduction

Electrical conduction is the movement of charged particles. The total conduction is the sum of the electrons moving in the conduction band and the holes moving in the valence band. The mobility is the ability of a charge to move when influenced by an electric field. For the conductivity σ, not only the velocity of the charges matters, but also how many charges there are. The total conductivity, with contribution from both electrons and holes, is

$$\sigma = q(n\mu_n + p\mu_p). \tag{2.10}$$

The current density is the product of the conductivity σ and the electric field $\mathcal{E}_x$ for flow in the x-direction

$$J_x = \sigma\mathcal{E}_x. \tag{2.11}$$

Several factors can affect the conductivity and mobility. Impurities and defects scatter the electrons so that the more defects there are the lower the mobility. Doping is a kind of defect, and large doping concentrations will reduce the mobility considerably. In very strong electric fields Equation 2.11 is no longer valid because the velocity of the charges saturates. This effect is increased by stronger doping and a more smaller depletion width.

2.3 Solar Cells

A solar cell converts light from the sun to electricity. The irradiance has an energy E according to its wavelength λ with the relation $E = \frac{hc}{\lambda}$, where

h is Planck's constant and c the speed of light in vacuum. This energy is transferred to an electron in the valence band, and if the energy is larger than the band gap of the material, the electron is excited into the conduction band.

2.3.1 Application of Bias on a P-n Junction

When an electron is excited to the conduction band it leaves a hole in the valence band. For this to be useful, there needs to be a mechanism for charge separation, and the solution is the p-n junction as described in Section 2.2.4. The differences in charge density between the p-type material and the n-type material causes the hole and the electron to separate.

When applying a bias to a p-n junction the potential will appear almost entirely over the depletion region because of little resistance in the neutral regions. Forward bias, which is a positive potential on the p-doped side, will decrease the potential across the junction because the positive potential counteracts the negative depletion charges there. Reverse bias, negative bias on the p-doped side, will add to the potential for the same reason.

The depletion region is dependent on the contact potential, but it is also dependent on the applied bias. Equation 2.9 can be modified for this additional component by setting the total junction voltage equal to the sum of the contact potential and the negative of the applied bias, $V_j = V_0 - V$

$$W = \left[\frac{2\epsilon V_j}{q}\left(\frac{1}{N_a} + \frac{1}{N_d}\right)\right]^{1/2}. \tag{2.12}$$

One effect of this is that the depletion width changes with the applied bias. With a forward bias the depletion width decreases, and with a reverse bias the depletion width increases. The energy difference between the p-side and the n-side is the product of the electronic charge and the total junction voltage. Thus a forward bias will cause the band separation to decrease, and a reverse bias will cause the band separation to increase.

When the potential barrier is lowered the majority carriers will more easily diffuse across the junction, but when it is raised the diffusion of the majority carriers will be smaller. The drift current is not notably changed because there are few minority carriers and they can drift to the other side regardless of the junction potential. With no applied bias the drift and the diffusion currents are equal, but opposite. The minority carriers have been generated by either light or thermal energy. With reverse bias, the generation current I_0 of these carriers will only travel in the drift direction because the barrier is too large to diffuse over. A forward bias will increase the diffusion current exponentially because of the lower barrier.

2.3.2 The Diode Equation

The total current across a p-n junction is given by the Shockley ideal diode equation, which is derived from the distribution of excess carriers found from the diffusion equation. It is derived in many text books, including Streetman [13]:

$$I = qA\left(\frac{D_p}{L_p}p_n + \frac{D_n}{L_n}n_p\right)(e^{qV/kT} - 1) \tag{2.13}$$

where the first term is abbreviated as

$$I_0 = qA\left(\frac{D_p}{L_p}p_n + \frac{D_n}{L_n}n_p\right). \tag{2.14}$$

p_n are holes on the n-side and n_p are electrons on the p-side. A is the cross-sectional area of the junction. D_p and D_n are the diffusion coefficients for holes and electrons respectively. L_p and L_n are the diffusion lengths, where $L_p \equiv \sqrt{D_p\tau_p}$, where τ_p is the average lifetime of a hole on the n-side. When V is decreasing, the exponential value approaches 0, and the negative value of I_0 corresponds to the straight line as seen in Figure 2.6. I_0 is also called the leakage current or the dark saturation current when there is no light generation of carriers.

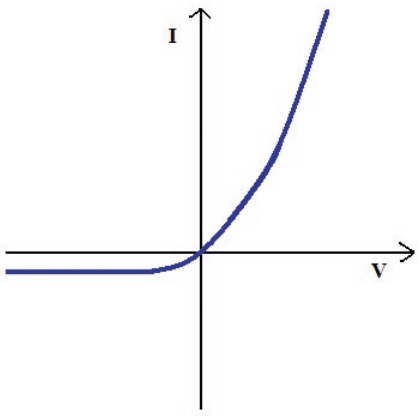


Figure 2.6: The diode equation.

Equation 2.13 consists of two parts: the injection of holes into the n-doped material and the injection of electrons into the p-doped material, giving the total current of holes and electrons. The excess carriers are calculated at the edges of the depletion region, which requires that there is no recombination within this region, and this is the depletion approximation. The excess carrier concentration will decrease exponentially once outside the depletion region because of recombination.

In real p-n junctions there can be recombination and generation within the depletion region. With a forward bias there will be charges of both types within the depletion region, and unless this region is very small, there will also be recombination. With a reverse bias the generation current I_0 can increase because of generation of charges in the depletion region. This happens only with a reverse bias because the holes and electrons would recombine in forward bias. To compensate for these recombination effects, a modified version of the diode equation is used:

$$I = I_0(e^{qV/nkT} - 1) \tag{2.15}$$

where n is the ideality factor. This factor varies between 1 and 2 depending on the amount of recombination in the depletion region and the neutral regions. There can also be a non-negligible resistance in the materials used,

so the voltage difference will not entirely be over the junction. Instead, there will be ohmic losses in the neutral regions. This causes the current to increase more slowly as a forward bias is applied. With a sufficient reverse bias the current will increase sharply due to breakdown effects.

2.3.3 Standard Design and Efficiency

The standard, simplified design of a solar cell today is shown in Figure 2.7. The light will penetrate a certain distance through the semiconductor material before most of it is absorbed. The p and n materials need to be thick enough so that all the light is used for exciting charges. Holes created in the n-type material and electrons created in the p-type material will diffuse to the junction if they are within about a diffusion length of the junction. If they are further away the charge carriers will recombine.

The p-n junction should be close to the surface of the solar cell because this is where most of the light is absorbed. Though not shown in Figure 2.7, the p-type and n-type layers can be interchanged. However, the mobility and diffusion length of minority carriers in p-doped Si is higher than in n-doped Si, so the p-doped layer is usually the thicker layer at the bottom. To improve the light absorption, solar cells have a coating of antireflective material and/or texturing. This layer will change the angle of the irradiance so that the path length increases, as will a reflective layer on the back side.

The charges need to be collected by the solar cell, so contacts are applied on the front and back surfaces. On the back surface the contacts usually cover the whole area, but the contacts on the front side are made as a compromise between resistance and shading of the sunlight. As much as 10% of the solar cell surface can be unusable due to shading from the contacts.

The output of a solar cell is measured in power $P = IV$. The maximum power output P_m can be visualized by finding the current I_m and voltage V_m that gives the maximum area in the bottom right quadrant of Figure 2.8.

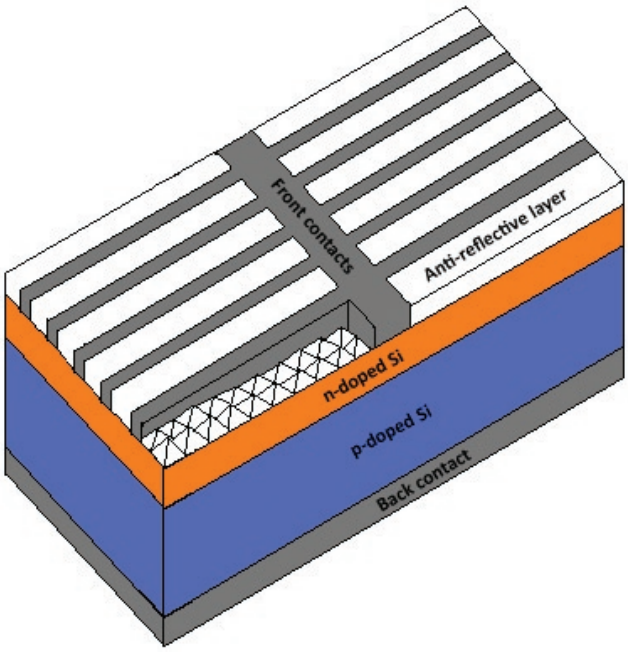


Figure 2.7: A standard solar cell design.

The more 'square' the area bounded by the graph and the axes is, the larger the power will be. This power is then $P_m = I_m V_m$. The highest theoretical power is the product of the x-axis and y-axis intercepts, which are the short circuit current I_{sc} and the open circuit voltage V_{oc}. The ratio of the real maximum power and the theoretical is called the fill factor:

$$FF = \frac{I_m V_m}{I_{sc} V_{oc}}. \tag{2.16}$$

The efficiency η is the ratio of the power out and the incident light power P_s.

$$\eta = \frac{I_m V_m}{P_s}. \tag{2.17}$$

The incident light power depends on several parameters, including time of the day, where in the world the solar cell is located, and weather conditions. Therefore, a standard value of $P_s = 1000$ Wm^{-2} is normally used when testing. The efficiency of crystalline Si cells have reached up to about 25%.

The solar spectrum consists of many different wavelengths, so the smaller

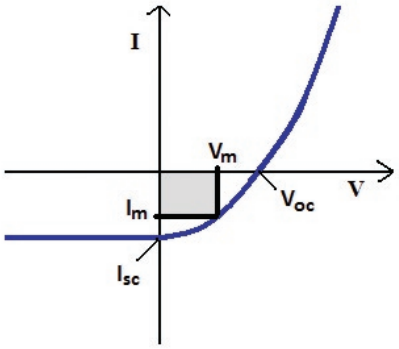


Figure 2.8: The IV-characteristics of a solar cell.

the band gap, the more irradiance is available for use. However, all energy in excess of the band gap is essentially lost as heat. One photon can only produce one electron-hole pair. Because of this, crystalline Si with a band gap of 1.1 eV has an efficiency limit of 29%. The optimal band gap is about 1.4 eV, which would have a 33% theoretical maximum. Possible ways to surpass these limits will be discussed in the next section.

2.3.4 Third Generation Solar Cells

First generation solar cells are cells based on a single p-n junction. To absorb the light, a silicon sheet needs to be about 300-500 μm thick. The second generation solar cells are thin film solar cells with low efficiencies, but considerably cheaper costs as well. The third generation improves upon the first two with more advanced effects, often based on nanotechnology.[1] These include dye-sensitized solar cells, organic polymer solar cells, hot carrier solar cells, and multi-band cells. A fifth option is to stack two p-n junctions with different band gaps, which is called a tandem solar cell. As it is not limited to two p-n junctions, the general term is multi-junction solar cells.

[1] Nanotechnology is usually defined as features at the nanoscale, below 100 nm. An additional definition is that it should have different properties than the bulk material, but this is not always used.

The advantage of a multi-junction solar cell is that a larger part of the solar spectrum can be utilized. The material with the highest band gap is placed on the top, so when a photon with insufficient energy enters this material it passes straight through. If, however, it has energy larger than the band gap of the second material, it can be absorbed there. The highest theoretical efficiency of a tandem cell with band gaps of 0.75 eV and 1.65 eV is around 56%, considerably higher than the single junction limit of 33%. For multiple junctions, the maximum efficiency is 69%.

A problem with multi-junction solar cells is that it is very difficult to match the materials used. Only a few materials are compatible because the lattice parameters need to be similar. The generated current needs to be equal for all the junctions to achieve maximum efficiency, so the thicknesses of the layers should be adjusted accordingly. Because of this they are very expensive to make. A possibly cheaper way to produce these cells is to use nanocrystals. Nanocrystals can be embedded in materials that have a good fit with commonly used semiconductor materials. The band gap of nanocrystals increases as their size decreases, and this make them an excellent choice for fine tuning the solar cell to have the band gap that works best for the complete solar cell.

The basic mechanism of the changing band gap of nanocrystals is caused by the Coloumb attraction between a hole and an electron after the electron has been excited. This electron-hole pair is called an exciton. They will feel the attractive force even at distances of several lattice parameters. When a particle is of about the same size as this force radius, the exciton can not move as freely as it otherwise could. When the particle is smaller than the exciton radius, the exciton will cease to exist. The hole and electron are forced together, and because they are interacting more strongly the separation of their energy levels increases. The effect of this is that the band gap of the nanoparticle increases as the particle gets smaller. Another

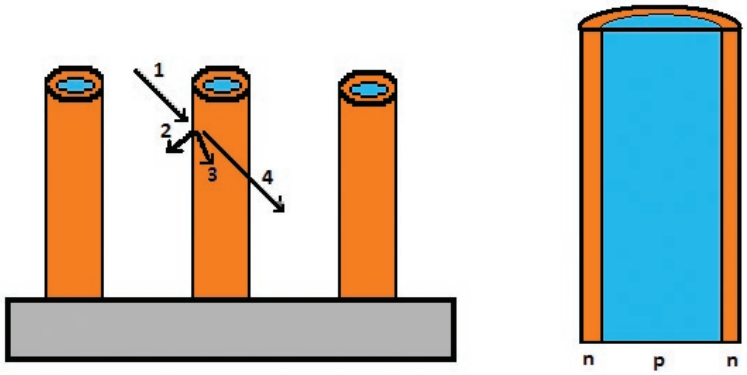


Figure 2.9: Schematic drawing of a nanowire solar cell. Possible events for the incoming light (1): reflected light (2), absorbed light (3), transmitted light (4). The core-shell structure is shown to the right.

effect is that the absorption of photons increases with decreasing particle size.

Silicon reflects about 30% of the incoming light. With the use of anti-reflective coatings this can be reduced to about 10%. Also, a Si solar cell needs to be thick enough to absorb all the light. To increase the absorption it is possible to make arrays of wires, preferably at the nano scale, as shown in Figure 2.9. One advantage of this is that the light can be reflected several times without going out of the cell. The surface area relative to the volume is increased, and the absorption will always happen near the p-n junction so that less excited charge carriers are lost to recombination.

Another advantage is that since less material is used, the solar cell can be made cheaper. The charge carriers can potentially have a shorter way to travel before being collected by contacts, and this makes possible the use of lower quality materials. A disadvantage is that the large surface area leads to a relative increase in surface effects that increases the resistance.

2.4 The MOS Structure

2.4.1 MOS Capacitor

MOS is an abbreviation for metal-oxide-semiconductor. In this structure, the top layer is a metal or a heavily doped semiconductor. The middle layer is a thin layer of oxide, and the bottom layer is a less doped semiconductor. This structure is a parallel plate capacitor with interesting properties.

A MOS capacitor works in different regimes depending on the applied bias. For this discussion the bottom layer is p-doped, but it can also be n-doped. With a negative bias at the metal layer, holes will be attracted from the p-doped material and accumulate right below the oxide. They will not pass through the nonconductive oxide unless a very large bias is applied. With a positive bias the gate will repulse the holes, leaving behind the negatively charged acceptor ions, making a depletion region.

With an applied bias, the energy bands of the semiconductor bend to accomodate for the accumulation or depletion of holes. The Fermi level in the semiconductor is constant because there is no current, but the valence and conduction bands change at the surface with the applied voltage. With a sufficient positive bias, the middle of the band gap can be below the Fermi level. This is called inversion. A measure of strong inversion is defined when the Fermi level is as much above the middle of the band gap as it is below far away from the surface of the semiconductor. At this point, electrons will be attracted to the oxide-semiconductor interface. The amount of bending ϕ_s at strong inversion is

$$\phi_s(str.inv.) = 2\frac{kT}{q} ln \frac{N_a}{n_i}. \tag{2.18}$$

The width of the depletion region is similar in a MOS capacitor as a p-n junction. However, some of the applied voltage will appear across the oxide because of the oxide capacitance. The voltage across the depletion region of

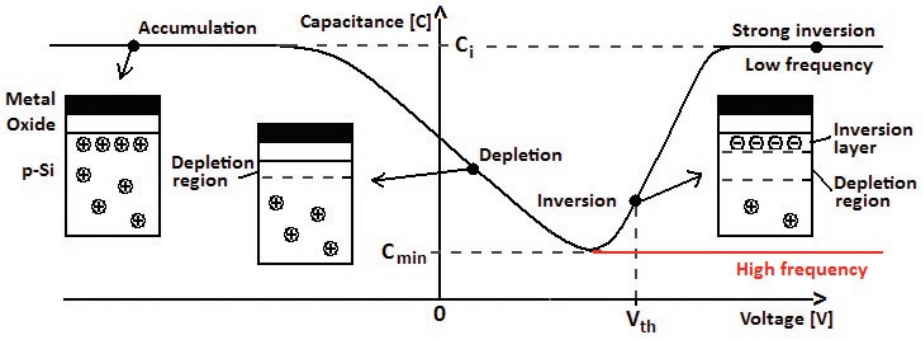


Figure 2.10: The dependence of capacitance on voltage in a MOS capacitor. Adapted from Streetman [13].

the semiconductor is ϕ_s. Equation 2.12 can then be simplified to

$$W = \left[\frac{2\epsilon_s \phi_s}{qN_a}\right]^{1/2}. \tag{2.19}$$

The maximum depletion width occurs at strong depletion $\phi_s(str.inv.)$ because from this point electrons are attracted rather than holes repulsed. Combining Equations 2.18 and 2.18 gives

$$W = 2\left[\frac{\epsilon_s kTln(N_a/n_i)}{q^2 N_a}\right]^{1/2}. \tag{2.20}$$

The total capacitance of the MOS structure is the series combination of the voltage independent oxide capacitance $C_i = \epsilon_i A/d$, and the voltage dependent capacitance from the depletion region $C_d = \epsilon_s A/W$, where the ϵ are permittivities ($\epsilon = \epsilon_r \epsilon_0$) and d and W are the oxide thickness and depletion width, respectively. The total capacitance is

$$C = \frac{C_i C_d}{C_i + C_d} \tag{2.21}$$

and its voltage dependence is shown in Figure 2.10.

In the accumulation region there is no depletion region, so only the oxide capacitance contributes to the total capacitance. With a positive bias, the holes are repulsed and a capacitance from the depletion region can be seen. When inversion occurs, electrons are attracted, and the capacitance

increases because it is not dependent on the type of charges. However, if the frequency of the AC voltage is high enough, the charges in the inversion layer do not have time to respond, and will not be measured. High frequency measurements will therefore follow the lower curve in Figure 2.10.

2.4.2 MOSFET

MOS capacitors are the basis of MOSFETs, metal-oxide-semiconductor field-effect transistors. Transistors are responsible for two of the most important functions in micro electronics: amplification and switching. Field-effect transistors are based on the principle that the circuit current will greatly increase by applying a small bias to a terminal called the gate. A MOSFET uses the channel created in the MOS capacitor structure to selectively pass a current between two contacts called source and drain.

The source and drain contacts are heavily n-doped, so the conducting charge carriers are mostly electrons. The substrate is p-doped, so when there is no bias, there is an energy barrier between the source and drain. Only in strong inversion, when electrons are attracted to the oxide-semiconductor interface, is there a channel between source and drain with good conductivity. The metal contact is called the gate because the bias applied on it controls the current passing through the channel.

The voltage required to achieve strong inversion is called the threshold voltage V_T, which is an important parameter in MOSFETs. This voltage needs to account for the voltage drop over the oxide in addition to ϕ_s. The charges in the depletion region contributes to a drop of $-\frac{Q_d}{C_i}$ over the oxide. There are also charges in the oxide. These charges can be impurities or interface states such as dangling bonds. The interface charges, which are separated from the metal by the rest of the oxide layer, change the threshold voltage by $-\frac{Q_i}{C_i}$.

There are also intrinsic energy differences between the metal and the

semiconductor that causes the bands to bend without an applied bias. These energy differences can be seen as differences in the work functions of the materials. The work function of a material is the energy required to move an electron from the Fermi level to the outside of the material. For practical purposes, the work functions used here are the energies required to move an electron from the Fermi level to the conduction band of the oxide. The work function of the metal is denoted as Φ_m, and Φ_s for the semiconductor. The bands will bend $\Phi_{ms} = \Phi_m - \Phi_s$, and thus contribute to the threshold voltage.

Combining these four effects, the threshold voltage is

$$V_T = \Phi_{ms} - \frac{Q_i}{C_i} - \frac{Q_d}{C_i} + \phi_s. \tag{2.22}$$

This parameter is important because it controls the switching of the transistor; it tells us at what gate voltage gives conduction from source to the drain. To avoid consuming power, V_T is usually optimized to be as small as possible.

Chapter 3

Previous Work

3.1 Basic Information on SiGe

SiGe has the same diamond cubic structure as Si and Ge. The lattice constant of SiGe depends on the composition of the two elements as well as other factors such as strain. The composition dependency was found by Dismukes et al. in 1964. The lattice parameter is almost linearly dependent on the composition, with a small negative deviance from linearity, Vegard's law, as seen in Figure 3.1. This work has had additional support more recently [16].

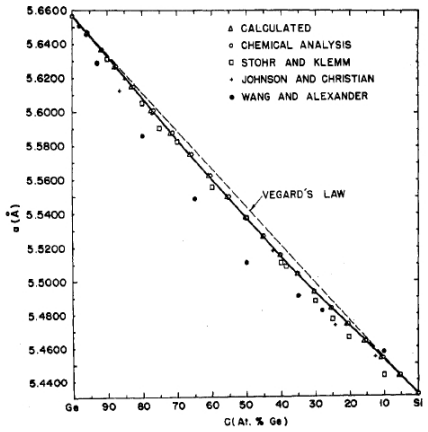


Figure 3.1: SiGe lattice parameter dependence on Ge composition, found by Dismukes et al. [17]

Si is often used as a substrate for SiGe. Because of the lattice mismatch between Si and Ge of 4% there will be strain in these layers. It also limits the thickness of the SiGe layer. This strain can be used to enhance the mobility, and is used to improve performance in MOSFET technology.

The band gap of SiGe is not linearly dependent on the composition of Si and Ge, as shown in Figure 3.2. Ge has a bandgap of 0.66 eV and Si has a bandgap of 1.12 eV [15]. For unstrained SiGe there are two regions of the bandgap, and this is because the conduction band symmetry is different for the two elements. At approximately 85% Ge, it changes from one symmetry to the other [18].

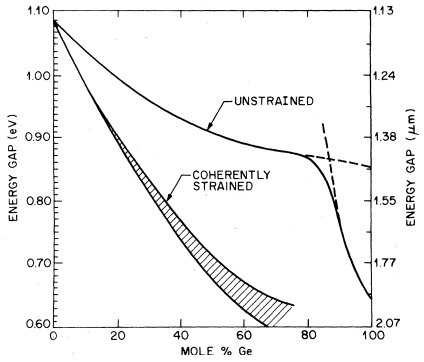


Figure 3.2: Band gap dependence on composition, determined by People [19].

Oxidation of SiGe is limited by the Si-Ge phase diagram. Si and Ge have a complete solubility. The top line in Figure 3.3, called the liquidus, limits the area where the mixture is purely a liquid. The bottom line is called the solidus, and the area it limits is where Si and Ge are both in a solid alloy. The oxidation temperature can not exceed the solidus line or the SiGe crystal will start to melt. The melting point of Ge is 938°C, and it is close to linear with the composition up to the melting point of Si at 1414°C. A substance with a higher concentration of Si can be oxidized at higher temperatures.

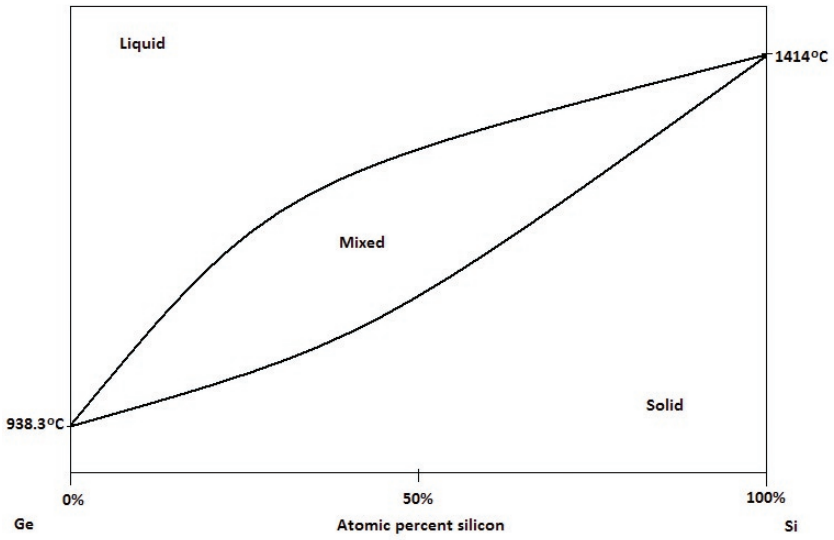


Figure 3.3: Schematic phase diagram of Ge-Si. Adapted from Campbell [20].

3.2 Previous Work on Oxidation

Si is the dominant semiconductor material today much because of SiO_2. As with Si, SiGe needs a good oxide to be used with the existing technologies, and so oxidation of SiGe has been researched at an increasing rate since the early 1970's. This is a summary of previous work focusing on the oxidation of SiGe.

Oxidation in this context is the reaction between oxygen and another substance to form an oxide, a mix of the two. The focus here is mainly on thermal oxidation of SiGe, where the reaction occurs because of high temperature. The oxidant and the oxidized species come in contact with each other because of temperature enhanced diffusion. Generally, this type of oxidation provides a good quality oxide, but is limited in processing by the high temperatures needed.

3.2.1 Si Oxidation

In 1965, Deal and Grove [21] established the theory on Si thermal oxidation. This theory is very accurate and still being used today. It is consistent with experimental results except for very thin oxides. The theory is based on the various fluxes involved. First there is a flux of oxidant to the surface of the material where it is adsorbed. Then it is transported across the already existing oxide where it reacts with the Si surface forming SiO_2.

This can be mathematically expressed with Fick's law and Henry's law, forming a system of equations with the solution

$$x^2 + Ax = B(t + \tau) \tag{3.1}$$

where x is the oxide thickness, t is the oxidation time, and A and B are experimentally determined constants. τ is a variable to deal with initial oxide thickness, and its use has been altered to account for the the enhanced growth rate of very thin oxides. There is a difference between wet and dry oxidation, and this is seen as a change in the A and B parameters. Wet oxidation of Si is generally faster than dry oxidation.

When the oxide is very thin, x^2 will be very small and can be omitted from Equation 3.1. This equation will then be reduced to

$$x = B/A(t + \tau) \tag{3.2}$$

which is a linear equation. Because the oxide is thin at this point, diffusion is fast, but the reaction rate is limiting the oxidation rate. Similarly for thick oxides, x^2 is much larger than x, so the equation will be reduced to

$$x = \sqrt{B(t + \tau)} \tag{3.3}$$

which is a parabolic equation. Diffusion is now the rate limiting process. These equations form two different regions of the oxidation, B is therefore called the parabolic rate constant and B/A is the linear rate constant.

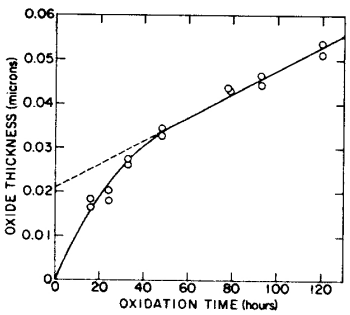


FIG. 6. Oxidation of silicon in dry oxygen at 700°C.

Figure 3.4: From Deal and Grove [21], showing the two Si oxidation regions.

Oxidation of Si has been extensively researched, but the exact mechanisms are still unknown. For an introduction to the subject, suggested reading is [22] and [23].

3.2.2 Early Research on SiGe Oxidation

The first SiGe oxidation study was done in 1972 by Margalit et al [24]. They studied wet oxidation of different samples from 4% to 37% Ge, both single crystal and polycrystalline. The samples were oxidized varying from 10 minutes to 16 hours at 1063 °C. The first time a sample was oxidized, they found no difference in the growth rate of SiO_2 compared to the oxidation of Si. When successively oxidizing the same sample with the oxide removed for each time, they found that more and more GeO_2 was formed. This was attributed to a Ge pileup at the interface between SiGe and the SiO_2. The oxidation rate was seen to increase for higher order oxidations. They also tested one of the oxidized samples in a MOS capacitor and a MOS transistor and found that the oxide was negatively charged, changing the flatband voltage. This charge was thought to be because of dangling Ge bonds. Also, the mobility was found to be low.

Not much research on SiGe oxidation was done until strained SiGe applications looked more viable in the late 1980's. In 1987, Fathy, Holland

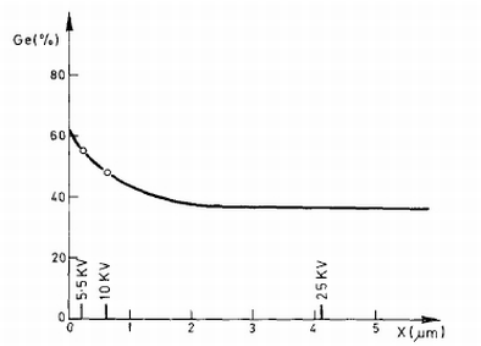


Figure 3.5: Ge pileup detected by electron microprobe analysis, from Margalit et al. [24]

and White published their results on oxidizing Ge-implanted Si [25] [26]. The oxidation was done at 900 °C in a steam ambient, and they found an increase in the growth rate when the thickness of the oxide was between 140 nm and 250 nm. They found that 140 nm corresponds to the pileup of one monolayer of Ge. They argue that the enhanced rate must be because there is an enhancement in the reaction rate; not due to damage or diffusion. This would change the A constant of Equation 3.1, and with this new A they were able to predict the oxidation rate for another experiment. They further reason that this is because the binding energy of Si-Ge is weaker than of Si-Si. Patton et al. [27] did steam oxidation of SiGe at 800 °C. An enhanced growth rate was seen for samples with 6% and 12% Ge, about 2.5 times increase in the initial 40 nm of growth. Above this the rate fell, but was steady at about 25-30% higher than oxidation of pure Si. The oxidation times were from 30 to 90 minutes. Similar results were confirmed by another group [28].

Nayak et al. did a series of experiments around 1990 with rapid thermal oxidation of strained SiGe layers. They found that there was a rate enhancement of 2-4 times when they did wet oxidation [29] at 870 °C and 960 °C, at oxidation times of only a few minutes in a rapid thermal processor. The rate enhancement was a function of Ge content. When doing dry oxidation

[30], there was no change in the growth rate compared to Si dry oxidation. Neither was the oxidation rate affected by Ge content of up to 20%. Nayak et al. also did capacitance-voltage measurements and found that a fixed negative oxide charge density in the range of 10^{11} - $10^{12}/cm^2$ and an interface trap level density of about $10^{12}/cm^2$ eV were present. With the same oxidation conditions, but a higher Ge content, both the oxide charge density and the trap level density increased.

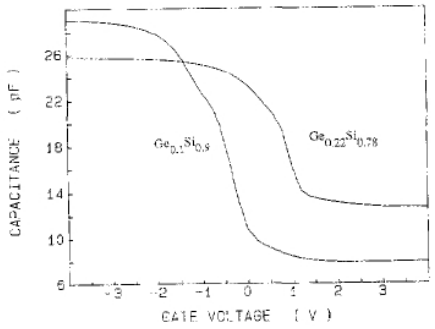


Figure 3.6: The C-V curve shifts to the right for higher Ge content, indicating a higher oxide charge density [29].

LeGoues et al. [31] [32] found that the oxide growth rate was enhanced by 3 times in wet oxidation at 800 °C. From RBS measurements they saw that the Ge was "snow-plowed" in front of the oxide. There was hardly any diffusion even for long oxidation times and pileup layers of Ge up to 500 Å thick with 75% Ge. With photoemission studies they found that the Ge had not changed at all during the oxidation, and concluded that Ge must be a catalyst for the reaction. By oxidizing a very thin SiGe layer, they showed that the breaking of the Si-Ge bonds was not the most important process for the enhanced growth rate. The 25 Å thick layer would not have provided enough Si, so the oxidation process happened mostly by breaking Si-Si bonds, and there was still an enhanced rate.

Eugène et al. [33] were the first in 1991 to do oxidation of SiGe with more than 50% Ge. They did wet oxidation at 900°C, and a sample with 25%

Ge was consistent with previous results. For their samples of 50% and 75% Ge, a two-layer oxide was formed, consisting of a mixed (Si,Ge)O_2 at the top, and SiO_2 near the SiGe interface. When the pileup is larger than the Si diffusion length the Ge will be oxidized until the pileup layer is thin enough for the Si to be oxidized again. The two high Ge content samples oxidized faster than the 25% one because the two oxides were formed simultaneously. For long oxidation times, 8 hours in this study, the oxidation rate decreased compared to oxidation of pure Si. This, they argued, is because of the eventual lack of Si. Even for this long oxidation time there is no GeO_2 in the oxidized sample with 25% Ge. Because the rate slows down, the Si will have time to diffuse even for a very thick oxide.

The conclusions drawn by Eugène et al. were supported by Liou et al. [34] using Auger depth profiling. They did dry oxidation at 880°C and found that to get a pure SiO_2 the critical Ge content was 50%. They also found (Si,Ge)O_2 as the top layer, and Ge pilup at the SiGe interface.

In summary, oxidation of SiGe is closely related to oxidation of Si, but not entirely. There is pileup of Ge, and for samples with above 50% Ge there is a mixed oxide of (Si,Ge)O_2. An enhanced growth rate is seen in the linear region for wet oxidation, about 2-4 times that in Si wet oxidation, but not for dry oxidation. For very long oxidation times the rate slows down. The reason for these effects is the interplay between kinetics and thermodynamics, i.e. the reaction rates and diffusion. The SiO_2 grown on SiGe is not of as good quality as the same oxide grown on Si; it has a high negative oxide charge density and trap density.

3.2.3 Newer Research on SiGe Oxidation

Most of the research done the last 10-15 years has focused on gaining more in-depth knowledge of the processes described in the previous section. Various experiments have been performed. One study did in situ oxidations at low

temperatures to see what happened at the transistion between pure SiO_2 and mixed $(Si,Ge)O_2$ [35]. It is found that the composition of SiGe matters on how the mixed oxide is formed, but does not matter on the formation of SiO_2. Spadafora et al. [36] studied rapid thermal dry oxidation at 1000°C of thin oxides. They conclude that the rate mechanisms of wet and dry oxidation must be the same, contrary to what had been proposed earlier. The proposed alternative is that SiGe suppresses interstitial injection, which they later show experimentally [37], as discussed in the Models section of this paper. The mechanisms of SiGe oxidation are still not clear, and there is an ongoing discussion about it.

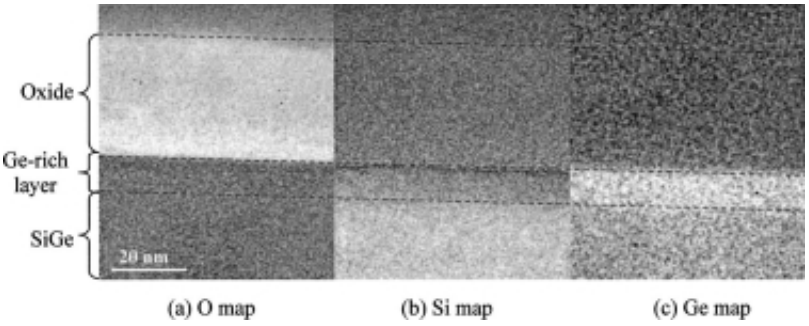


Figure 3.7: TEM images showing the Ge pileup layer [36].

In 2009, Dkhissi et al. [38] performed extensive density functional theory (DFT) calculations to confirm that oxidation of Si is more likely to happen than oxidation of Ge. In fact, oxygen will tend to position itself closer to Si when absorbed in SiGe because of a lower energy cost.

The quality of the oxide is an important issue, and the effect of the Ge pileup layer on the oxide/SiGe interface has been investigated by Ahn et al. [39] [40]. They propose a mechanism where Ge is initially bonded as Si-O-Ge, and this bond is easily broken to form Si-O- dangling bonds with a negative charge. Another study looked at stacking faults caused by relaxation of the Ge pileup layer [41].

The temperature dependence of Ge pileup and its depth profile has been

investigated. Zhang et al. [42] studied the formation of GeO_2 by oxidizing SiGe with 50% Ge at temperatures of 800°C and 1000°C. At 800°C a mixed oxide was formed, and at 1000°C a pure SiO_2 was formed. Sugiyama et al. [43] concludes that the Ge profile is strongly dependent on oxidation temperatures. At 1200°C the Ge diffuses more into the sample than it does at 1050°C, and the effect of Ge pileup is not as evident. Oxidation at 1200°C also reduces the dislocations in the sample. Tanaka et al. have done wet oxidation of SiGe in the temperature range of 625-950°C. At low temperatures there was an enhanced growth rate, but not for high temperatures. For high temperatures the Ge content at the surface is less, so there is less catalytic activity, because of diffusion into the substrate. In a middle temperature the oxidation rate only changed for Ge content less than 20%.

Rapid thermal oxidation has been done to get interesting results. One such study did dry oxidation at 1000°C of very thin SiGe layers of Ge content less than 30% [44]. They were the first to get GeO_2 into the oxide at high temperature dry oxidation for Ge content less than 50%, and GeO_2 was found in all their samples. Another study looked at the interface properties and leakage current of rapid thermal oxides [45]. When the temperature is increased, GeO_2 changes to metallic Ge and is left at the oxide/SiGe interface, degrading the oxide quality.

When a SiGe sample is oxidized for very long times, a few hours, it is possible for the oxidation to be self-limited. Shimura et al. oxidized at 1000°C, and believed the Ge-rich layer melted and provided an effective stop for Si diffusion, as shown in Figure 3.8. At 1100°C the oxidation did not stop, and from the phase diagram it can be seen that the Si concentration in the melt is four times higher for 1100°C than for 1000°C. Zhang et al. [47] also did long oxidation times, but do not agree that it is self-limited because of a melting Ge layer. Their idea is that the oxide strain increases as the thickness increases, and that this strain prevents further oxygen from

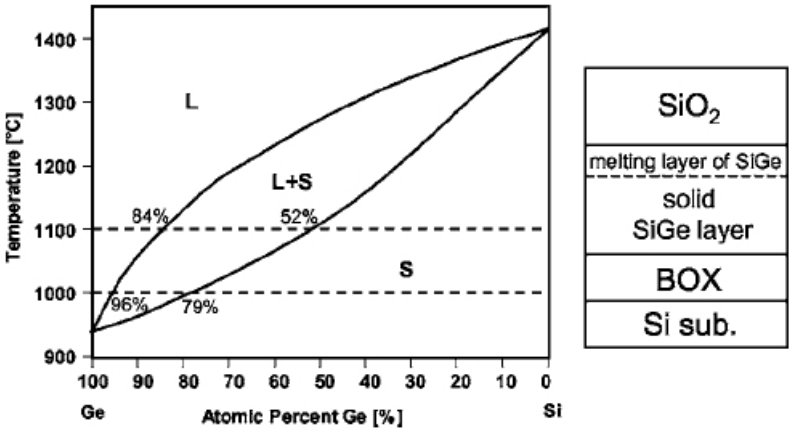


Figure 3.8: Phase diagram of Si-Ge system and a schematic drawing of the melting layer for the saturated SiGe layer, from Shimura et al. [46].

diffusing to the oxide/SiGe interface.

3.2.4 Models of SiGe Oxidation

Several models have been developed to explain and predict the oxidation of SiGe. A good model should be able to predict the thickness of the oxide, the change in growth rate, the difference in wet and dry oxidation, and the effects of the Ge pileup layer.

Srivatsa et al. [48] modelled the oxidation based on the assumption that Si-Ge bonds are easier to break than Si-Si bonds. This would lead to a change in the linear rate constant in the Deal-Grove model. They propose a change in the Deal-Grove equation (3.1) for only the part where the oxidation is enhanced

$$x^2 + A\delta + A'(x - \delta) = B(t + \tau) \tag{3.4}$$

where δ is the oxide thickness when enhanced oxidation begins.

Frey et al. [49] proposed a three step kinetic model in 1993. First Ge is rejected by the oxidation and only Si is oxidized, while a layer of Ge is formed at the interface. This ends when the Ge-rich layer reaches a critical

thickness. In the second step, there is both a Ge-rich layer and Ge in the oxide. If all of the SiGe is oxidized, the oxide will again be pure SiO_2, and only a Ge-rich layer will exist. Frey et al. used RBS measurements and calculated the critical thickness before a mixed oxide was formed. They also calculated when a mixed oxide will form when the oxide is in the parabolic rate region. They tested their results on experimental data from another group, and they concluded that the simulations fit the data very well.

Park et al. [50] found that the oxidation duration was proportional to the square of the oxide thickness when doing wet oxidation of polycrystalline SiGe at 500°C with Ge contents of 10%, 20%, 28%, and 47%, for oxidation times up to 40 hours. Their model is the Deal-Grove model with a new parabolic rate constant, for SiGe dependent on temperature. The parabolic rate constant was found for these compositions, and they also did oxidations at other low temperatures and found the activation energy of the constant.

In their model, Hellberg et al. [51] assumed that GeO_2 and SiO_2 are both formed, but GeO_2 is quickly reduced by available free Si. When there is not enough Si, GeO_2 will not be reduced and thus exist as a mixed oxide. The reaction

$$Si + GeO_2 \rightarrow SiO_2 + Ge$$

has a Gibbs free energy of -356kJ/mol O_2 at 1000 K. This model showed a good fit with experimental results from wet oxidizing two samples of 30% and 50% polycrystalline SiGe. The experimental support of this model is not enough, and there are uncertainties relating to the parameters used.

Kilpatrick et al. [52] developed a kinetic model to help predicting the oxide type resulting from a given set of growth conditions. This model is based on the balance of fluxes of Si, Ge and oxide, and is an attempt at creating a more in-depth model than the one developed by Frey et al. [49].

In 2005, Rabie et al. [53] took into account three different phenomena thought to occur during oxidation of SiGe. The first, weaker Si-Ge bonds,

is an effect that would enhance both wet and dry oxidation compared to Si oxidation. Because Si and Si-Ge dry oxidations have been found to be very similar, this effect can not be very large. The second effect is that GeO is formed at the same time as SiO_2 and reduced by free Si, unlike the idea proposed by Hellberg et al. [51] who assumed GeO_2 is formed. This effect is also the same for wet and dry oxidation.

The third effect deals with injections of intersitial Si atoms into the oxide during oxidation. This effect has been investigated in Si [54] and later also in SiGe [55]. The interstitial injections are suppressed in SiGe oxidations compared to Si oxidation, and this is possibly a rate limiting step only for wet oxidation because of the larger diffusion. Their simulations were compared to experimental data from Liu et al. [56], LeGoues et al. [32], Zhang et al. [57] and Nayak et al. [29]; a diverse pool of data. The agreement of these data is good, but still varying up to 25% on the final oxide thickness. The model is sometimes off at the intial stages of the oxidation, and sometimes at the later stages.

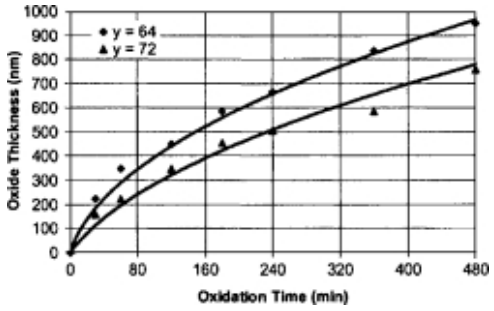


Figure 3.9: Simulation results of the Rabie et al. model compared to the measurements of Liu et al. [53]

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3.2.5 Formation of Nanowires by Oxidation

SiGe nanowires are getting more and more popular. They have a large number of potential applications, an important application being MOSFETs.

They can have a better electronic transport because there is only one dimension where the electrons are unconfined. With a gate-all-around structure, the necessary doping can be reduced and channels made of nanowires can be made shorter than the limit of today's Si technology. A review of the subject is written by Singh et al., [58] but the focus in this paper will be on nanowires created by oxidation of SiGe. A review of SiGe field effect transistors in general has been written by Xie [59].

Liow et al. [6] oxidized SiGe fin structures with widths varying from 80-650 nm with 15% Ge. The fin structures were made by lithography, after a layer of strain-relaxed SiGe had been deposited on a graded SiGe buffer layer on a Si substrate. The dry oxidation was done at 875°C to be sure the Ge did not melt. The fins consisted of a Ge-rich layer surrounding a SiGe core, as shown in Figure 3.10. The narrow fins were found to contain no dislocations.

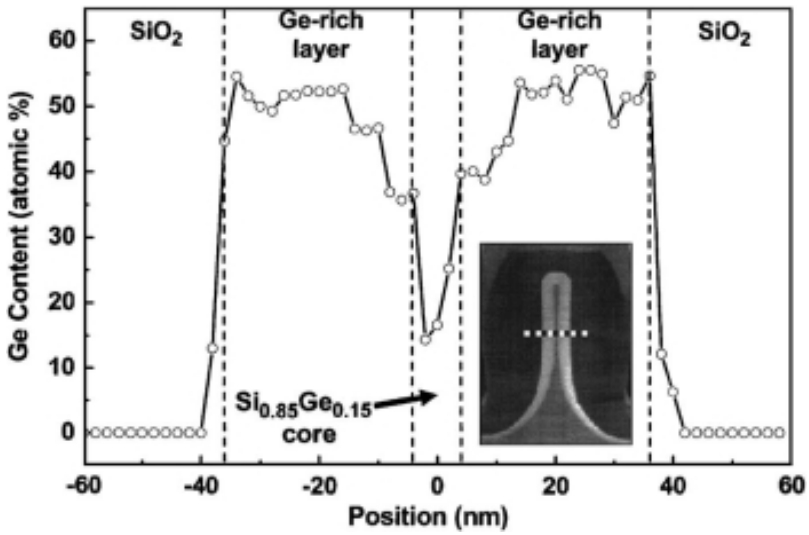

Figure 3.10: Ge concentration in a fin structure oxidized by Liow et al. [6], measured by TEM EDS.

Balakumar et al. [60] aimed to provide a better understanding of the fin structure. They made different types of structures by etching in different

conditions, before they proceeded with oxidation. The resulting Ge pileup layer had various shapes including circular, square and hexagonal, depending on the starting structure and the Ge content.

The oxidation characteristics of nanowires of SiGe with 15% Ge were investigated by Kim et al. [61]. The oxidation was similar to oxidation of thin films, except that the oxidation rate was slower for nanowires of diameter less than 150 nm because the oxidation saturated.

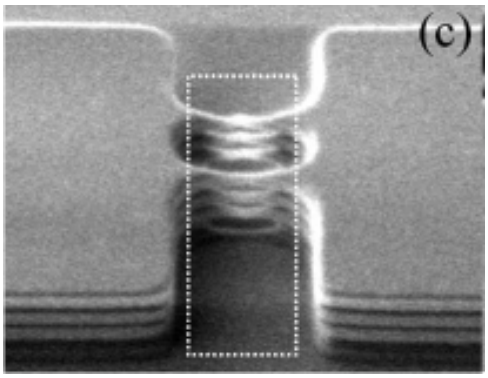

Figure 3.11: An array of stacked nanowires used as a gate in a MOSFET made by Fang et al. [62].

Fang et al. [62] were in 2007 able to fabricate nanowire arrays that are compatible with current CMOS technology. The nanowires were made by lithography and etching from alternating Si and SiGe (Ge 25%) layers. A core of Si with Ge around it was left after all SiGe had been oxidized. The finished devices, shown in Figure 3.11, displayed excellent performance.

Jiang et al. [63] made a MOSFET with SiGe source and drain regions with 30% Ge and the channel region of 70% Ge. The nanowire structures were made by lithography and etching. When they were oxidized, the source and drain were oxidized from the top, but the channel was oxidized from all four sides, decreasing its size from 40 nm to 13 nm. Their device had a drive current improvement of 4.5 times a similar device with a 30% Ge composition throughout.

3.2.6 Summary

Oxidation of SiGe is found to be similar to that of Si, but not entirely. With a low Ge content, the only oxide formed is SiO_2. It is found that when the Ge content is higher than about 50%, the oxide will contain some GeO_2, and this happens because there is not enough Si available to form only SiO_2. The most significant difference between Si oxidation and SiGe oxidation is that there is a pileup of Ge at the interface of the SiGe and SiO_2. This pileup causes problems for MOSFET devices because it relaxes the desired strain. The SiO_2/SiGe interface is not of as good quality as that of SiO_2/Si. The oxide is negatively charged and this is thought to occur because of dangling bonds. Several groups have tried to account for this by developing methods to prevent the Ge pileup.

A faster oxide growth is reported for wet oxidation of SiGe. There are several theories on why this happens. Most groups report no growth rate enhancement for dry oxidation, attributing it to the slower oxidation rate so that Si has enough time to diffuse to the surface. The more recent contributions are models using both kinetics and thermodynamics, and experiments going more in-depth to find the exact oxidation mechanisms. Also, there has been an increasing amount of research on creating SiGe nanowires by oxidation for use in MOSFETs.

Chapter 4

Experimental Techniques and Details

This chapter introduces the methodology and the experimental details of the thesis. Because one of the main focuses of this study is the experimental techniques, many of the parameters used will be discussed in the Results and Discussion chapter. Only basic parameters are given here.

Magnetron sputtering theory is written based on Campbell [20], Chapman [64] and an informatial review article by Ellmer [65]. The theory on photolithography is written based on Campell [20] and Streetman [13]. Rutherford backscattering spectrometry is written based on Chu [66]. The scanning capacitance microscopy section is written based on Brandon and Kaplan [67], as well as the other sources listed in that section.

4.1 Sample Information

4.1.1 SiGe Nanowires

Two SiGe wafers were provided by the Epitaxial Semiconductor Nanostructures group of IM2NP, UMR CNRS 6242, in Marseille, France. The wafers were epitaxially grown SiGe on p-type Si (100). The wafer named AG12 has

an 80 nm thick SiGe layer with 15% Ge content, and the AG16 wafer has a 70 nm thick SiGe layer with 20% Ge content. The wafers were cut into smaller pieces and oxidized at various temperatures and times.

For use as SiGe sputtering substrates, samples of about 1 cm^2 were cut from a p-type Si (100) wafer. As an overview, the process flow for these samples is included below.

Process flow

- 21 samples were sputtered with nine different sets of parameters using a SiGe target with 15% Ge.
- RBS characterization and thickness measurements were done on some of the samples.
- Some samples were oxidized for comparison with the epitaxially grown SiGe samples. RBS was done for these samples.
- Some samples that were not oxidized were patterned by photolithography and etched.
- Finally, oxidation and characterization by SCM was done.

In addition, three control samples that were not sputtered were also processed as a reference to the sputtering and etching.

4.1.2 Si Nanocrystals

Two samples with silicon nanocrystals (Si NCs) embedded in a SiO_2 matrix were provided by the University of Aarhus. These two samples, called VN01_3 and VN01_8, are a part of a larger group of samples [68]. Si/SiO_2 bilayers were deposited on a p-type Si substrate, doped to 20-100 $(\Omega\ cm)^{-1}$ with boron. The two samples had nanocrystals of different sizes, as given in Table 4.1.

The p-type Si substrate was doped with boron to 20-100 $(\Omega\ cm)^{-1}$, which corresponds to a doping concentration of about $1x10^{14}$-$7x10^{14}$ cm^{-3} [69]. A

Sample name	Si NC size	SiO_2 layers[1]	N[2]	SiO_2 cap[3]
VN01_3	3.4 and 5.1 nm	4.9 nm	10	3.5 nm
VN01_8	3.8 and 5.6 nm	6.0 nm	15	6 nm

Table 4.1: Size properties of the VN01_3 and VN01_8 samples. All parameters were provided by the University of Aarhus [68]. [1]SiO_2 layer thickness between Si NC layers. [2]Number of layers. [3]Capped SiO_2 layer thickness.

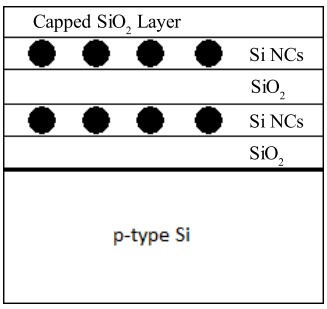

Figure 4.1: Structure of Si NC/SiO_2 samples. The number of Si NC and SiO_2 layers is given in Table 4.1.

test sample, a piece of a p-type Si wafer, was prepared together with these two samples as a reference. The process flow is included below.

Process flow

- ITO was deposited on the samples using a DC magnetron sputter.
- Photolithography and etching was done to create contacts of different sizes.
- Dark and light I-V characteristics were measured.
- C-V measurements were done.

4.2 Experimental Techniques

4.2.1 Magnetron Sputtering

Magnetron sputtering is a widely used deposition technique, which has been used to grow thin films of various compositions since the 1920's. Magnetron sputtering is a form of physical vapor deposition, where a coating material is transferred to a substrate in a vacuum chamber.

The material to be deposited is called the target and is installed at the top of the chamber as seen in Figure 4.2. Magnets positioned behind the target trap free electrons so that collisions between the electrons and the sputtering gas are frequent in the area close to the target. The sputtering gas is an inert gas, usually argon, that moves around randomly in the chamber. When the electrons and the sputtering gas collide with high enough energy, electrons are broken free from the gas so that it becomes a positively charged plasma. A negative bias is put on the target and the positively ionized gas is attracted to and collides with the target. Consequently, neutral pieces of the target are broken loose and travel in a straight line towards the substrate, which is at the other side of the chamber. This ensures that the substrate is coated atom by atom in a controlled manner. The chamber has a high vaccuum to improve the throughput and the crystal quality.

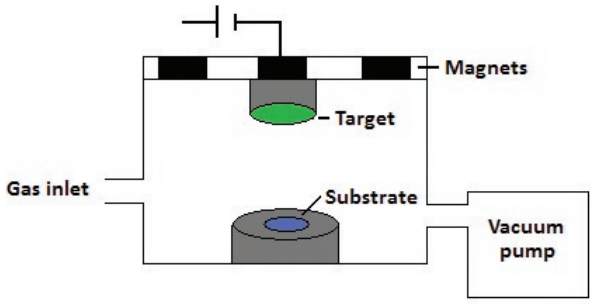

Figure 4.2: The setup of a DC magnetron sputter.

Preparations before sputtering include installing the appropriate target,

cleaning the chamber and equipment to avoid contamination, and cleaning the samples to provide an as good as possible surface. The sample cleaning was done with the standard RCA procedure which is provided in detail in Appendix B.1. A p-type silicon wafer was cut into several pieces. Aluminum foil was put on some of the samples for subsequent thickness measurements in a Veeco Dektak 8 Stylus Profiler, before they were placed on the substrate holder.

Power, temperature, type of gas, gas pressure and time are relevant parameters for sputtering. The deposition rate is approximately linearly dependent on the power and potentials involved [65]

$$R = cqP(1-\gamma)\left(1+\frac{V_p - V_{thres}}{|V_{dc}|}\right) \tag{4.1}$$

where c is a constant, P is the power, γ is the secondary electron emission coefficient, V_p is the peak applied potential, V_{thres} is a threshold voltage, and V_{dc} is the discharge voltage. The type of gas can change the deposition rate because gas molecules with higher mass will generally break lose target atoms more easily. Noble gases are preferred because they do not interact with the substrate, but it is also possible to use reactive gas molecules in a technique called reactive sputtering.

The temperature is important for controlling the growth quality of the sputtered film. When an atom or molecule from the target hits the substrate, it diffuses around until it binds with either another atom or the substrate. Two atoms are more stable on the substrate than one, and will therefore not diffuse as much. The stability increases as the clusters get larger. An increase in temperature increases the mobility of the atoms so that they have a better chance at finding such a low energy site. A low deposition rate will give the atoms time to find these sites. The proper regulation of these two parameters improves the crystal quality and makes the formation of single crystal layers more likely.

The gas pressure is an important parameter as well. There should be

enough gas atoms to sustain the plasma, but the more gas atoms there are the more the target ions collide with the gas, and the sputtering yield decreases.

Magnetron sputtering can be used in both DC and RF modes. In DC, the plasma is sustained by secondary electrons broken lose by ions hitting the cathode. In RF, electrons oscillate back and forth inside the plasma. The oscillation has a high frequency so that the ions are not affected. DC sputtering requires higher ion energies and a higher gas pressure than RF sputtering.

In this thesis, a DC magnetron sputter CVC type AST-601 system was used for sputtering indium-tin-oxide (ITO) contacts on the Si NC samples[1].

The RF system used for SiGe sputtering was a SC Tri-Axis Batch Sputtering System provided by Angstrom Sciencies. It is equipped with three indirect cooled 3 inch wide cathodes, and has a balanced magnetron field. The target used for SiGe sputtering has a Ge content of 15% and a stated purity of 99.99%.

4.2.2 Photolithography

Photolithography is a technique used to define a pattern on a material. Very briefly, photolithography includes three steps: Adding a light sensitive material on top of the sample called a photoresist, shining light on this material through a mask to change the chemical state of certain areas, and finally removing the least stable areas with a developer. These steps are shown in Figure 4.3. When this is done there is a pattern of stable photoresist that can be used for other processes like etching, doping implantation or contact deposition. This makes photolithography a very useful technique, but it

[1]The deposition of ITO contacts on the Si NC samples was done as a summer job, and should not be counted towards work on this master thesis. However, DC sputtering was also done on a reference sample, which was a part of the thesis.

is also a very critical step in microelectronic fabrication because it is both complicated and expensive.

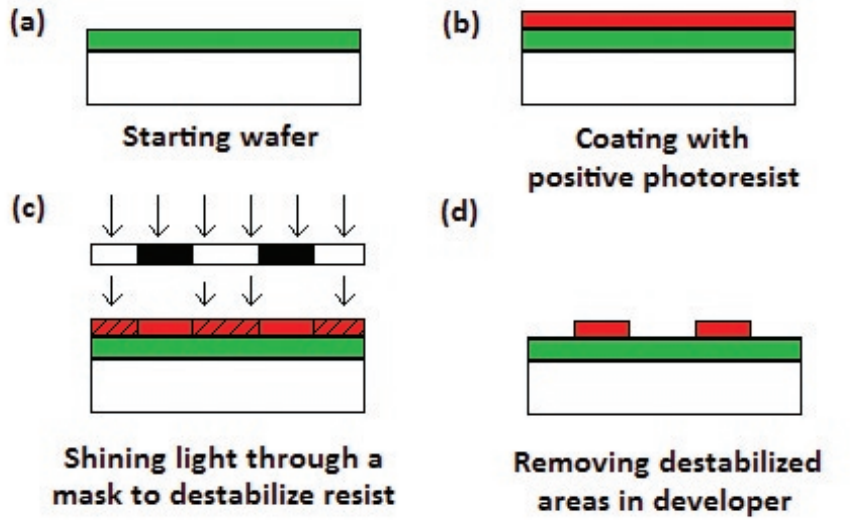

Figure 4.3: A lithography process using positive photoresist.

A general cleaning is done in acetone for 30 seconds, then a bubble rinse for another 30 seconds. After this, the sample is dry baked at 110°C for 10 minutes. The next step is to put a layer of photoresist on the sample. Depending on what pattern is wanted, it is possible to use either positive or negative resist. Positive resist is stable, but will become unstable when exposed, so that the transparent part of the mask is what will disappear. Negative resist is unstable and becomes more stable when exposed, so that the resist under the opaque pattern of the mask will be removed. A positive resist of the type Microposit S1813 was used in this work. The sample is coated with the resist before putting it in a spinner. The spinner creates a uniform layer, and was set to rotate at 3500 rounds per minute for 30 seconds. The sample is heated, called a soft bake, for five minutes at 95°C for better adhesion.

The mask that is used is simply a transparent plate with a pattern that

is opaque to light. Because there is always ambient light in the room where photolithography is used, the light used to expose the photoresist is UV-light, and to protect against accidental exposure the light in the working room is yellow. It is important that the mask is very transparent at the exposure wavelength, and to be precise it should not scatter the light. The exposure tool was a Karl Suss Mask Aligner.

When exposure is done, the sample is put into a solution called a developer that removes the unstable parts of the resist. The developer used was Microposit 351. After this, the sample is hard baked at 120°C to better hold the resist that is left.

The underlying layer is then ready to be etched or otherwise changed. After the etch, the rest of the photoresist can be removed and the process is done.

4.2.3 Oxidation

The theory on oxidation is presented in the chapter on Previous Work (3.2). Thermal dry oxidation was done in a Heraeus D6450 Hanau oven, model ROF 10/100. The oxygen flow was set to a value of 3-4 with arbitrary units, but which should provide a sufficient oxygen flow. Oxidation was done in collaboration with University of Oslo (UiO) PhD student Ethan Long, for a multitude of different temperatures and times.

4.3 Characterization Techniques

4.3.1 X-Ray Diffraction

X-ray diffraction (XRD) is based on the principle that irradiation will be reflected by crystal planes. A constructive interference between the reflected rays occurs when the distance they travel is proportional to their wavelength. The geometry in this system is changed by the distance between these planes,

the irradiation wavelength, and the angle at which the irradiation travels between the planes. In XRD, the wavelength and the distances between the planes are constant, but the angle is changed. The constructive interference is imaged as intensity peaks versus the measurement angle.

The XRD system used was a Bruker D8 Discover with a Lynx-Eye detector which has a resolution of $d\theta = 0.014°$. A Goebel Mirror was used to get Cu $K_{\alpha 1}$ rays with a wavelength of 1.5406 nm. This technique had a minor role in the characterization of samples.

4.3.2 Rutherford Backscattering Spectrometry

The Rutherford backscattering spectrometry (RBS) system used in this thesis is located at the Ångström Lab of Uppsala University, Sweden. It uses a 5 MV Pelletron Tandem Accelerator from National Electrostatics Corporation and a surface barrier Si detector from ORTEC. Measurements were done by UiO researcher Alexander Azarov, and were done with 2 MeV $^4He^+$ ions backscattered into the detector at 100° for the epitaxially grown samples and 170° for the sputtered samples.

4.3.2.1 Overview

RBS is an analysis technique that relies on the backscattering of a projectile when hitting a target. The projectiles are most often alpha particles (^{4}He nuclei), which are accelerated onto the target. If the target sample is thin, most of these particles will go straight through the target, but some will be reflected. Those who are reflected back out of the target are said to be backscattered, and are the particles detected in the RBS. The particles enter a detector which amplifies the signal and outputs the data in the form of an energy spectrum, hence the name backscattering spectrometry.

The backscattering spectrometry equipment has four parts: the beam, the target, the detector and the vacuum pump. The vacuum should be

about 10^{-5}-10^{-6} Torr, which is a moderately low requirement. From the backscattering spectrum one can get a quantitive measurement of the depth distribution of atomic species. It is fast and there is no need to calibrate the equipment with a reference sample. It can destroy structures sensitive to a small dose of irradiation like a p-n junction, but except for this it is a nondestructive technique. Also, for single-crystal samples channeling can give a measure of crystalline perfection.

However, RBS does not measure the surface of the sample, and it is difficult to detect light elements. Light elements will not scatter as effectively as heavy elements, and are therefore more difficult to detect. The energy of the scattered particle is dependent on the atom it was scattered by and the depth from where it was scattered, and these two parts of the spectrum can overlap for elements of similar mass. RBS is not as sensitive as other techniques such as SIMS, and it is also dependent on a relatively smooth surface. If surface artifacts such as scratches and dust particles are present in sufficient amounts, they can modify the spectrum.

4.3.2.2 Physical Concepts

When the projectile atom collides with an atom in the sample, the collision is assumed to be simple elastic. For the collision to be simple elastic the energy of the incoming particle needs to be much bigger than the binding energy of the sample atom. The energy should not be so large that there are nuclear reactions or resonances. When these two conditions are satisfied, it is possible to calculate the ratio of the incoming energy of the particle and the outgoing energy, based on the mass of the atom it collides with and the scattering angle. This ratio is called the kinematic factor K.

The significance of the kinematic factor can be understood when looking at a simple spectrum. The highest energy part of the graph for an element will be positioned at KE_0, where E_0 is the incoming particle energy. This

can then be used to identify the elements in the sample. The highest energy ledge is at the surface of the sample, and further into the sample the projectile will gradually lose energy.

The yield of scattering from each mass is determined by the scattering cross section σ. The total number of detected particles A is

$$A = \sigma\Omega \cdot Q \cdot Nt \tag{4.2}$$

where Ω is the angle of the detector opening relative to the sample. Q is the total number of particles hitting the target, Nt is the number of target atoms per unit area. σ depends on the square of the atomic numbers of the incoming particle and the target atom, and the inverse of the incoming energy squared. More scattering occurs with heavier incoming particles and target atoms, and with a smaller incoming energy. The scattering yield also depends on the scattering angle, but does not change much near 180°, where most detectors are located. σ is known for a lot of elements, so Equation 4.2 can be used to find the number of atoms per area in a sample.

Because the scattering cross section depends on the incoming projectile energy, the yield will change as the projectile proceeds further into the sample. The projectile will lose an energy dE/dx as it passes through electron clouds of atoms or collides with nuclei. The ratio of the energy loss and the density of the sample is called the stopping cross section ϵ, and is defined as

$$\epsilon \equiv (1/N)(dE/dx) \tag{4.3}$$

where N is the atom density of the target. For compound targets, the stopping cross section can be added for each of the constituent atoms. This is because the projectile particle will only interact with one atom at a time, and this is known as Bragg's rule. In reality, a particle will lose a different amount of energy for each pass through a target. These fluctuations are called energy straggling and limit the resolution of the spectrum.

Rearranging Equation 4.3 gives

$$dx = dE/\epsilon N. \tag{4.4}$$

Therefore, when calculating the thickness of a layer in a sample, it is enough to know the energy change from the surface to the bottom of the layer, the atomic density and the stopping cross section. The energy change can be seen from the spectrum, and the stopping cross section can be found for most elements when using ^{4}He projectiles, and the density is often known.

4.3.2.3 Simulation of RBS Spectra

Simulation of the RBS spectra is done using the simulation software SIMNRA 6.05 [70], which has been created by Matej Mayer at the Max-Planck-Institut für Plasmaphysik in Germany, and can be found at `http://www.rzg.mpg.de/~mam/`. The program uses a collection of stopping cross section data to estimate the energy loss of the incident ion beam.

The setup parameters that should be known before doing the simulation are: the projectile ion and its incident energy, the incident angle, the exit angle and the scattering angle. Energy calibration of the axes and setting the target parameters can be done to make the simulation fit the spectra.

The target can be calibrated with informative assumptions. SIMNRA uses the composition and the thickness of the target layers. Often the composition is known and the thickness is adjusted to fit the spectrum. The thicknesses are entered in atoms/cm^2, which means the density of each layer (atoms/cm^3) should be known to give the equation

$$atoms/cm^2 = cm \times atoms/cm^3. \tag{4.5}$$

The substrate layer can be set to an arbitrarily large number, but can be adjusted to fit the spectrum. There is a lot of noise at the lowest energies because the backscattered particles are more easily diverted with low energies.

The mass density of Si is 2.32 g/cm^3, which gives an atomic density $\rho(Si)$ of 4.97 $\times$ 10^{22} atoms/cm^3. Ge has a mass density of 5.32 g/cm^3, corresponding to a $\rho(Ge)$ of 4.41 $\times$ 10^{22} atoms/cm^3 [13]. Dismukes et al. [17] have found the density of SiGe for a wide range of compositions, as shown in Figure 4.4. Linear interpolation is done to get values between the experimentally determined data points.

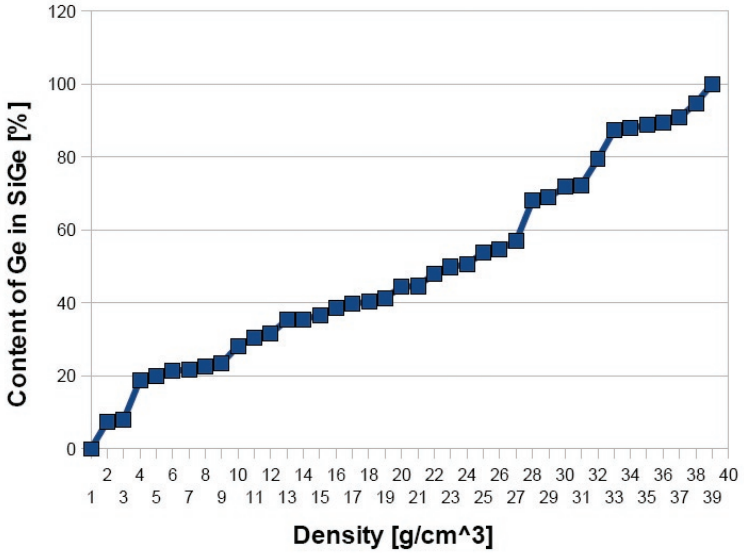

Figure 4.4: Density of SiGe for different Ge contents, found by Dismukes et al. [17].

4.3.3 Scanning Capacitance Microscopy

Scanning capacitance microscopy (SCM) is a form of scanning probe microscopy (SPM), where a tip attached to a cantilever resonates at a certain frequency. The tip is brought into close proximity with the sample, and the electric forces felt by the tip changes the frequency of the cantilever oscillation. This frequency produces an output voltage that is turned into an image or spectrum as the probe is scanned over the sample [71]. The resolution of SPM is mostly limited by the probe radius, so it is important

that the probe is sharp. Data collection is slow compared to the scanning electron microscopes and transmission electron microscopes because only one data point is recorded at a time [67].

In SCM, a thin insulating layer is needed between the tip and the semiconductor or metal sample. As a simple approximation, the SCM tip and the sample can be modeled as a MOS capacitor [71]. The tip will cause either accumulation, depletion or inversion in the semiconductor depending on the voltage used. The tip measures the capacitance changes as the voltage is changed, and outputs the dC/dV-V characteristics of the sample.

The SCM can make good topographical images and is a non-destructive technique, but it is not widely used. It is a technique sensitive to small changes, and there can also be hysteresis effects because of surface charges [71]. Work on understanding theory behind the charge distribution caused by the tip, and getting more quantitative information has been done [72, 73], and is still ongoing.

The resolution is limited by the angle of the cone shaped or pyramid shaped probes. The probes used in this study have a front angle of 25° and a back angle of 15°. By tilting the probe it is possible to use one side of the probe to measure step angles approaching 90°. This makes the angle measurements of the opposite side worse, but it can be remedied by scanning back and forth across the sample.

SCM can also be used for features smaller than its spatial resolution. It can not be considered a parallel plate capacitor in this case because the tip is not flat and will experience forces from the sides. Nevertheless, the SCM probe will cause accumulation and depletion of charges in the sample, which causes a screening effect. The use of SCM to characterize nanocrystals and nanowires has been investigated by Ruda and Shik [74].

The SCM used in this thesis was an atomic force microscope (AFM) run in SCM mode. It simultaneously outputs a topographical image based on

the AFM function and an electrical image based on the SCM function. The system was a NanoScope Dimension 3100 SPM from Digital Instruments Veeco Metrology Group, with NanoScope 5.3 software. The probes used are Bruker SCM-PIC with a Pt/Ir coating. They have a working height of 10-15 μm above the sample, and the nominal tip radius is 20 nm.

4.3.4 Electrical Characterization

The Si NCs were electrically characterized. Both the dark and light I-V characteristics were measured using a Keithley 6487 Picoammeter/Voltage Source. Silver paste was applied to the back side of the samples to provide a better contact, and a needle was used to connect the front contacts. For light simulations, a solar Newport 91193-1000 Large Area Light Source with an AM1.5 filter at 1000 W/m^2 was used.

For C-V measurements an Agilent 4284A Precision LCR Meter (20 Hz - 1 MHz) was used. The software used to record both I-V and C-V measurements was LabVIEW 7.1 by National Instruments.

Chapter 5

Results and Discussion

5.1 Sputter Deposition

The goal of the sputtering was to make SiGe films cheaply as an alternative to the more expensive, epitaxially grown films. Oxidation experiments depend on a sufficient supply of substrates to test a range of parameters.

The SiGe target had a Ge content of 15%. Several studies have been made to find the sputtering yield of SiGe, and its composition dependence [75, 76, 77]. The sputtering yield is not linearly dependent on the composition, but rather follows an S-curve; dipping below linearity for low to medium Ge content and going above linearity for medium to high Ge content. The deposited film composition is affected by Si being lighter than Ge, but Ge has a lower surface binding energy than Si. These two parameters compensate for each other, and there is only a small change in the final compensation [77]. This has been done experimentally, and one study started with a $Si_{0.8}Ge_{0.2}$ target and measured about 25% Ge in the sputtered film [78].

The sputtering parameters were varied to investigate potensial quality differences. To keep the thickness of the sputtered layer constant, the sputtering time was changed inversely with sputtering power. Aluminum foil

was put on a sample in each of the depositions for thickness measurements with a profilometer.

5.1.1 Experimental Details

Depositions were done using parameters listed in Table 5.1. The gas flow, and thus the working pressure, was changed because of events described below. The power was varied to see if this mattered for the quality of the SiGe film. The substrate temperatures of 500°C, 600°C and 650°C were chosen to give a good crystalline quality. There is not much literature on SiGe sputtering, but polycrystalline films have been made by Nakamura et al. [79]. They did RF magnetron sputtering at 500°C and 600°C, and saw a clear improvement in crystallinity of the 600°C deposition. They were also able to get polycrystalline samples at 400°C with the addition of H_2 gas. This gas is believed to create radicals that enhance the crystallization process.

Samples	**Temperature** [°C]	**Power** [W]	**Pressure** [mTorr]
A1, A2	500	100	7.5
A3, A4	500	150	20.6
A5, A6	600	100	14.4
A7, A9	600	150	20.5
A8, A10	650	100	20.5
A11, A12	650	150	20.4

Table 5.1: Parameters used for sputtering, set 1. Three different working pressures were used for the A3 and A4 samples.

Samples A3 and A4 were sputtered with several different parameters because of problems with the plasma. During the presputtering of these samples, the working bias suddenly went from 363 V to 5 V and the plasma

turned off. Another attempt was made, but after 10 minutes of presputtering and 2 minutes of deposition the plasma turned off again.

The problem is likely to be because the plasma is not sustained by the gas flow at high temperatures. Therefore, for the A3 and A4 samples the gas flow was increased from 30 to 60 standard cm^3/minute, giving a working pressure of 14.4 mTorr. There were still problems with the plasma, so a working pressure of 20.6 mTorr was used. The samples A5 and A6 were sputtered inbetween these changes, and were successfully processed at 14.4 mTorr. A possible reason it worked for these samples is the increase in power, which would help sustain the plasma. The rest of the samples were done at about 20.5 mTorr for an attempt at consistency.

For the second set of sputtering depositions, listed in Table 5.2, it was decided to do the sputtering at room temperature and instead consider other crystallization options such as annealing. Tajima et al. [78] sputtered with a $Si_{0.8}Ge_{0.2}$ target at 200°C, and annealed at 850°C and 950°C. Both annealings produced crystalline samples, but the 950°C annealing was of better crystalline quality. An Ar gas flow was used to supress oxidation of the sample during annealing. Another option is annealing at lower temperatures for longer times. Jelenkovic and Tong [80] annealed sputtered SiGe films at 550°C from 24 to 120 hours to get crystallization. There was a small redistribution of Ge in this experiment, but no pileup region of Ge was found. Annealing equipment that would not oxidize the samples was not available for use in this study, but this seems a viable option for making crystalline SiGe films with sputtering deposition.

Samples	Temperature [°C]	Power [W]	Pressure [mTorr]
B1, B2, B3	20	100	20.4
B4, B5, B6	20	150	20.4
B7, B8, B9	20	125	20.5

Table 5.2: Parameters used for sputtering, set 2.

5.1.2 Results and Discussion

XRD was used to find the crystalline quality of the sputtered films. Sample A12 was the most likely to be crystalline because of the high sputtering temperature used. A θ-2θ scan of 2θ angles from 20° - 90° was done and is shown in Figure 5.1. The strongest peak is seen at 69.19°, and this is the Si (004) peak. Another peak is seen at 32.98°. This peak has previously been identified as corresponding to the forbidden Si (002)-plane [81].

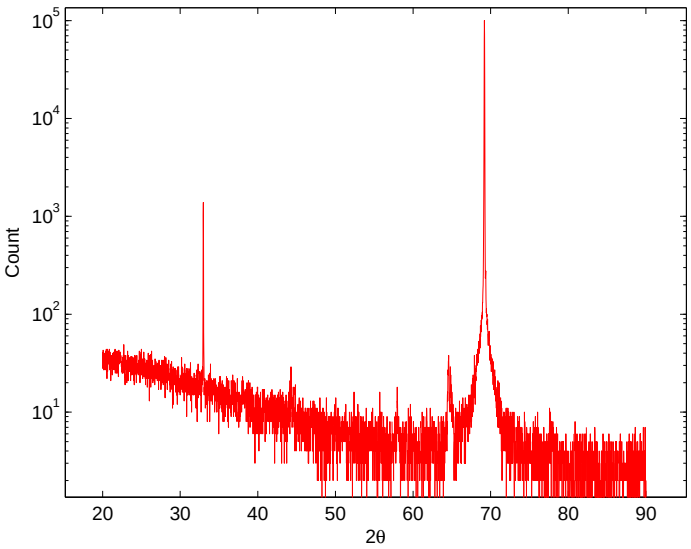

Figure 5.1: A Locked Coupled θ-2θ scan of sample A12. The 32.98° peak and the 69.19° peak are Si (002) and Si (004), respectively.

No Ge peaks were seen in this spectrum. The smaller peaks that can be seen in Figure 5.1 are too small to be distinguished from the noise. For example, the peak at 64.59° has a count of 38. To investigate this further, gracing incidence XRD was done. Gracing incidence uses small angles to look at only the top of the sample, thus reducing the influence from the substrate. No peaks were found, and it was concluded that the sputtered SiGe is amorphous.

RBS was done on samples A1 and A8, and is shown in Figures 5.2 and 5.3. The spectra show one layer with Si, Ge and O on top of the Si substrate. The reason for the high oxygen content of the sputtered films is not known. Either the oxygen was there before sputtering, it was deposited during sputtering, or the samples were oxidized after sputtering. It is unlikely that the latter is the case, because the oxidation would be dominant on the outside, and not evenly distributed as it seems to be from the RBS spectra.

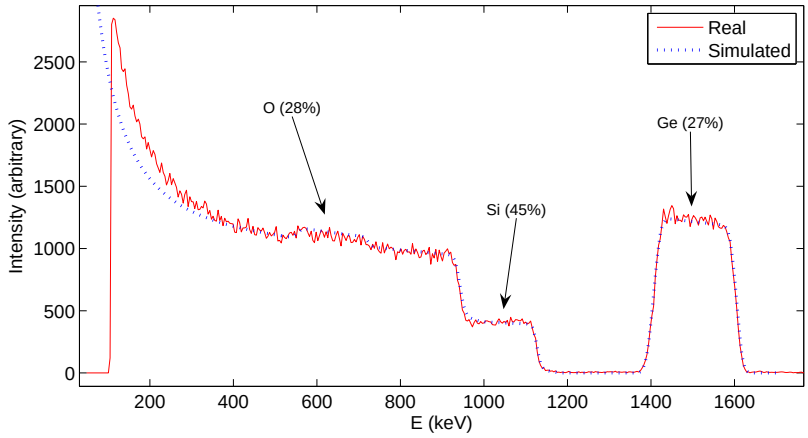

Figure 5.2: RBS spectrum of sample A1. Si, Ge and O, which are all in the sputtered layer, are identified.

It is also unlikely that such a distribution can be caused by the native oxide layer because it takes several days for a layer of 1 nm to form [82]. However, the samples were RCA cleaned more than a week before sputtering,

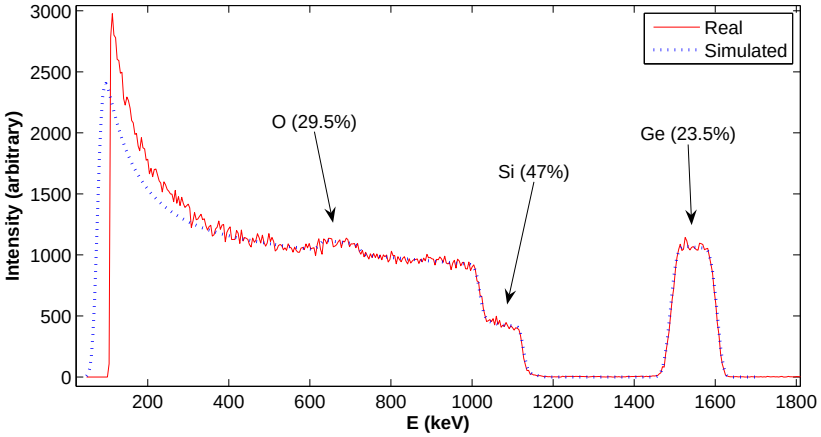

Figure 5.3: RBS spectrum of sample A8. One layer of Si, Ge and O was found.

so it is likely that there was a native oxide layer. The samples were cleaned right before inserting them in the magnetron sputter for the second set of depositions.

Magnetron sputtering was done with a pressure of 10^{-6} Torr, so there should not be any oxygen in the chamber, and though oxygen gas is available, it was not used. It is possible that the target has a composition differing from $Si_{85}Ge_{15}$. A native oxide on the target is not a likely cause because it would be gradually removed after successive depositions. The composition of the target could be investigated using a scanning electron microscope (SEM) with energy dispersive spectroscopy; in a SEM that can handle large samples.

The uncertainty of the O peaks is large, and the actual O content could be lower. The uncertainty of RBS simulations is not trivial, but is closely related to the stopping power data used by the software [70]. It also increases for light elements and compounds like oxides. A rough estimation of the error can be seen directly from the measured RBS spectrum. For the O peak of A1, a fit with the topmost points gives a concentration of 33%. An

average gives about 18%, while a few points on the bottom are below the line for the Si substrate concentration. Though this is a large difference, the simulations are based on compromises between the different parts of the spectra. The Si shelf has half the count difference of the O peak, and the upper fit gives an O concentration of 23% and the bottom fit gives 31%.

Estimations need to be done to determine the thickness values. When simulating the thickness in SIMNRA, the numbers are entered with the units atoms/cm^2. To convert this to a thickness value, the density needs to be known to use Equation 4.5.

What form oxygen is in is not known. It is probable that oxides have formed in the sputtered layer, but it is uncertain whether there is only SiO_2, or if there is GeO_2 also. Assuming that all the O has formed SiO_2, the Ge content in $Si_{1-x}Ge_x$ is 0.47 in A1 and 0.42 in A8. Using a linear interpolation between data collected by Dismukes et al. [17], densities of 3.86 g/cm^3 and 3.70 g/cm^3 can be assumed, respectively.

The density of SiO_2 varies depending on the deposition method and the oxide thickness. Rzodkiewicz and Panas [83] measured the densities of three thermally grown, dry oxide films of SiO_2 on Si, at an oxidation temperature of 1000°C. A SiO_2 layer of 45 nm resulted in a density of 2.31 g/cm^3, 94 nm was 2.24 g/cm^3, and 172 was 2.22 g/cm^3. This was compared to data from five other studies, and the averages were 2.28 g/cm^3, 2.22 g/cm^3 and 2.22 g/cm^3, respectively.

Assuming a SiO_2 density of 2.22 g/cm^3, and assuming the densities do not overlap, the weighed average density of the sputtered layer of A1 is 5.35×10^{22} atoms/cm^2 and 5.36×10^{22} atoms/cm^2 for A8. This leads to a thickness of 374 nm and 224 nm, respectively. The A8 thickness measured with the profilometer was about 180 nm, but no such measurement was done for the A1 sample. The main reason for the 60% thickness difference is most likely the threefold increase in pressure, as the extra gas atoms will reduce

the mean free path of the atoms coming from the target.

For the second set of depositions, sputtering was done at room temperature in case the high temperature in the chamber had an effect on the oxygen content. The average compositions based on simulations of the RBS data of the B3, B6 and B7 samples is shown in Table 5.3. The simulations are based on a two layer structure with slightly varying concentrations, both including Si, Ge and O. Surprisingly, there is a higher O content in these samples than in samples A1 and A8, while the Si content is lower. The Ge content is lower as well, but not by as much as the Si content.

	B3	B6	B7
Si content	32%	31%	34%
Ge content	15%	16%	16%
O content	53%	53%	50%
Ge in SiGe	32%	34%	32%
Total thickness	272 nm	275 nm	249 nm

Table 5.3: RBS data for samples B3, B6 and B7. The concentrations are the average of the two simulated layers.

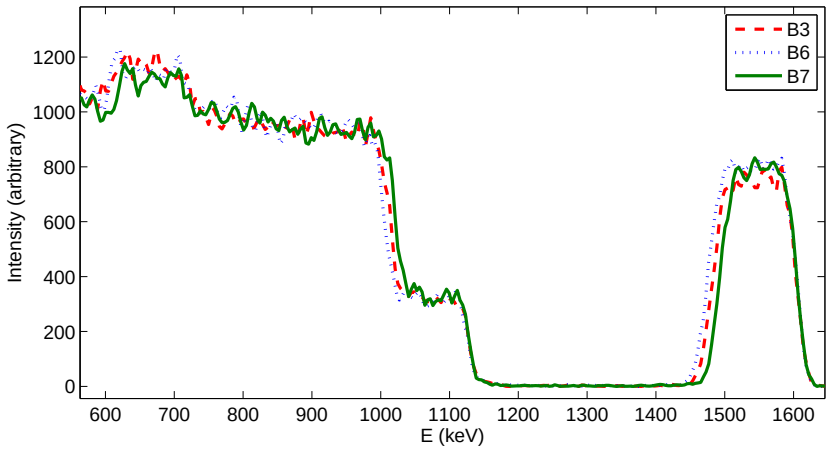

Figure 5.4: RBS spectra of samples B3, B6 and B7.

The power parameter does not affect the oxygen content in the first or second set of depositions, and neither did the working pressure. This indicates that the incorporation of oxygen is not changed by the deposition rate. Only the temperature change seems to have an effect. A possible mechanism is that for higher temperatures Si and Ge atoms find low energy sites more easily and thus form a higher quality layer. The trapping of oxygen will then be reduced and less oxygen is incorporated into the sputtered film. It is not likely that a normal oxidation process occurs because of the long oxidation times required to get a 250 nm thickness. It is more likely that the oxygen is incorporated into a SiGe film with many vacancies.

In Figure 5.4, the oxide peaks can be seen to be more irregular than the Ge peak and the Si shelf. This could be because RBS has more trouble detecting light elements, and it also means the simulations are less accurate. It is difficult to be sure the oxygen is evenly distributed throughout the sputtered film, and variations can be seen especially in the RBS data of sample B6.

The fraction of Ge with respect to Si is fairly stable across the samples. Except for in sample A1, where the Ge fraction is 37%, all the other fractions are between 32 and 34%. Though a composition higher than 15% was expected, this high composition was not expected.

The thicknesses of the layers are similar, but they do not correspond linearly to the sputtering power. However, the estimations are made based on densities of the unknown SiGeO layer, and are therefore not certain.

The estimated thicknesses are higher than the thicknesses measured in the profilometer. Aluminum foil was used to cover parts of the samples, but there is a large thickness gradient at the edge of the foil, which makes measurements uncertain. This is because of both a shadowing effect and sputtered atoms accessing the space between the foil and the sample. The numbers listed in Table 5.4 come from repeated measurements, but are still

Sample	Thickness, profilometer	Thickness, estimated
A8	180 nm	224 nm
B3	250 nm	272 nm
B6	270 nm	275 nm
B7	200 nm	249 nm

Table 5.4: Film thicknesses measured with a profilometer and estimated from RBS simulations.

only approximate. The profilometer could only be used as an estimate of the film thicknesses.

For use as nanowires, the sputtered films should not have any oxygen in them, as this will degrade the solar cell quality. In addition, the films should be crystalline. This is possible to achieve after sputtering with annealing. For further work on this topic, the first step is to get rid of the oxygen. This can be done by looking into where the oxygen originates, whether through a faulty substrate or sputtering target, or other sources.

5.2 Oxidation of SiGe

5.2.1 Epitaxially Grown SiGe

Oxidation of epitaxially grown SiGe was done with the parameters in Table 5.5. From the specifications received with the samples, AG12 had 15% Ge and AG16 had 20% Ge. The oxidations done at 900°C were done to see the trends for different oxidation times. The other oxidations were made to get approximately the same oxide thickness, to study differences in the Ge pileup. The RBS spectra in this section have all been normalized, and the y-axes of the RBS spectra are therefore not a direct value of the count measured, but close.

AG12		**AG16**	
Temp. [°C]	**Time [min]**	**Temp. [°C]**	**Time [min]**
900	25	900	25
900	67.3	900	67.3
900	150	900	150
800	240	800	240
850	75	850	60
950	25	950	20
1000	20	1000	20

Table 5.5: Oxidation parameters of epitaxially grown SiGe samples AG12 and AG16.

RBS simulations were done to get quantitive data of the layer structure of the oxidized samples. The layer structure consists of SiO_2 in the top layer, a Ge pileup region below this, then a SiGe layer that is mostly unaffected by the oxidation, and finally the Si substrate. The results of the simulations are presented in Table 5.6 and 5.7. The samples are referenced by their oxidation temperature and time, like AG12-900-25.

Sample	SiO_2	Ge Pileup		SiGe	
	d [nm]	d [nm]	C_{Ge} [%]	d [nm]	C_{Ge} [%]
AG12-asgrown	0.0	0.0	0	59.4	17
AG12-900-25	24.4	5.2	33.5	48.3	16.5
AG12-900-67	32.2	7.3	40	40.2	15.5
AG12-900-150	55.4	14.7	42	23.1	16.5
AG12-800-240	36.7	10.3	36	34.2	15
AG12-850-75	36.0	8.8	41	38.2	15.5
AG12-950-25	37.5	8.4	44	36.2	15.8
AG12-1000-20	36.7	9.3	36	35.2	14.5

Table 5.6: RBS simulation results of epitaxially grown SiGe sample AG12. The numbers are based on a three layer structure, where d is the thickness of the layer, and C_{Ge} is the Ge content of that layer.

Sample	SiO_2	Ge Pileup		SiGe	
	d [nm]	d [nm]	C_{Ge} [%]	d [nm]	C_{Ge} [%]
AG16-asgrown	0.0	0.0	0	46.9	20
AG16-900-25	16.5	3.6	59	34.3	19
AG16-900-67	34.5	8.5	57	26.5	20
AG16-900-150	56.9	12.9	65	11.5	35
AG16-800-240	34.5	12.5	40	22.2	19
AG16-850-60	34.5	13.0	44	24.5	20
AG16-950-20	30.0	14.6	34	24.2	18
AG16-1000-20	33.7	13.7	45	21.4	21

Table 5.7: RBS simulation results of epitaxially grown SiGe sample AG16. The numbers are based on a three layer structure, where d is the thickness of the layer, and C_{Ge} is the Ge content of that layer.

Figures 5.5 and 5.6 show the simulated RBS data of the two samples oxidized at 900°C for three different times. The simulated data is shown because it shows the peak and shelf differences more clearly than the real data. The real RBS spectra have been included in Appendix A.

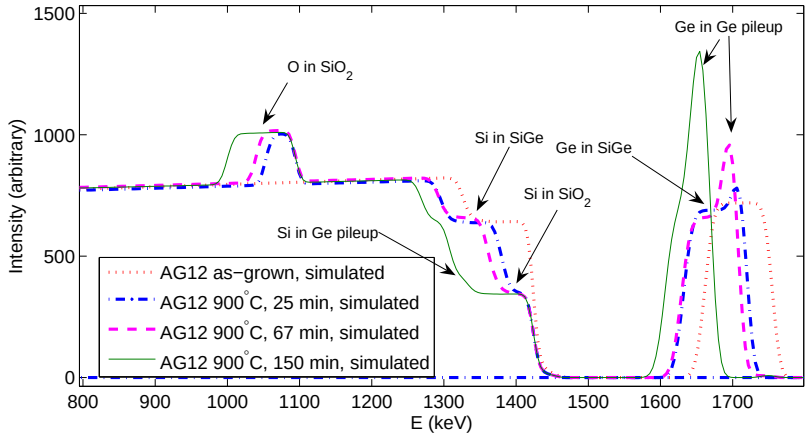

Figure 5.5: Simulated RBS data for AG12, oxidations at 900°C

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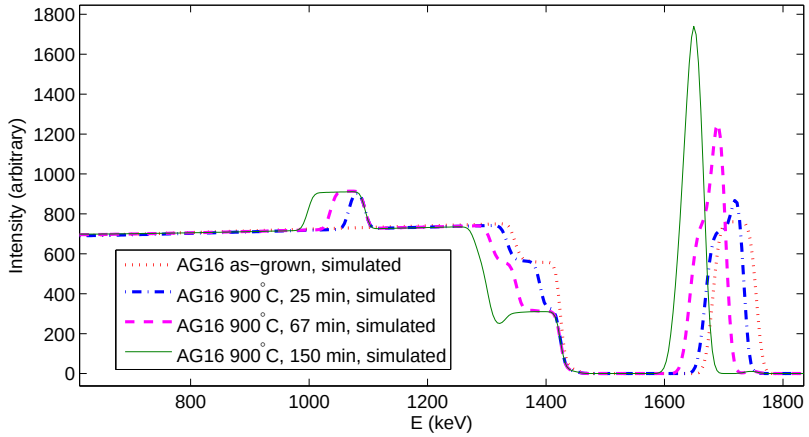

Figure 5.6: Simulated RBS data for AG16, oxidations at 900°C

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The trends in Figures 5.5 and 5.6 are similar. The original Si in SiGe shelf, as seen in the as-grown samples, becomes thinner and moves deeper

(relative to the surface) into the sample as the oxide is formed on the outside. Another Si shelf emerges below this, with a smaller Si content, because of the SiO_2. This shelf becomes wider as the oxide becomes thicker.

Because the Ge pileup region is narrow, the effect of Si in this region is not as easily recognizable. When the Si content of the Ge pileup region is sufficiently high, the Si in SiO_2 shelf is curved up at its edge. When the Si content is lower the shelf curves down, as can be seen in Figure 5.6 for sample AG16-900-150.

The Ge peak is shifted to a lower energy because the oxide layer is grown on top. It is not a one-to-one relationship because of the different stopping powers of O and Ge, which is the reason why the x-axis can not be shown as depth in the sample. If the whole peak is shifted the oxide layer is pure SiO_2, but there is a small amount of Ge in the oxide which will be discussed later. As the Ge is piled up, a new peak emerges on the right hand side of the original peak, which indicates it is at the interface between SiGe and SiO_2. This peak gets wider and taller as the Ge concentration and the width of the pileup region increases.

AG12-900-150 has a narrow Ge shelf with close to the original Ge content, but for AG16-900-150 the Ge content is 35% in this layer, which can be interpreted as the pileup region having spread to the whole film. The change from the pileup layer to the SiGe layer is likely gradual, and the two layer model is only made to fit the spectra.

This imposes a limit on the fabrication of SiGe/Ge core-shell nanowires. If a certain composition of SiGe is wanted in the core, the oxidation has to be limited. This also imposes a restriction on the Ge content in the pileup region. For AG16-900-150 the Ge content is 65%, which seems to be an upper limit without affecting the deeper layer. This is the highest Ge content measured in any of the oxidized samples. If a higher Ge content is wanted, the original SiGe layer has to be thicker as well.

Figure 5.7 shows the change in oxide thickness with oxidation time. The oxidation rate slows down over time for both samples as shown by Deal and Grove [21] for samples below 30 nm. Because only two of the thicknesses are above 30 nm, it is uncertain whether this region will be linear, as in the Deal Grove model. Two studies have found that the oxidation rate goes to zero for longer oxidation times [46, 47]. Except for the oxide thickness of AG12 after 25 minutes, the other thicknesses of the two samples correspond well. The dry oxidation rate for SiGe should be the same as that of Si [30], which means it should be independent of the composition.

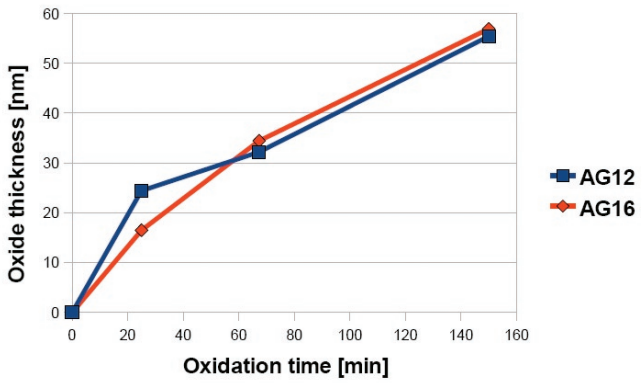

Figure 5.7: Oxide thicknesses for oxidations at 900°C, both epitaxially grown samples.

In Figure 5.7 it can be seen that the oxide thickness of AG12-900-25 is thicker than the trend of the other thicknesses. It is possible to make this oxide layer thinner in the simulations. Not every simulation is a perfect fit. It can be difficult to fit the O peaks because of irregularities in the spectra. In some samples compromises between the Si shelf and the Ge peak had to be made.

Figure 5.8 shows a good example of the compromise that sometimes had to be done when simulating RBS data. It was not possible to fit both the O peak and the Si shelves. The oxide is 18.0 nm thick in the thinner oxide simulation, and 24.4 nm in the other. It can therefore be tempting to say

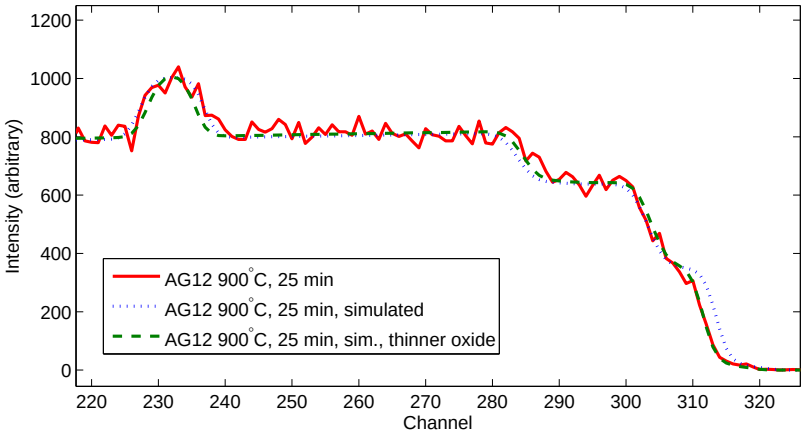

Figure 5.8: RBS data for AG12, oxidation at 900°C for 25 minutes. The simulations are a compromise between Si shelf fit and oxide thickness.

that the thinner oxide simulation is more 'valid'. In this thesis, the choice was made to first prioritize the Ge peak, then the O peak, and finally the Si shelves. The Si shelves consist of several layers and are therefore more complex than the O peak. However, there is no decisive reason to choose the one fit over the other.

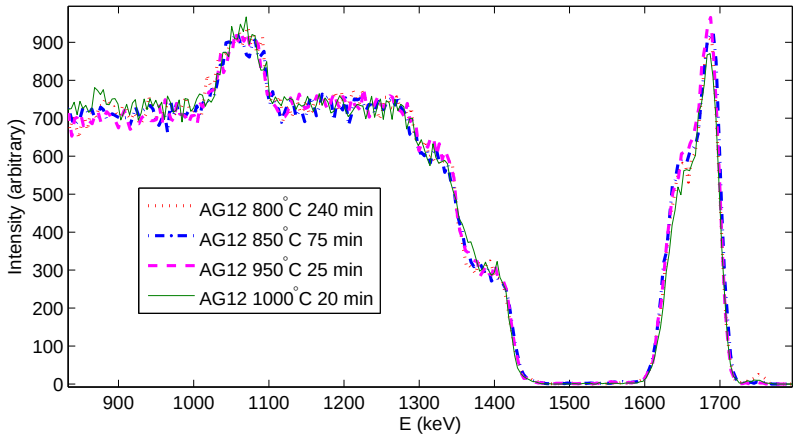

Figure 5.9: RBS spectra of oxidations at different temperatures for AG12.

The oxidations at 800°C, 850°C, 950°C and 1000°C are shown in Figures

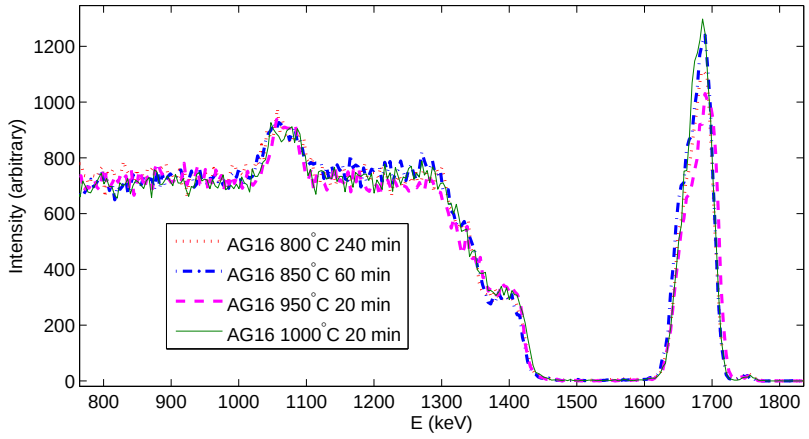

Figure 5.10: RBS spectra of oxidations at different temperatures for AG16.

5.9 and 5.10. Oxide thicknesses are very similar, but AG16-950-20 has a thinner oxide. To get the same thickness, a 25 minute oxidation time would be better, as in AG12-950-25. The only noticeable difference in the AG12 RBS spectra is that AG12-1000-20 has a slightly smaller Ge content.

The two Ge layers are not as distinquished for the oxidations done at different temperatures compared to the 900°C oxidations, especially for the AG16 sample. This is not because of a difference in the samples, but rather an effect of the measurements themselves. An upgrade of the detector at the University of Uppsala was done after the RBS characterization of the AG16 different temperature oxidations.

A close-up of the Ge pileup of the oxidations at 900°C is shown in Figure 5.11. The Ge content of the pileup is on average 22% higher for AG16 with an original SiGe composition of 20% Ge as for AG12 with an original SiGe composition of 15% Ge. A high Ge content in the pileup region is useful in solar cell applications because the difference in band gaps between the SiGe core and the Ge shell will be larger.

The Ge pileup region seems to reach a high Ge content already in the 25 minute oxidation, and only increasing a few percent for the 150 minute oxi-

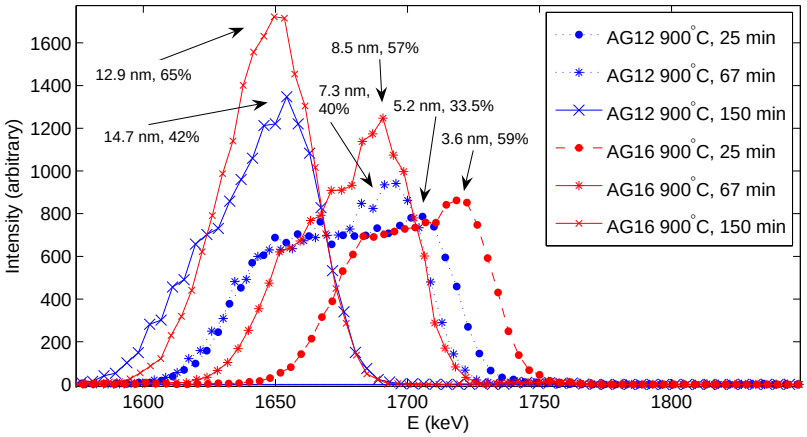

Figure 5.11: Ge pileup of AG12 and AG16 oxidized at 900°C.

dation. It is believed that the relationship between the original Ge content and the Ge content in the pileup region is maintained by interdiffusion of Si and Ge caused by the gradient in their concentrations [53]. It is therefore important to consider the starting composition of the SiGe, when attempting to get a Ge pileup region of a known composition. There is not much data on this yet, as most studies have focused on decreasing the pileup region because it relaxes the strain of the underlying SiGe [84].

To find out if the pileup region changes differently from the oxidation rate, the pileup thickness versus the oxide thickness is plotted in Figure 5.12. The group of AG16 oxidations done at different temperatures deviates from the linear relationship of the other oxidations. It is not a sample difference because the AG16 900°C oxidations agree to the linear fit. Therefore, it can be assumed that the pileup regions of the AG16 different temperature oxidations really are thinner than the simulations show. This also means that the pileup Ge content is higher for this sample, fitting with the discussion in the previous paragraph.

The linear fit equation for the Ge pileup thickness $d(pileup)$ as a function

of the SiO_2 thickness $d(SiO_2)$, based on the other simulations, is

$$d(pileup) = 0.26d(SiO_2) - 0.58 \tag{5.1}$$

More measurements should be done to confirm this linear fit. It would also be interesting to see if there are deviations from the fit at smaller oxide thicknesses. If both AG12 and AG16 pileup thicknesses can be linearly approximated with the same fit, there must be plenty of Si available for oxidation, which means that Si has no trouble diffusing through the pileup layer regardless if it has 40% Ge or 60% Ge. Oxygen diffuses through the SiO_2 layer, where it oxidizes Si which has diffused through the pileup layer.

Because the oxidation rate is known, the pileup rate can be easily calculated by Equation 5.1. If the linearity is true, this is useful for RBS simulations, as it would limit the number of possible parameters to change.

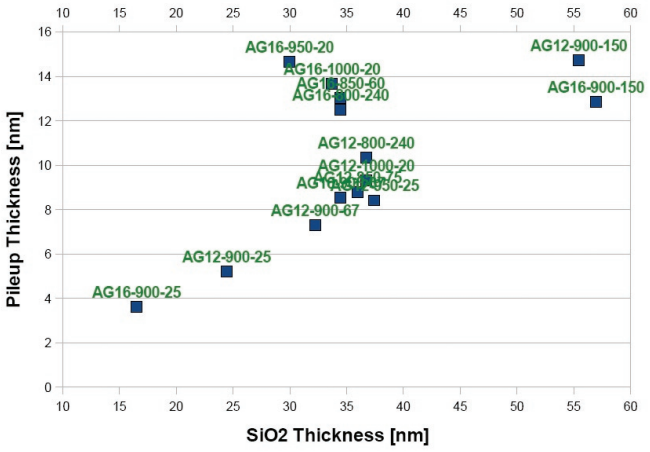

Figure 5.12: Comparison of Ge pileup thickness versus SiO_2 thickness.

A small amount of Ge was found in the SiO_2 layer for almost all the samples. Some of this can be caused by the uncertainty of the simulations, but it is distinguishable in the group of samples oxidized at different temperatures. The RBS spectra of these samples is shown in Figure 5.13. The Ge in SiO_2 peak is not next to the pileup Ge peak, and the best simulation fit is for a $(Si,Ge)O_2$ layer on the outside of the SiO_2 layer. A surface layer

of (Si,Ge)O_2 was found by both Eugene et al. [33] and Liou et al. [34], however, this layer was only formed for a Ge content above 50% in the original SiGe.

Samples AG12-800-240 and AG12-800-240 had the most Ge in the oxide; the RBS simulation of AG12-800-240 shows that there is approximately 2.1% Ge in a 3 nm thick layer of SiO_2. Zhang et al. [42] found less (Si,Ge)O_2 in high temperature oxidations because of diffusion of Ge into the sample, and this was supported by Tanaka et al. [85].

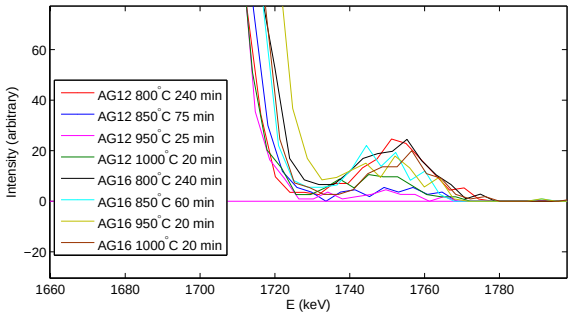

Figure 5.13: Ge found in the SiO_2 for the group of samples oxidized at different temperatures.

Though most studies report no Ge in the oxide for a Ge content less than 50%, this is not always the case. Terrasi et al. [44] reported finding Ge in the oxide for samples with as low as 6% Ge. They are not certain whether this result was caused by their use of rapid thermal oxidation. It is believed that this is the first time Ge is found in the oxide for thermal dry oxidation.

5.2.2 Sputtered SiGe

Samples A1 and AC1 were oxidized at 900°C for 67 minutes and 30 seconds. Samples A8 and AC2 were oxidized at 1000°C for 20 minutes and 15 seconds. AC1 and AC2 are control samples from a p-type Si wafer. The goal of this oxidation was to find out how the oxidized sputtered samples differed from oxidized epitaxially grown SiGe samples. The RBS spectra with the

simulated fits are shown in Figures 5.14 and 5.15.

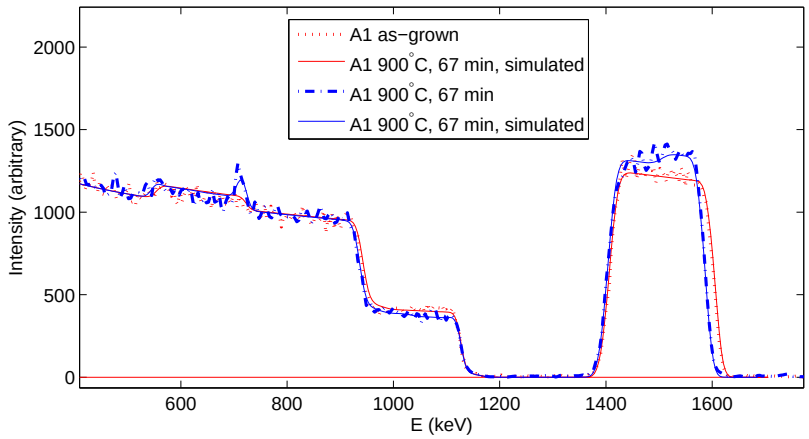

Figure 5.14: RBS spectra of A1 as-grown and A1 oxidized at 900°C for 67 minutes and 30 seconds.

There is no pileup region in these samples, however, there is an increase in the Ge content by a few percent. An oxide layer 3-5 nm thicker than the oxide in AG12-900-67 and AG16-900-67 is seen for the oxidized A1 sample. The oxide layer of A8 is 5-8 nm thicker than the oxide layer of AG12-1000-20 and AG16-1000-20. The Si control samples, AC1 and AC2, have slighty more narrow oxide layers than the epitaxially grown samples, which is unexpected.

The RBS spectra for the control samples are not as complex as for the SiGe samples because there are fewer parameters to fit. Therefore, the only indication of O is from the O peak, whereas the SiGe samples are also fit by their Si and Ge shelves and peaks, which means the uncertainty of the oxide fit in the Si samples is larger.

A 7.5 nm SiO_2 layer was found at the SiGe/Si substrate interface. It is likely that some of the O inside the sample has diffused to the surface and the Si substrate/SiGe interface where it reacts and forms a layer of SiO_2. On the surface this creates an enhanced oxidation rate, while a new SiO_2

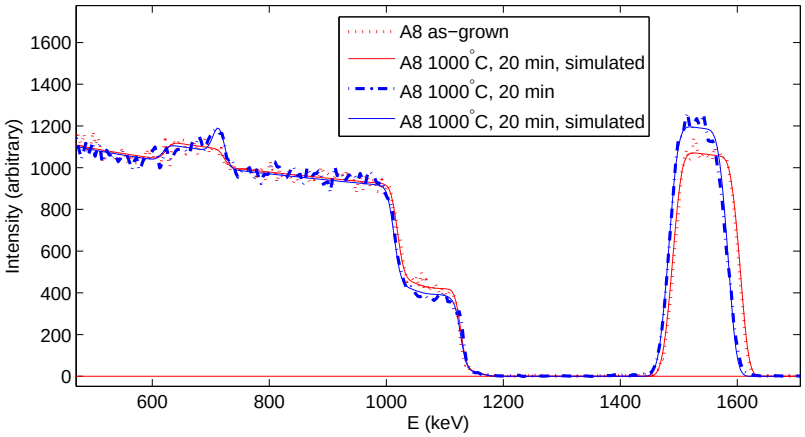

Figure 5.15: RBS spectra of A8 as-grown and A8 oxidized at 1000°C for 20 minutes and 15 seconds.

layer is formed inside the sample. It is also possible that the inner SiO_2 layer was there for the unoxidized A1 and A8 samples. When simulating the RBS data, there is a certain freedom of choice when it comes to the layer structure of the material.

5.3 Fabrication of SiGe Nanowires

Electron beam lithography (EBL) has been used in other studies to create nanowires. The biggest advantages of EBL over photolithography are a better resolution and more control of the exposure, but the problem is a low throughput. The pattern exposed by the electron beam can be programmed and no mask is needed. Notargiacomo et al. [86] used EBL and wet etching to create 60 nm SiGe nanowires. Another study has created 100 nm Si nanowires by EBL [87], but both of these studies have only made horizontally lying nanowires.

To create vertical nanowires catalytic etching can be done. Huang et al. [88] put polystyrene spheres on a Si substrate. These spheres are ordered because they are close packed. The spheres are etched to a smaller size and a Ag film is deposited around them. This film acts as a catalyst for etching and the spheres act as a mask, creating 3.5 μm nanowires with a diameter of 270 nm. Similar techniques have been used by other research groups [89, 90, 91].

There are many other possible ways to create nanowires. Photolithography was chosen for the formation of the SiGe column structures due to a lack of time to make other potential techniques work. These structures are tens of micrometers large, but the principle of oxidizing the structures to make them smaller remains the same.

5.3.1 Photolithography

Exposure parameters for the SiGe samples were very different from the parameters used in the Si NCs lithography. For the Si NCs, the exposure was done at 283 W for 10 seconds. For the SiGe sputtered samples, the exposure parameters that were found to give the best results were 270 W for 70 seconds. The large difference in time is most likely because the resist and the light intensity had changed during this time. The Si NCs were patterned

more than a year before patterning the SiGe samples.

Some of the samples were best exposed at 270 W for 35 seconds. A new flask of photoresist was used for these exposures, so it is clear that the quality of the resist changes the exposure parameters. Because the lamp power can change over time, it was noted that the light intensity was 6.51 mW/cm^2, which is a more stable parameter.

5.3.2 Etching

After lithography, the parts of the samples without photoresist were etched. The goal of the etching was to remove the SiGe not covered by resist to form column structures. Preferably, the etch should stop before it reaches the Si substrate, but this is difficult to do without much testing of etching rates. Therefore, an etch that stops when reaching the Si was wanted.

Most Si etchants should also etch low Ge content SiGe. KOH is an anisotropic etch that has been much used for Si etching. However, when all SiGe is removed the etch will continue removing the Si substrate below. Because KOH is anisotropic, the Si (100) plane will be etched, but the more atomically dense (111) edges will not be. The result is that the etching will stop after inverted pyramids are created in the substrate [92].

To avoid this effect it is preferable to use an etch that selectively removes SiGe and not Si. Such etchants have been developed for use in microelectronics [93]. Hartmann et al. [94] have used HCl as a selective etch, while others are using fluorine compounds in a dry etch process [95, 93].

Another type of etch uses a mixture of an acid that oxidizes only Ge, and an acid that removes this oxide. Johnson et al. [96] use NH_4OH:H_2O_2:H_2O, where H_2O_2 is the oxidizing agent and NH_4OH removes the oxide. Another combination is using HNO_3 to oxidize and HF to remove the oxide [93]. The etching solution chosen was a mixture of HF and H_2O_2, and diluted with water. Carns et al. [97] have studied this etch in detail.

The samples were etched in a 1:2:12 solution of HF:H_2O_2:H_2O. The SiGe film went through a cycle of colors from green to red and brown until it started looking like the Si substrate. The etching was stopped after 12 minutes. Figure 5.16 shows the profilometer measurement of the contacts of sample A5. Except for a few rather large grains, the surface has few irregularities. The contact heights are 250-260 nm, which is the same that was measured after the sputter deposition. It is therefore likely that not a lot of Si has been etched.

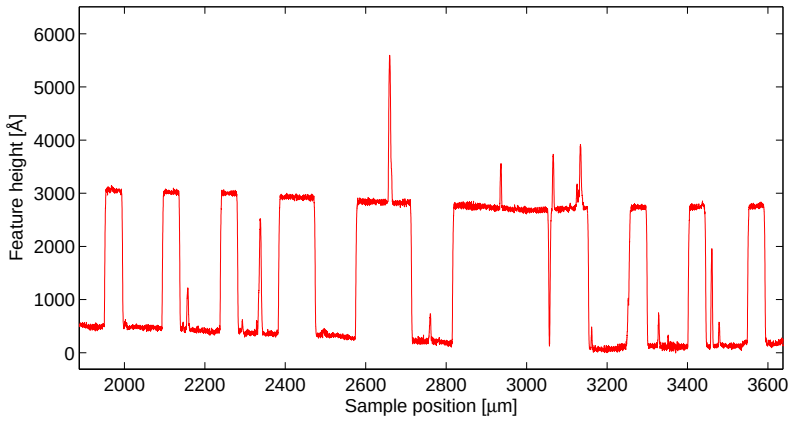

Figure 5.16: Profilometer measurement of sample A5 after photolithography and etching.

The trench at about 3050 µm on the x-axis is a 10 µm line that borders a group of contacts. The bottom is only 2 µm wide as seen in the profilometer, but this is not necessarily because of the lithography process, it could be a resolution limit of the profilometer. Looking at other side walls, it is confirmed that the slopes are about 4 µm wide.

A Si reference sample was patterned by the same process. This sample was etched for 12 minutes in HF:H_2O_2:H_2O (1:2:12), and the resist was moved. The sample was studied with the profilometer, and it was found that the height difference between the etched and the not etched regions fluctuated from 0 to 100 nm, with the most common step height being 80

nm. This is not nearly as much as the Si layer in sample A5 was etched. Because the SiGe layer was etched until the Si layer was seen, it is not likely that the Si below the SiGe is etched more than one minute. One minute would, based on the Si reference sample etch, etch about 6-8 nm of Si.

5.3.3 SCM Characterization

The ambition of the SCM measurements was to image the capacitance variations of the SiGe nanowires. Because oxidation between closely spaced nanowires can cause an uneven oxide layer in the troughs and on the nanowire sides, a measure of this was wanted. SCM has been mostly used for mapping doping profiles [98, 99, 71], where a change in doping levels in the sample results in a changed depletion width, which changes the capacitance. However, a variation in the oxide thickness should also be detectable as a change in the capacitance, and this has been done by Yanev et al. [100].

The SiGe samples in this study are not doped, and therefore they have no depletion region. Because of this, the only capacitance that contributes to the electrical signal is from the oxide. The sensistivity of the SCM used is 10^{-22} F/$\sqrt{Hz}$, and the frequencies used are between 880 and 1050 MHz. The oxide thickness d needed to be below this sensitivity can be calculated assuming a parallel plate capacitance between the tip and the SiGe layer:

$$C = \frac{\epsilon_0 \epsilon_r A}{d} \tag{5.2}$$

ϵ_0 is the vacuum permittivity, ϵ_r is the relative permittivity of SiO_2, 3.9. A is estimated as the tip area πr^2, with a given radius of 20 nm. This puts a requirement on the oxide thickness to be less than 13.4 nm. However, the working area is often considered to be larger than the tip area, as the sides of the tip also influence the sample. The only minimum thickness requirement is that the oxide has to be thick enough to avoid tunneling.

Sample A5 was oxidized for 17 minutes and 10 seconds at 900°C. This corresponds to about 10 nm oxide thickness, according to the Massoud model

[101]. The Massoud model is based on the Deal-Grove model, but is more complex and has a better fit for thin oxides. According to data collected by PhD student Ethan Long, but not yet published, SiGe oxidation follows this model closely.

The sample was measured with an AC bias of 5 V and a DC bias of 2 V, at a sampling frequency of 0.5 Hz and a trace distance of 5 µm. Several parts of the sample were measured, but there was no electrical signal for any of them. Because of earlier failed attempts by colleagues to get even the control sample to show an electrical signal, and the fact that the sputtered SiGe samples were all of questionable quality, no more samples were tested.

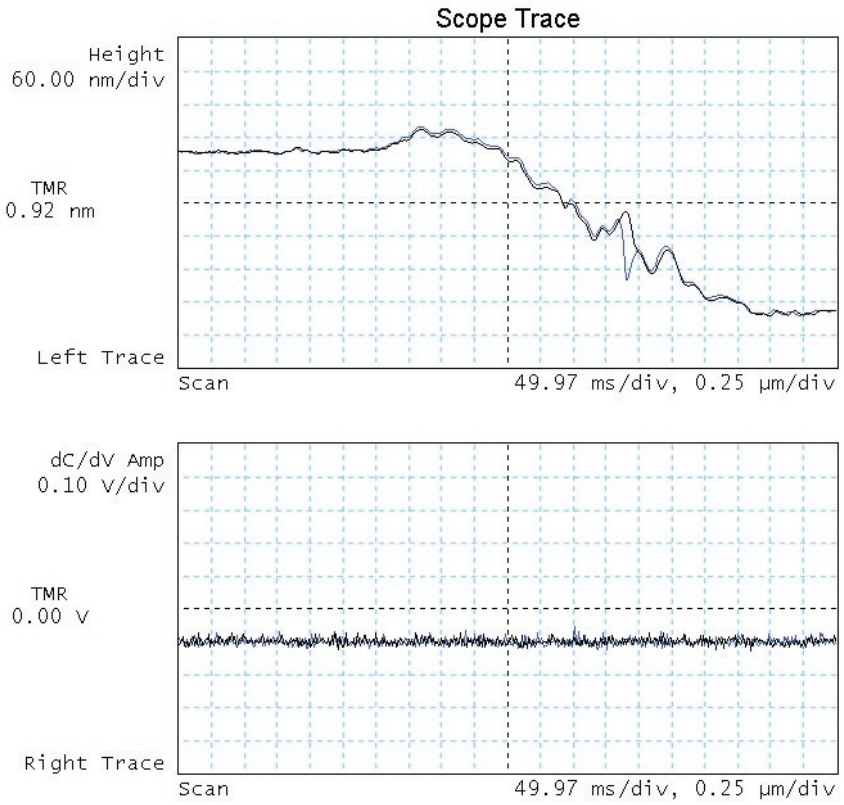

Figure 5.17: Adapted screenshot from the NanoScope software showing the edge of an etched step of sample A5. No electrical signal was measured.

In Figure 5.17, a screenshot of a measurement is shown, at the edge between an unetched part and an etched part of the sample. The incline is more than 2 μm wide, so the photolithography and successive oxidation did not produces edges of sufficient sharpness for use as nanowires. The step is about 300 nm high, which is 50 nm higher than the sputtered film thickness measured in the profilometer. This means that either some Si was etched, or there is a difference in the oxidation between top and bottom of the step.

There are several reasons why the SCM measurements did not and will not work. The SiGe is not doped, so there are no depletion region changes to measure. The high oxygen content and the in general poor quality SiGe layer would lower the capacitance. Previous studies on oxidation of SiGe have found a large amount of negative charges in the oxide [30, 39], which would interact with the measurements.

Even with perfect SiGe and SiO_2 layers, the oxide layer would not provide good capacitance signals for most of the sample. On the side walls of the nanowires the oxide would be too thick, and on the top of a nanowire the oxide layer should be uniform. The only places where a change in the capacitance could be measured is on the edges, but analysis of the data here would be complicated because of the input from the side walls.

As seen by the RBS data presented in the last section, the Ge pileup thickness caused by the 10 nm oxidized layer will be less than 3 nm. This is neither enough to reduce the size of the SiGe column structures sufficiently to get nanowires, nor does it give a thick enough Ge layer to be useful in solar cells. The restrictions on the SCM make it a bad choice for this purpose.

Though Yanev et al. [100] have used SCM to measure oxide thickness, it is not ideal for use with nanowires. The tip of the probe is thin, but it is wider further up, which means the resolution is limited in deep trenches. It is also a problem that the tip breaks easily with a changing topography. Another approach to the characterization of the oxidized SiGe/Ge core-shell

nanowires should be used.

Instead, the cross section of the samples could be investigated in a scanning electron microscope (SEM) or tunneling electron microscope (TEM). Column structures made by photolithography are large enough to not be destroyed in the sample preparation. The SEM is an easy and quick tool for characterization of these sizes. It would also be a good input to have surface images of the samples throughout the fabrication process.

5.4 Electrical Characterization of Si NCs

The goal of this part of the study was to find out if the layer of Si NCs in SiO_2 was conductive and if the samples showed a diode characteristic. Further investigations into the charge characteristics were also done. ITO was deposited by sputtering and patterned to form contacts on the Si NC samples. ITO is a much studied material because of its use as a transparent conductor. It is an n-doped material and makes a p-n junction with the p-doped Si. With the oxide layer in the middle it makes a MOS capacitor structure. The reason ITO was used is because of it makes a good match with the Si substrate and because of availability in the lab.

5.4.1 IV Results and Discussion

Three different sized contacts on each sample were investigated, but because their current densities were similar, one of the sizes (size C) has been used throughout the report. The contacts used are circular and with a radius of 0.625 mm. The results were repeatable for each contact, but there were larger differences between the same sized contacts on the same sample than the difference between the different sized contacts.

The Si NC samples show a rectifying effect and diode characteristics in the dark measurements shown in Figure 5.18 and in the light measurements shown in Figure 5.19. It is not straight forward to compare this to literature values of ITO/Si junctions because of the large leakage current of the Si NC samples. Orders of magnitude between 3 and 3.5 have been found in other studies [102, 103], which corresponds well to the rectifying effect seen in the test sample. If using the -1 V value of the Si NC samples in Figure 5.18, the rectifying effect is almost 5 orders of magnitude. If using the highest reverse voltage measured, -5 V, it is not much smaller than for the test sample.

The current density is much smaller for the Si NC samples than for the test sample. At -2 V the difference is about two orders of magnitude. The

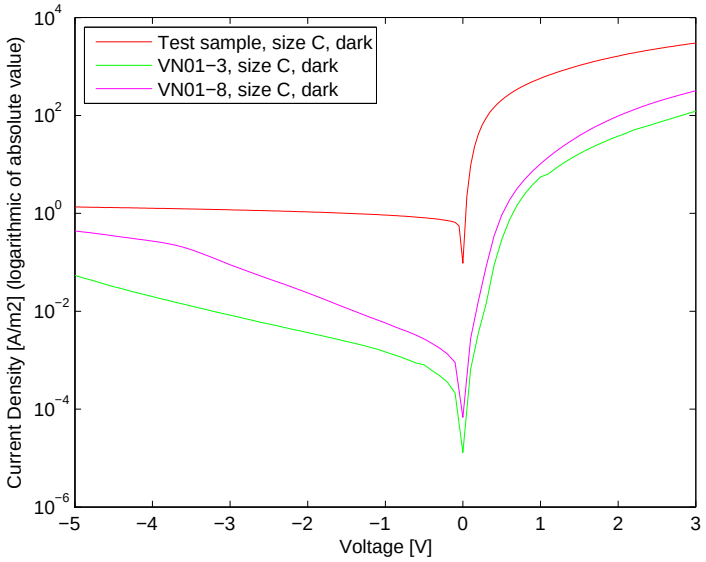

Figure 5.18: Dark measurement IV characteristics of test sample, VN01_3 and VN01_8.

leakage current is also worse for the Si NC samples. In the VN01_8 sample it is not constant, but drops linearly before plunging at 0 V. This is because the transition region of the p-n junction is not depleted of mobile charges, which strays from the ideal behavior of a diode [13]. The photogenerated current was calculated in reverse bias, at -2 V and -4 V, as the difference between the dark and light current. This data is presented in Table 5.8 and shown in Figure 5.20.

Fitting the slope of an almost ideal diode, using the diode equation with an ideality factor, to the slopes of VN01_3 and VN01_8 in Figure 5.18 from 0.1 V to 0.5 V, the ideality factor of the Si NC samples was estimated to be about 2.5. This is much higher than the 1.6 achieved in another study [104] on ITO/Si solar cells. A value of 2 means the recombination in the transition region is very high [13], but the ohmic losses are very high both in the experimental setup and probably also in the ITO/Si NC interface [102], so it is not possible to conclude on a cause. Neither is there a defined linear

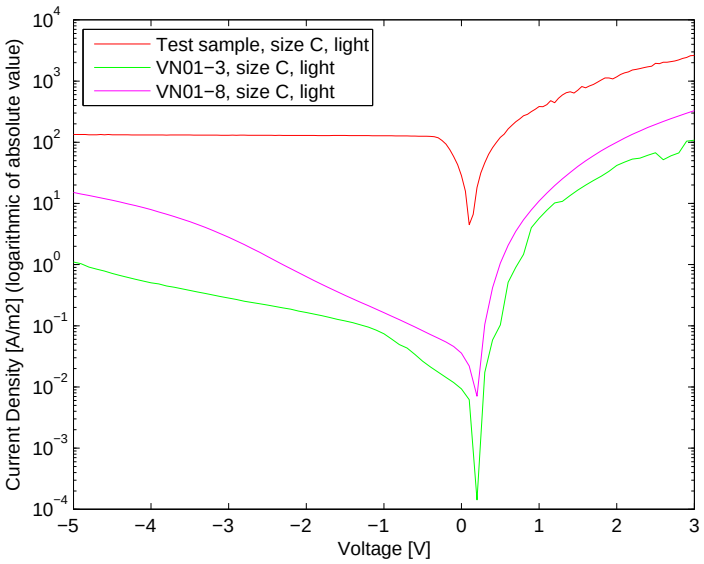

Figure 5.19: Light measurement IV characteristics of test sample, VN01_3 and VN01_8.

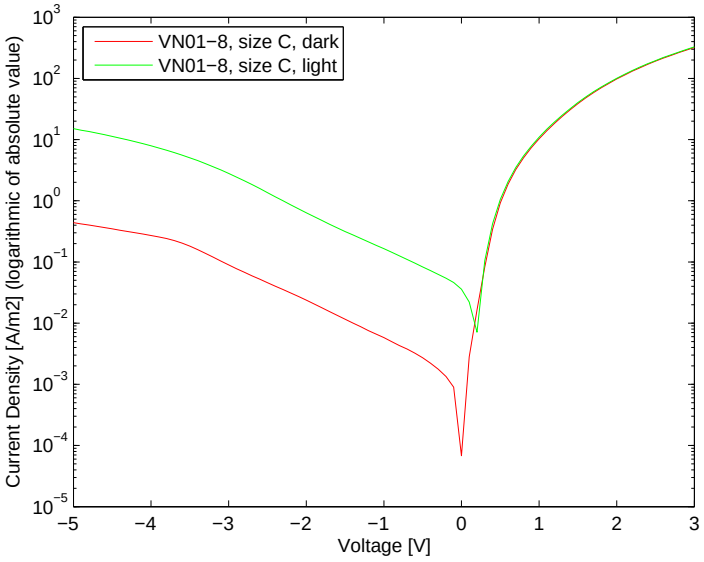

Figure 5.20: Dark and light measurements compared for VN01_8.

part of the graphs to be certain of the slope. To investigate this further smaller steps in the voltage would have to be made in the measurements, to find linear areas.

VN01_3 sample

Bias	Dark current [10^{-8} A]	Light current [10^{-7} A]	Photogenerated [10^{-7} A]
-2 V	0.450	2.03	1.98
-4 V	2.44	6.17	5.93

VN01_8 sample

Bias	Dark current [10^{-8} A]	Light current [10^{-7} A]	Photogenerated [10^{-7} A]
-2 V	2.92	7.81	7.52
-4 V	33.2	97.1	93.8

Table 5.8: The photogenerated current in the VN01_3 and VN01_8 samples.

A reference sample of the approximate same thickness as the Si NCs, 100 nm, was characterized, and the sample was found not to be conducting.

The efficiency of a solar cell is given by $\eta = J_m \times V_m / P_s$ where the m subscript denotes the maximum power and P_s is the incident light power density [3]. J_m and V_m were calculated so that they formed the biggest rectangle possible in the area limited by the x-axis, the y-axis and the I(V) graph. For the test sample the IV graph was approximated as linear in this area with the equation $V_m = 240 J_m - 28.5$. This gave the calculated values of $J_m = -14.3\ A/m^2$ and $V_m = 0.0594\ V$. The incident light power density was 1000 W/m^2, which gives an efficiency of about $\eta = 8.5 \times 10^{-2}\%$. One reason for this small value is that the current increased and approached zero in reverse bias before entering the forward bias area. The Si NC samples did not have this effect.

For the Si NC graphs there were only three measurement points in the power area, which gives two different slopes, as seen in Figure 5.21. A rough estimate of the maximum power was made by assuming the largest area was formed with one corner of the rectangle at the coordinate of the middle point. For the VN01_3 sample this resulted in an efficiency of $\eta = 6.2 \times 10^{-5}\%$ and for the VN01_8 sample $\eta = 2.2 \times 10^{-4}\%$. These efficiency values are only comparable to each other and not to literature values because of the lack of measurement resolution and the large ohmic losses in the experimental setup.

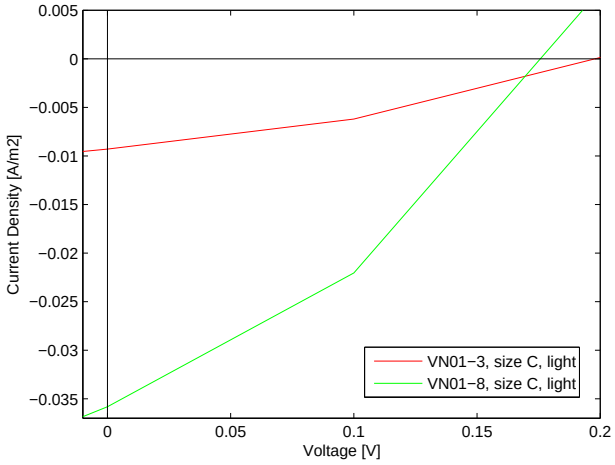

Figure 5.21: Light measurements; area with power output.

The depletion region will be almost entirely within the oxide and p-Si because of the high doping of ITO. According to Chang et al. [104], n $\approx$ $5{\times}10^{20}$ cm^{-3}, but because ITO is a compound material this number can vary. Equation 2.12 is used to find the depletion region width where V_0 is the only unknown, and is the difference of the work functions of the materials divided by the electron charge

$$V_0 = (\Phi_{pSi} - \Phi_{ITO})/q \tag{5.3}$$

The value of the ITO work function is not well known, and could vary from 4.4-4.7 eV [105]. In addition to the rough estimate of the doping of the p-type Si, this makes calculations on these materials qualitative at best. The work function of Si Φ_{Si} is 4.85 eV, but the doping level needs to be accounted for to get Φ_{pSi}. Based on derivations from Streetman [13]

$$\Phi_{pSi} = \Phi_{Si} + E_i - E_f = \Phi_{Si} + kT \times ln\frac{N_a}{n_i} = 4.85\ eV + 0.23\ eV = 5.08\ eV \tag{5.4}$$

with $E_i - E_f$ calculated from a doping of $N_a = 1 \times 10^{14}$ cm^{-3}. For $N_a = 7 \times 10^{14}$ cm^{-3}, $E_i - E_f$ is 0.28 eV. An assumed Φ_{ITO} of 4.6 eV gives a V_0 of 0.48 V. Based on the uncertainties in the work functions and doping, the width varies from a minium of 0.95 µm for $N_a = 7 \times 10^{14}$ cm^{-3} to a maximum of 2.6 µm for $N_a = 1 \times 10^{14}$ cm^{-3}.

For more quantitative calculations, it is suggested not to use ITO as contacts. ITO has a work function that can vary from 4.4 to 4.7 eV and the solar cell efficiency of an ITO and p-Si p-n junction is so small it is difficult to compare with other measurements. Also, the doping of Si can be more accurately measured using resistivity measurements.

5.4.2 CV Results and Discussion

Figures 5.22 and 5.23 show the capacitance measurements of VN01_3 and VN01_8, respectively. Measurements were done at 5, 10, 50, 100, 500 and 1000 kHz. The CV characteristics differ from the ideal case outlined in Figure 2.10 in section 2.4.1 of the Background chapter. The accumulation region is voltage dependent, and the capacitance does not increase for low frequency measurements in the inversion region. It is likely that the capacitance is kept low at higher voltages because of conduction by tunneling in the Si NCs.

The accumulation capacitance is also frequency dependent. This relation has been studied by Kwa et al. [106], and they do not attribute it to tunnel-

ing, but to a large concentration of traps in an interface dielectric layer. In other studies, large curvatures in the reverse bias region of the capacitance is thought to be because of both surface states and fixed charges in the oxide [107, 108, 109]. Based on this, the Si NCs will affect the curvature of the CV characteristics, as clearly seen in the plots.

The CV characteristics in Figures 5.22 and 5.23 are similar to those measured by Turut and Saglam [109], who measured a Schottky diode of Al and Si. The exact origin of the charges is difficult to find, and is usually put into an extra parameter called excess capacitance C_0 [107, 108]. The total capacitance is then plotted as $1/(C - C_0)^2$. A measure of the excess capacitance has not been attempted in this thesis.

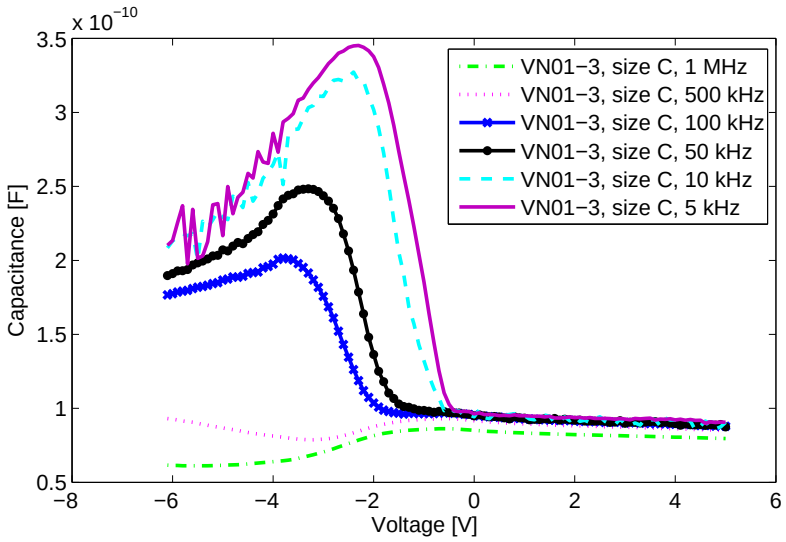

Figure 5.22: CV measurements of VN01_3 at six different frequencies.

CV measurements can be used to find the contact potential from the relationship between the capacitance and the depletion width:

$$C = \frac{\epsilon A}{W} = \frac{\epsilon A}{\sqrt{\frac{2\epsilon(V_0 - V)}{q}\left(\frac{1}{N_a} + \frac{1}{N_d}\right)}} \tag{5.5}$$

Because N_d in ITO is much larger than N_a in Si, and with some rearranging,

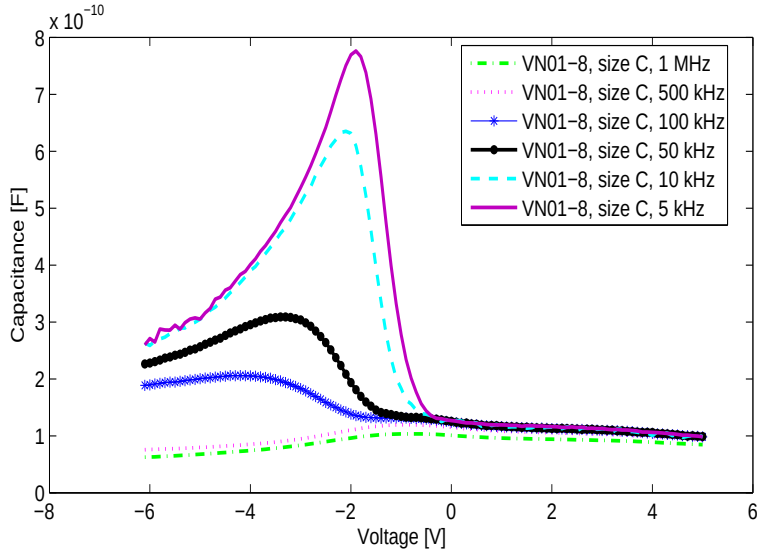

Figure 5.23: CV measurements of VN01_8 at six different frequencies.

this can be written as

$$\frac{1}{C^2} = \frac{2(V_0 - V)}{\epsilon A^2 q N_d} \tag{5.6}$$

The $1/C^2$ graph of VN01_8 is shown in Figure 5.24. When there is no applied voltage V, the x-intercept value is the contact potential V_0, which is -10.2 V. This value is much lower than the expected potential. An oxide layer between the metal and the semiconductor has been found to give an increased V_0 [107]. It is likely that bad quality IV characteristics also means the CV characteristics differ from the ideal case.

CV measurements can be used to estimate the equivalent oxide thickness of the Si NC layer [110, 111]. Kanbur et al. [111] used high frequency measurements to find the oxide capacitance C_i from its relation to the oxide thickness $C_i = \epsilon_i/d$, with $\epsilon_i = 3.8\epsilon_0$. Based on the accumulation value of the 1 MHz measurements of VN01_3 and VN01_8, the thicknesses estimated are 655 nm and 671 nm, respectively. This is much larger than the estimated thickness based on the structure of the sample, which is about 150 nm for VN01_8 and 100 nm for VN01_3. It is also expected that the dielectric

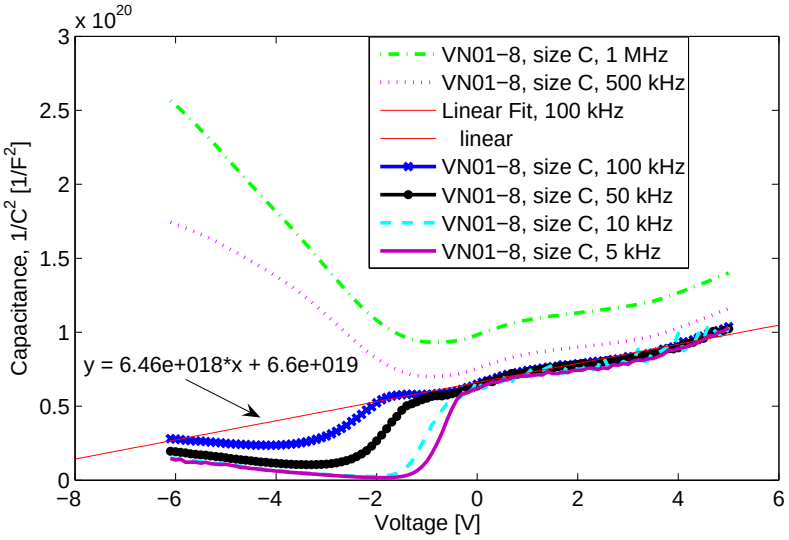

Figure 5.24: Equation 5.6 plotted for VN01_8 at 1 MHz with a linear fit of the 100 kHz measurement from 0 V to 5 V.

constant of the SiO_2 will be higher because of the charges in the Si NCs.

If considering the maximum values of the low frequency measurents as the oxide capacitance, as proposed by another study [106], the estimated equivalent oxide thickness of VN01_3 is 120 nm and 53 nm for VN01_8. These values are closer to the real values, but it is unexpected that VN01_3 is thicker than VN01_8. It is likely that the uncertainties are simply too large to use the CV measurements for calculations.

Chapter 6

Summary

6.1 Conclusions

Fabrication steps leading toward SiGe/Ge core-shell nanowires have been investigated. Magnetron sputtering was done to get SiGe films, and patterning of the films was done by photolithography. The resulting column structures were oxidized to reduce their size and create a SiGe/Ge core-shell structure with a layer of SiO_2 on the outside.

Sputtering depositions were done to get a supply of cheap SiGe films. The films were amorphous even at a sputtering substrate temperature of 650°C, and contained a large amount of oxygen. The oxygen was found to be uniformly distributed in the sputtered SiGe layer. The average oxygen content of the films sputtered at high temperature was 29%, and 52% for room temperature depositions. The reason for the high oxygen content was not found.

Oxidation was studied on flat samples because this is a critical process in the fabrication of SiGe nanowires. Epitaxially grown SiGe layers with 15% and 20% Ge were oxidized and investigated using RBS with trends similar to those found in previous studies. The Ge pileup region was found to have between 57 and 65% Ge for the SiGe sample with 20% Ge, and between 34

and 44% for the SiGe sample with 15% Ge. This is a relationship that needs further study because it is important for potential applications making use of the pileup layer.

The thickness of the Ge pileup region is found to be linearly dependent on the SiO_2. Deviations from this linearity are concluded to be because of low resolution measurements and the simulation of these. Other problems with RBS simulations are also discussed. Ge was found in the SiO_2 layer in the samples oxidized at 800°C, 850°C, 950°C and 1000°C, and the (Si,Ge)O_2 was on the surface of the pure SiO_2 layer.

Photolithography was done to create column structures, but electron beam lithography or catalytic etching is suggested for smaller structures. The samples were etched in a solution of HF:H_2O_2:H_2O, which etched SiGe preferentially to Si. SCM was investigated as a characterization technique for the structured and oxidized SiGe films. Because of the low quality of the SiGe films, and the restrictions of the SCM, it is concluded that SCM is not a good characterization tool for SiGe nanowires.

The electrical characterization of Si nanocrystals embedded in a SiO_2 matrix with ITO contacts and a p-type Si substrate was done. The MOS-like structures showed diode characteristics, but with a large leakage current and a high ideality factor. CV measurements also deviated from those of more ideal MOS capacitors with large voltage dependencies of the capacitance in the accumulation region. An attempt at finding the contact potensial and depletion width was made, but the deviations from ideal theory makes this complicated.

6.2 Suggestions for Further Work

The areas of sputtering, lithography, oxidation, RBS and SCM all need further research to optimize the fabrication of SiGe/Ge core-shell nanowires.

Oxidation studies are ongoing and the exact oxidation mechanisms of

SiGe are still not known. To be used in nanowire technology, the oxidation needs to be well understood and controllable. Much research has been done on getting rid of the Ge pileup region, and less on the formation of it. With a proper understanding, the pileup region can be adjusted to fit band gap requirements in applications.

Investigations into the parameters of SiGe sputtering only scratched the surface. The exact sputtering yield of the individual components of SiGe are not known, but should be known for various compositions. All sputtering parameters, including power, working pressure, use of different gases, and temperatures, will have an effect on the crystalline quality of the deposited SiGe films. Not many studies have been done on this topic, but it can be useful for creating cheaper SiGe films.

The method of nanowire fabrication used in this thesis is not satisfactory. Photolithography does not have a high enough resolution to make nanowires of the size needed for applications. The oxidation of these wires will make them smaller, but there are limits caused by the Ge pileup. Other means of creating nanowires should be investigated. This thesis was not able to show the fabrication of SiGe/Ge core-shell nanowires, but it is a step in the right direction and a possible starting point for others who wish to attempt the same.

A thin oxide was grown on the SiGe column structures for characterization with SCM. It would be interesting to investigate the effect of longer oxidation times on these samples. It is not certain that the columns would be oxidized uniformly or that the core-shell structure would remain. The characterization of these structures could be done with the TEM.

Appendix A

RBS Spectra of Oxidized SiGe

A.1 Epitaxially Grown SiGe

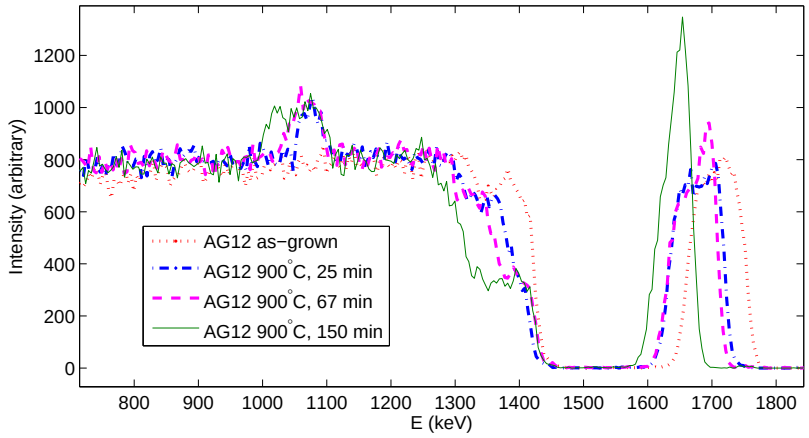

Figure A.1: RBS data for AG12, oxidations at 900°C. The as-grown Ge peak and Si shelf have a large abnormality in the measurement. It is an abnormality because it is not possible to get a fit for this shape, and it is likely a bad measurement.

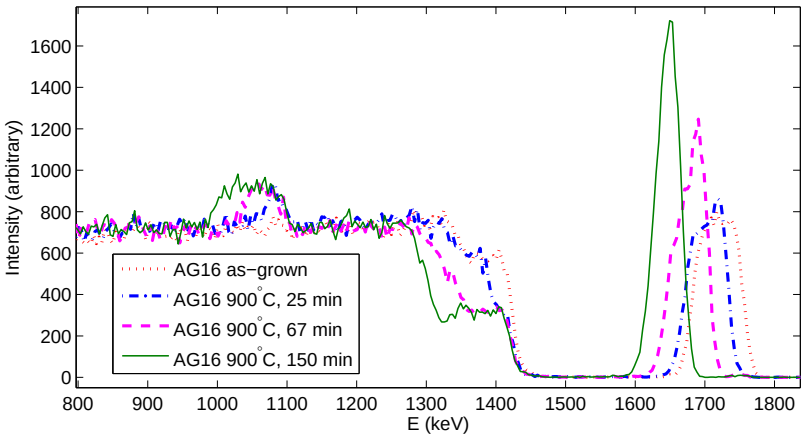

Figure A.2: RBS data for AG16, oxidations at 900°C.

Appendix B

Procedures

B.1 RCA Cleaning

The RCA clean is a commonly used cleaning of samples. The procedure used in this thesis is as follows:

Step 1

- Chemicals: NH_4OH:H_2O_2:H_2O in a 1:1:5 ratio
- Parameters: 15 minutes at 75°C, followed by a 5 minute bubble rinse
- Use: Removes organic residues.

Step 2

- Chemicals: HF:H_2O in a 1:50 ratio
- Parameters: 10 seconds at room temperature, followed by a 30 second bubble rinse
- Use: Removes oxide.

Step 3

- Chemicals: HCl:H_2O_2:H_2O in a 1:1:5 ratio
- Parameters: 15 minutes at 75°C, followed by a 5 minute bubble rinse
- Use: Removes ionic contamination.

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