UNIVERSITY OF OSLO
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Two lateral RF MEMS varactors and an experimental switch made using a CMOS-MEMS process

Master Thesis

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Abstract

An expanding wireless industry creates a demand for smaller and smarter devices, while maintaining the high performance requirements. Todays solutions often use off-chip components to meet these demands, which lead to additional area, cost and parasitic components. RF MEMS can beneficially replace a great number of these components, and in integration with CMOS offer small devices at low cost with on-chip signal processing.

One important component in RF systems is the variable capacitor, or varactor. This thesis presents two varactor designs made using a CMOS-MEMS process that enable monolithic integration of MEMS and CMOS. The varactors are electrothermal actuated and based on interdigitated combs moving lateral, parallel to the substrate. A latch mechanism is used so that the varactors only require power when switching. Since the fabricated circuit did not arrive in time for measurements only calculated and simulated results are presented. Bimetal actuator theory is used for theoretical understanding of the actuator and the various design parameters are thoroughly analyzed and discussed. The capacitances of the varactors is in the range of $133 - 897fF$, with tuning ranges of 440% and 489% and Q-factors of ~ 30 at $2GHz$.

In addition an experimental lateral DC series switch has been made. The purpose of this switch is to investigate how well defined the sidewalls of this CMOS-MEMS process are to determine if it is possible to obtain a good metal-to-metal connection. This work will be important for future work on CMOS-MEMS switches.

All simulations have been done using Coventorware, while the layout of the chip has been made in Cadence. The chip has been fabricated in a $0.25\mu m$ CMOS process from STMicroelectronics through the broker service Circuit Multi Projects (CMP), France. The post-process has been done at Carnegie Mellon University (CMU), USA and Sintef, Norway.

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Chapter 1

Introduction

The earliest attempt to build micromechanical elements can be found as far back as the 1960s, in the beginning of the integrated circuit (IC) industry [1]. However, this work was never refined for any commercial adoption, and MicroElectroMechanical Systems (MEMS) as we know it today can be dated back to the beginning of the 1980s with the first approaches to use silicon as a mechanical material [2][3]. During the last centuries MEMS have seen a rapid development and are today used in a range of applications such as cars, projector displays, mobile phones, etc.

The motivation for MEMS is the need for communication between the ICs and the real-world, better known as sensors and actuators. These components were and are often still today non-electrical off-chip components that lead to additional parasitic elements, area and cost. Even though a wide range of MEMS devices such as accelerometers, pressure sensors, chemical sensors and gyroscopes have been made, MEMS are still in its early stage and many challenges lies ahead.

One of the promising areas for MEMS is the expanding communication industry that creates a demand for smaller and smarter wireless devices at low cost. Many of the radio frequency (RF) systems in use today use off-chip components such as external inductors, crystals, SAW and ceramic filters to meet the high performance requirements. These off-chip components are often costly, have a high power consumption and are a major obstacle in order to a achieve miniaturization. Micromechanical components can beneficially replace a great number of these off-chip components, and in combination with CMOS make smaller systems with high performance on-chip signal processing.

Although MEMS shows promising results there are still some challenges remaining concerning both performance and fabrication techniques. One of the main challenges is integration with CMOS for miniaturization and on-chip signal processing. Several methods have been proposed to solve this, and in the beginning of this thesis an overview of some of these methods

will be presented. The Nano and Microelectronics group at the University of Oslo (UoO) have used one of these approaches to make a fully integrated MEMS and CMOS circuit with good results [4]. The fabricated circuit for this thesis is the second of this kind to be made at UoO [5].

One important component in RF systems is the variable capacitor, or varactor. Varactors can be used for many RF applications such as low noise amplifiers, filters, oscillators and mixers [6, 7]. Modern RF systems need to work for a large range of frequencies, which requires varactors with large tuning range to cover the entire frequency band of interest while maintaining a high quality factor (Q). Most high frequency applications today are forced to use off-chip inductors and varactors to meet these demands. Several MEMS varactors with high Q-factor and large tuning range have been made, and it is not unlikely that micromechanical varactors can replace a great number of these off-chip passive component in near future.

However, combining the need of high-Q varactors with large tuning range with the wish to combine MEMS and CMOS on the same integrated system creates new difficulties. In this thesis two varactor designs with high tuning ranges and high Q-factors have been made using a fabrication technique that allows complete integration of MEMS and CMOS. The varactors are electrothermal actuated and are based on the work of Altug Oz from Carnegie Mellon University (CMU), USA [8, 9]. The actuators moves a set of combs lateral, parallel to the substrate, and a latch mechanism is used so that the varactors only have a dynamic power consumption. The various design parameters of the actuator and the varactors are thoroughly analyzed and discussed, but since the fabricated chip was not finished in time for measurements only calculated and simulated results are presented. In addition an experimental switch has been made to examine how well defined the sidewalls of the CMOS-MEMS structures are after the release etch. This experiment will be important for future work on CMOS-MEMS switches.

All simulations have been done using Coventorware, while the layout of the chip has been made in Cadence. The chip has been fabricated in a $0.25\mu m$ CMOS process from STMicroelectronics through the broker service Circuit Multi Projects (CMP), France. The post-process has been done at CMU, USA and Sintef, Norway.

1.1 Thesis overview

- **Chapter 2: CMOS-MEMS** - The basic concept of CMOS-MEMS will be explained followed by a short overview of some of the different fabrication methods. In the end of the chapter various challenges with the chosen method, details about the fabrication process and the simulation parameters used in this thesis will be presented.

- **Chapter 3: System overview** - The principle of operation for the varactors, the latch mechanism and the switch are explained.
- **Chapter 4: Actuators, design and modeling** - The most common actuation methods are presented followed by a more detailed explanation of the electrothermal actuator used in this thesis. Bimetal actuator theory is used for to predict the effect of the different design parameters before the actuator is analyzed and discussed. At the end of the chapter, a short summary, the design parameters used for the fabricated circuit and the layout of the actuator is presented before the latch mechanism is explained.
- **Chapter 5: Tunable capacitors, design and modeling** - Various tunable capacitor topologies are presented followed by a more detailed explanation about the two designs made in this thesis. The analytic equations and the simulation models are explained, and in the end of the chapter the calculated and simulated results and the layout of the varactor can be found.
- **Chapter 6: Experimental switch** - A short overview of MEMS switches in general followed be the design, modeling and the layout of the experimental switch.
- **Chapter 7: Summary and discussion** - A short summary of the achieved results followed by a discussion of remaining challenges and suggestions for improvements. At the end of the chapter a short comparison between the varactors made in this thesis and state-of-the-art MEMS is presented.
- **Chapter 8: Conclusion** - The thesis is concluded followed by suggestions to future work.

Chapter 2

CMOS-MEMS

2.1 What is CMOS-MEMS?

MEMS fabrication processes are often special and unique for each device. The wish to standardize the fabrication process and to integrate both MEMS and CMOS on the same chip is the motivation for CMOS-MEMS. CMOS fabrication has many advantages. It is fast, repeatable, reliable, economical, available through external foundries and because CMOS is the leading technology in IC design there are a lot of investments for upgrading. Having CMOS and MEMS on the same chip will lead to smaller devices, less parasitic components, reduce routing noise and allow on-chip signal processing. Integration of MEMS and CMOS can be categorized in three different categories pre-, intermediate- and post-CMOS [10].

In pre-CMOS the MEMS structures are formed before the CMOS process. This method gives the opportunity to optimize the MEMS structures while obtaining integration between CMOS and MEMS. The drawback is that it is often large topographic differences after MEMS fabrication, which makes it necessary to planarize the surface before CMOS production. In addition, most CMOS foundries are unwilling to accept "dirty" MEMS wafers in their production lines, and due to high temperature during processing they will not accept use of low melting point metals such as aluminum [11]. Sandia National Laboratories have however come up with a solution for this, where the MEMS structures are embedded in an anisotropic etch trench in the substrate, the trench is then filled with oxide and chemical-mechanically polished before it is sealed with a nitride cap prior to the CMOS fabrication, as shown in figure 2.1 [12].

An alternative method is intermediate-CMOS where the CMOS process is interrupted to add additional thin film or micromachining steps. This method gives some limitations concerning optimization of the MEMS structures, and requires that the CMOS foundries are willing to add additional micromachining steps to their fabrication process. Some

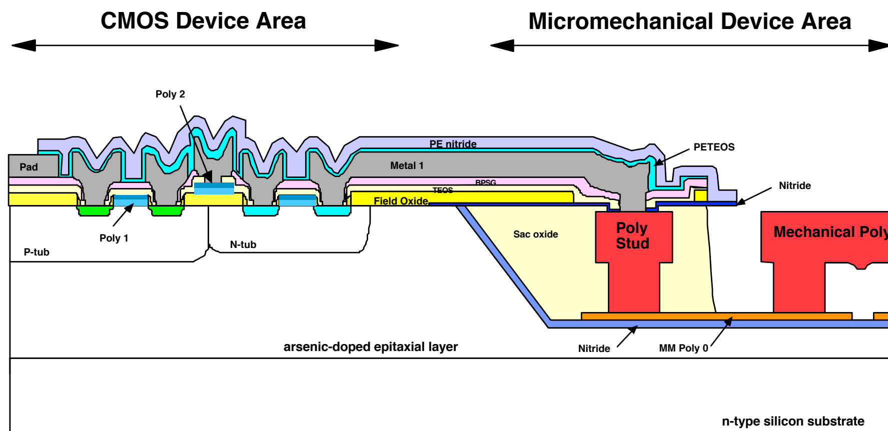


Figure 2.1: Cross section of Sandias pre-CMOS process [12]

structures have been made using this method e.g. an accelerometer from Analog Devices [13]

The MEMS structures can also be built after the CMOS process. There are two different strategies for post-CMOS. The first one is based on building the MEMS structure completely on top of the CMOS structure, leaving the CMOS layers untouched. The problems with pre-CMOS was large topographic differences and to get the CMOS foundries to accept the "dirty" MEMS wafer into their production lines. Since the surface of the CMOS wafer is planar after fabrication these problems are avoided with this method. There is however a problem concerning the optimization of the MEMS structure, since the CMOS structure contains low melting point metals such as aluminum. This means that high temperature MEMS processing steps can destroy the CMOS metalization, and the MEMS structures are therefore limited to materials that can be fabricated at low temperature. One solution to solve this problem is to change the aluminum in the CMOS process with tungsten that can withstand a much higher temperature.

The second strategy is what we in this thesis refer to as CMOS-MEMS and is based on building the MEMS structures in a standard CMOS process, without any additional processing steps, followed by a simple post-process to release the movable parts. This method uses only CMOS materials and achieves complete integration of MEMS and CMOS. The following sections will give a short overview of some different post-processes used for CMOS-MEMS fabrication.

CMOS-MEMS have some disadvantages and introduces new challenges like out-of-plane curl, a restricted set of available materials and producing vertical multilevel structures. This will be further discussed in section 2.3.

2.2 Fabrication

There are several different methods for the CMOS-MEMS post-process. This section contains a short overview of four different methods and their advantages and disadvantages. These methods are from CMU in USA (section 2.2.1 and 2.2.3) and National Chung Hsing University in Taiwan (section 2.2.2 and 2.2.4). The etchants used for these examples are taken from the articles referred to, but some of the methods can be done with other etchants as well.

CMOS-MEMS post-processing contains several etch step. These steps can be both isotropic or anisotropic. Isotropic etch provides the same etch rate in all directions while anisotropic etch provide different etch rates in different directions, as seen in figure 2.2.

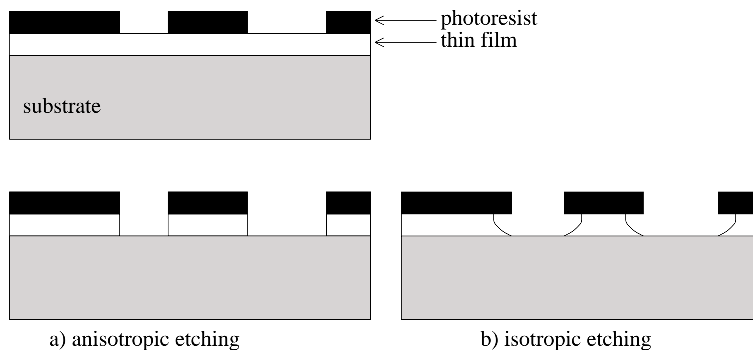


Figure 2.2: Schematic of isotropic and anisotropic thin-film etching

2.2.1 Maskless post-processing

The first post-process is based on using the top metal layer in the CMOS process as an etch-resistant mask [14]. The circuit is produced in a standard CMOS process, followed by a post-process consisting of three dry etch steps, as shown in figure 2.3. The first step is an anisotropic CHF_3/O_2 reactive ion etch (RIE) (b). This step forms the structural sidewalls masked by the top metal layer. The next step is an anisotropic silicon etch, using SF_6/O_2, to extend the structural sidewalls into the substrate (c), and the final step is an isotropic plasma etch using SF_6 (d). This step removes the bulk silicon and releases the movable parts.

The advantages of this method is that it is simple. Because it does not need any additional masks it can be performed on a single chip that gives the opportunity to use Multi Project Wafers (MPW, many different projects on the same wafer). Maskless post-processing demands less equipment and uses

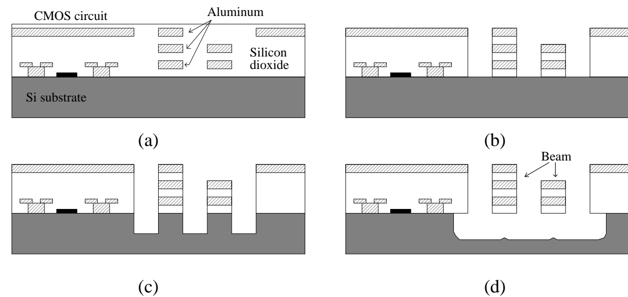


Figure 2.3: Schematic of the maskless post-processing

only CMOS materials, which gives it an economical advantage compared to some of the other post-processes. Lateral actuation and movement is typical for this process, while the electrode gap will be defined by the precision of the fabrication process as specified by geometrical design rules. Since this post-process makes it impossible to produce underlying electrodes it is difficult to make vertical structures (this can be done using bimetal thermal actuation, as shown in section 4.1.2). This will also be a problem for the post-process using a PR-mask (2.2.2) and the post-process using a backside etch (2.2.3), while the post-process using a single wet etch gives the opportunity for underlying electrode, as seen in section 2.2.4.

2.2.2 Post-processing using a photoresist (PR) mask

The second post-process is based on adding a PR layer, which is patterned with a photo mask before the etch process [15]. CF_4/O_2 is used for the oxide etch, while SF_6/O_2 is used for the silicon etch. The etch process contains the same three etch steps as the maskless post-process in section 2.2.1, and after the etching process the PR mask is removed. The PR mask helps to protect the bonding pads and the need of floating metal layers to protect the CMOS circuit is unnecessary. The test results by Dai et al. shows that the performance of the circuit is almost the same before and after the post-processing when using a PR mask.

One problem with this method was that the PR mask was burned during RIE because of the high temperature. The burnt PR mask was very difficult or impossible to remove. This problem was solved by reducing the etching time and repeat the etching process three times. However, adding and removing the PR mask is a technically difficult process and can not be done on a single chip without special equipment. This means that a Single Project Wafer (SPW, just one project on the entire wafer) has to be used, or a special platform to handle single chips has to be build. Because of these problems using a PR mask gives an additional cost compared to the maskless post-process discussed in the previous section.

2.2.3 Maskless post-processing using a backside etch

The third post-process is quite different from the first two and the schematic of the post-process is shown in figure 2.4 [16, 17]. The first etch step is a backside deep reactive ion etch (DRIE) that thins the substrate leaving a 10-100 μm thick silicon membrane (a). The next step is a front-side anisotropic RIE of the dielectric layers masked by the top metal layer (b). For the previous methods the last step was an isotropic silicon etch to release the movable part, whereas in this method the last step is an anisotropic etch leaving a thick silicon layer on the microstructure (c). In addition an optional lateral underetch can be used to remove the silicon layer under small beams to achieve e.g. electrical isolation of certain silicon areas (d). With this method thicker MEMS structures can be made, which gives less out-of-plane curl (see section 2.3.1) and it is advantages if large mass is required. On the other hand, this method gives an additional economical cost and technological difficulties.

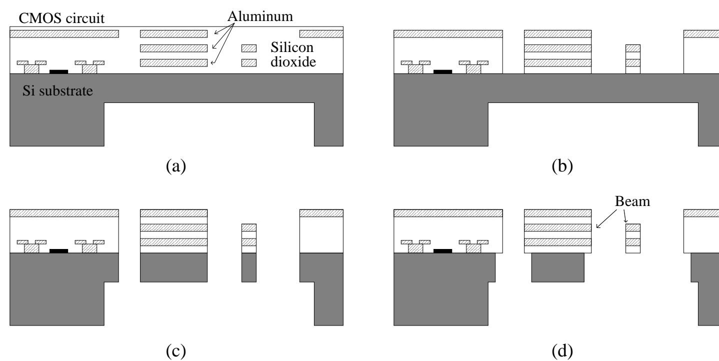


Figure 2.4: Schematic of the post-processing using a backside etch

2.2.4 Maskless post-processing using a single wet etch

The last post-process makes it possible to fabricate vertical movable structures in CMOS-MEMS, and contains only one etch step [18, 19]. The post-process is done as shown in figure 2.5, with a wet etch using silox vapox III etchant and with the metal layers as an etch-resistant mask. This method has low cost, is easily executed and solves the problem of making vertical structures in CMOS-MEMS, and has been used to make switches and resonators with good results [18, 19, 20]. However, it has only been demonstrated for vertical movement, and it is uncertain how it will work for structures moving lateral. The reason for this is that it can not be used to make layered microstructures of metal and silicon dioxide.

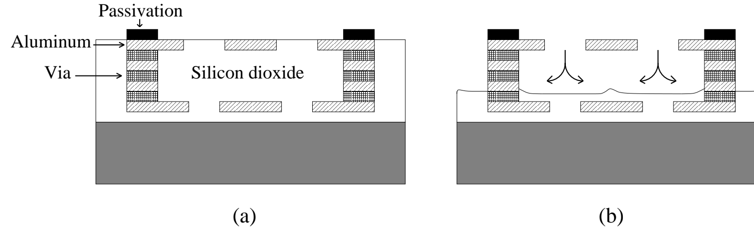


Figure 2.5: Schematic of the post-processing using a single wet etch

2.3 Challenges with CMOS-MEMS

For this thesis the maskless post-process explained in section 2.2.1 is used. This process enables fabrication of layered microstructures for lateral movement at low cost, allows complete integration with CMOS and is easily executed. But there are some disadvantages and remaining challenges. Due to the simplicity of the process the materials available for fabrication will be limited by the CMOS process, and although various combination of the different metal layers can be used, all microstructures will have a layered composition of metal and dielectric. As mentioned, it is also impossible to make underlying electrodes, which makes vertical movement difficult. In addition to this the structures tend to curl after release due to built-in stress during fabrication. This curl is one of the main challenges with this CMOS-MEMS process and will be further discussed in the following sections.

2.3.1 Out-of-plane curl

After release CMOS-MEMS structures tend to get an out-of-plane curl due to built-in residual stress during CMOS processing. This effect occurs because residual stress in the metal is tensile, while it is compressive in the surrounding dielectric. In other words, the the metal will contract while the silicon dioxide will expand when released and the structure will curl, as shown in figure 2.6. The out-of-plane curl can lead to an offset between lateral electrodes or sensing nodes that will lower the performance of the circuit or in worst case make it not working at all. Because of the different Temperature Coefficients of Expansion (TCE) in the metal and the silicon dioxide, the out-of-plane curl will also vary with temperature. Residual stress in the different layers vary for the different CMOS processes, and the out-of-plane curl can vary as much as 30% from run to run [21]. This means that it is hard to predict how much a structure will curl, and an error due to curling will vary with both temperature, process and from run to run.

Various methods can be used to minimize this effect, both by the designer and by optimizing the fabrication technique.

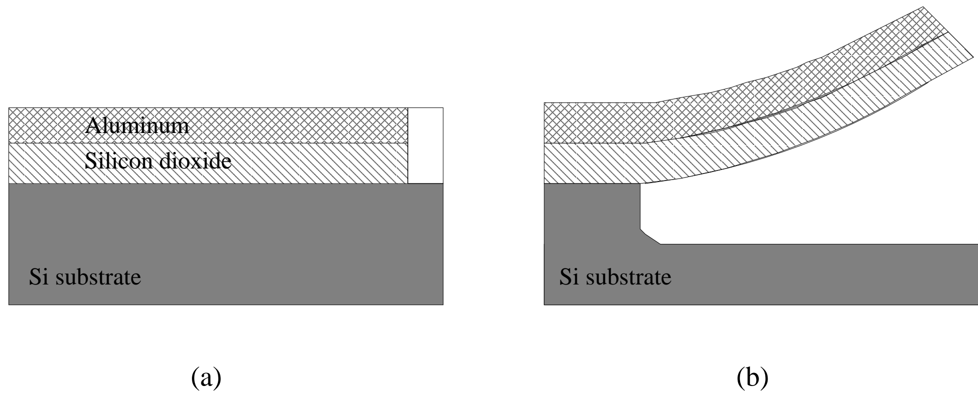


Figure 2.6: (a) Micromachined beam before release (b) Curled micromachined beam after release

One important design technique to minimize the effect of out-of-plane curl is to use a curl compensation frame [22]. In traditional MEMS design the anchors for two beams are often placed on the opposite side of each other, as shown in figure 2.7 (a). In CMOS-MEMS these beams will curl in opposite directions when released (b), which will reduce the sidewall capacitance significantly and give large variations with temperature, process and from run to run. It is therefore important to have the anchors aligned along a common axis (c), and to build a curl compensation frame which will curl in the same direction as the rest of the structure, as shown in figure 2.7 (d). A curl compensation frame will optimize the sidewall capacitance, lead to better temperature stability and more accurate results from run to run. However, due to fabrication mismatches it is difficult to get equal curl for large structures, even if a curl compensation frame is used.

A different method to compensate for mismatch between electrodes or sensing nodes are temperature stabilization. By having embedded polyheaters in the structure it is possible to use these to compensate for any misalignments due to curl. By heating the structure it will bend down again because of different TCEs in the metal and the silicon dioxide. This technique is used in addition to a curl compensation frame as a fine tuning of the structures after production. An accelerometer using this technique has been made by Lakdawala et.al. [23], and it gained an improved DC bias stability from $1.7G$ ℃$^{-1}$ to $42mG$ ℃$^{-1}$, and the sensitivity variation was reduced from 60% to 18%

Modern CMOS processes need better stress matching between the metal and the silicon dioxide to enable chemical-mechanically polishing of wafers with a diameter of 8" or above (minimum gate lengths better or equal to

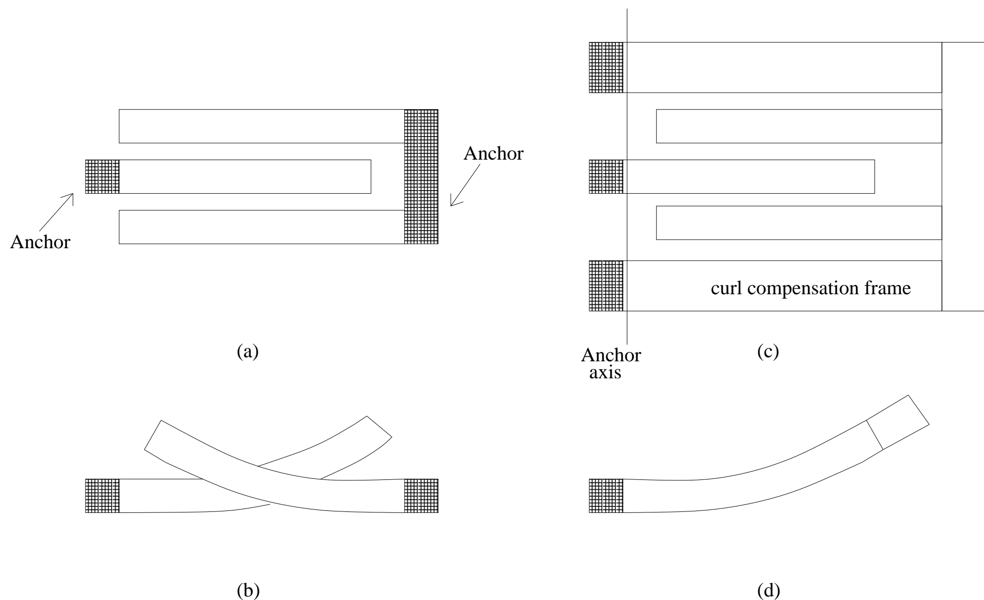


Figure 2.7: (a) Traditional MEMS design, top view (b) Traditional MEMS design, side view (c) Aligned along a common anchor axis, top view (d) Aligned along a common anchor axis, side view

$0.35\mu m$) without delamination of the thin films [11]. This will automatically lead to less out-of-plane curl for CMOS-MEMS structures made in modern CMOS processes. Although modern CMOS processes have less built-in stress, the field oxide has high compressive stress for all processes. It is therefore important that the designer removes this for the MEMS structures. This can be done by using the "active" or "OD" mask in the layout, which removes the field oxide and leaves a thin oxide layer beneath the structure (same as is used for the thin oxide beneath the gate of a transistor).

2.3.2 Lateral curl

Lateral curl occurs because of lateral offset between the different metal layers. If a lower metal layer has a small offset compared to the metal layer above there will be some silicon dioxide beside the metal after post-processing, and due to the different stresses in the metal and the silicon dioxide, the structure curls. Offset between the different metal layers is a result of manufacturing misalignment due to the finite precision of the photolithography. For some applications a small lateral displacement will be crucial, but as for the out-of-plane curl some curl matching techniques have been proposed. One of these techniques is the tapered beam structure [24], where the lower metal layers are made wider, as shown in figure 2.8. If the width different is larger

than the photolithography error there will be no silicon dioxide at the side of the metal layers, which will lead to a significant reduction in lateral curl. However, lateral curl can be exploited to a benefit as for the electrothermal bimetal lateral actuator in chapter 4.

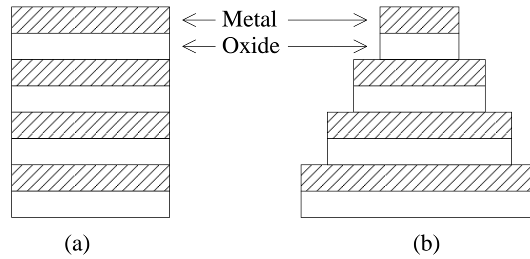


Figure 2.8: (a) Regular beam (b) Tapered beam

2.4 CMOS-MEMS modeling in Coventorware

All structures in this thesis were modeled using Finite Element Method (FEM) analysis in Coventorware, and have a layered composition of metal and silicon dioxide, where the top metal layer is used as an etch-resistant mask.

The main challenge in modeling CMOS-MEMS is the out-of-plane and lateral curl. Curling can lead to offset between sensing nodes, and different curl-matching techniques must be used to minimize this effect. Modeling of this is important in order to predict and verify curl in different structures. The different built-in stresses in metal and silicon dioxide is caused by high deposition temperature during fabrication. The simulation software do not consider this when building a model with layers of metal and silicon dioxide. In other words, a modeled CMOS-MEMS beam will lack the built-in stress and will not initially curl. In addition the built-in stress can not be put directly into the simulation model as a parameter. Therefore an alternative method has to be used in order to model the out-of-plane and lateral curl. Only the out-of-plane curl will be discussed in this section, but this method will also model the lateral curl.

As mentioned earlier a CMOS-MEMS beam will curl back in plane when heated due to the different TCEs in the metal and the silicon dioxide. Since the structure will curl back in plane when heated it will also curl out-of-plane when cooled down. This means that by lowering the temperature during simulations we will be able to model the out-of-plane curl caused by built-in stress. Figure 2.9 shows the displacement out of the plane for

a beam with layers of metal and silicon dioxide modeled in Coventorware for a temperature range from $100 - 400K$. The figure shows that the beam will curl out-of-plane for low temperatures and back in the plane for high temperatures.

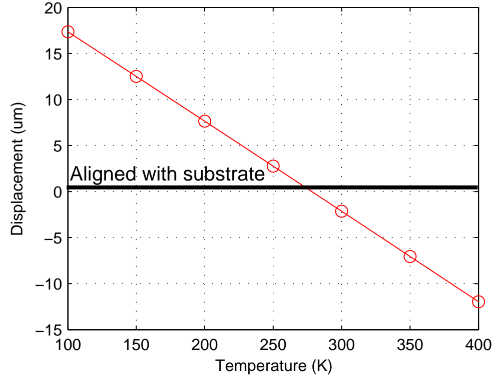


Figure 2.9: The displacement of a layered beam in Coventorware for a temperature range of $100 - 400K$

Lakdawala [21, 25] has defined a characteristic temperature T_0 for CMOS mikromachined beams. This temperature has been derived experimentally for different CMOS-MEMS cantilever beams, and is the temperature where the beam is completely flat (aligned with the substrate). At this temperature the displacement caused by heating the CMOS-MEMS beam is equal to the displacement caused by built-in stress during fabrication. This temperature can be used to set a simulation temperature

$$T_{set} = -T_0 + T_{sim} + T_d \tag{2.1}$$

where T_{sim} is the initial temperature of the simulator and T_d is the ambient temperature. Equation (2.1) gives an offset temperature that can be used to model the curling due to built-in stress. This is done by setting the temperature of all the layers in the simulator to T_{set}. However, this will only give a approximately curl because of the huge variation in CMOS micromachined structures from run to run (30%). The simulation temperature used for the structures in this thesis will be presented in the following section.

2.5 Overview of fabrication processes and simulation parameters used for this thesis

All structures in this thesis are made in the $0.25\mu m$ SiGe BiCMOS process from STMicroelectronics (STM) and are post-processed at CMU and Sintef using the top metal layer as an etch-resistant mask, as explained in section 2.2.1. The STM BiCMOS process offers 5 metal layers, where the first metal layer is made of tungsten, the fifth has two options, either copper or aluminum and the rest of the layers are made of aluminum. All structures must follow the CMOS design rules from STM in order to be fabricated.

The post-process also has some restrictions concerning minimum gap size, minimum structure width, maximum structure width without etch holes, etc. These restrictions are due to fabrication techniques such as the RIE resolution and undercut of the structures for the last anisotropic etch step. CMU has provided special set of CMOS-MEMS design rules, which have to be met in addition to the CMOS design rules. It will be shown in the following chapters how these design rules influences the different designs

As mentioned in section 2.4 a temperature offset has to be used in order to model the out-of-plane curl. This is done by using equation (2.1) where the initial temperature of the simulator $T_{sim} = 273K$ for Coventorware and an ambient temperature from $T_d = 294K$ (room temperature, 21°C) to $T_d = 443K$ (170°C) are used for all structures. For temperatures higher than 170°C the material properties of the aluminum starts to change [21]. All structures are made with four metal layers and a polysilicon layer, and a characteristic temperature $T_0 = 328K$ is used. This gives a simulation temperature

$$T_{set} = -328K + 273K + T_d = -55K + T_d \tag{2.2}$$

$$238K \leq T_{set} \leq 367K \tag{2.3}$$

It should be mentioned that the connection beams of the switch are made without the polysilicon layer, but a characteristic temperature $T_0 = 328K$ is used for this simulation as well due to actuators.

Since we use a different CMOS process, with more metal layers and different built-in stresses, compared to what has been used by Lakdawala the characteristic temperature used in this thesis is not necessarily correct. The temperature used will give an approximate curl, but for future work the characteristic temperature for the STM $0.25\mu m$ BiCMOS process should be derived for more precise modeling.

The material properties for the different layers of the CMOS process vary from process to process. In addition there will be some variations between the different metal layers in a given process. However, most of this information is not available from the CMOS foundry. Therefore only the standard material

properties for the simulator have been used for modeling of the structures in this thesis. The different material properties used are shown in table 2.1.

Table 2.1: Material properties used for simulation

Material	**TCE** (K^{-1})	**Young's modulus** (GPa)
Aluminum (Al)	$2.31 \cdot 10^{-5}$	77
Tungsten (W)	$4.50 \cdot 10^{-6}$	410
Silicon dioxide (SiO_2)	$5.00 \cdot 10^{-7}$	70
Polysilicon	$3.50 \cdot 10^{-6}$	160

Chapter 3

System overview

Two lateral varactors and an experimental switch have been made. This chapter will give a short overview of the systems, where the different parts will be further discussed in the following chapters.

3.1 Varactors

Varactors are important parts of adaptive RF systems, and can be used in e.q. variable oscillators and filters. The varactors in this thesis are voltage controlled by electrothermal actuators. An actuator is a transducer that transforms electric energy to mechanical energy or vice versa. In this case electric current is transformed into heat to achieve a lateral displacement in order to change the capacitance.

A simplified version of the system is shown in figure 3.1. The actuators move the movable frame to the left when heated to increase the overlapping area of the fingers, and thereby increase the capacitance. The static combs are attached to a curl compensation frame so that the static combs curls in the same direction as the movable combs. The figure shows that the anchors are not properly aligned along a common axis as discussed in section 2.3.1, but since the difference is much smaller than the length of the structure the curl will still be approximately equal. However, it is important to remember that it is difficult to get good curl matching for large structures due to fabrication mismatches.

To minimize the power consumption a latch mechanism is introduced, so that the varactors only uses power when switching. The latch is controlled by a similar electrothermal actuator as is used to move the combs, and is used to lock the movable frame as shown in figure 3.1. A sketch showing the principle of operation for the latch is shown in figure 3.2. The actuator controlling the latch is first heated to unlock the structure. Then the actuators controlling the movable frame moves the combs to their desired position before the latch locks the movable frame as the current controlling the actuator of the latch

is shut off. A more detailed description of the latch can be found in section 4.5

Two lateral varactors have been made, and the principal of operation for both varactors are as explained above. However, there are some small differences between the designs. These differences will influence the gap between the fingers and the maximum overlapping area of the fingers.

Design A

In design A both actuators are active, and are designed such that they have an equal force in the same direction. In other words, one of the actuators will push the movable frame, while the other will pull. This is done to get maximal displacement and thereby maximum overlapping area of the fingers. However, there is a small problem with this approach. In order to get maximum displacement the fingers need to have a small overlap in the layout, and the gap between the fingers will then be limited by the post-CMOS design rules. This means that design A will get a larger overlapping area of the fingers, but also a larger finger gap than design B. Design A has a size of $424\mu m$ x $627\mu m$, without the anchors.

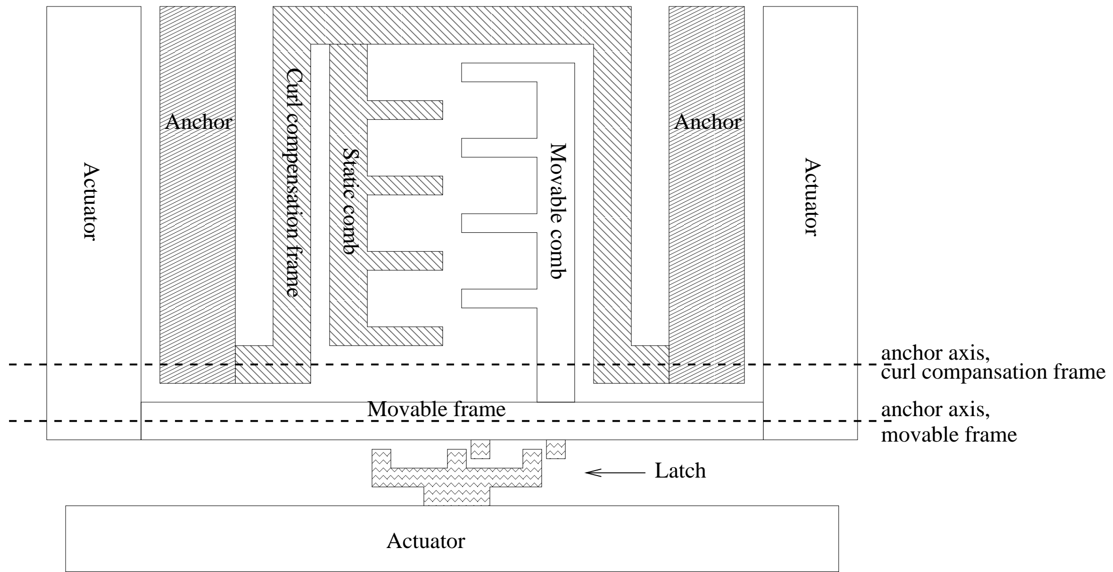
Design B

In design B only one of the actuators is active. The fingers are designed without any overlap in layout, and will not move after release. When heated, only one of the actuators will move the structure, while the other only works as a spring. In design A the gap between the fingers were limited by the post-CMOS design rules, but since this fingers have no overlap in the layout the gap between the fingers can theoretically be made infinite small. The finger gap for design B is only limited by fabrication mismatches such as width bloating that can cause the gap to be too small for the fingers to interdigitate. However, since the combs are designed to stay in the same position after release as in the layout the maximum overlapping area of the fingers will be smaller than for design A. Design B has a size of $424\mu m$ x $550\mu m$, without the anchors.

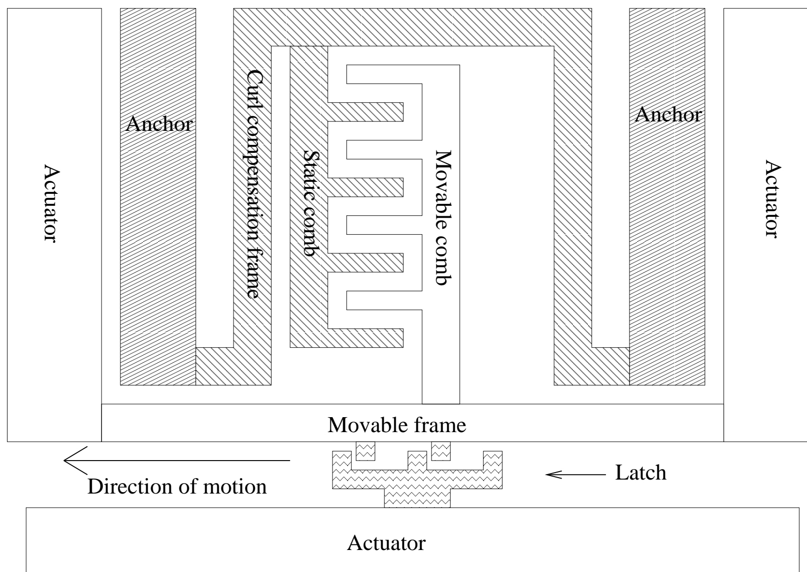
A more detailed description of the actuators and the varactor designs can be found in chapter 4 and 5.

3.2 Experimental switch

An experimental lateral DC switch has also been made, to investigate how well defined the sidewalls of the structures are, and if it is possible to get a good metal-to-metal connection. Since the post-CMOS structures are built with layers of metal and silicon dioxide, they will have smaller metal area



(a)



(b)

Figure 3.1: Simplified system overview (a) Idle state (C_{min}) (b) When heated (C_{max})

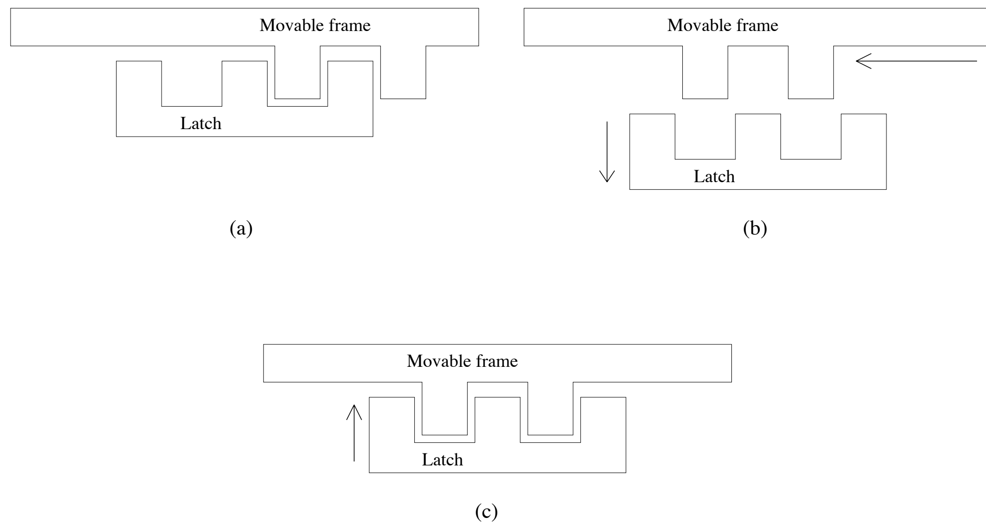


Figure 3.2: Principle of operation for the latch (a) Idle state (C_{min}) (b) When heated (c) Locked after heated (C_{max})

than regular MEMS structures. This means that any vertical offset between the beams can be crucial in order to obtain connection. Figure 3.3 shows the principle of operation for the switch, and it is implemented using the same electrothermal actuators as used for the varactors. The actuators are designed such that they will push the beams together when released to obtain connection, and pull them in the opposite direction to break the connection when heated. A similar latch mechanism as used for the varactors is added so that the switch only requires power when switching. This switch is designed to investigate the metal-to-metal connection for future research, and is so far not intended for any specific application. The switch has a size of $340\mu m$ x $302\mu m$, without the anchors. More details on the switch can be found in chapter 6.

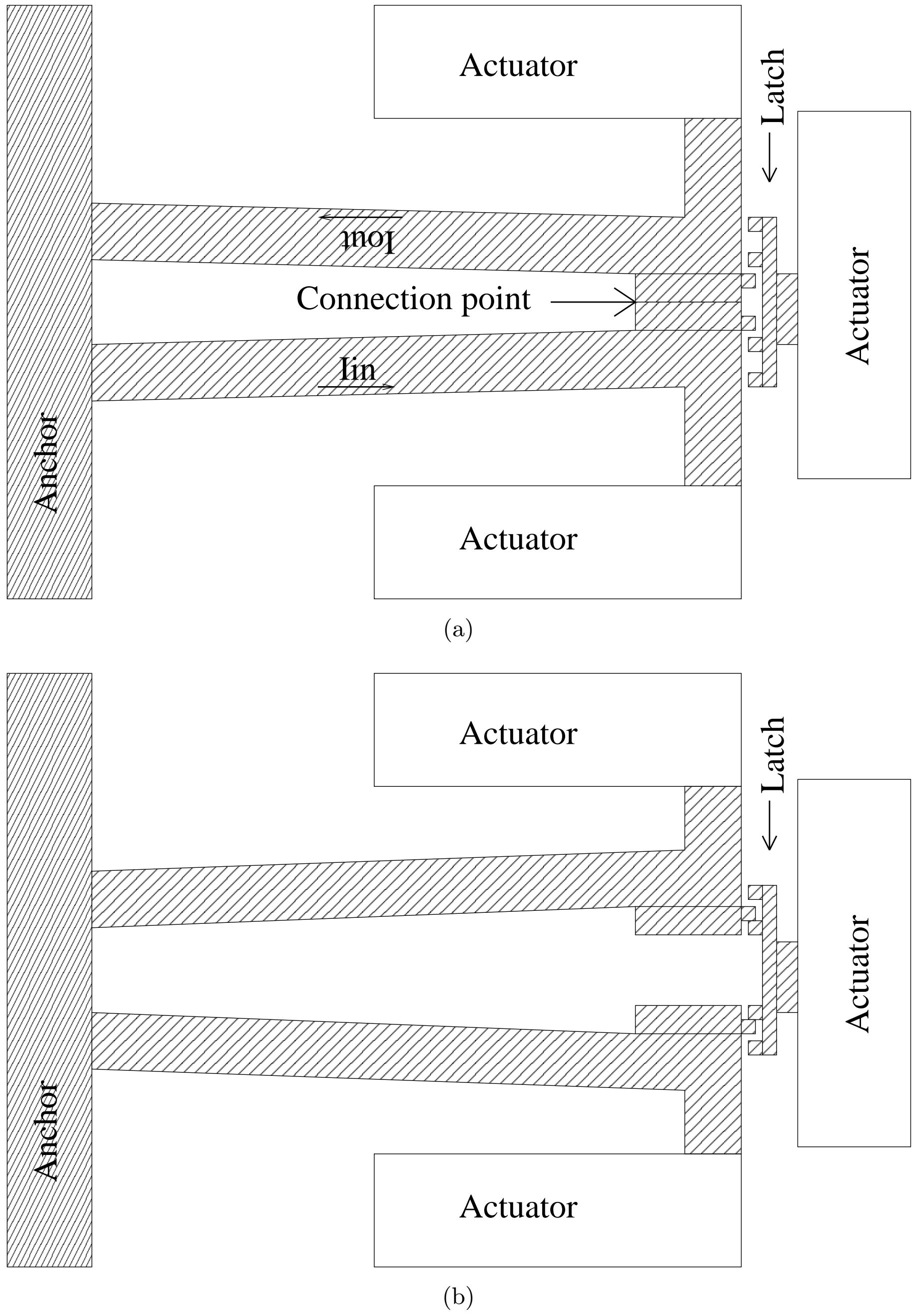


Figure 3.3: Principle of operation for the switch (a) Idle state (connected) (b) When heated (disconnected)

Chapter 4

Actuators, design and modeling

4.1 Actuator topologies

Actuators are used to transform electric energy to mechanical energy or vice versa, and are important parts of MEMS systems. Different actuator topologies are presented in this section with its pros and cons and its compatibility with CMOS-MEMS.

4.1.1 Electrostatic actuators

The most common actuator type for MEMS devices is the electrostatic actuator that is based on the electrostatic force between two conductors with different charge. The electrostatic force F is given by the capacitance C, the co-energy W^* and the voltage difference V between the conductors.

$$C = \frac{\epsilon A}{g} \tag{4.1}$$

$$W^* = \frac{1}{2} C V^2 \tag{4.2}$$

$$F = -\frac{\delta W^*}{\delta g} \tag{4.3}$$

$$F = \frac{\epsilon A}{2g^2} V^2 \tag{4.4}$$

where ϵ is the permittivity of the material (often air), A is the overlapping area and g is the gap.

Electrostatic actuators are often implemented by a capacitor structure with one fixed plate and one suspended plate free to move. By setting a voltage difference between the two plates an electrostatic force is produced according to equation (4.4), and the movable plate will be dragged towards the static plate. Electrostatic actuation is the most suitable actuation

method for RF systems because it is fast, but since the electrostatic force is weak an electrostatic actuator requires a large driving voltage. A challenge with the CMOS-MEMS process is that structures are built by layers of metal and silicon dioxide. Therefore the structures have a smaller metal area than other MEMS structures that results in a smaller electrostatic force according to equation (4.4). Maximum driving voltage is also limited, if the driving voltage is in contact with the CMOS circuitry.

4.1.2 Thermal actuators

Thermal actuation makes use of the ability of a material to deform when heated, and different materials or geometrical differences in the structure is used to induce motion.

Thermal actuators can be divided into three main groups, as shown in figure 4.1. For the first group the structures consist of only one material, and the geometrical differences determine the direction of motion. One famous example is the hot/cold arm thermal actuator, which consists of one thin arm and one wide arm (a) [26]. Both arms are exited with the same current, but because the electrical resistance for the thin arm is higher than for the wide arm, the temperature of the thin arm will be higher than for the wide arm. Since they are both made of the same material, the thin arm expand more than the wide arm, and lateral motion is induced.

The second group is often referred to as bimetal actuators and consist of at least two different materials (b). Heating a bimetal beam will cause one material to expand more than the other due to different TCEs and the beam will curl. Bimetallic thermal actuators are usually used for motion vertical to the substrate, but can also be used for lateral motion as shown in section 4.2.1. A more detailed explanation of bimetal actuators will be presented in the following sections.

The last group is called pneumatic actuators and uses thermal expansion of gas and liquid to induce motion (c) [27], but this method is not compatible with CMOS-MEMS.

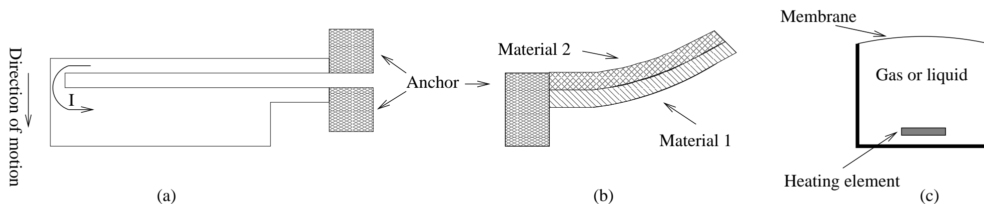


Figure 4.1: (a) Hot/cold arm actuator (b) Bimetal actuator (c) Pneumatic actuator

Most thermal actuators are heated by putting a voltage on a material with high resistance, and are often referred to as electrothermal actuators. The materials are heated according to Joule's law which states that a material generates some heat when exited with an electric current. The actuator presented in this thesis is an electrothermal actuator that is suitable for CMOS-MEMS, and exploits the difference in TCEs between metal and silicon dioxide to a benefit. Thermal actuators have greater deflection and energy density than electrostatic actuators, but are also much slower and often requires a larger area [7].

4.1.3 Other actuators

Other actuators such as magnetic actuators and piezoelectric actuators have been made [7]. Both of these actuator principles use materials that are not available in CMOS, and are therefore not possible to make in CMOS-MEMS.

4.2 Electrothermal actuator in CMOS-MEMS

The bimetallic electrothermal actuator used in this thesis was presented by Oz et al. [8, 9], and is based on exploiting the different stresses and TCEs in the metal and the silicon dioxide. The electrothermal actuator is used both for the varactors and the experimental switch.

4.2.1 Self-assembling and electrothermal actuator principles

Two actuators have been made (A and B). Both actuators are based on the same principle, which will be explained in this section. The CMOS structure is built by layers of metal, where the layers are separated by silicon dioxide. The actuators are based on lateral curl as explained in section 2.3.2, and motion is obtained with an asymmetric structure of metal and silicon dioxide. The top metal, used as an etch-resistant mask, covers the entire structure while the lower metal layers are used to induce motion. The lower metal layers have an offset to the top metal and are covering half of the beam for half of the beam length. This offset is opposite for the other half of the beam length, as shown in figure 4.2. The lateral curl explained in section 2.3.2 was due to unintentional offset between the metal layers. For the actuators in this thesis, the lateral curl is exploited to a benefit and cause the actuators to get a displacement $\Delta x_{release}$, once released. After release the actuators can be heated by a polysilicon-resistor placed at the bottom of the beams. When a current passes through the polysilicon-resistor it will be heated by Joule heating, and motion is induced due to the difference in TCEs between the different sides of the beams (metal side and silicon dioxide side). When heated the actuators gets a displacement Δx_{heated} in the opposite direction of the displacement when they were released. Δx_{heated} is measured from

the layout position of the actuator, and the total displacement is given by $\Delta x = \Delta x_{released} + \Delta x_{heated}$.

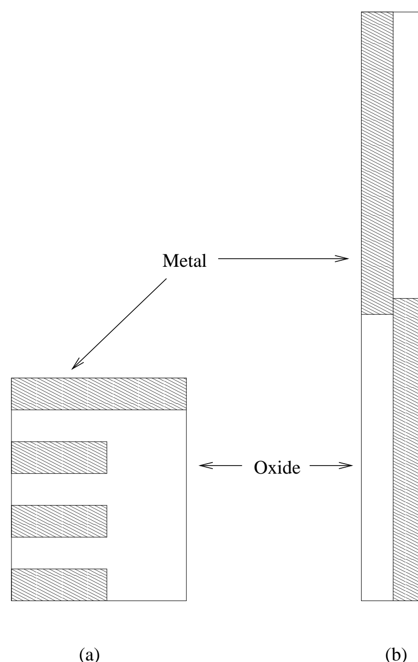


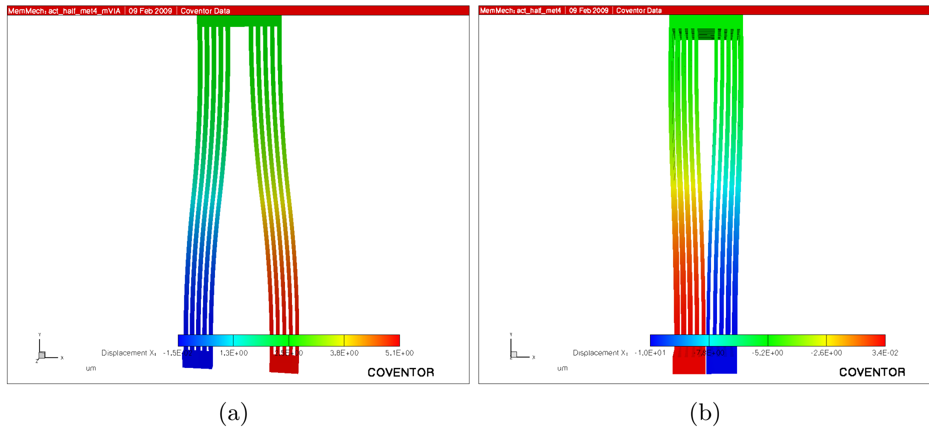
Figure 4.2: (a) Cross section of actuator beam (b) Top view of actuator beam

The actuator would have obtained maximum displacement if the different sides of the beams had been uniform. However, since the CMOS-MEMS structure consists of layers of metal and silicon dioxide, the average TCE on the metal side of the beams will be smaller. Another important factor is the top metal layer that covers the entire structure, and therefore increases the average TCE on the silicon dioxide side of the beams. These factors decrease the difference in TCEs between the metal and the silicon dioxide sides of the beams and lead to less displacement. How this effect influences the design of the actuator will be further discussed in the following sections.

Actuator A is designed to expand once released. The asymmetric structure makes the actuator move to an "S" shape after post-processing, as shown in figure 4.3(a). We call this effect self-assembling and it is exploited for one of the varactors in chapter 5. A more detailed description on how the self-assembly effect can be modeled is explained in section 4.3.1 and 4.3.2. When heated actuator A contracts, as shown in figure 4.3(b).

For actuator B the metal offset in the beams is changed to the other side of the beams, as shown in figure 4.4. This change makes the actuator contract instead of expand once released. The displacement for actuator B will

be almost equal to actuator A, but in the opposite direction. When heated actuator B expands.



(a) (b)

Figure 4.3: Actuator movements for design A (a) After release (b) Heated

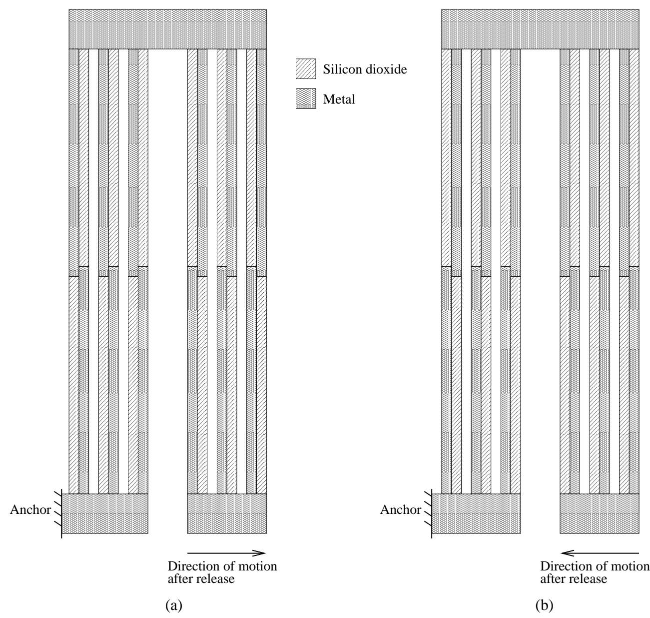


Figure 4.4: Actuator designs (a) design A (b) design B

4.3 Modeling

The displacement of the actuators determines the overlapping area of the fingers, and hence determines both the capacitance and the tuning range. A larger displacement allows a larger overlapping area, and it is therefore important to be aware of all the different factors that influence the displacement. Various design parameters, such as materials and geometry must be considered. In the beginning of this section the various parameters will be discussed, and at the end a short summary will be presented. The design parameters used for the fabricated circuit and the layout can be found in section 4.4. All simulations shown have been done for design A, but the conclusions drawn are also be valid for design B.

Analytic calculations for the CMOS-MEMS electrothermal actuator used in this thesis is complicated, so only simulated results will be presented. However, bimetal actuator theory can be used to predict the effect of the different parameters, and a short description of this theory and how it is related to the electrothermal actuator will be presented. FEM simulation was done using Coventorware, and the actuator has been simulated for a temperature range of 294-443K (21-170 ℃). To be able to model the curl a temperature offset is used, as explained in section 2.4. Due to this temperature offset the simulation temperature T_{set} is in the range of 238-367K.

4.3.1 Bimetal actuator theory

Mathematical model of bimetal actuators can be used for a theoretical understanding of the actuator. This model is only valid for a uniform beam, as shown in figure 4.5.

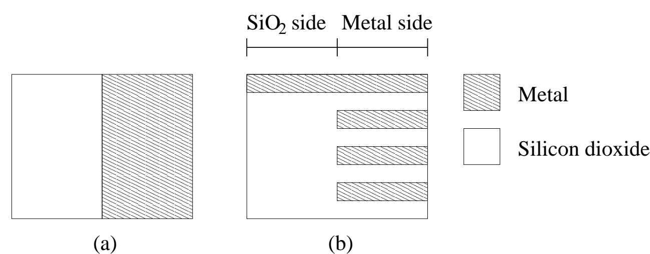


Figure 4.5: (a) Uniform beam (b) Actuator beam

The model is insufficient for calculation of lateral curl for a CMOS-MEMS beam, since it does not consider the silicon dioxide between the metal layers or the top metal layer that covers the entire structure. However, it will be shown how this model is related to the electrothermal actuator in section 4.3.2. The mathematical model can be found in [25, 28, 29].

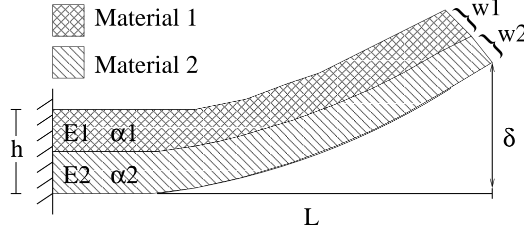


Figure 4.6: A cantilever beam composed of two different materials

The model states the a bimetal beam will curl in the shape of a circle due to different TCEs, as seen in figure 4.6. For a simple cantilever beam heated from $T - T_0$ letting $m = \frac{w_1}{w_2}$ where w is the width of the layers, $n = \frac{E_1}{E_2}$ where E is the Young's modulus, the radius of curvature (ρ) is given by

$$\frac{1}{\rho} = \frac{6(\alpha_2 - \alpha_1)(T - T_0)(1 + m)^2}{h\left(3(1 + m)^2 + (1 + mn) + \left(m^2 + \frac{1}{mn}\right)\right)} \tag{4.5}$$

where $(\alpha_1 - \alpha_2)$ is the difference in TCEs between the materials and h is the total width of the beam. Or if the width of both layers are equal $w_1 = w_2$, $m = 1$

$$\frac{1}{\rho} = \frac{24(\alpha_2 - \alpha_1)(T - T_0)}{h(14 + n + 1/n)} \tag{4.6}$$

The deflection (δ) of a cantilever beam is

$$\delta = \frac{L^2}{2\rho} \tag{4.7}$$

where L is the length of the beam.

It can be seen that the radius of curvature is inverse proportional to the temperature, and the deflection will therefore be proportional to the temperature. From this we can expect a linear change in the displacement of the actuator in respect to a change in temperature.

Equation (4.5) and (4.6) shows how the material properties will influence the design. The first factor $(\alpha_2 - \alpha_1)$ is the difference in TCEs between the materials. The TCE tells us how much a material expands with a change in temperature. A material with a high TCE expands more than a material with low TCE. According to these equations, the radius of curvature will be inversely proportional to the difference in TCEs, which means that a large difference TCEs increases the deflection.

The other material parameter included in the equations is the Young's modulus (E). The Young's modulus is the ratio between applied stress on

a structure and the amount of strain. In other words the Young's modulus tells us how stiff a material is. The Young's modulus is represented in the equations by $n = \frac{E_1}{E_2}$, and from equation (4.6) it can be seen that

$$\frac{1}{\rho} \propto \frac{1}{14 + n + 1/n} = \left(14 + \frac{2(E_1 + E_2)}{E_1 E_2}\right)^{-1} \tag{4.8}$$

which means that an increase in Young's modulus for one of the two materials gives a larger radius of curvature and a decreases the deflection.

To analyze the curl it is also interesting to look at the various geometrical parameters. Equation (4.5) and (4.6) shows how the total width (h) of the beam influences the radius of curvature. These equations state that the radius of curvature is proportional to the width, which means that a wider structure will have less deflection.

We can also see that the radius of curvature do not depend on the length of the beam (L), but equation (4.7) shows that the deflection (δ) at the tip of the beam is proportional to L^2.

The last design parameter of interest is the width ratio $m = \frac{w_1}{w_2}$. It is not easy to predict how this will effect the radius of curvature and the deflection just by looking at the equations, so the deflection was therefore calculated for several different values of m. Figure 4.7 shows the deflection of a beam as a function of the length for different values of m and figure 4.8 shows the deflection as a function of m with $L = 100\mu m$. The graphs show that the deflection increases for larger values of m until it flattens and slowly start to decrease. The maximum defection is obtained for $m = 2$.

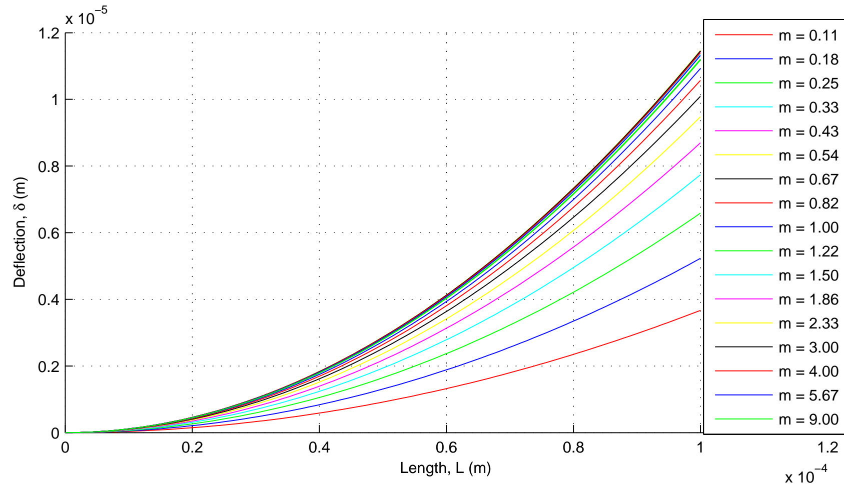


Figure 4.7: Deflection as a function of length (L)

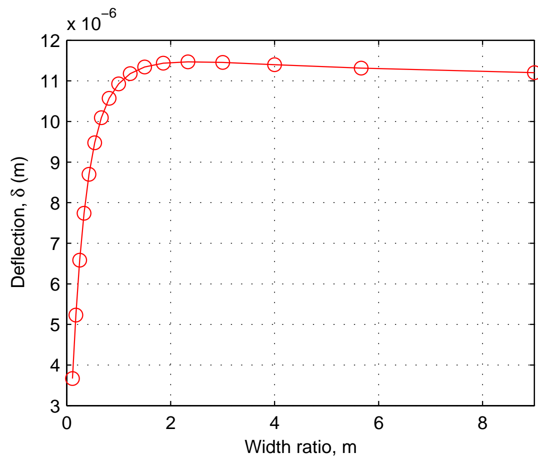


Figure 4.8: Deflection as a function of width ratio (m)

4.3.2 Modeling of the electrothermal actuator using bimetal beam theory

The bimetal beam theory predicts the deflection of a cantilever beam consisting of two different materials. The electrothermal actuator presented in this thesis can be divided into four bimetal beams, as shown in figure 4.9(a). After release, each of these beams will curl, as explained in section 4.3.1. The beams will have a deflection δ_i, and it can be seen from figure 4.9(b) that the total displacement of the actuator after release is $\Delta x_{released} = \sum_{i=1}^{4} \delta_i$. The bimetal actuator theory can therefore be used to predict the effect of the different design parameters of the actuator, but in order to use this for analytic calculation of the displacement a model of the layered actuator beam has to be made (fig. 4.5). However, this has not been done in this thesis. The bimetal beams of the actuator will curl the in the other direction when the actuator is heated, which makes the actuator contract.

4.3.3 Materials and number of metal layers in use

In some CMOS processes all metal layers are made of aluminum. However, for the STM 0.25μm process used in this thesis the first metal layer is made of tungsten. Simulations have been done for both cases (first metal layer made of both aluminum and tungsten).

Table 4.1 shows the different TCEs and Young's Modulus for the different materials. As mentioned earlier, the motion of the electrothermal actuator is caused by different TCEs in the metal layers and the silicon dioxide. From table 4.1 we see that the aluminum has $\sim$ 100 times larger TCE than silicon dioxide. Tungsten on the other hand has only $\sim$ 10 times larger TCE than

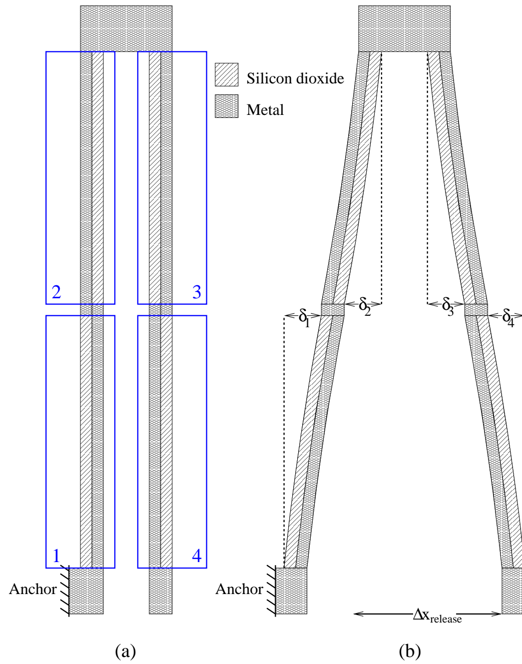


Figure 4.9: (a) Layout view of the actuator, consisting of four bimetal beams (b) The actuator after release, where $\Delta x_{released} = \sum_{i=1}^{4} \delta_i$

silicon dioxide. In addition tungsten has ~ 5 times larger Young's modulus, which means that tungsten is a much stiffer material than aluminum. Figure 4.10 shows the displacement of an actuator with the first metal layer made of tungsten and an actuator with the first metal layer made of aluminum. The graph shows that, due to less difference in TCEs between tungsten and silicon dioxide and the high Young's modulus, the actuator made with tungsten have less displacement than the one made with aluminum. The graph also shows us that the change in displacement is linear in respect to a change in temperature, as predicted.

Table 4.1: Material properties used for simulation

Material	**TCE** (K^{-1})	**Young's modulus** (GPa)
Aluminum (Al)	$2.31 \cdot 10^{-5}$	77
Tungsten (W)	$4.50 \cdot 10^{-6}$	410
Silicon dioxide (SiO_2)	$5.00 \cdot 10^{-7}$	70
Polysilicon	$3.50 \cdot 10^{-6}$	160

Another important factor is the effect given by the number of metal layers

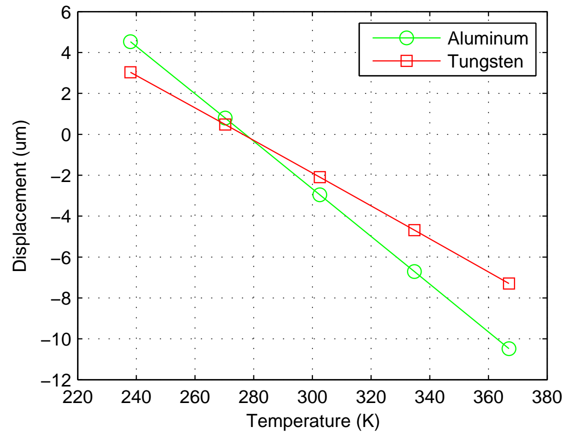


Figure 4.10: Displacement as a function of temperature for one actuator with the first metal layer made of aluminum and one actuator with the first metal layer made of tungsten

used. All the metal layers used for the simulations have the same material properties. In real life the material properties will be slightly different for the different metal layers. However, this information is not available from the CMOS foundries.

According to the mathematical model of bimetal actuators, the thickness of the beams have no influence on the displacement. However, as mentioned before this is not valid for the CMOS-MEMS structure used for this actuator, since the mathematical model does not consider the silicon dioxide between the metal layers or the top metal layer that covers the entire structure. The silicon dioxide between the metal layers are thicker than the metal layer itself, so adding more metal layers decreases the average TCE on the metal side of the beams. This leads to a smaller TCE difference between the different sides of the beam, and therefore a smaller displacement. According to this it would be better to make the actuator with as few metal layers as possible, but this is not correct due to the top metal layer. The top metal layer increases the average TCE on the silicon dioxide side of the beam. How much the top metal layer influences the average TCE on the silicon dioxide side of the beam decreases with the thickness of the structure. Figure 4.11 shows the displacement of an actuator made with four metal layers and an actuator made with only three. The graph shows that the actuator with four metal layers has a larger displacement than the one made with only three metal layers, and the conclusion is therefore that the increase in average TCE on the silicon dioxide side of the beams, due to the top metal layer, is larger than the decrease in TCE on the metal side of the beams.

We have seen that an actuator with tungsten as the first metal layer

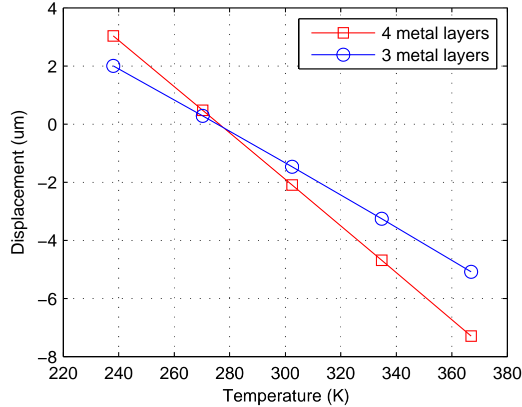


Figure 4.11: Displacement as a function of temperature for one actuator made with three metal layers and one actuator made with four metal layers

gives smaller displacement than one with aluminum, due to the material properties. We have also seen that use of more metal layers give larger displacement. A fair question is therefore how large the displacement will be if we do not use the first metal layer at all. All metal layers will then be made of aluminum, but it will be a larger concentration of silicon oxide on the metal side of the beams. The thickness of the structure will be the same as for a structure with all four layers, so the increase in TCE on the silicon dioxide side of the beams, due to the top metal layer, will be the same. Figure 4.12 shows the displacement as a function of temperature for one actuator with four metal layer, where the first metal layer is made of tungsten, and one actuator where the first metal layer has been removed. Since the tungsten is a much stiffer material than aluminum, removing it will increase the displacement. However, by removing the tungsten the average TCE on the metal side of the beam will decrease and the displacement will therefore be smaller. The graph shows that these two effects equal each other and the displacement is almost the same with and without the first metal layer (the actuator without tungsten has a bit larger displacement). On the other hand, due to the high Young's modulus of tungsten, the actuator will get less out-of-plane curl if the first metal layer is used. However, the out-of-plane curl is not considered to be a problem for this actuator.

As mentioned, the average TCE for the different sides of the beams has an impact on the displacement of the actuator. The use of VIAs (contacts between the metal layers) increases the metal density and thereby increases both the average TCE on the metal side of the beam and the displacement. Figure 4.13 shows the displacement as a function of temperature for an actuator with VIAs between the metal layers and one without. The use of

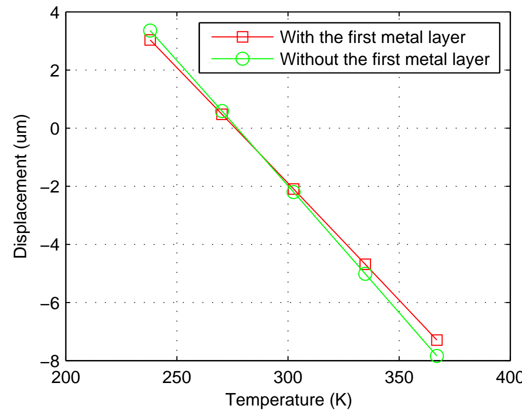


Figure 4.12: Displacement as a function of temperature for one actuator with four metal layers and one actuator without the first metal layer

VIAs will always increase the displacement, independently of the other design parameters. To be able to run a simulation of an actuator with VIAs the model was simplified. The VIAs were modeled by thin metal beams between the layers, and not as separate contacts. Oz concluded in his master thesis that VIAs between the metal layer of the beams increased the lateral self-assembly displacement with around seven times [9], which is far from the result obtained in this thesis. This can be due to the simplification used for the simulation, but seven times larger self-assembly displacement seems unlikely.

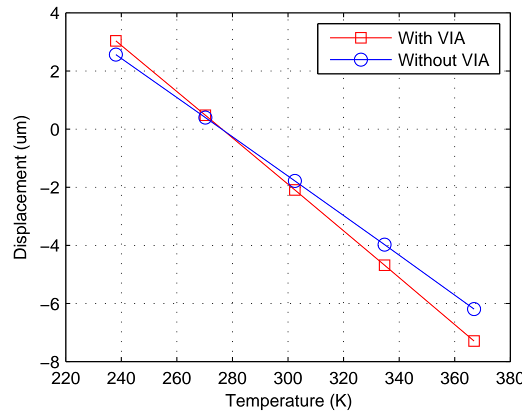
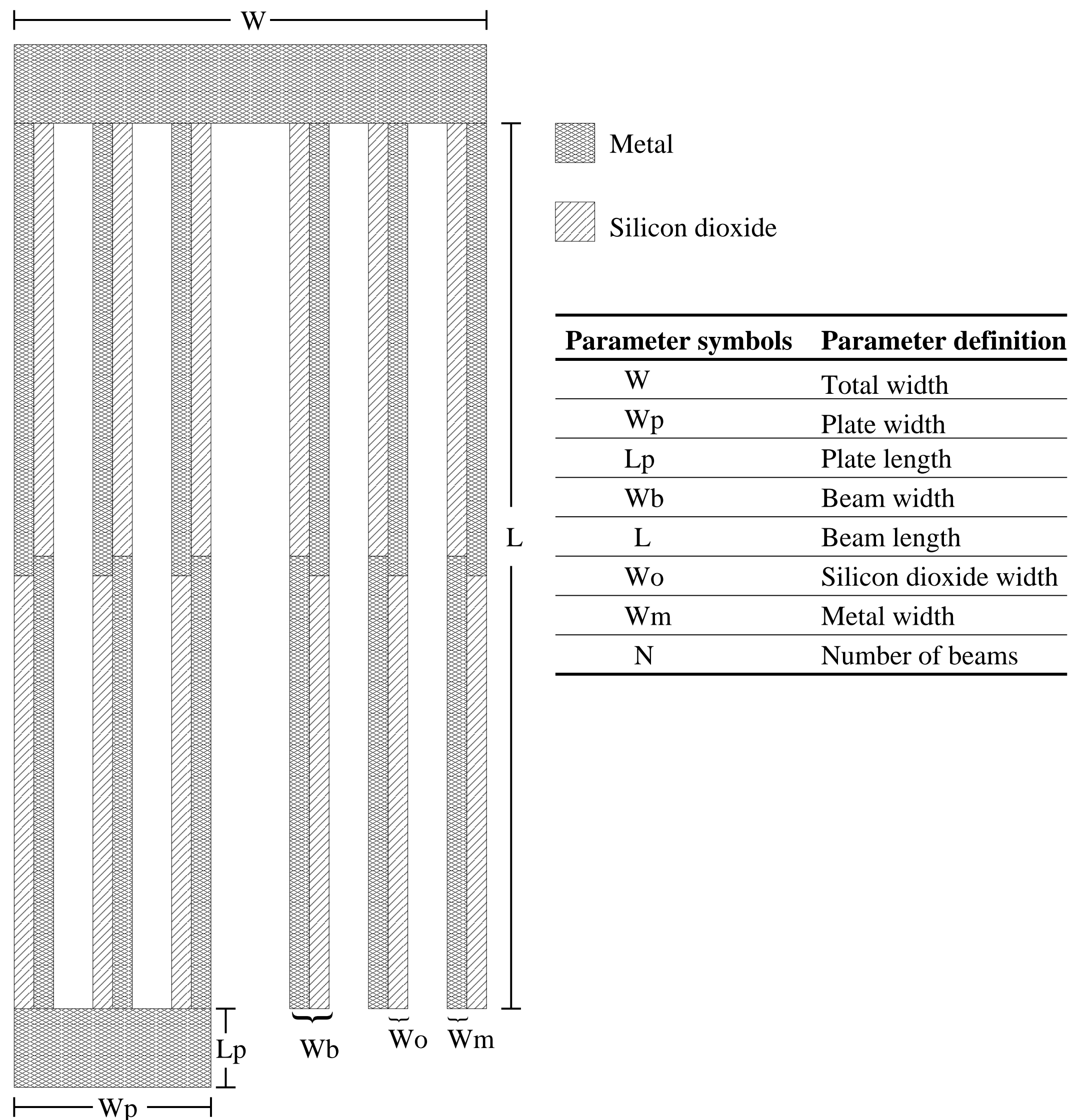


Figure 4.13: Displacement as a function of temperature with and without VIAs between the metal layers

4.3.4 Geometry

The geometrical parameters for the actuator are shown in figure 4.14. Changing the geometrical parameters can give larger displacement, but it is important to remember that these parameters often are restricted by the post-CMOS design rules and general requirements concerning the size of the structure. The most crucial parameters for the actuator are the length and the width of the beams.



Parameter symbols	Parameter definition
W	Total width
Wp	Plate width
Lp	Plate length
Wb	Beam width
L	Beam length
Wo	Silicon dioxide width
Wm	Metal width
N	Number of beams

Figure 4.14: Geometrical parameters

The mathematical model presented in section 4.3.1 showed how the geometrical parameters influenced the deflection (δ) of an ideal bimetal cantilever beam. Equation (4.7) states that δ is proportional with L^2, where L is the length of a bimetal cantilever beam. This mean that the displacement of the actuator should increase with larger L. Figure 4.15 shows the displacement as a function of temperature for an actuator with $L = 100, 150$ and $200um$ (a) and as a function of length (b). It can be seen that the displacement increases with somewhere between L and L^2.

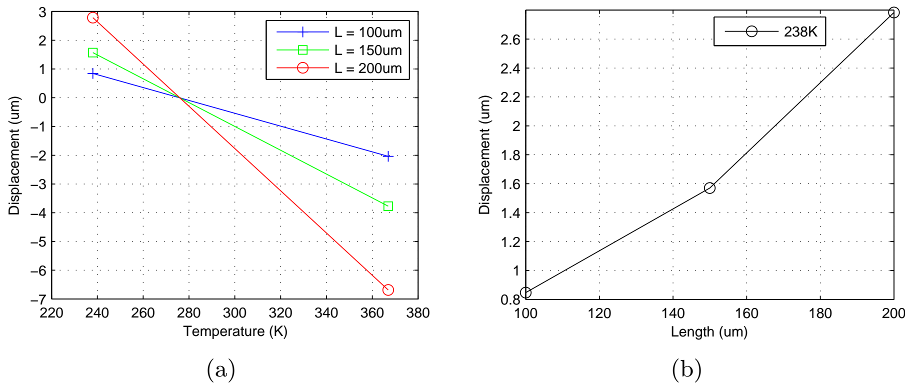


Figure 4.15: Displacement as a function of (a) temperature for an actuator with different L (b) length for $T_{set} = 238K$

According to the bimetal beam theory (eq. (4.6)), the radius of curvature will be proportional with the width for a bimetal cantilever beam. This means that the displacement of the actuator should decrease with larger width. Figure 4.16 shows how the width of the beams W_b influences the displacement of the actuator. It can be seen from this graph that the behavior is as predicted.

Figure 4.8 showed how the ratio between the width of the different layers influenced the curl of an ideal cantilever beam. According to this graph, a ratio $m = 2$ gives largest curl. An actuator with total beam width $h = 2\mu m$ has been simulated with $0.67 \leq m \leq 1.86$. Figure 4.17 shows that the actuator get maximum displacement for $m = 1.22$ before the displacement slowly decrease.

The last geometrical parameter of interest is the number of beams of the actuator (N). This parameter will have no influence on the displacement of the actuator, since each beam will have an equal displacement (fig. 4.18(a)). However, more beams will give a larger force, as seen in figure 4.18(b). The force is measured in the direction of motion for the actuator (lateral, parallel to the substrate), and it will be shown that a large force is important for one of the varactor designs in chapter 5.

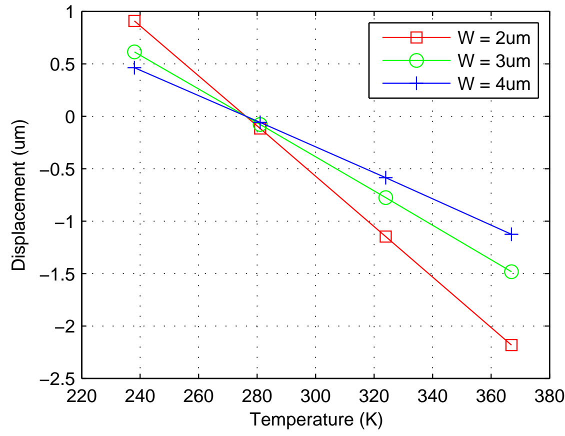


Figure 4.16: Displacement as a function of temperature for an actuator with different W_b

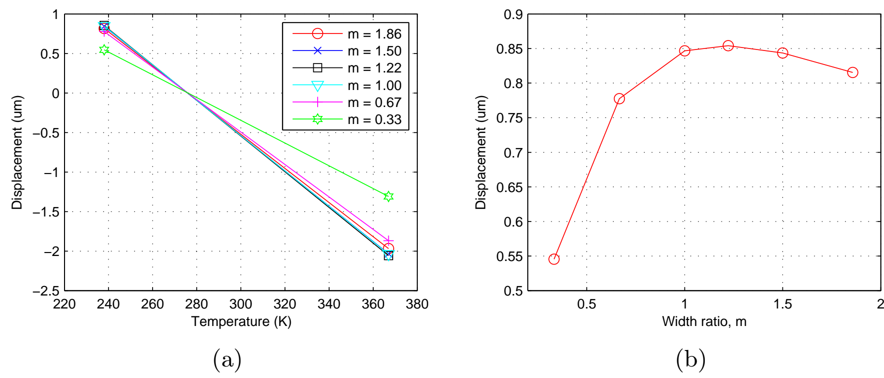


Figure 4.17: Displacement as a function of (a) temperature for different width ratios (b) width ratio (m)

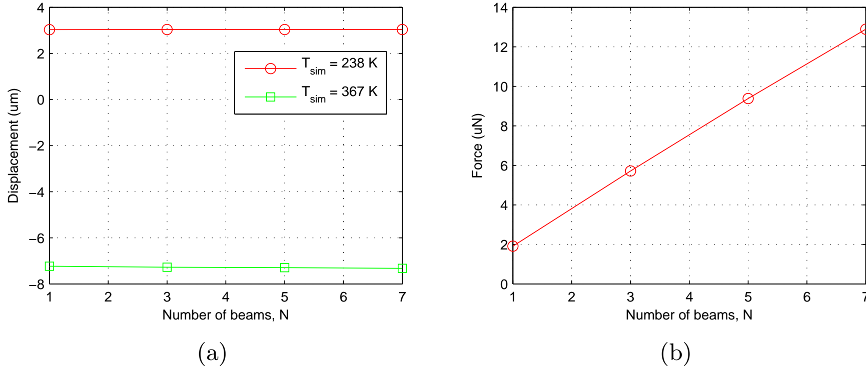


Figure 4.18: (a) Displacement as a function of number of beams (N) (b) Force as a function of number of beams (N)

4.3.5 Driving voltage and power consumption

The electrothermal actuator use a polysilicon loop as a heating element to induce motion. The polysilicon used for the actuators in this thesis is low resistive, which will give a large current for a small voltage. The total resistance for the polysilicon loop has been calculated to 263Ω, and Coventorware has been used to model the temperature of the polysilicon for a given voltage. It should be mentioned that the resistance of polysilicon is a function of temperature [25], but this has not been considered for the simulation model, and the simulated results will therefore be a bit different from the actual temperature. Coventorware also requires that a part of the structure is held at a steady temperature during simulation ($294K$ used for this simulation). This creates a unnatural condition that may influence the result. The power consumption has been calculated as $P = \frac{V^2}{R}$. Figure 4.19(a) shows the temperature and figure 4.19(b) shows the power as a function of different voltages. It can be seen that according to these simulations the required driving voltage for this actuator is around $3V$, which corresponds to a power consumption of around $3.3mW$. This is a dynamic power consumption due to the latch mechanism. However, these simulation results are not accurate due to the simplifications mentioned above, but gives a general idea of what can be expected.

4.3.6 Summary

The most important design parameters of the actuator, and how they influence the displacement have been analyzed and discussed. It has been shown that the first metal layer that is made of tungsten decreases the displacement, and that the displacement was slightly improved if the first

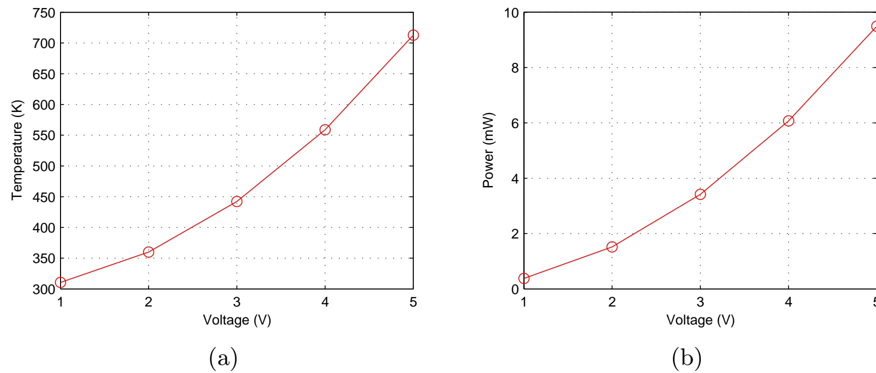


Figure 4.19: (a) Temperature as a function of voltage (b) Power as a function of voltage

metal layer was removed completely. This also shows us that the actuator probably will get a larger displacement if a different CMOS process is used, where all metal layers are made of aluminum.

The next design parameter analyzed was the number of metal layers used. Here it was shown that more metal layers gave a larger displacement, due to the influence of the top metal layer. However, it is uncertain if this is valid for CMOS processes with more metal layers than the STM 0.25μm process used in this thesis, but this was never further analyzed.

Various geometrical parameters were modeled, and the results matched the beam theory for a bimetal actuator. It has been shown that the length of the beams increases the displacement while the width of the beams decreases the displacement. The maximum length of the actuator will be given by the total chip area available for the device, while the minimum width on the other hand will be given by the CMOS design rules that determine the minimum width of the polysilicon layer. In addition the post-CMOS design rules states that the metal layers must cover the polysilicon layer with a certain overlap on either side. More interesting was the results from changing the beam width ratio. According to the mathematical model the largest deflection should be obtained with a width ratio of 2:1, but due to the special structure of the CMOS-MEMS beams the largest displacement was obtained for a width ratio of 11:9. In addition the analysis showed that the displacement was independent of the number of beams of the actuator. However, the force in the direction of motion increased with more beams, and figure 4.18(b) showed that the force is linear with the number of beams.

A last important observation is that the displacement is linear to the temperature. It can be seen from mathematical thermodynamic models that the temperature is non-linear to the voltage, since the voltage is non-linear to the power. However, this is only valid if the resistivity of the polysilicon is

constant, and it has been shown that the resistivity of polysilicon is a function of temperature [25]. Experiments shows that this change in resistivity causes the displacement to be linear to the voltage for a bimetal actuator [30].

4.4 Implementation

Table 4.2 shows the design parameters used for the fabricated actuators. Some of the conclusions made earlier in this chapter were first discovered after the chip was sent to production. One of the factors that should have been improved is the width of the beams. The width should have been made smaller to achieve larger displacement, as seen in figure 4.16. However, as mentioned in the summary the minimum beam width will be limited by both the CMOS design rules (minimum width of the polysilicon layer) and the post-CMOS design rules (minimum metal overlap for the polysilicon layer). Also note the the width ratio m has been set to 1 instead of 1.22. However, this will have small impact on the displacement, as seen in figure 4.17. Figure 4.20 shows the layout of the actuators used for the varactors, the switch and the latch. The actuator of the latch is two of the actuator used for the varactors connected together, therefore the design parameters used for this actuator is the same as for the actuators of the varactors.

Table 4.2: Design parameter used for the fabricated actuators

Definition	**Symbol**	**The actuators of the varactors**	**The actuators of the switch**
Total width	W	$70.8\mu m$	$63.6\mu m$
Beam length	L	$240\mu m$	$120\mu m$
Plate width	W_p	$28.8\mu m$	$28.8\mu m$
Plate length	L_p	$12\mu m$	$12\mu m$
Beam width	W_b	$3.2\mu m$	$3.2\mu m$
SiO_2 width	W_o	$1.6\mu m$	$1.6\mu m$
Metal width	W_m	$1.6\mu m$	$1.6\mu m$
Number of beams	N	5	5

4.5 Latch

The actuator presented in this thesis consumes a large amount of power when heated. A latch mechanism is added to the designs so that the varactors only consume power when switching [8]. The latch mechanism uses the

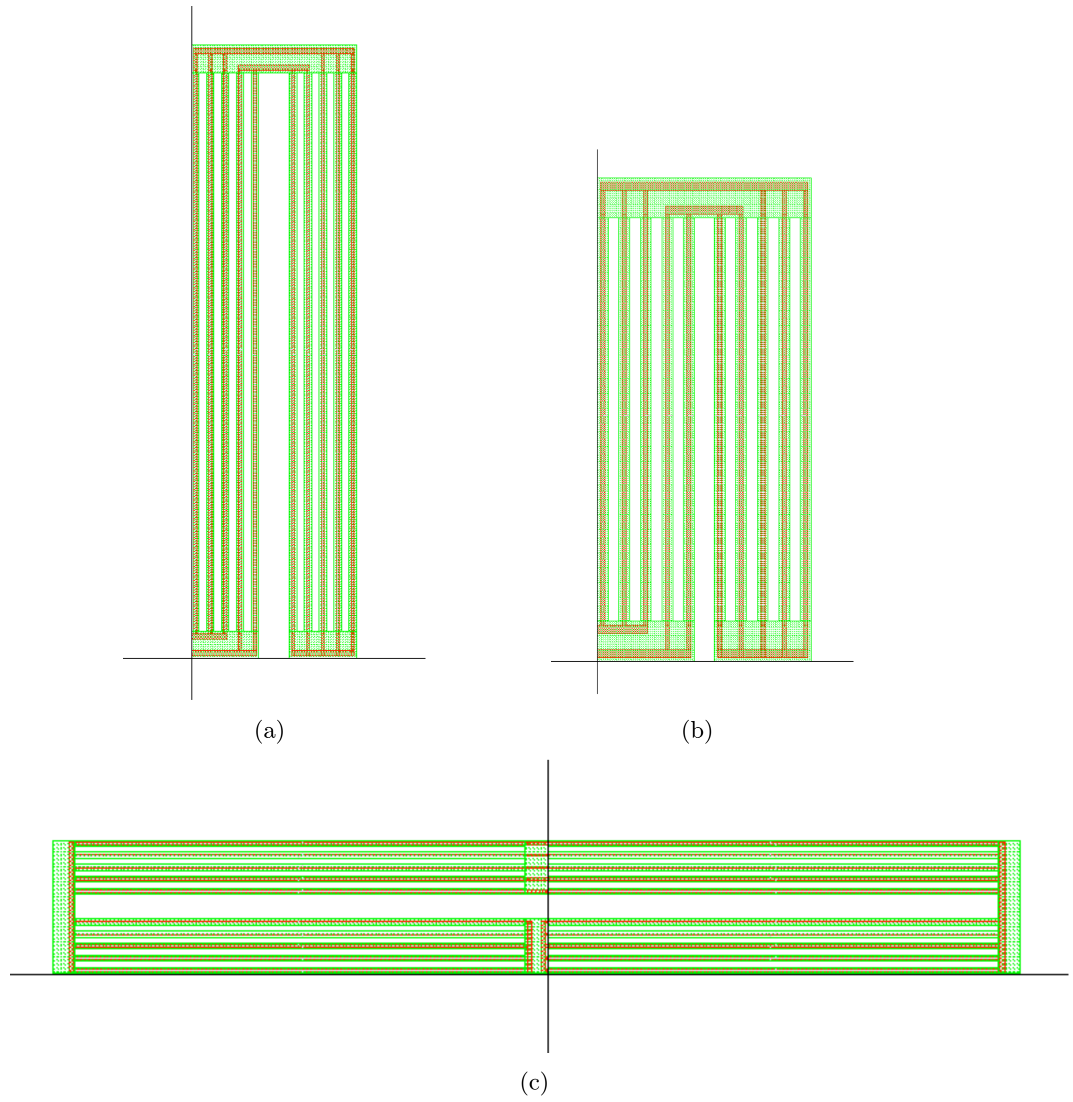
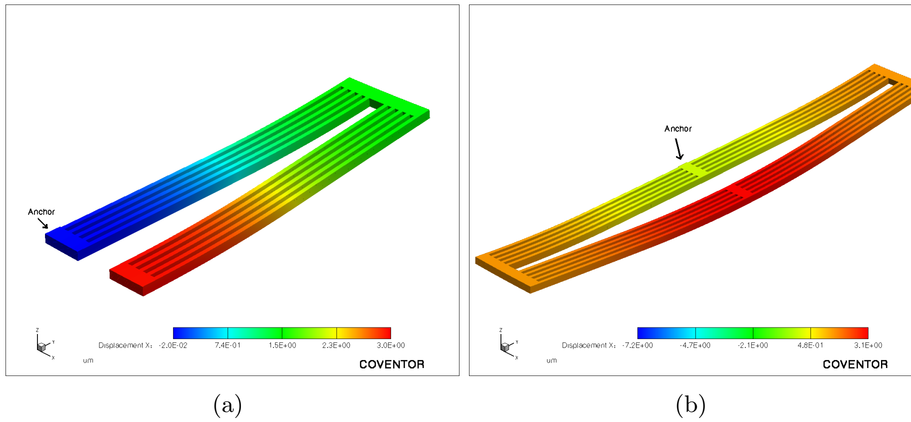


Figure 4.20: The layout of the actuator used for (a) the varactors (b) the switch (c) the latch

electrothermal actuator design A as explained in section 4.2.1 and makes use of the self-assembly to lock the movable frame after release. Special for the actuator controlling the latch is that it is double in size compared to the actuators used for controlling the varactors, as shown in figure 4.21. This is done to maintain symmetry in the design.



(a) (b)

Figure 4.21: Actuator used (a) for the varactors (b) for the latch

The basic operation of the latch is illustrated in figure 3.2. As mentioned, actuator A expands once released and contracts when heated. The latch is in the "heated" state in the layout, but due to the self-assembly effect of the actuator the latch moves to the "idle" state once released. As for the actuators controlling the varactors, the actuator controlling the latch is heated with a polysilicon loop. When heated the actuator contracts and the slots of the latch disengage with the pegs on the movable frame. The actuators of the varactors are then free to move the combs to their desired position. When the desired position is obtained the latch lock the movable frame, as the current controlling the actuator of the latch is shut off.

The latch used for this thesis have only two slots, which gives two different stable positions. This means that two steady capacitance values can be obtained. However, the latch can be extended with more slots if desired [6].

The latch does not only lower the power consumption, it can also be used to make sure the combs get in the desired position even if the displacement of the actuators are different than modeled. Since these designs have two slots, this will only work if the displacement of the actuators are larger than predicted. If the displacement is smaller the latch used in these designs will not work at all. However, if the latch is extended with more slots the latch will work even if the displacement is smaller than modeled.

Chapter 5

Tunable capacitors, design and modeling

5.1 Tunable capacitor topologies

The capacitance between two conductors is defined as

$$C = \frac{\epsilon A}{g} \tag{5.1}$$

where ϵ is the permittivity, A is the overlapping area and g is the gap. Various tunable capacitors (varactors) can be made by varying one or more of these factors. Some of the elements that are used to characterize the performance of varactors are the tuning range (TR), the quality factor (Q) and the actual capacitance value. More detail on each of these factors will be further explained in 5.3.1. The TR and Q-factor are defined as

$$TR = \frac{C_{max}}{C_{min}} - 1 \tag{5.2}$$

where C_{max} is the maximum capacitance and C_{min} is the minimum capacitance of the varactor.

$$Q = \frac{stored\ energy}{energy\ loss\ per\ cycle} \tag{5.3}$$

which tells us how much relative energy is lost during a cycle. A high Q-factor gives a low energy loss per cycle, which means that the performance of the capacitor is more "ideal".

In this section some of the most common varactor topologies will be explained.

5.1.1 Gap tuning

As the name implies these varactors vary the capacitance by varying the gap between two conductors. This can be done by two parallel plates moving vertical, normal to the substrate, as seen in figure 5.1(a). The varactor can then be actuated electrostatically by applying a voltage between the plates. However, the tuning gap is limited by the pull-in voltage. If the electrostatic force gets too strong the movable plate will snap down to the fixed plate. The theoretical limit for this is $\frac{1}{3}$ of the total gap, which means that maximum tuning voltage that can be obtained will be limited to 50%.

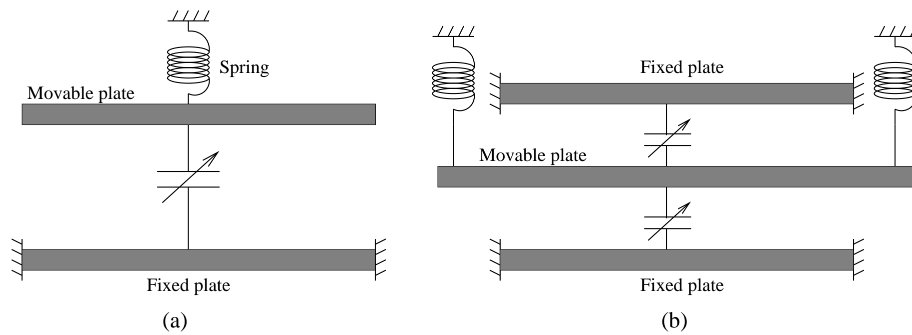


Figure 5.1: Parallel plate gap tuning capacitor

Other gap tuning capacitors with larger tuning range have been made, e.q. the three plate parallel plate system where two fixed plates on either side of the movable plate are used [31] (fig. 5.1(b)). This configuration allows a theoretical tuning range of 100%. Gap tuning capacitors with other forms of actuation such as electrothermal have also been made, where the tuning range is not limited [32].

5.1.2 Area tuning

Another popular way of tuning capacitors is area tuning. For area tuning capacitors the gap is constant while the area is changed. Contrary to the gap tuning parallel plate, the tuning range of area tuning capacitors does not have any theoretical limitation even if electrostatic actuation is used. The tuning range is only limited by geometrical design parameters and the actuator. The most common implementation of area tuning capacitors is interdigitated comb structures moving laterally, parallel to the substrate [33]. This implementation allows large overlapping area for the capacitor within a small chip area. However, the maximum capacitance of these varactors is limited by fabrication techniques such as RIE resolution, which limits the gap between the fingers.

5.1.3 Dielectric tuning

Equation (5.1) shows that the capacitance also can be altered by changing the dielectric between the conductors. This can be done by either moving a slice of material between the conductors or by altering the material properties of the material already present. Dielectric tuning of capacitors is not as common as gap and area tuning since it often requires implementation of some special dielectric material, without any advantages regarding performance. Some varactors based on dielectric tuning have been presented [7], but since CMOS-MEMS structures are limited to the materials available for the CMOS process used, dielectric tuning is not compatible with this post-CMOS process.

5.1.4 Gap&Area tuning

As mentioned it is also possible to vary more than one of the factors in (5.1). This leads to a tuning topology known as gap&area tuning, where both the gap and area change. This can be implemented with a comb structure, where the combs are not initially interdigitated. When actuated the gap of the varactor will change until the combs are interdigitated, then the capacitance value can be increased even further by area tuning of the fingers. By this method the minimum capacitance will be smaller than for area tuning capacitors, and the tuning range will be increased according to equation (5.2).

5.2 Varactor designs in CMOS-MEMS

The main challenge with varactor designs in CMOS-MEMS is the out-of-plane curl mentioned in section 2.3.1. Any offset between the conductors will lead to a significant reduction in sidewall capacitance due to a reduction in overlapping area. Curl matching techniques must be used to get comparable curling of both the static and the movable comb. However, the out-of-plane curl can be exploited to a benefit to make an out-of-plane varactor, as shown in [5].

Two different variable capacitor designs have been made. Both varactors are defined as gap&area tuning capacitors with comb structures moving laterally, parallel to the substrate. However, after the fingers interdigitate the capacitors will be based on area tuning only.

The block diagram of the varactors is shown in figure 3.1, and a detailed description of the actuators can be found in chapter 4. Both varactors use the same vertical curl compensation frame to get comparable curl between the static and the movable comb. A simulation model of this frame is shown in figure 5.2. The frame is modeled without the comb fingers, to reduce simulation time. Figure 5.2 shows that both the static and the movable

combs curl in the same direction, but the small difference in anchor axis (fig. 3.1) gives $\sim 1\mu m$ offset between the combs. However, due to fabrication mismatch the out-of-plane displacement is hard to predict, so the actual offset may be a bit different. The frames and the combs are all built with four metal layers and the polysilicon layer. Due to the use of the polysilicon layer the field oxide beneath the structures can not be removed (CMOS design rule). As mention in section 2.3.1 the built-in stress in the field oxide is highly compressive and increases the curl of the structure. However, due to the high Young's modulus of the polysilicon layer the structure will curl less with both the polysilicon layer and the field oxide than without either of them [25].

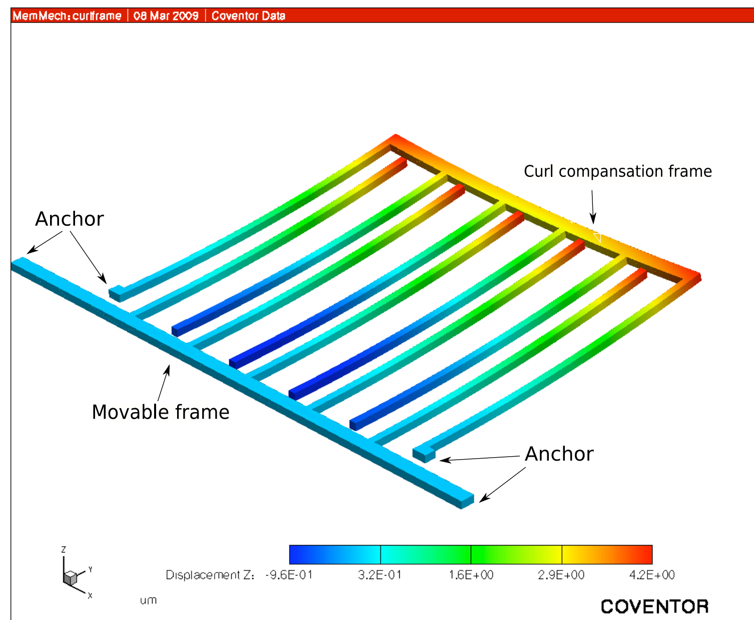


Figure 5.2: Simulated model of the static and the movable combs with a curl compensation frame

If the combs get any lateral curl, contact between the fingers can occur, which can lead to an electrical connection between the signal combs and ground. To avoid this the back of the combs should have been made as tapered beams, as explained in section 2.3.2. However, this first came to mind after the chip was sent to production and has therefore not been used for these designs.

5.2.1 Design A

In the first design the fingers have a small overlap L_0 in the layout, as shown in figure 5.3(a). When released the self-assembly effect of the actuators

moves the combs so the fingers are no longer interdigitated, and the C_{min} state of the varactor is obtained (b). To be able to achieve this, with the design shown in figure 3.1, both the actuators A and B as explained in section 4.2.1 are used. The difference between the two actuator designs are that one actuator will contract when released while the other actuator will expand. Since the actuators are placed on each side of the movable frame, their force will be equal in the same direction. This means that one actuator will pull the frame, while the other actuator will push. When heated the actuators moves the frame such that the fingers interdigitate and C_{max} is obtained (c).

The advantage of having a finger overlap in the layout is that the maximum finger overlap L_{omax} will be equal to the maximum displacement Δx of the actuators.

$$L_{omax} = \Delta x = \Delta x_{release} + \Delta x_{heated} \tag{5.4}$$

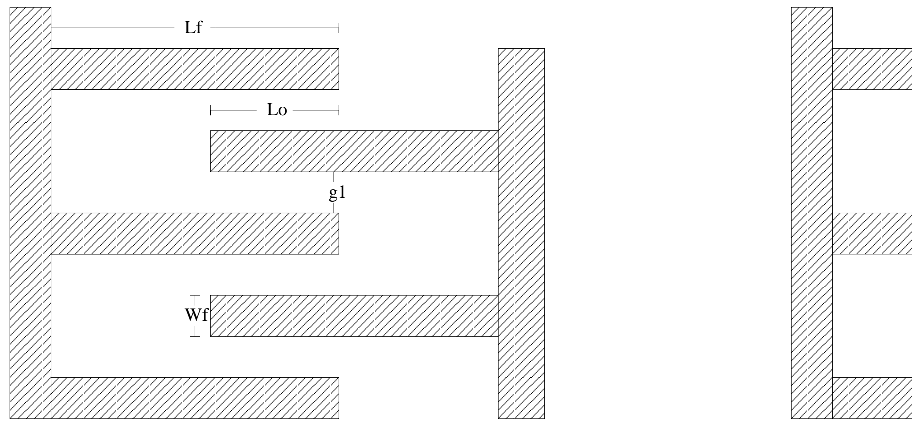
where $\Delta x_{release}$ is the displacement of the actuator after release and Δx_{heated} is the displacement of the actuator when heated, measured from the layout position.

A larger finger overlap gives a larger overlapping area and a larger capacitance according to equation (5.1). However, due to the post-CMOS design rules the gap between the fingers will be limited, and a larger gap gives a smaller capacitance. Analytic calculations and simulation values for the capacitances, the tuning range and the Q-factor can be found in section 5.3.3.

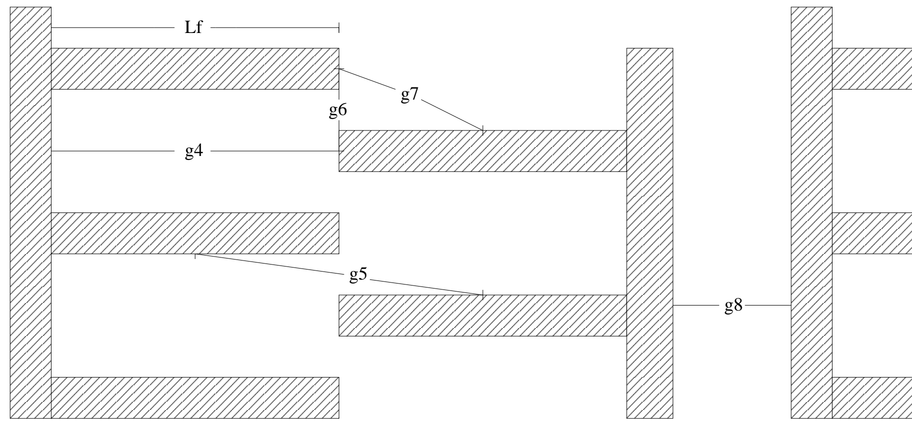
5.2.2 Design B

Design B is quite similar to design A, and are built as shown in figure 3.1, with one actuator on each side of the movable frame. The difference between the designs is that the combs in design B have shorter fingers than the combs in design A, and the fingers in design B have no overlap in the layout. In addition, both actuators used in design B are similar, and expands when released. Since both actuators are similar they will have an equal force, but in opposite direction. This means that both actuators will push the movable frame when released, and the combs are intended to stay in the same position after release as they did in the layout (fig. 5.4(a)). After release only one of the actuators is heated, while the other only work as spring. For this design it is important that the actuator moving the frame has a large enough force so it will be able to move the frame even with the other actuator working as a spring.

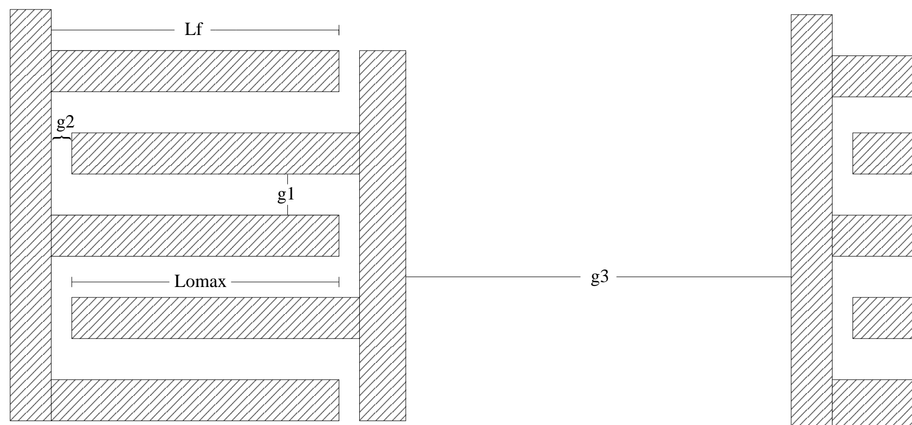
The disadvantage with design A is that the gap between the fingers is limited by the post-CMOS design rules. Due to no overlap in the layout, the gap between the fingers for design B can be made smaller. A smaller gap will, for a given area result in a larger capacitance since the capacitance is



(a) Layout



(b) After release (C_{min})



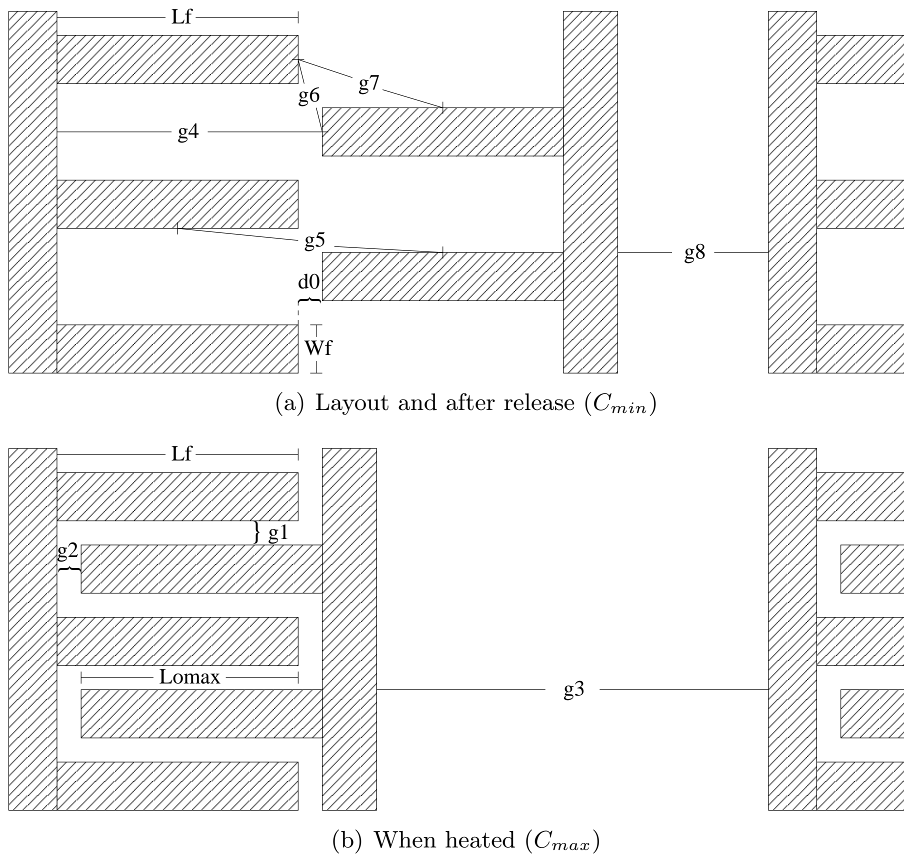
(c) When heated (C_{max})

Figure 5.3: Varactor design A

inverse proportional to the gap (eq. (5.1)). However, due to no finger overlap in the layout the maximum overlap L_{omax} will be less then for design A. The maximum overlap will be given by the displacement for the actuators when heated Δx_{heated} and the distance between the combs in the layout d_0.

$$L_{omax} = \Delta x_{heated} - d_0 \tag{5.5}$$

In theory the finger gap for design B can be made infinite small. However, due to fabrication mismatches, the minimum finger gap in design B is also limited. One effect that can be crucial is width bloating of the fingers. This can cause the gap to be too small so the fingers are unable to interdigitate [9]. Analytic calculations and simulation values for the capacitances, the tuning range and the Q-factor can be found in section 5.3.3.



(a) Layout and after release (C_{min})

(b) When heated (C_{max})

Figure 5.4: Varactor design B

5.3 Modeling

In this section analytic calculations and simulation results will be presented. In the beginning of this section the different equations used for the calculation of the capacitances and the Q-factors and the models used for the simulations are explained. At the end of the section the different results will be presented with a short comparison of the calculated and the simulated values.

5.3.1 Analytical equations for the capacitances and the Q-factor

Capacitance

Precise calculations of the capacitance can be difficult to achieve. Equation (5.1) are only valid if $A \gg g$, since it only takes into account the electric field lines normal to the plates, neglecting the field line at the end of the plates (fig. 5.5). These field line are often referred to as fringing fields and result in a larger capacitance than calculated using (5.1). Since the fringing fields can not be neglected for these designs, a simplified first-order formula is used to calculate the capacitance with the fringing fields [34]

$$C \approx \epsilon \frac{(t+2g)(L+2g)}{g} \approx \epsilon \left[\frac{tL}{g} + 2t + 2L \right] \tag{5.6}$$

where g is the gap, t is the thickness and L is the length of the structure.

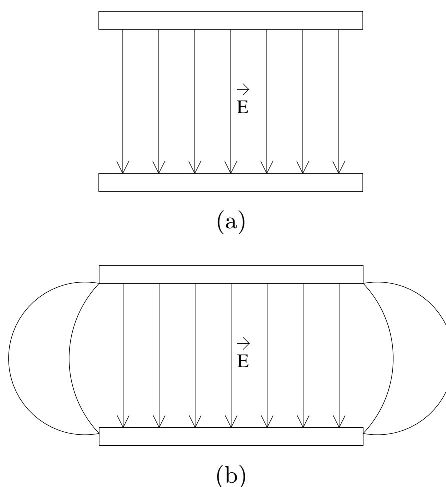


Figure 5.5: Electric field lines between two conductors (a) without fringing fields (b) with fringing fields

In order to calculate the total capacitance of the varactors, the capacitance between the finger groups (C_{comb}) and the capacitance between the signal electrode and the substrate, anchors and all the other grounded parts of the design (C_p) must also be added, as seen in equation (5.7).

$$C_{total} = C_{fingers} + C_{comb} + C_p \tag{5.7}$$

where $C_{fingers}$ is the capacitance between the fingers, C_{comb} is the capacitance between the finger groups and C_p is the capacitance between the signal electrode and all parts connected to ground (substrate, anchors, etc.). Figure 5.6 shows the different capacitances between the fingers and between the finger groups for both the C_{min} and the C_{max} state of the varactor. Note that these capacitances are per finger, which means that they have to be multiplied with the number of fingers n and the number of combs N in order to obtain the total capacitance.

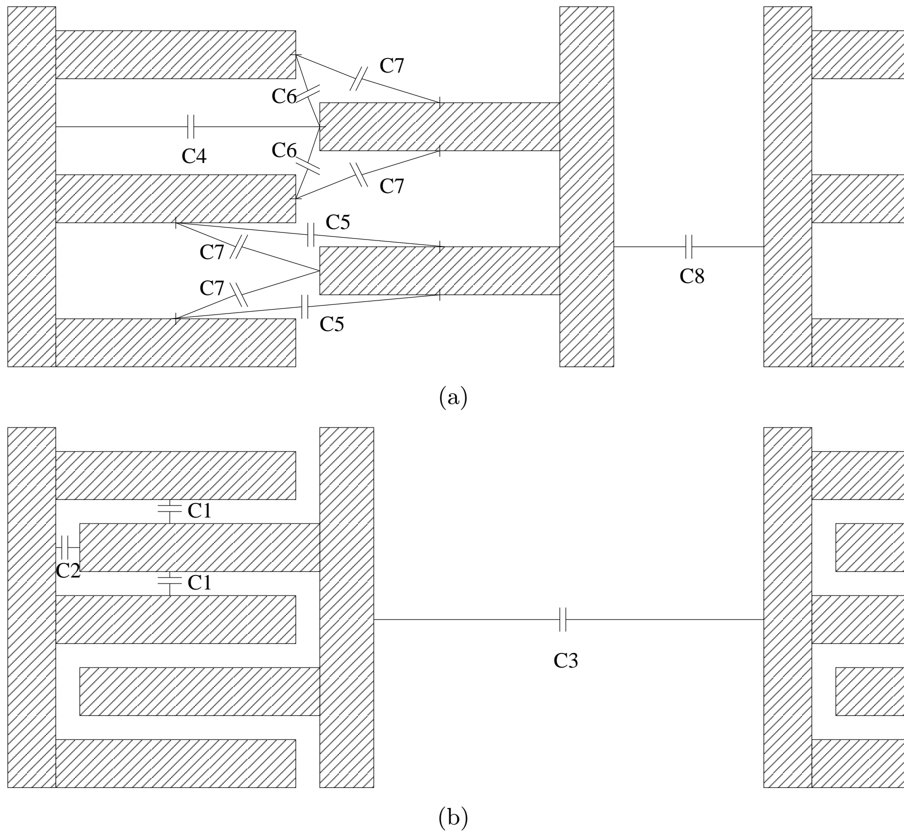


Figure 5.6: The different capacitances used for calculations of (a) C_{min} (b) C_{max}

Equation (5.8) to (5.15) are used to calculate the capacitances in (5.7), and the calculated values for each design can be found in section 5.3.3. Calculation have been done both with and without fringing fields. The equations used to calculate C_p are the same as used for calculation of C_{finger} and C_{comb}, and will not be further derived.

Without fringing fields

Equation (5.1) is used to calculate the capacitance for each finger and between the finger groups without fringing fields. Figure 5.6 shows the different capacitances and the various lengths, widths and gaps referred to are shown in figure 5.3 and 5.4, n is the number of fingers on each comb, while N is the number of combs. Note that C_7 is multiplied with two since it is four capacitances for every finger pair.

C_{max}, figure 5.6(b)

$$C_{finger} = N(2n-1)(C_1 + C_2) = N(2n-1)\epsilon\left(\frac{L_f \cdot t}{g_1} + \frac{W_f \cdot t}{g_2}\right) \tag{5.8}$$

$$C_{comb} = NC_3 = N\epsilon\frac{L_b \cdot t}{g_3} \tag{5.9}$$

C_{min}, figure 5.6(a)

$$\begin{aligned} C_{finger} &= N(2n-1)(C_4 + C_5 + C_6 + 2C_7) \\ &= N(2n-1)\epsilon \cdot t\left(\frac{W_f}{g_4} + \frac{L_f}{g_5} + \frac{W_f}{g_6} + \frac{2W_f}{g_7}\right) \end{aligned} \tag{5.10}$$

$$C_{comb} = NC_8 = N\epsilon\frac{L_b \cdot t}{g_8} \tag{5.11}$$

With fringing fields

In order to calculate the capacitance with the fringing fields, equation (5.6) is used. Figure 5.6(b) shows the capacitances used for calculation of C_{max}. If the capacitances in figure 5.6(a) are used to calculate C_{min} some of the fringing fields will be added more than one time, and therefore a simplified model is used [9]. This model transforms the capacitances in figure 5.6(a) to a parallel plate with length $W_f + L_f + g_1$ and gap $g4$, as seen in figure 5.7.

C_{max}, *figure 5.6(b)*

$$C_{finger} = N(2n-1)(C_1 + C_2)$$

$$= N(2n-1)\epsilon\left(\left(\frac{L_f \cdot t}{g_1} + 2t + 2L_f\right) + \left(\frac{W_f \cdot t}{g_2} + 2t + 2W_f\right)\right) \quad (5.12)$$

$$C_{comb} = NC_3 = N\epsilon\left(\frac{L_b \cdot t}{g_3} + 2t + 2L_b\right) \quad (5.13)$$

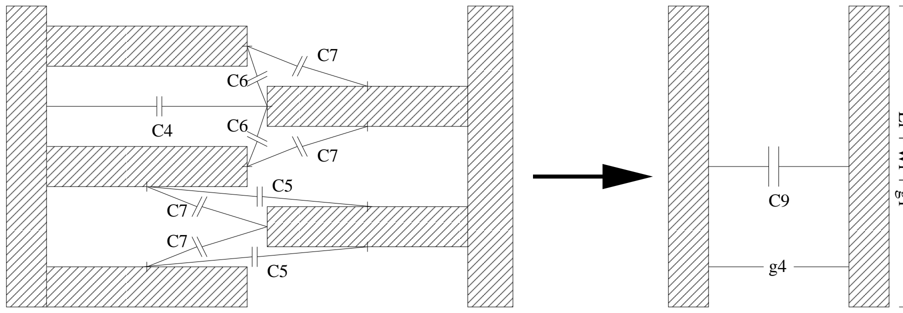


Figure 5.7: Simplified model for calculation of C_{min} with fringing fields

C_{min}, *figure 5.7*

$$C_{finger} = N(2n-1)\epsilon\left(\frac{t(W_f + L_f + g_1)}{g_4} + 2t + 2(W_f + L_f + g_1)\right) \quad (5.14)$$

$$C_{comb} = N\epsilon\left(\frac{L_b \cdot t}{g_8} + 2t + 2L_b\right) \quad (5.15)$$

Thickness of the CMOS-MEMS structure

Due to the sandwich structure of the CMOS-MEMS beams that consist of layers of metal and dielectric it is not obvious how the thickness of the structure used for calculation should be defined. Since the varactor presented in this thesis is based on the capacitance between the sidewalls of the structure, the thickness of the beams will influence the total area and therefore the capacitance according to equation (5.1) and (5.6). The dielectric between the layers do not contribute to the total capacitance between the beams, and can be considered as holes in the structure for this analysis. If just considering the electric field lines normal to the sidewall, the thickness used for calculation will be smaller than the total thickness of the structure. However, due to the fringing fields these dielectric "holes" between the metal layers will be "filled" and will not influence the capacitance [35]. This means that the total thickness of the structure can be used for calculation, and it will be shown in section 5.3.3 that this gives approximate the same capacitance as for the simulated model.

Q-factor

The Q-factor is defined in equation 5.3 and tells us how much relative energy is lost per cycle. In order to calculate the Q-factor the capacitor is modeled as a simple R,L,C circuit, as shown in figure 5.8.

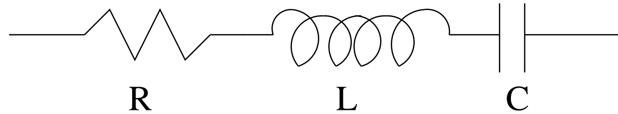


Figure 5.8: R,L,C model of the capacitor

By using this model the Q-factor of the capacitor will be

$$Q = \frac{|\Im m(Z)|}{\Re e(Z)} \approx \frac{1}{\omega RC} \tag{5.16}$$

where Z is the total impedance, $|\Im m(Z)|$ is the net reactance and $\Re e(Z)$ is the equivalent series resistance of the varactor. Equation (5.16) shows that a large resistance R will give a smaller Q and greater resistive loss for the varactor. It is also important to note that the inductance associated with the varactor has to be kept as low as possible, since the varactor will be unusable

beyond the self-resonance frequency where the inductance will dominate the total impedance of the device [7]. Therefore the self-resonance frequency of the device must be kept much higher than the intended signal frequency of the varactor. However, since the fabricated circuit was not finished in time for measurements the inductance of the varactors has not yet been found, and the Q-factor has therefore been calculated without this.

The resistance R is found by adding the sheet resistance of all the different layers in parallel.

$$\frac{1}{R} = \frac{1}{Rm1} + \frac{1}{Rm2} + \frac{1}{Rm3} + \frac{1}{Rm4} + \frac{1}{Rpoly} \tag{5.17}$$

where $Rm1$, $Rm2$, $Rm3$, $Rm4$ are the sheet resistance of the metal layers 1,2,3 and 4 respectively and $Rpoly$ is the sheet resistance of the polysilicon layer. Since polysilicon has a much higher sheet resistance than the metal layers, the use of the polysilicon layer will lower the Q-factor. However, since the total resistance will be all the layers in parallel the contribution from the polysilicon layer will be small.

By combining equation (5.16) and (5.17) with the geometrical parameters of the varactor, the Q-factor can be calculated for the entire frequency band of interest. Calculated values can be found in section 5.3.3.

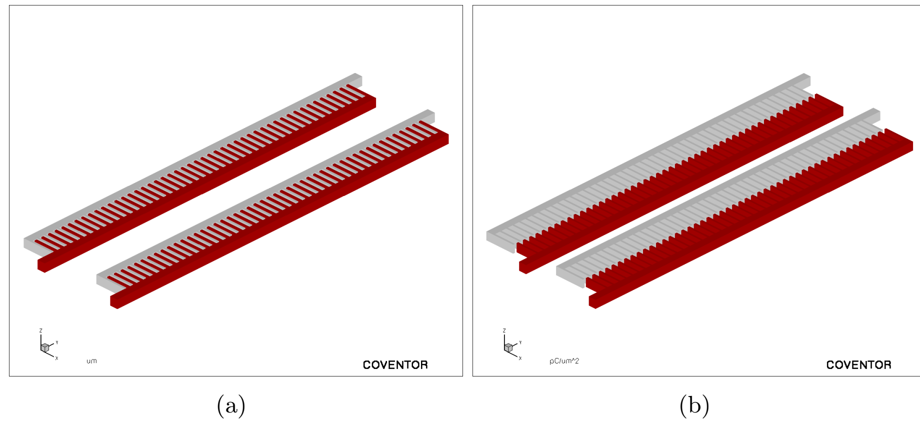
5.3.2 Simulation models

One problem with the simulation of the capacitances is that the varactors are quite large. This means that a simulation with a fine mesh of the whole system is impossible. Therefore the different parts of the varactors were simulated separately in order to get accurate results. All part was simulated using Coventorware. Figure 5.9 shows the models used for the simulations of the capacitances between the fingers (C_{finger}) and the finger group (C_{comb}) for the C_{max} and the C_{min} state of the varactors. The model consist of four combs, where the figure 5.9(a) shows the C_{max} state and figure 5.9(b) shows the C_{min} state.

Figure 5.10 shows the model used for simulation of the capacitance between the static frame (used as the signal electrode) and all parts connected to ground (movable frame and anchors). This model does not take into account the capacitance between the static comb and the substrate, which has only been analytically calculated for the varactors in this thesis.

5.3.3 Calculations and simulations results

In this section the calculated and simulated values for the capacitances, the TR and the Q-factor for both the varactor designs are presented. All equations used for the analytic calculations of the capacitances and the Q-factors are shown in section 5.3.1 and the models used for the simulations



(a) (b)

Figure 5.9: Simulation model for C_{finger} and C_{comb} for (a) C_{max} (b) C_{min}

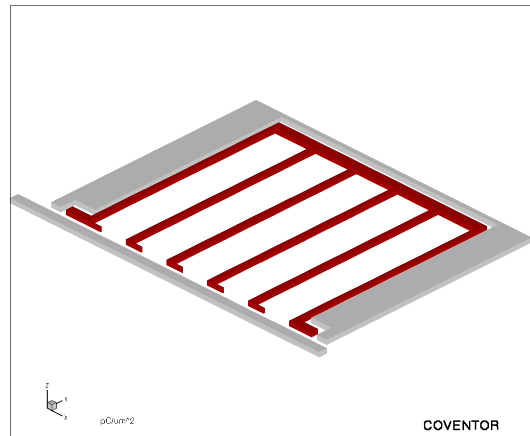


Figure 5.10: Simulation model for C_p without the capacitance to the substrate

are shown in section 5.3.2. The TRs have been calculated using equation 5.2.

Capacitance

The parameters used for calculation of C_{max} and C_{min} are listed in table 5.2 (design A) and 5.3 (design B), and the various lengths, widths and gaps used are shown in figure 5.3 and 5.4. The total thickness of the structures has been used for area calculations, as explained in section 5.3.1. Note that the parameters used for calculation of C_p are not listed. However, C_p is included in the calculations of C_{max} and C_{min} as described in equation 5.7. The capacitance between the substrate and the signal electrode is calculated without fringing fields for all cases including the simulations.

Table 5.1 shows the different capacitance values for both the varactor designs, and it can be seen that the contribution from the fringing fields is quite large ($\sim 40\%$). It is also interesting to note that the difference between the calculated C_{max} with fringing fields and the simulated C_{max} is small. This indicates that the equation used for calculation of the capacitance with fringing fields is quite accurate. However, the difference in C_{min} values are large. The reason for this can be that the transformation used to calculate C_{min} with fringing fields (fig. 5.7) is inaccurate. Due to this the calculated tuning ranges with fringing fields is much lower than both the calculated tuning ranges without fringing fields and the simulated tuning ranges.

If we compare the capacitances of the different varactor designs, we see that the differences are small. However, it is interesting to note that design B has higher C_{max}, but smaller tuning range than design A. One reason for this can be the difference in g_8 for design A and B (the gap between the finger groups for C_{min}). It can be seen from table 5.2 and 5.3 that this gap is smaller for design B than for design A. It is no reason that this gap should be smaller, and g_8 can be increased for design B without influencing any other parameters than the total area of the device. On the other hand, even if g_8 was increased for design B, this would have had small impact on the capacitance values and the tuning range, and design B would still have higher capacitances and lower tuning range than design A (has been analytical calculated).

As mentioned, due to the special metal/dielectric composition of the CMOS-MEMS structures, the thickness of the structures used for calculation must be considered. For the capacitances in table 5.1 the total thickness of the structures is used, and it can be seen that the calculated and simulated results match. This supports the theory that the fringing fields will "fill" the dielectric "holes".

However, it is important to remember that all these analyses do not consider any vertical curling between the combs and the fingers. As mentioned earlier, any differences in curl between the static comb (signal)

and the movable comb (ground) will lead to a significant reduction in sidewall capacitance, and it is therefore reason to believe that the actual capacitance values will be a bit lower than modeled.

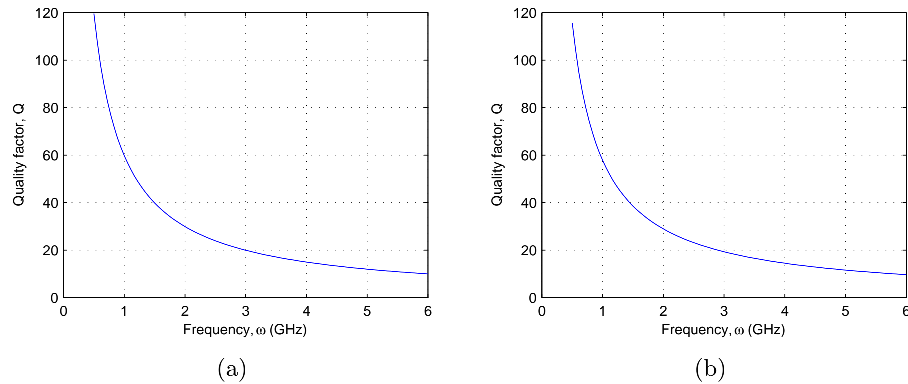
Further discussion of the results and the varactors compatibility with RF applications can be found in chapter 7.

Table 5.1: Calculated and simulated values for C_{max}, C_{min} and TR

	Calculation without fringing fields		**Calculation with fringing fields**		**Simulated**	
	Design A	Design B	Design A	Design B	Design A	Design B
C_{max}	483.6 fF	553.8 fF	794.4 fF	848.1 fF	781.4 fF	897.3 fF
C_{min}	67.8 fF	86.9 fF	310.6 fF	290.9 fF	132.8 fF	166.3 fF
TR	613	477	155.7	191.5	488.6	439.5

Q-factor

The Q-factors have been calculated by using equation 5.16 for the simulated C_{min}. It can be seen from figure 5.11 that the Q-factor is approximately 30 at $2GHz$ for both designs. The serial resistance of the whole structure is calculated to 125.9Ω for design A and 103.9Ω for design B, but design B has a slightly lower Q-factor due to a higher C_{min}. The Q-factors for these designs are a bit lower than state-of-the-art MEMS varactors, but at an acceptable level for CMOS-MEMS varactors.



(a) (b)

Figure 5.11: Q-factor as a function of frequency for (a) design A (b) design B

Table 5.2: Parameters for calculation of capacitances for design A

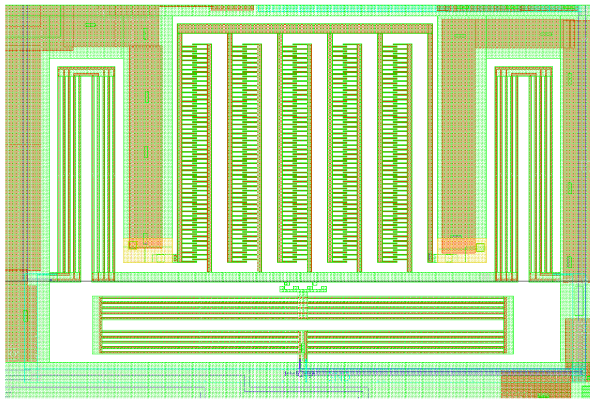
Parameter	**Symbol**	**Value**
Length of beam	L_b	$268\mu m$
Length of finger	L_f	$17.6\mu m$
Width of finger	W_f	$1.6\mu m$
Total thickness of structure	t	$\sim 6.5\mu m$
Number of finger groups	N	5
Number of fingers in one group	n	48
Gap between fingers (C_{max})	g_1	$1.2\mu m$
Gap between fingertip and beam (C_{max})	g_2	$0.6\mu m$
Gap between beams (C_{max})	g_3	$31.2\mu m$
Gap between fingertip and beam (C_{min})	g_4	$17.6\mu m$
Gap between fingers (C_{min})	g_5	$17.6\mu m$
Gap between finger tips (C_{min})	g_6	$2.8\mu m$
Gap between finger tip and finger (C_{min})	g_7	$9.0\mu m$
Gap between beams (C_{min})	g_8	$14.2\mu m$

Table 5.3: Parameters for calculation of capacitances for design B

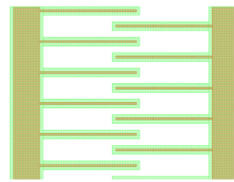
Parameter	**Symbol**	**Value**
Length of beam	L_b	$267.6\mu m$
Length of finger	L_f	$11.4\mu m$
Width of finger	W_f	$1.6\mu m$
Total thickness of structure	t	$\sim 6.5\mu m$
Number of finger groups	N	5
Number of fingers in one group	n	56
Gap between fingers (C_{max})	g_1	$0.8\mu m$
Gap between fingertip and beam (C_{max})	g_2	$0.6\mu m$
Gap between beams (C_{max})	g_3	$22\mu m$
Gap between fingertip and beam (C_{min})	g_4	$12.6\mu m$
Gap between fingers (C_{min})	g_5	$12.6\mu m$
Gap between finger tips (C_{min})	g_6	$2.7\mu m$
Gap between finger tip and finger (C_{min})	g_7	$5.9\mu m$
Gap between beams (C_{min})	g_8	$10.0\mu m$

5.4 Implementation

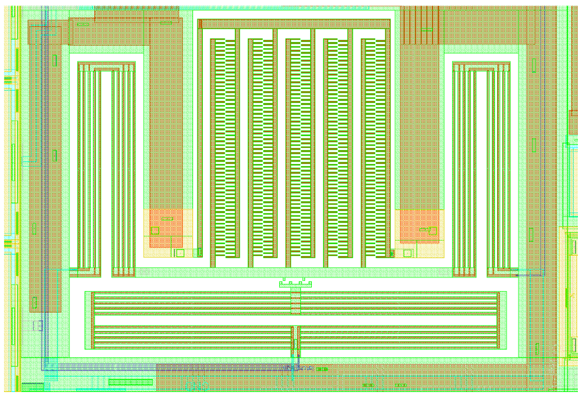
Figure 5.12 shows the layout of the varactors, the fingers of the varactors and the latch. In order to measure the small capacitance created by the varactor separately without the parasitic capacitances from the wires and bonding pads a dummy wire is made. This wire is only connected to a bonding pad, and is routed next to the signal wire. By extracting the capacitance of the dummy from the signal, the capacitance from the varactor can be obtained. The various geometrical parameters for the designs can be found in table 5.2 and 5.3.



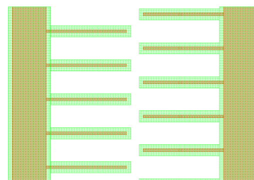
(a)



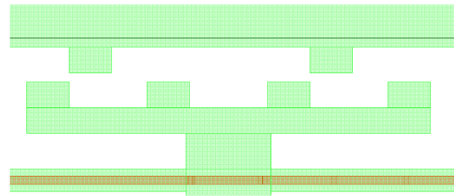
(b)



(c)



(d)



(e)

Figure 5.12: The layout of (a) varactor design A (b) the fingers of varactor design A (c) varactor design B (d) the fingers of varactor design B (e) the latch

Chapter 6

Experimental switch

6.1 MEMS switch topologies

Switches are small, but important parts of RF systems. Solid state switches such as PIN diode have low switching time at high frequencies, but suffer from high insertion loss or poor isolation (shunt, serial) and consume a considerable amount of power. MEMS switches on the other hand, are characterized by low insertion loss, high isolation, low power consumption and can beneficially replace a great number of the solid state switches used in communication systems today. However, there is still some remaining issues that need to be solved in order to obtain the high performance required for modern RF systems. Some of the remaining challenges for MEMS switches are switching time, total area of the device and integration with CMOS.

Switching systems can be divided into two main groups; series switches and shunt switches. For series switches the switch is placed in the signal path and breaks the connection when turned off, while for shunt switches the signal is short-circuited to ground when the switch is turned on, as seen in figure 6.1. Both these topologies have been used to make MEMS switches, with good results [7].

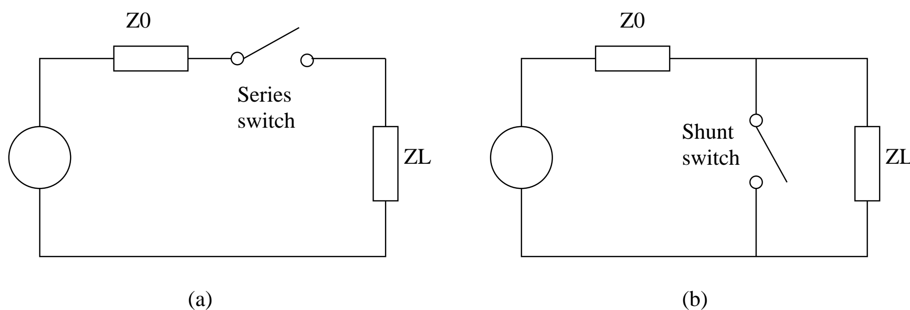
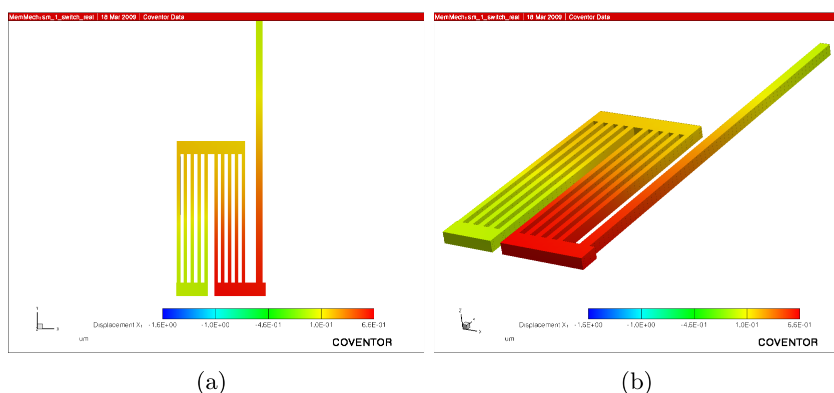


Figure 6.1: (a) Series switch (b) Shunt switch

6.2 Design and modeling

As mention earlier, the switch presented in this thesis is designed to investigate the possibility of obtaining good a metal-to-metal connection between the sidewalls of two CMOS-MEMS beams. The switch is a lateral DC series switch and the principle of operation is shown in figure 3.3. The switch uses two electrothermal actuators as presented in chapter 4 that are attached to two cantilever beams. The actuators are designed to expand once released, thereby pushing the beams together to obtain connection.

Figure 6.2 shows the model used for simulation of the switch. Only half of the switch has been simulated in order to verify that the deflection of the actuators are sufficient to push the beams together once released. However, as mentioned in chapter 4, the width of the actuator beams should have been made smaller, but this was first discovered after the chip was sent to production. Also the fact that the first metal layer is made of tungsten was discovered after the chip was sent to production. These two factors decreases the displacement of the actuators, which in worst case can mean that the deflection will be two small to obtain connection for the switch.



(a) (b)

Figure 6.2: Simulation model of experimental switch (a) top view (b) side view

The stiffness of the connection beams will also lower the deflection for the actuators. However, this has been taken into account during simulation of the switch, as seen in figure 6.2. The beams are designed without the polysilicon layer, due to the high Young's modulus of polysilicon. The characteristic temperature T_0 (eq. (2.1)) used for simulation should therefore be higher than for structures with the polysilicon layer. However, since the actuator is made with the polysilicon layer $T_0 = 328$ has been used for this simulation as well.

Table 6.1 shows the displacement of connection beam for a simulation temperature of $238K$ and $367K$. With the temperature offset explained

in section 2.4 this corresponds to 21 ℃ and 170 ℃. The gap between the beams is $1.2\mu m$ in the layout, and it can be seen that each beam will have a displacement of $0.66\mu m$ after release according to the simulated model. This means that the displacement will be sufficient to close the gap, but with a small margin. This has happen because the switch was modeled with aluminum as the first metal layer before the switch was sent to production. To be sure to obtain connection a longer actuator should have been used.

Table 6.1: Displacement of the connecting beam

Temperature, T_{set}	Displacement
$238K$	$0.66\mu m$
$367K$	$-1.59\mu m$

6.3 Implementation

Figure 6.3 shows the layout of the switch. The actuators used are shown in figure 4.20(b) and the latch mechanism is similar to the one shown in figure 5.12(e). The geometrical parameters of the actuators can be found in table 4.2 and the connecting beams have a size of $256.8\mu m$ x $6\mu m$.

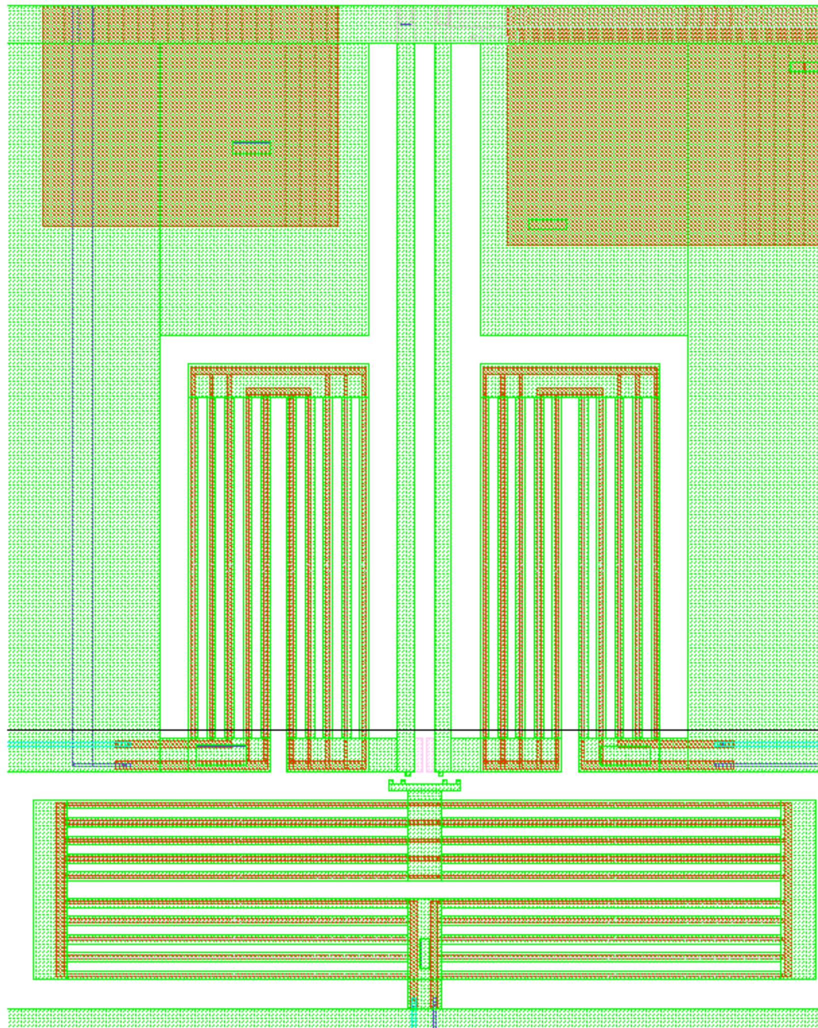


Figure 6.3: The layout of the switch

Chapter 7

Summary and discussion

In this section a short summary of the achieved results will be presented and remaining issues concerning the designs will be discussed with some suggestions for improvements. At the end of this chapter a short comparison between the designs in this thesis and state-of-the-art RF MEMS components can be found.

7.1 Short summary of achieved results

7.1.1 Actuator

In chapter 4 the different design parameters of the actuator were analyzed, and a summary of how those parameters influenced the performance of the actuator was presented in section 4.3.6. Table 7.1 gives a overview of the various design parameters and how they effect the displacement of the actuator. In addition to these analyses it was shown that the actuator got a slightly larger displacement by removing the first metal layer that is made of tungsten. This had however small impact on the total displacement. Note that the number of beams of the actuator had no influence on the displacement, but as seen in figure 4.18 the force in the direction of motion is linear with the number of beams. Table 4.2 shows the design parameters used for the fabricated actuators.

7.1.2 Varactor designs

Two different varactor designs have been presented. A description of the designs and their differences can be found in chapter 5. Table 7.2 shows the calculated and simulated capacitances and the tuning ranges for the varactors, and the Q-factor was calculated to approximately 30 at $2GHz$ for both designs.

Table 7.1: Summary of the different design parameters of the actuator

Design parameter	**Effect on displacement**
Tungsten instead of aluminum as the first metal layer	Tungsten gives a smaller displacement, due to a lower TCE and a higher Young's modulus than aluminum
Number of metal layers used	More metal layers gives a larger displacement, due to the effect of the top metal layer
Use of VIAs between the metal layers	VIAs gives a larger displacement, due to an increase in metal density on the metal side of the beam
Beam length	An increase in beam length gives a larger displacement
Beam width	An increase in beam width gives a smaller displacement
Width ratio between the metal and the silicon dioxide	Largest displacement was obtained for a beam ratio of 11:9
Number of beams	Have no effect on the displacement, but a larger number of beams give a greater force

Table 7.2: Calculated and simulated values for C_{max}, C_{min} and TR

	Calculation without fringing fields		**Calculation with fringing fields**		**Simulated**	
	Design A	Design B	Design A	Design B	Design A	Design B
C_{max}	483.6 fF	553.8 fF	794.4 fF	848.1 fF	781.4 fF	897.3 fF
C_{min}	67.8 fF	86.9 fF	310.6 fF	290.9 fF	132.8 fF	166.3 fF
TR	613	477	155.7	191.5	488.6	439.5

7.1.3 Switch

An experimental lateral DC series switch has been built using the same electrothermal actuator as for the varactors. A description of the switch and how it was modeled is explained in chapter 6. The displacement of the switch was found using FEM analysis and the results are shown in table 7.3. The gap between the connecting beams is $1.2\mu m$ in the layout, which means that the minimum displacement needed for each beam is $0.6\mu m$.

Table 7.3: Displacement of the connecting beam

Temperature, T_{set}	Displacement
$238K$	$0.66\mu m$
$367K$	$-1.59\mu m$

7.1.4 Implementation

The chip sent to production was made together with one other master student and a PhD student. The chip contains a resonator, filters, varactors and the experimental switch made using the STM $0.25\mu m$ process. Figure 7.1 shows the layout of the entire chip where varactor 1 and 2 are varactor designs A and B respectively and the switch is the experimental switch presented in this thesis. The bonding pads used are designed such that they will not be destroyed by the etching process and two probing pads have been added to be able to test more designs. The anchors and the empty spaces between the components have been filled with different metal layers and polysilicon in order to meet the density requirements given by the CMOS design rules. Close-up figures of the different components can be found i section 4.4, 5.4 and 6.3.

7.2 Remaining challenges and suggestions for improvement

In this section remaining challenges and suggestions for improvement will be discussed. Some of these suggestions have not been further analyzed, and might lead to new difficulties not yet discovered.

Due to fabrication problems the performance of the fabricated circuit have not yet been measured. It is therefore difficult to determine how accurate the modeling of this CMOS-MEMS process is. One key parameter for the structures in this thesis is the built-in stress for the metal layers and the silicon dioxide. To be able to model this a simulation temperature T_{set}

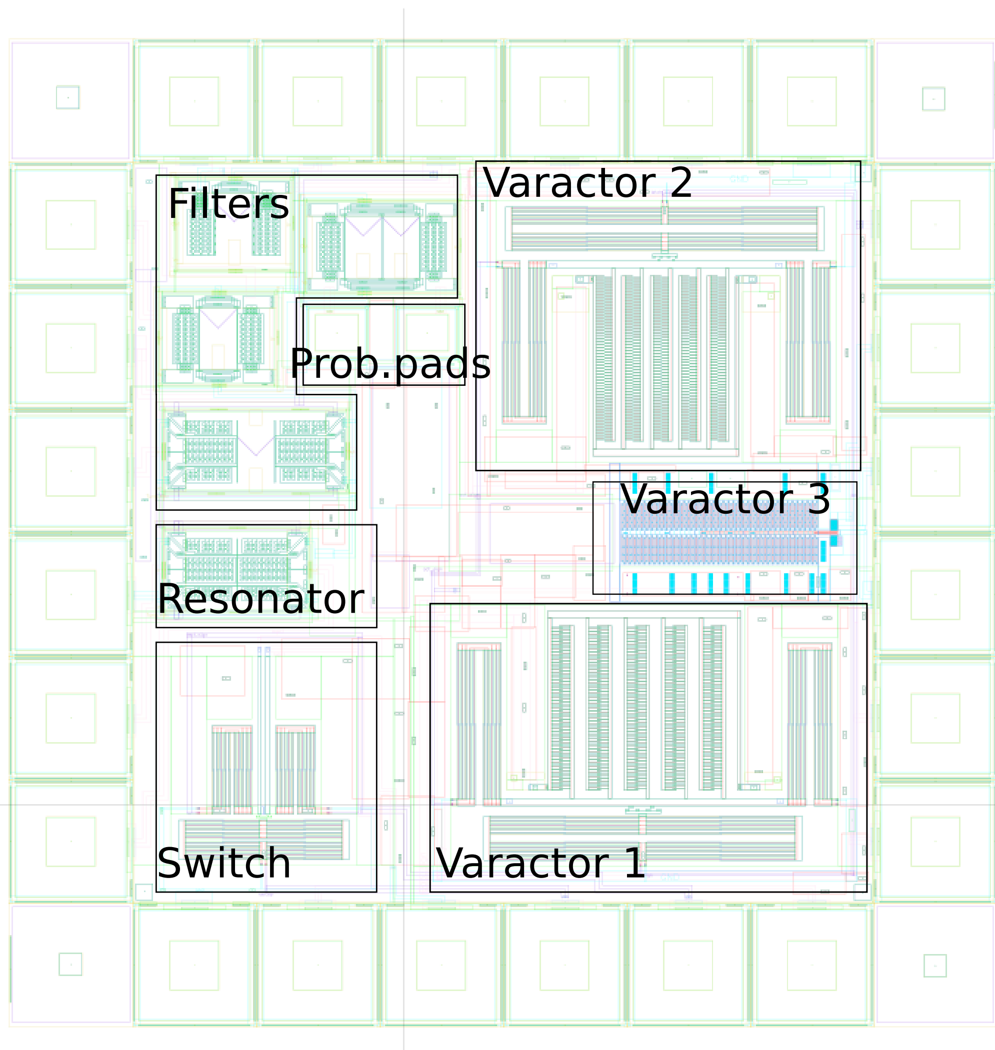


Figure 7.1: The layout of the chip

was calculated using equation (2.1), which depended on the characteristic temperature T_0. T_0 have been measured for different CMOS-MEMS beams by Lakdawala [25], but for a different CMOS process than the one used in this thesis. This means that the T_0 used for these structures is inaccurate and for more precise modeling T_0 should be derived for the STM $0.25\mu m$ process. Another simplification used in order to model the CMOS-MEMS structures was the material properties. Most of these properties are not available from the CMOS foundries, but can be derived experimentally.

As seen in chapter 4, some of the various geometrical parameters used for the fabricated actuators could have been improved. It was shown that the beam width of the actuator should have been made smaller in order to increase the displacement. However, tuning the geometrical parameters will only have small impact on the displacement. A more interesting approach will be to remove the polysilicon layer used to heat the beams. The polysilicon layer have a large Young's modulus and by removing it the beams will get larger deflection according to equation (4.5). However, some polysilicon is needed to heat the structure and if removed completely the actuator will not work. If the polysilicon was removed from the beams of the actuators, and the structure was heated with polysilicon heaters placed in the anchor and the side plates, greater displacement might be obtained. This requires that the polysilicon heaters placed in the anchor and the side plates of the actuator are sufficient to heat the whole structure.

It was shown that the material choice for the actuator was crucial for the total displacement, but the CMOS-MEMS structures are restricted to the available materials in the CMOS process. However, by using a different CMOS process other materials will be available. For the STM $0.25\mu m$ process used in this thesis the first metal layer was made of tungsten. As explained earlier the use of tungsten gave less displacement, due to high Young's modulus and small TCE. One advantage with tungsten is that it can withstand a much higher temperature than aluminum. This means that if only tungsten is used the structures can be heated to a higher temperature, which will give a larger displacement. However, this will only give a larger displacement in the "heated" state of the actuator (Δx_{heated}), while if only aluminum was used a larger self-assembly displacement could be obtained ($\Delta x_{release}$).

Another metal used in some CMOS processes is copper. Copper has a higher Young's modulus than aluminum, but a bit smaller than tungsten. In addition copper has lower TCE than aluminum, but higher than tungsten. This means that for the actuator used in this thesis the use of copper will lower the displacement compared to aluminum, but it will increase the displacement compared to tungsten. However, copper can withstand a higher temperature than aluminum, which means that a higher temperature can be used.

It was mentioned in chapter 2 that modern CMOS processes needed

better stress matching between the metal and the silicon dioxide to enable chemical-mechanically polishing of wafers with a diameter of 8" or above. Stress matching will lead to less out-of-plane and lateral curl, and will for most CMOS-MEMS structures improve the performance. However, since the actuators in this thesis exploits the lateral curl to a benefit, modern CMOS processes with better stress matching will lower the displacement. On the other hand, better stress matching will give less out-of-plane curl for the combs of the varactors, which will lead to an improvement of the sidewall capacitance.

In addition to different materials and stress matching, there will be some other factors that need to be considered if transferring these designs to another CMOS process. Various process parameters such as the number of metal layers, the thickness of the different layers and the material properties must be considered. By switching to another process, some of the conclusions made earlier in this thesis might not be valid, such as the influence of the top metal layer and the width ratio.

Another CMOS process will also have some different design rules which can lead to unexpected difficulties. However, it should be mentioned that a smaller version of the actuator presented in this thesis are planned to be used in a resonator circuit at UoO using the STM 90nm process. The planned application for this actuator is a nano-gap structure [36]. Here the self-assembly effect of the actuator is exploited to move the electrode closer to a resonator after release. By doing this the gap between the resonator and the electrode can be made much smaller than the minimum gap size set by the design rules, which will lead to better performance.

One of the remaining challenges for the varactor designs is the out-of-plane curl. Even though a curl compensation frame has been used it is expected that there will be some misalignments between the static and movable combs due to curling. Improved curl matching will lead to higher capacitances and higher tuning range. The curl can be reduced by using the post-processing technique with a backside etch, as explained in section 2.2.3. This technique leaves a thick silicon layer on the structures that will reduce the out-of-plane curl, but will lead to additional cost and technological difficulties. Other beam compositions (e.g. the use of fewer metal layer) may also reduce the curl, but this will also influence the total capacitance.

The total capacitance can be improved by either improving the displacement of the actuator to achieve larger finger overlap, or by improving the fabrication technique to reduce the gap between the fingers. Improving one of these factors will not only increase the capacitances, but also increase the tuning range of the varactors.

An alternative method to increase the tuning range is to build a varactor array. By arranging several varactors that can be tuned individually in parallel a higher tuning range can be achieved. If the varactor dimensions are chosen such that the maximum capacitance is doubled for each varactor

as seen in figure 7.2(a), fine tuning of the total capacitance will be possible. With this configuration the minimum capacitance will be determine by the sum of C_{min} for all the varactors. Another configuration that can be used to lower C_{min} even further is the use of MEMS switches to connect and disconnect the varactors, as shown in figure 7.2(b). With this configuration even larger tuning range can be obtained, and an even higher level of fine tuning will be possible. However, this configuration will require a much larger area, depending on the size of the switches.

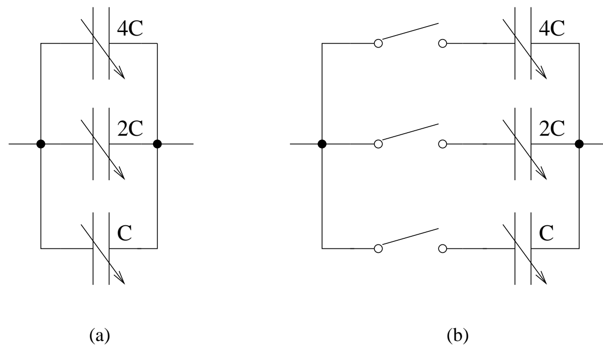


Figure 7.2: Varactor array (a) without switches (b) with switches

To improve the Q-factor the equivalent series resistance of the varactors must be decreased. This is will be difficult to achieve due to the special restrictions set by the post-CMOS process. The resistance can be reduced by using wider conductors, but this will influence other parameters such as the width of the beams and the number of fingers. Choosing other materials may also reduce the resistance, but this will only be possible if a different CMOS process is used. One material that has lower resistance than aluminum is copper. On the other hand, since modern CMOS processes with more metal layers also have thinner layers, the sheet resistance might be higher, even if copper is used. Since the fabricated circuit is not yet finished, the inductive part of the varactor have not yet been measured.

The switch presented in this thesis is for experimental use only. The main problem with the proposed switch is the switching time, due to slow electrothermal actuators. In addition the total area of the device is quite large. However, if the experimental result shows that a metal-to-metal connection can be obtained with this post-CMOS process, further work can be done to design better CMOS-MEMS lateral DC series switches, and by using electrostatic actuation switching time can be reduced. On the other hand, since electrostatic actuators have smaller deflection and energy density than electrothermal actuators, the connecting beams must be made softer in order to get large enough deflection to obtain connection. Figure 7.3 shows a possible implementation of an array of electrostatic switches using

this post-CMOS process. It is uncertain if this design will have low enough switching time for RF applications, but it can be used to switch between several different test designs which can lower the number of bonding pads needed.

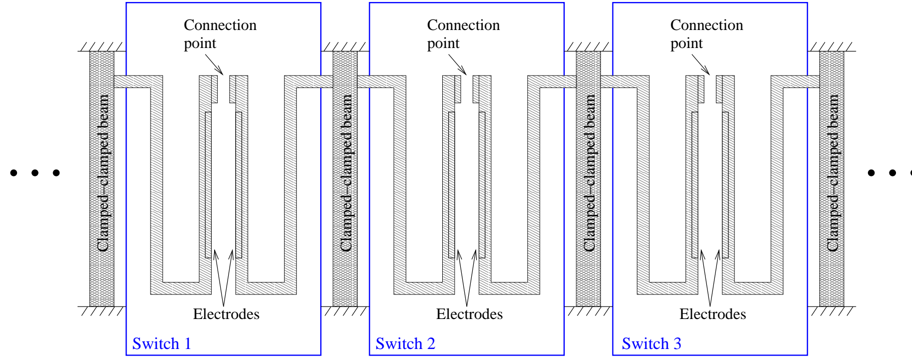


Figure 7.3: Switch array

7.3 This work compared to state-of-the-art RF MEMS components

Table 7.3 shows the capacitance, tuning range, driving voltage and Q-factor for a few state-of-the-art MEMS varactors [37, 38, 39, 40]. Note that these varactors are made using dedicated MEMS fabrication processes.

Table 7.4: Comparison of different RF MEMS varactors

Authors	**Capacitance**	**Tuning range**	**Driving voltage**	**Q-factor**
Peroulis et al.	$40 - 160fF$	300%	20-34V	80@40GHz
Lee et al.	$305 - 430fF$	41%	0-5.5V	34.9@5GHz
Fang et al.	$605 - 792fF$	31%	0-13.5V	51.6@1GHz
Nishimoto et. al.	$130 - 630fF$	480%	0-3.2V	100@7.5GHz

It can be difficult to compare different RF MEMS components, due to the range of various factors that need to be considered. It is important to remember that the components presented in this thesis are made using a CMOS-MEMS process that offers monolithic integration with CMOS at low cost. The material properties of the microstructures made with this process will not be as good as the state-of-the-art MEMS components made with dedicated MEMS processes, due to the stacked beam structure of metal

and dielectric. However, since these microstructures are on-chip with the CMOS circuitry the reduction in material properties can be outweighed by the possibility of fast on-chip signal processing. Common challenges such as impedance matching may be ignored since the signal paths are on-chip and therefore much shorter than for other RF MEMS systems.

Compared with the work by Altung Oz from CMU, the varactors in this thesis is approximately equal concerning performance. One problem with the varactor presented by Oz was the the fingers would not interdigitate due to width bloating. To avoid this the gap in design B has been made a bit larger than the one used by Oz. For design A this will not be a problem since the fingers are already interdigitated in the layout. The actuators have a bit less displacement than the one made by Oz. The reason for this can be that a different CMOS process is used, and that the width of the beams of the actuator was made too large. In addition it should be mentioned that some of the conclusions drawn by Oz do not concur with the simulation results from this thesis. The reason for this can be inaccurate simulation models and/or the use of a different CMOS process.

Several MOS varactors have been made with high tuning range and high Q-factor [41]. However, one problem with these varactors is high phase noise. Innocent et al. have compared a RF MEMS varactor with a MOS varactor for a $5GHz$ VCO [42]. This paper concludes that the MEMS varactor have less phase noise than the MOS varactor, but that the driving voltage has to be lowered and the risk of accidental pull-in has to be avoided if MEMS varactors should be an alternative for mainstream applications. The varactors presented in this thesis have low driving voltage, the electrothermal actuation avoid pull-in and the post-CMOS process enables complete integration of MEMS and CMOS. VCOs made using RF MEMS components fabricated with the same post-process and with approximately equal performance as the varactors presented in this thesis has been made [6, 43], which shows that these CMOS-MEMS varactors can be used for LC VCO with low power and phase noise.

Chapter 8

Conclusions

Two lateral RF MEMS varactors and an experimental switch have been made using electrothermal bimetal actuators. All the devices have been thoroughly analyzed and show promising results. Bimetal actuator theory has been used to predict the effect of the different design parameters and it has been shown how this theory can be used to calculate the displacement of the actuator. The effect some of the design parameters had on the displacement was first discovered after the chip was sent to production, and it has been shown that the beam width of the actuator should have been made smaller. For the varactor it was shown that the back of the combs should have been made as tapered beams to avoid lateral curl. Since the fabricated circuit did not come back from production in time for measurement only analytic calculations and simulated results have been presented. The capacitances of the varactors is in the range of $133 - 897fF$, with tuning ranges of 440% and 489% and Q-factors of ~ 30 at $2GHz$. Since no measurements have been done, it is uncertain if the proposed switch will work. A summary of the achieved results can be found in chapter 7.

One of the challenges with MEMS structures is that they often requires an expensive and unique fabrication process. In addition the MEMS devices and the CMOS circuitry are often produced on separated chips, which lead to additional parasitic components, area and cost. The fabrication process used for this thesis is a post-CMOS process that offers a complete monolithic integration of MEMS and CMOS on the same chip. This is both area and cost efficient and reduces the number of parasitic components. Although microstructures produced using this post-process shows a bit lower performance than state-of-the-art MEMS structures, these disadvantages can be outweighed by fast on-chip signal processing. A temperature offset have been used to model the built-in stresses in the different layers of the CMOS process. However, the main obstacle with this work has been inaccurate modeling, due to the lack of information about the material properties for the STM $0.25\mu m$ CMOS process. In addition, these properties vary from

process to process, which means that they have to be derived all over again when switching to a different CMOS process.

8.1 Future work

The post-process used shows promising results, but for future work several material properties must be derived for more precise modeling. As mentioned, these properties are not available from the CMOS foundries and must therefore be derive experimentally.

Various design parameters of the actuator have been presented. A discussion on how these parameters can be tuned to obtain maximum deflection can be found in chapter 7. The most interesting suggestion to improvement is to use a different CMOS process. It has been shown that the tungsten layer in the STM $0.25\mu m$ process lowers the performance of the actuator, and it is therefore reason to believe that a different CMOS process, where all the metal layers are made of aluminum will give a larger displacement.

An analytical model have been presented to predict the effect of the different design parameters, but in order to use this model for analytic calculations of the displacement of the actuator a model of the layered CMOS-MEMS beams must be derived.

If the experimental switch shows that the roughness of the sidewalls are small enough to obtain a good metal-to-metal connection future work can be done to make a faster, smaller and more energy efficient lateral DC series switch in this post-CMOS process.

The structures in this thesis was made using a CMOS-MEMS process, but was fabricated without any CMOS circuitry. If the future measurements of the components concur with the modeling, an integrated system with both MEMS and CMOS can be made.

Appendix A

Published paper

RF MEMS front-end resonator, filters, varactors and a switch using a CMOS-MEMS process

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RF MEMS front-end resonator, filters, varactors and a switch using a CMOS-MEMS process

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Abstract: The paper describes the design of multiple RF MEMS front-end components that could replace off-chip units in future transceivers. The components can effectively be combined and co-fabricated with CMOS circuitry. A CMOS-MEMS approach is used, which means that the microelectromechanical parts are made by multi-layer structures in a standard CMOS process. The ASIMPS procedure offered by CMP uses the CMOS processing at STMicroelectronics, and a simple post-CMOS release-etching step is performed at Carnegie Mellon University, USA. The paper presents a resonator, resonating filters, electrothermally operated varactors and an experimental switch. The components are modeled and simulated by using CoverntorWare FEM software. A test chip is currently in production.

I. INTRODUCTION

To make future wireless sensor devices smaller, smarter and more autonomous, fully integrated and multifunctional nodes will be required. It is challenging to design on-chip RF front-end devices, and today's solutions typically use discrete, off-chip components to meet the RF performance requirements (external inductors, crystals, SAW and ceramic filters). It has been shown that micromachined components (RF MEMS) can beneficially replace a great number of those bulky off-chip components with even better performance, smaller size and lower power consumption [1].

The combination of micromechanical components (MEMS) and microelectronics (CMOS) has traditionally been done by using multi-module packaging involving part production and assembling at diverse premises and costly handling steps. The future of radio communication is moving toward integration of multiple radio standards into a 'single chip radio'. To see this vision come through, on-chip varactors and filters with high Q-factor and large tuning range are needed [2,3].

This paper presents one resonator, four filters, three varactors and one experimental switch that can be used as RF MEMS components. These RF front-end components are analytically modeled and simulated using FEM (Finite Element Method) software.

II. THE CMOS-MEMS PROCESS

In this paper, a circuit has been designed by using a conventional 0.25µm CMOS process from ST-Microelectronics. The MEMS parts of the circuit are etched by post- processing at Carnegie Mellon University in Pittsburgh, USA, through the broker service CMP [4]. By using laminated structures of metals and dielectrics, it is possible to make micromechanical structures that can be used as RF MEMS components, operating in close interaction with CMOS circuits. Figure 1 shows the post-CMOS process, which is used for these RF MEMS designs.

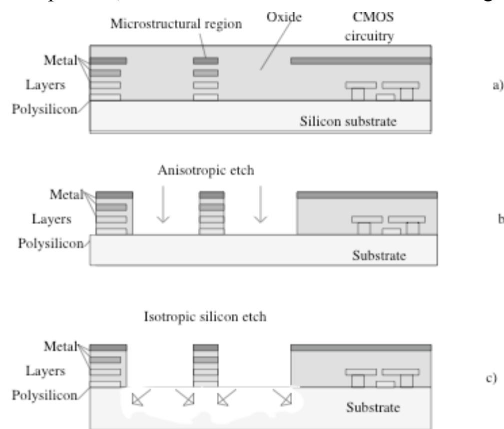

Fig. 1. Description of the post-CMOS process

This post-CMOS technique is particularly interesting because it does not require any modifications of the original CMOS process and the technique does not need additional photomasks for post-processing. The residing top metal layer will define the microstructures and will also serve as a mask to protect the underlying CMOS circuitry from being etched. The microstructures are etched and released using RIE etching equipment. This dry etching technique makes it possible to etch narrow gaps with a high aspect ratio. This post-CMOS technique has yielded good results for various applications from research institutes such as Carnegie Mellon University in USA, National Tsing Hua University in Taiwan and University of Oslo in Norway [5,6,7,8].

The number of metal layers used to define the structure determines the resulting thickness of a microstructure. A thick structure is in most cases preferred, but the thickness is limited by the number of metal layers in the actual CMOS process. When the materials are deposited in a CMOS process residual stress occurs, showing its effect when the structures are released. Stress tends to make the structures curl and care must be taken when designing structures that are supposed to be flat. The curling of a MEMS structure may in some cases be used as an advantage (see section V).

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III. RF MEMS RESONATOR AND FILTERS

One resonator architecture and four filter architectures have been investigated. These filters and resonators are structures that move laterally, parallel to the substrate. The resonator and the filters are made by a laminate of metal and dielectric using metal layer 1 through metal layer 4 as shown in figure 2. For the filters, the coupling beam between the resonators is designed as a 45° V-shaped beam, constrained by the CMOS process. The location of a coupling beam along the beam length affects the bandwidth of the filter; placing the coupling beam close to the anchors gives a high percentage bandwidth. The number of resonators that are coupled together determines the order of the filter.

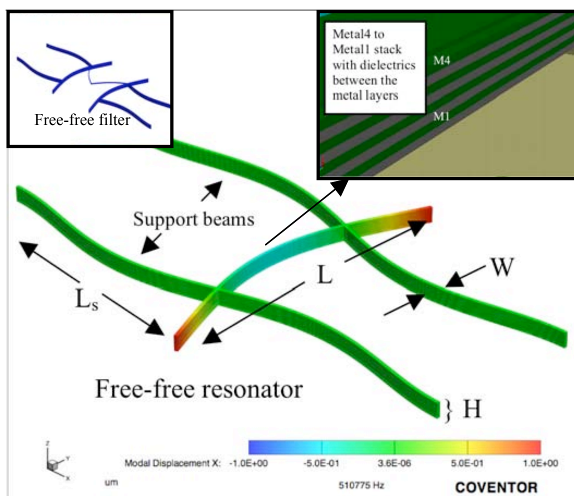


Fig. 2. A free-free resonator (middle) and a free-free filter (top left)

Fig. 2 shows a free-free resonator that has support beams with the length L_s at position L/4 and 3L/4 of the length of the resonator. Because of the chosen dimensions, the free-free beam is designed so that the support beams operate at their second resonating mode (mode number two) while the beam in the middle operates at mode number one. The support beams exert extensional forces to the beam in the middle, representing "infinite" impedance. Due to the nearly infinite impedance from the support beams, a minimum of energy is lost per cycle by the device, making it possible to operate this device with a high Q-factor even at atmospheric pressure. The resonators and filters in this paper all have a length L, a width W and a thickness H as shown in figure 2. Fig. 3 shows a top-down view of the free-free resonator and a 4th order free-free filter using the V-shaped coupling beam. The red crosses indicate the anchor points of these structures. The arrows indicate the input and output of the resonator and filters. Equation (1) shows the equation for the resonance frequency where κ depends on the type of resonator (cantilever, clamped-clamped, free-free).

$$f_0 = \kappa \sqrt{\frac{E}{\rho} \frac{W}{L^2}} \qquad (1)$$

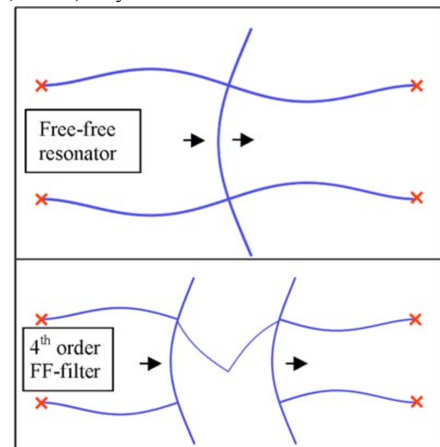


Fig. 3. Top: Free-free resonator. Bottom: Free-free filter

Figure 4 shows three other filters that have been made. One cantilever (one fixed end) and two clamped-clamped beam (two fixed ends) filters have been designed by having two and three resonators coupled together using the V-shaped coupling beam. The 6th order CC-filter gives a better stop band attenuation compared to a 4th order CC-filter.

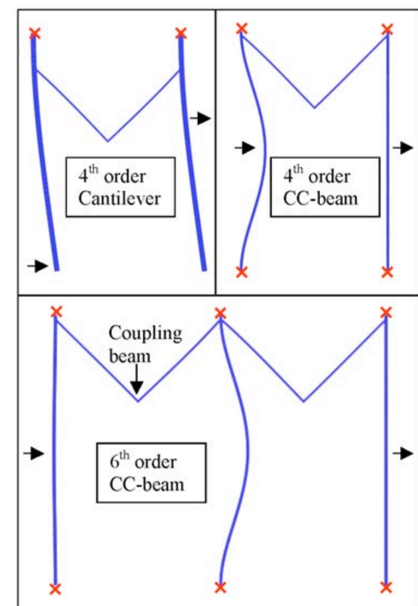


Fig. 4. Top left: 4th order cantilever filter. Top right: 4th order clamped-clamped (CC) filter. Bottom: 6th order CC-filter

The input and output electrodes are not shown in these figures but are situated close to the input and output arrows. The length L_s for the free-free resonator and filter is described by equation (2) [9].

$$L_S = 0.5 \cdot 1.683 \left(\sqrt{\frac{E}{\rho} \frac{W}{f_0}} \right)^{1/2} \qquad (2)$$

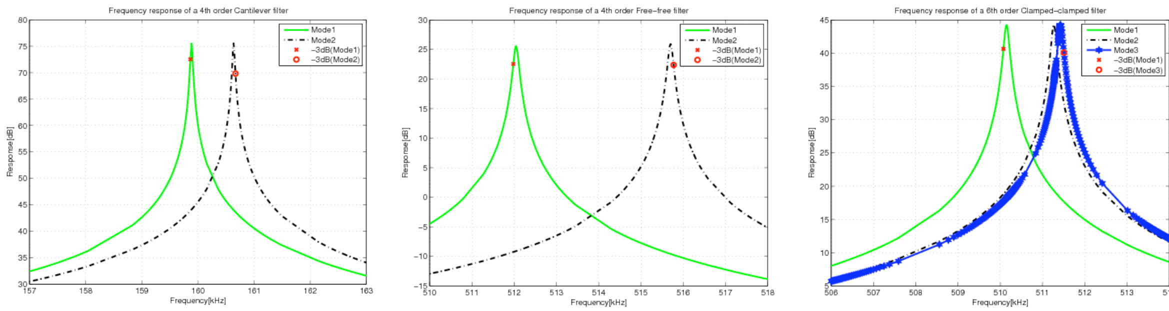


Fig. 5. Left: 4th order cantilever filter. Middle: 4th order free-free filter. Right: 6th order clamped-clamped filter

Figure 5 shows the filter response (CoventorWare, mechanical simulations) for a 4th order cantilever filter, a 4th order FF-filter and a 6th order CC-filter, respectively. It can be seen from these graphs that the -3dB value is located before and after the first and last mode of the response. The 6th order filter has a better attenuation in the stop-band of the filter. The pink line between the first and second mode in fig. 6 shows a theoretical representation of a flattened filter using termination resistors at the input and output of the filter.

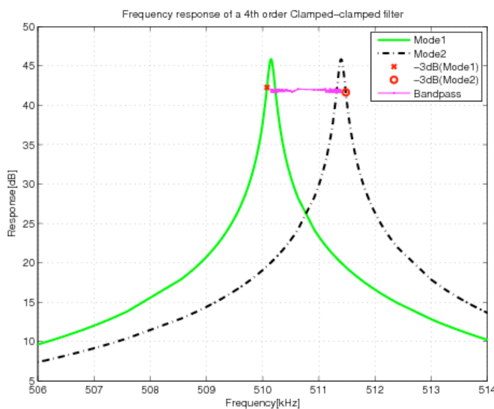


Fig. 6. Filter response for a 4th order CC-filter

Table I summarizes the dimensions of the filters and the single resonator as well as showing their respective resonance frequency (without applied polarization voltage).

TABLE I
Resonator dimensions

	Cantilever	Clamped-clamped	Free-free
Thickness H (µm)	4.8	4.8	4.8
Width W (µm)	2	1	1
Length L (µm)	100	100	100
Electrode length (µm)	75	80	42
Electrode gap (µm)	1.2	1.2	1.2
Resonance freq. (kHz)	159.45	510.63	510.774

The bandwidth of these filters have been made by tuning the coupling beam location towards the anchor points described in equation (3) where k_{12} is a normalized coefficient, k_{s12} is the coupling beam stiffness and $k_r(y)$ is the resonator stiffness [3].

$$BW = \frac{f_0}{k_{12}} \frac{k_{s12}}{k_r(y)} \qquad (3)$$

TABLE II
Filter characteristics

	Cantilever 4th order	Clamped-clamped 4th order	Clamped-clamped 6th order	Free-free 4th order
Coupling-to-anchor (µm)	15	1.5	1.5	0.5
Center frequency (kHz)	160.266	510.778	510.949	513.872
Band-width (kHz)	0.803	1.403	1.431	3.793
Q-filter	199.6	364.1	357.1	135.5
Termina-tion resistance [MΩ]	1.19	4.81	6.94	12.92

Table II shows the performance of the filters. The free-free filter has a high bandwidth and has a good resonator Q-value. The cantilever beam has a low operational frequency but instead it has a relatively good percentage bandwidth. The 6th order CC-filter has a slightly lower percentage bandwidth than its 4th order counterpart, however the rejection ratio of a 6th order CC-filter is much better as can be shown by the Cadence simulation in figure 7.

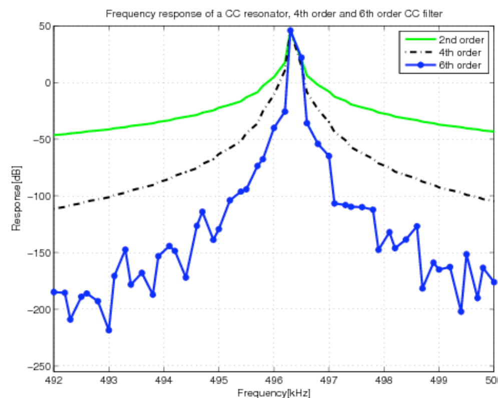


Fig. 7. Frequency response for a 2nd to 6th order CC resonator-filter

IV. Lateral Varactors

Two lateral varactor architectures with high tuning range have been made. Both capacitors are based on area tuning of combs moving laterally, parallel to the substrate, as seen in fig 8. A common problem with post-CMOS is the out-of-plane curl that can cause offset between two electrodes or sensing nodes. Any offset between the combs will lead to a significant reduction in sidewall capacitance. The out-of-plane curl can be minimized by aligning the anchors along a common axis. A curl compensation frame is used to get equal out-of-plane curl for both the movable and the static comb.

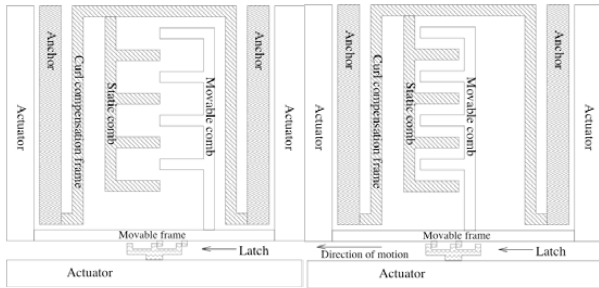
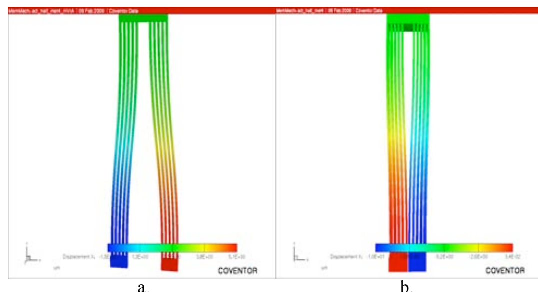


Fig.8 Lateral varactor principle

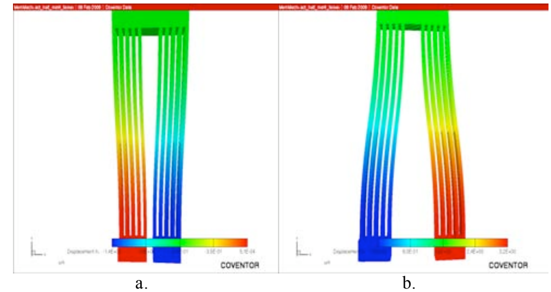
Both varactors are controlled by electrothermal actuators as presented by Oz et al. [10]. The actuators have an offset between the top metal layer (used as an etch resistive mask) and the lower metal layers. The lower metal layers have been placed asymmetrically by being offset to one side of half the beam length. For the other half of the beam, the metal layers are offset to the other side. Because the residual stress in aluminum is tensile while the residual stress in silicon dioxide is compressive, the actuator will move in an 'S' shape when released (self-assembly) as seen in fig 9. When heated by embedded poly-resistors placed at the bottom of the beams, the actuator will contract due to the different TCEs (Temperature Coefficient of Expansion) for aluminum and silicon dioxide. VIAs are used between the layers to achieve higher metal density and thereby greater deflection. Two electrothermal actuators have been made. The first actuator is shown in figure 9. This actuator will expand when released (a), and contract when heated (b). The total displacement are given by $\Delta x = \Delta x_{released} + \Delta x_{heated}$



a. b.

Fig.9 a) First actuator after release b) First actuator heated

By changing the metal offset in the beams to the other side, the actuator will contract instead of expand once released (Fig. 10). The displacement is almost equal to that of the first actuator.

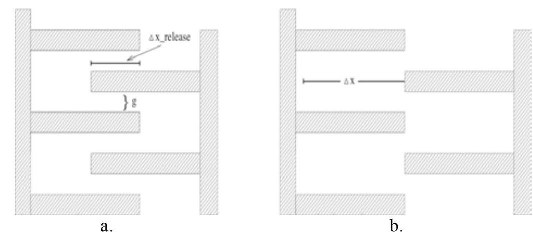


a. b.

Fig.10 a) Second actuator after release b) Second actuator heated

A latch mechanism for keeping the beams in a fixed position is added so the actuators only require power during switching [10]. The latch used for these designs have two slots which gives two different stable positions. This means that two steady capacitor values can be obtained. The latch can be extended with more slots if desired.

There are two varactor designs: Design A and design B. In design A, both actuators are used while in design B only one of the actuators is used. The combs in design A have a small finger overlap in the layout (Fig. 11), which equals the anticipated displacement $\Delta x_{release}$ of the actuator after release. This design uses both actuators; one actuator will push the combs while the other will pull. By exploiting the self-assembly of the actuators maximum overlap Δx will be obtained. However, because the fingers have an overlap in layout, the gap between the fingers will be restricted by the post-process design rules. Design A has a size of 626.6x424.3μm without the anchors, with a finger gap g = 1.2μm and Δx = 17μm.



a. b.

Fig.11 Varactor design A: a) layout b) after release

Design B has shorter fingers without any overlap in the layout and the fingers are intended to stay in the same position after release. Since the fingers have no overlap in layout, the gap can be made smaller than for design A. A smaller gap will for a given overlap area offer larger capacitance. However, the maximum overlap, LO, for design B will be less than Δx_{heated}. Design B has a size of 549.6x424.3μm without the anchors, with a finger gap g = 0.8μm, Δx_{heated} = 12μm and LO = 10.8μm.

TABLE III
Capacitance values

	Analytic calculation		Simulated with Coventorware	
	Design A	Design B	Design A	Design B
Cmin	296 fF	291 fF	133 fF	166 fF
Cmax	780 fF	848 fF	781 fF	897 fF
Tuning range	163 %	192 %	489 %	439 %

Table III shows calculated and simulated capacitance values for the two varactor designs. The simulation of the varactors has been separated in different parts in order to achieve more thorough results.

V. An Out-of-Plane Varactor

Simulations of a large tuning range varactor based on an out-of-plane curled cantilever are presented. The cantilever has comb fingers attached on both sides (rotor), which in the layout overlap a set of stationary fingers (stator). Utilizing the initial curl due to residual stress in the CMOS-MEMS process and the different TCE in metal and oxide layers, an out-of-plane actuator can be made by a single cantilever beam. After the release of the structure, the actuator initially elevates the tip of the rotor comb over the chip plane. When the beam is heated with a built-in poly resistor, the cantilever will uncurl and flatten towards the anchored stator comb due to temperature dependent radius of curvature. As the actuator uncurls, the rotor comb folds into the stationary comb, the area overlap is increased and thereby the capacitance is increased. The capacitor is shown in figure 12.

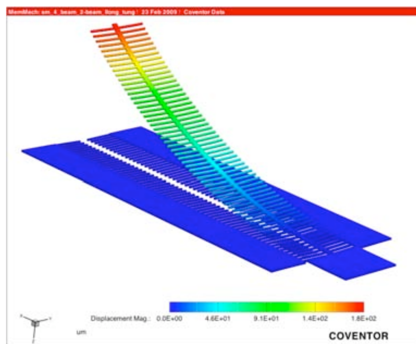


Fig 12. Curled comb varactor

A. Initial out-of-plane curl

Layers in the beam are deposited and metallized at high temperatures. As the structure is cooled the large difference in TCEs for aluminum and oxide builds up compressive and tensile stress in the oxide and aluminum layers, respectively. When the structure is released, stress in the multilayer beam forces it to curl out of the plane [11, 12]. The initial curl is given by the combination of layers. Results from [11] were used as a guide for prediction of the initial curl in the post-CMOS process, and to maximize the initial curl, metal-1, metal-2 and oxide layers were mainly used. The "ACTIVE" layer in the CMOS process was avoided, since the field oxide is much more compressive stressed than thin oxide and makes the structures curl even more [13]. Simulations of mechanical and electrical behavior are done with the CoventorWare simulator, and to model the initial curl, a simulator-offset temperature is set [11].

The metal and dielectric layers have different TCEs, which will cause the MEMS structures to bend upward or downward dependent on the temperature. For this structure, heating is used to reduce the out-of-plane deflection and align the actuator with the substrate. The temperature dependency for a 300µm long metal-1+metal-2 beam is simulated to 0.3µm/K. The maximum temperature for the CMOS-MEMS structures is 570K before the material yields, which can give a theoretical maximum deflection of 90µm if the structure is initially held at room temperature. The predicted initial curl, based on [11], is 50 to 30µm. This gives an in-plane alignment temperature from 186 to 120 °C.

To heat the structure, a current is passed trough a polysilicon resistor placed under the beam. The resistor is formed as a loop under the beam to distribute the heat. The steady-state temperature is linear with dissipated power in the resistor [14].

B. Variable capacitor design

The simulated capacitor is composed of one static (stator) and one moving comb (rotor). The comb fingers are 44µm long and the distance between the fingers in the stator and rotor comb are 1.5µm. The rotor comb is 320µm long and has 80 fingers, which gives a total of 160 fingers. Distances and numbers of fingers per area are limited by the post-CMOS design rules. Figure 13 show the capacitance change as the actuator is heated and uncurled. To simulate the initial curl, the in-plane alignment temperature has to be subtracted in the simulator. This gives the offset temperature axis in figure 13.

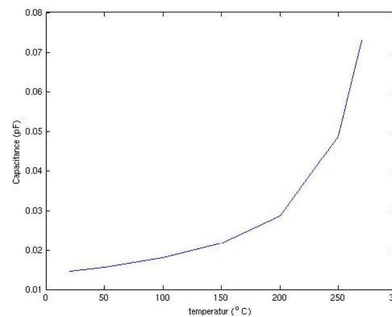


Fig. 13. The capacitance increases non-linearly with increasing temperature

Initial curl of 50 to 30 µm corresponds to a simulator temperature offset of 173 to 100K, which gives a minimum capacitance of 18 to 25fF. The maximum capacitance (varactor aligned with the substrate at 186-120 °C) is simulated to 74fF and the tuning range from 200 to 310 %.

VI. An Experimental Post-CMOS Switch

An experimental lateral DC series switch is designed as a test structure to see if it is possible to make a metal-to-metal connection by using this post-CMOS process (Fig.14). Since the CMOS structure is built by using layers of aluminum and oxide, the contact area will be smaller for this CMOS-MEMS process than for other MEMS processes. If there is any vertical offset between two CMOS-MEMS structures, that should intentionally connect, then the possibility of obtaining a connection between the metal layers could fail. By this test structure we will investigate how well defined the sidewalls of the beams are. The switch is actuated with similar electrothermal actuators as used for the lateral capacitors described in section IV (only smaller dimensions). A metal-to-metal connection will be obtained after release due to the self-assembly effect of the actuators. When heated the electrodes will be drawn apart and the connection will be broken. A similar latch mechanism as described in section IV has been used to minimize the power consumption. If the experimental electrothermal yields good results, it would be possible to try to make an electrostatic switch.

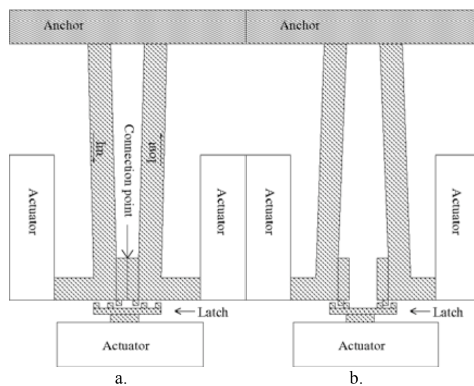


Fig.14 Experimental switch a) after release b) heated

VII. Conclusion

Several front-end RF MEMS devices integrated in a CMOS-MEMS process has been shown. Simulation results using CoventorWare has been done for these devices. The simulations of these CMOS-MEMS components show that these components yield sufficient results to be used in an analog front-end radio transceiver. The laminate of metal and dielectric results in an adequate performance that is not as good as state-of-the-art MEMS. However, by avoiding off-chip components, these on-chip filters and varactors combined with on-chip processing electronics yields sufficient performance for a modern radio front-end transceiver.

The RF MEMS components presented in this paper shows filters operated at 160 and 510kHz, varactors with a tuning range of ~450% and ~300%. In addition, an experimental electrothermal switch has been presented. Figure 15 shows an overview of the chip-layout in Cadence.

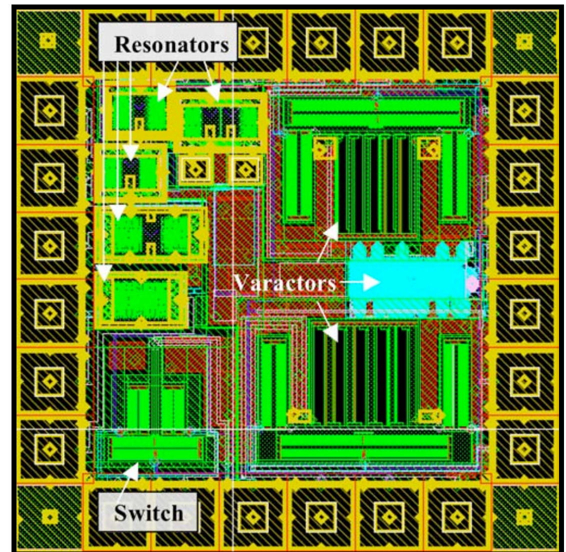


Fig.15 Chip layout of the resonator-filters, varactors and the switch

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