Out-of-plane CMOS-MEMS variable capacitor

Master thesis

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Abstract

To be able to create small integrated wireless radio front ends, variable capacitors that can be monolithically integrated on the same chip as the electronic circuits are needed. Today’s radio front ends are based on solid-state diode varactors which suffer from poor tuning range and phase noise and do not meet the requirements for a fully integrated wide band radio front end. In this thesis we will look at possibilities for implementation of a monolithic integrated MEMS varactor.

A post-CMOS-MEMS process is used to manufacture the structures. The post-process is a combination of anisotropic RIE dry etch steps and an isotropic release step, which makes monolithic integration simple and low cost. The actuation mechanism is based on an out of the plane curled cantilever beam. Initial curling of the structure as a result of residual stress in the CMOS layers of the chip is utilized to initially levitate the actuator over the chip plane. To actuate the varactor combs, the actuator is heated with a joule-heating element placed under the structure. When the the actuator is heated to the in-plane alignment temperature, maximum capacitance is obtained. Simulations and analytic models are used to predict the performance of the actuator and varactor. The analytic models presented and developed make development of out of plane curled varactors more efficient and simpler than with FEM simulations only. The complete varactor design was included in a test circuit sent to production in November 2008.

Simulations and models yield good results for tuning range and Quality-factor. The tuning range is predicted to be between 240 % and 325 % and the Q-factor is calculated to be $\approx 30@1.5GHz$. The tuning voltage required for operation of the varactor is within 8 V and the varactor does not suffer from pull-in, which is the case for electrostatic based varactors.
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## Contents

Abstract i

1 Introduction 1
   1.1 40 years of MEMS 1
   1.2 Motivation 2
   1.3 Proposed structure 2
   1.4 Thesis disposition 3

2 CMOS and MEMS monolithically integrated 5
   2.1 RF MEMS 5
   2.2 Microfabrication 6
      2.2.1 Bulk micromachining of silicon 6
      2.2.2 Surface micromachining 7
   2.3 Monolithic integration 8
      2.3.1 Pre-CMOS 8
      2.3.2 Intermediate CMOS 8
      2.3.3 Post-CMOS 9
   2.4 STM BiCMOS7RF ASIMPS Production Process 10
      2.4.1 CMOS 10
      2.4.2 Integration 10
      2.4.3 Maskless post-CMOS MEMS 11
      2.4.4 Structural composition 11

3 Varactor 13
   3.1 Theory of variable capacitors 14
   3.2 CMOS-MEMS varactor designs 15
      3.2.1 Gap tuning 15
      3.2.2 Area tuning 16
      3.2.3 Gap Tuning varactor by Oz and Fedder 16
      3.2.4 Area and Gap Tuning varactor by Oz Fedder 2nd generation 16
      3.2.5 Out-of-plane CMOS-MEMS resonator 18
   3.3 Out of plane varactor proposal 19
4 Out-of-plane actuation 21
4.1 Residual stress in laminated structures 21
4.1.1 Thermal Stress 22
4.1.2 Intrinsic Stress 23
4.2 Initial Curl predictions 23
4.2.1 Stress Tuning 24
4.3 Temperature dependency 25
4.3.1 Curling of two-layer cantilever 25
4.3.2 Curling of multilayer cantilever 27
4.3.3 Characteristic temperature 28
4.4 Experimental results 29
4.5 Derivation of $\frac{\partial \delta}{\partial T}$ 29
4.5.1 Ion-milling of top-metal-layer 29
4.6 Out-of-plane actuator discussion 30

5 Models and simulations 31
5.1 Finite Element Method 31
5.2 Thermal distribution 33
5.3 Actuator 34
5.3.1 Modeled vs simulated temperature dependency $\frac{\partial \delta}{\partial T}$ 35
5.3.2 Stress simulations 37
5.3.3 Ion milling 39
5.4 Capacitance 39
5.4.1 Field distribution 40
5.4.2 Modeling of the capacitance 41
5.4.3 Minimum gap 44
5.4.4 Comb length 46
5.4.5 Simulated vs modeled capacitance, test structure 46
5.4.6 Modeled capacitance, proposed structure 49
5.4.7 Q-factor, proposed structure 49

6 Implementation 53
6.1 Die layout 53
6.1.1 Dummy capacitor 55
6.2 Design considerations 55
6.3 Structure layout 56
6.3.1 Poly heater 56
6.3.2 Comb fingers 58

7 Discussion 59
7.1 Features and benefits 60
7.1.1 Tuning range 61
7.1.2 Area efficiency 61
7.2 Challenges 62
Chapter 1

Introduction

1.1 40 years of MEMS

When IC fabrication started 50 years ago, there has always been an interest for transducing mechanical, optical, chemical or thermal input to electric signals. In the 1960s etched silicon sensors were developed and a decade later, the term "micromachining" was introduced for this kind of process. The further development of more complex and high production volume applications was driven by the automotive industry. Engine control for reducing fuel consumption and emissions was their main focus. In the 1980s the technology evolved and more complex devices emerged. Late 1980s the term MEMS (MicroElectroMechanical Systems) was established. In the 1990s, single actuators and sensors moved to more integrated microsystems. Research was now more focused on accelerometers and driven by the automotive airbag market. MEMS devices dominated and are still dominating this market due to high volume, low cost properties of MEMS production.

In the 1990s MEMS research was divided into several sub-fields like RF (Radio Frequency) MEMS, MOEMS (Optical MEMS), fluid MEMS and bioMEMS. Development of MEMS-switches, resonators, and antennas for RF was now denoted as the sub-field RF MEMS. Moving into a new millennium, the interest for wireless integrated microsystems (WIMS) increased [1]. One research area and our research is now focused on monolithic integration of wireless front-end devices based on RF MEMS.
1.2 Motivation

To meet our visions of an integrated wireless device for several frequency bands, high quality RF components have to be developed. The quality of variable capacitors or more commonly called a varactor is critical when it comes to the frequency tuning range, accuracy of tuning, Quality-factor and noise of the whole system. Today’s varactors, based on solid-state p-n junctions, are for demanding applications not meeting the required tuning range, Q-factor, phase noise and size. A way to overcome these problems can be a micromachined mechanically controlled capacitor on the same chip as the rest of the transceiver [2] [3].

This inspired us to investigate how high tuning range/Q-factor varactors can be implemented in MEMS. Important criterias for this implementation are easy monolithic integration with CMOS and a minimum of additional steps to the standard CMOS process. Based on literature studies, a new way of implementing a varactor in CMOS-MEMS is proposed.

1.3 Proposed structure

In this thesis we will look at how we can implement a MEMS-varactor in a CMOS/BICMOS process. A post-CMOS fabrication process is used to create the MEMS structures. The top metal layer of the CMOS layout here acts as a mask defining the mechanical structures. The microchip is then etched and the structures are released. This process flow makes integration with conventional CMOS electronics and a monolithic implementation practical.

The varactor is composed of an actuator and two combs. To tune the capacitance of the capacitor, a voltage controlled actuator moves the combs into and out of each other. The actuator is based on out of plane curling due to residual stress in the MEMS structures and variation of TCE (thermal coefficient of expansion) in the layers of the actuator. The rotor comb of the capacitor is attached to the actuator and when the actuator is heated, the combs fold into each other and become aligned. This increases the capacitance. When the actuator is cooled the capacitance decreases due to the decreased overlapping area and increased gap. Figure 1.1 displays the varactor in the anticipated initial condition at room temperature.
1.4 Thesis disposition

In Chapter 2, CMOS and MEMS monolithically integrated, integration of CMOS electronics and MEMS and why it is beneficial with monolithic integration are discussed. The maskless post-CMOS MEMS process used in the varactor design is presented. **Chapter 3, Varactor,** presents basic theory of variable capacitors and different examples on how varactors can be implemented in a post-CMOS-MEMS process. **Chapter 4, Out-of-plane actuation,** covers residual stress in CMOS-MEMS structures and how the stress affects released MEMS structures. An analytic model for the out of plane curl and the temperature dependency is presented. In **Chapter 5, Models and simulations,** the analytic models are applied to the proposed structure and compared with simulation results form CoventorWare. An analytic model is developed and in combination with computer simulations are used to predict the capacitance with respect to the applied control voltage. The implementation of the proposed structure is presented in **Chapter 6.** The predicted performance of the proposed varactor is compared with CMOS-MEMS varactors from the literature in **Chapter 7.** Advantages and drawbacks of the design are also discussed in this chapter. **Chapter 8 concludes the work.**
Chapter 2

CMOS and MEMS monolithically integrated

There are several benefits from integration of control/measurement electronics and the MEMS structures on one die. Monolithic integration implies reduced size and minimum bonding. Depending on the application, packaging cost, which is a major expense, can be reduced with monolithic integration compared with a multi-chip-module approach. For RF applications that do not require environmental input and benefit from minimized interconnect, monolithic integration seems like a good approach.

Due to limitations in existing RF devices, new and more efficient devices are needed. Many interesting structures and integration methods have been shown in the literature. With an on-chip integration of RF components, small-sized, high frequency radio systems can be created [3].

2.1 RF MEMS

In RF systems, components such as capacitors, inductors, varactors, switches, amplifiers, matching networks and filters are important for the overall performance. High performance MEMS components are good candidates for replacing solid-state components and improving today’s RF communications systems. Many passive components with better performance than solid-state passives have been shown in the literature [3], but a major challenge for both MEMS and CMOS industries are standardization and integration of RF MEMS. Especially monolithic integration looks feasible for future communications and WIMS systems, where minimal use of RF transmission lines, size and cost are critical [4].
C.T.-C Nguyen at UC Berkley has presented a futuristic vision of how RF MEMS components can be used in a RF front end receiver [5]. Figure 2.1 shows a possible architecture of a RF transceiver where the solid-state RF components are replaced by RF MEMS. If all the system blocks can be monolithically integrated, a radio transceiver can move from today’s printed circuit board (PCB) packaging to a single package level.

![System-level block diagram of a RF transceiver where the areas marked with green is RF MEMS passive components (Fig from [5])](image)

**Figure 2.1**

### 2.2 Microfabrication

There are many different processes for implementing MEMS designs. Micromachining has been the fundamental technology for fabrication of MEMS devices since MEMS devices started to be produced. Micromachining is typically divided into two fabrication methods: bulk and surface micromachining.

#### 2.2.1 Bulk micromachining of silicon

Bulk-micromachining is a way of using the substrate of a single-crystal silicon wafer to create structures. Selectively removing wafer material with wet-etch or dry Reactive Ion Etch (RIE), large and heavy structures with very good accuracy can be created. The different etchants that are used to create these structures are typically isotropic or anisotropic wet etch and anisotropic dry etch. Isotropic etch is used to undercut and release structures from the silicon wafer. Anisotropic wet etch in combination with etch-stop techniques is used to create thin diaphragms and membranes.
Due to crystal orientation in a silicon crystal, strong-base etchants etch slower in some planes. In a (100) silicon crystal the 111 plane is etched much more slowly than the other planes. The 111 plane has atoms connected with 3 bonds directed into the crystal, while in the 110 and 100 planes, atoms have 2 bonds directed into the crystal. This makes the 100 and 110 planes more vulnerable to the etchant and higher etching speed is observed. When a mask is laid out and an etchant is applied, the etching direction to the plane is 54.7°. Different methods can be used for etch stop. A principal figure of bulk anisotropic etch is shown in fig 2.2. [6] [7]

![Figure 2.2: Anisotropic wetetched bulk micromachined diaphragm](image)

### 2.2.2 Surface micromachining

Surface micromachining is based on integrated circuit production processes from the 1960s. Materials are deposited on a silicon wafer, patterned with photolithographic masks and the selected area is etched away like in IC production. The principal difference between IC and Surface micromachining processing is the underlying sacrificial layers. These sacrificial layers are temporarily scaffolds for the suspended structures and are fully etched away. This results in structures that are partially released from the substrate [8]. Structures can be made small and accurate with this technique, and integration with CMOS is straightforward because the structures can be made on a wafer that is compatible with CMOS. Integration can be done with pre-CMOS MEMS structures that are created in a trench, and protected with a flattening sacrificial layer. Integration is further explained in section 2.3
2.3 Monolithic integration

There are three different approaches to monolithically integrate CMOS with MEMS. The approaches are denoted as pre- intermediate and post-CMOS MEMS, where post-CMOS means that the MEMS structures are fabricated after the CMOS electronics.

2.3.1 Pre-CMOS

When the micromechanical structures are made before the CMOS-electronics it is a pre-CMOS process. The reason for a pre-CMOS approach is that high temperatures are needed to anneal the MEMS structures. To anneal and get a nearly stress free polysilicon structure, temperatures over 1000 °C are used. This will destroy any electronics.

The major problem with the pre-CMOS production is CMOS requirements for a planar and uncontaminated wafer. If MEMS structures are put directly onto a wafer high topographic variations occur and CMOS fabrication is impossible. Introducing contaminated wafers into CMOS production can destroy the equipment and stop the whole production line. A way to planarize a wafer for CMOS production is to build the MEMS structures in trenches. The trenches are deeper than the height of the MEMS structures and the trenches are filled with a planarization material. Now the wafers are flat and ready for CMOS processing. The planarization material also protects the CMOS production equipment from contamination from materials used under the MEMS production. When CMOS fabrication is finished, the planarization material is removed and the structures are released. An example of this approach is the SUMMiT-V process by Sandia [9].

2.3.2 Intermediate CMOS

Here the CMOS production process is interrupted when the MEMS steps are applied. The structures are often surface micromachined and the structural material is most often polysilicon. Interrupting the CMOS process can be difficult when an external foundry is used.

To not alter the CMOS-diffusion and CMOS component behavior, polysilicon annealing temperatures are typically limited to 900 °C and these high temperature MEMS steps have to be finished before CMOS metallization [9].
2.3.3 Post-CMOS

Here the MEMS structures are created after the CMOS electronics. There are two different approaches to integrate MEMS structures with finished CMOS electronics. The DLP mirror array from TI is an example of a post-CMOS process where the MEMS are created on the top of the CMOS chip (stacking). First the CMOS addressing matrix is built and planarized, electrodes, hinges and mirrors are then micromachined on top of the CMOS chip [10].

Another approach is to use the CMOS die itself as structural material. The MEMS structures can be defined by additional masks or by the CMOS metal layers.

At the National Chung Hsing University Taiwan, Dai et al have presented a post-CMOS MEMS process that use the aluminum layers and vias as sacrificial layers (figure 2.3). First a passivation layer is added to define where the MEMS structures are supposed to be released. An isotropic Al etch is then applied to etch holes down to the substrate. A wet etch is then used to under-etch the substrate and release the structures. The Al etch can also be used as a under cut etch and two-layer structures can be created [11].

An even simpler process has been developed at Carnige Mellon University by Fedder et al. Only the top metal layers here define the MEMS structures. To release the MEMS structures a three step etch is used [12]. This will be further described in section 2.4.

Figure 2.3: a) After CMOS process b) Al etch c) anisotropic Si etch
2.4 STM BiCMOS7RF ASIMPS Production Process

The production process used in this thesis to manufacture the structures is developed at Carnegie Mellon University by Fedder et al. [13] and will be described more thoroughly in the following sections.

2.4.1 CMOS

The CMOS chip is manufactured in France by STMicroelectronics via Circuits Multi-Projects (CMP) Multi Project Wafer (MPW) and the technology used is the SiGe 0.25\( \mu \)m BiCMOS process (BiCMOS7RF). This is a low-noise process with many features suitable for RF applications. Low noise bipolar transistors, high quality conductors and high quality passive components, which are important for RF applications, are offered in this process. Other features are presented in table 2.1 [14].

2.4.2 Integration

When it comes to integration of MEMS, a difficulty for some of the pre and intermediate CMOS processes is introduction of MEMS process steps into the CMOS process. The expenses of changing a CMOS foundry process line is large and many foundries do not allow “dirty” MEMS materials in their process line. A post-CMOS MEMS process is chosen because it allows us to use CMOS production lines unchanged, and add the MEMS steps afterwards.

<table>
<thead>
<tr>
<th>Technology</th>
<th>STM SiGe 0.25( \mu )m (BiCMOS7RF)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Substrate</td>
<td>Silicon Germanium</td>
</tr>
<tr>
<td>CMOS well isolation</td>
<td>50Å gate oxide</td>
</tr>
<tr>
<td>Metal 1</td>
<td>Tungsten</td>
</tr>
<tr>
<td>Metal 2-4</td>
<td>Al</td>
</tr>
<tr>
<td>Metal 5</td>
<td>Al or Cu 2.5( \mu )m thick</td>
</tr>
<tr>
<td>Polyresistor</td>
<td>P+ (85 ( \Omega /sq )),N+ (180 ( \Omega /sq )) , P- (1000( \Omega /sq ))</td>
</tr>
<tr>
<td>Transistors</td>
<td>BJT, CMOS (Isolated NMOS and PNP BJT)</td>
</tr>
<tr>
<td>Capacitor</td>
<td>5( fF / \mu m^2 ) MIM</td>
</tr>
<tr>
<td>Varactors</td>
<td>MOS &amp; Junction</td>
</tr>
<tr>
<td>Inductors</td>
<td>High Q</td>
</tr>
</tbody>
</table>

Table 2.1: STM SiGe 0.25\( \mu \)m BiCMOS(BiCMOS7RF) process features
2.4.3 Maskless post-CMOS MEMS

After the CMOS process is done, the post-CMOS MEMS steps are performed. The post process is a three step etch (illustrated in figure 2.4). Using the metal interconnect layers of a regular CMOS process as an etch-resistant masks, MEMS structures can be defined and released. No additive steps are needed after CMOS, which makes the fabrication of MEMS structures fast, reliable, repeatable and economical. This MEMS process is in theory compatible with any conventional CMOS process and will be used to manufacture the structures described in this thesis. This is a cheap solution for monolithic integration and gives many advantages, although the structural material will not be as good as for specialized MEMS processes. The maskless post process (ASIMPS - application-Specific Integrated MEMS Process Service) is developed at CMU by Fedder et al and 5 of the dies will be post-processed at CMU. [12]

- **Step 1** Anisotropic oxide dry etch, CHF$_3$ RIE. Removes the silicon oxide down to the silicon substrate. Defined by the top metal layer (Fig 2.4 b)).
- **Step 2** Anisotropic silicon dry etch, SF$_6$ DRIE. Etches trenches down into the silicon substrate where the substrate is exposed (Fig 2.4 c)).
- **Step 3** Isotropic silicon dry etch, SF$_6$ RIE. The final etch of the silicon substrate to releases the structures from the substrate (Fig 2.4 d)).

[12] [15]

2.4.4 Structural composition

MEMS structures can be made with different compositions of structural layers. If we use only metal-1 to 3 and poly, there are 14 combinations which have different mechanical properties. The Cu layer is not usable as a structural layer due to delamination and metal-1 layer, which is made of tungsten and will get etched by the post-CMOS steps, cannot be used as top layer. Due to very different physical properties for each combination of structural layers, care must be taken when structures are designed.

One of the challenges when designing CMOS MEMS structures is out of plane curl due to residual stress in the different layers. Initial curl and temperature dependency is different for every combination of metal and poly layers. Initial curl, residual stress and temperature dependency will be further explained in Chapter 4.
Figure 2.4: a) After CMOS process b) anisotropic oxide etch c) anisotropic Si etch d) isotropic Si etch to release structure from substrate
Chapter 3

Varactor

The last few years there have been a large growth in wireless communication markets and many new wireless communication standards have been developed. In the near future ‘everything’ will have a wireless communication, sending and receiving information to multiple wireless devices. For example wireless sensor networks (WSN) will be important for gathering information in complex systems like military, automotive, other transportation systems, healthcare and more [16]. This will result in a large number wireless devices trying to communicate with each other and a huge amount of data to be sent over the network. To handle the data flow wireless devices need to support a wide frequency band with many communication channels. If today’s radio transceivers are used, one radio transceiver for a narrow frequency band is needed. Use of multiple radio transceivers in a single device is not optimal when it comes to area used, total device size, power consumption and price. To see a radio that can be used for a large range of communication standards, a radio with large frequency tuning range is required.

The majority of today’s transceivers are based on a voltage controlled oscillator (VCO) as the frequency tuning component. And the key component in many of the VCO architectures is the electronically tunable capacitor or varactor. The varactor directly controls the oscillator frequency. Hence, the performance of the varactor is critical when it comes to the frequency tuning range, accuracy of tuning, Quality-factor and noise of the whole system. Especially the limitation in the tuning range of today’s devices is a bottleneck for making multi standard radios. Today’s varactors, often based on solid-state p-n junctions, suffer from poor tuning range, low Q-factor, phase noise and large size. A way to overcome these problems can be a MEMS capacitor integrated with CMOS [3].

In this chapter we will look at the basic theory behind varactors and
examples on how varactors can be implemented in CMOS-MEMS. At the end of the chapter the idea behind the proposed varactor and how it can be implemented is described.

### 3.1 Theory of variable capacitors

A basic capacitor is composed of two conducting parallel plates with a gap between them. The gap is filled with air or another dielectric material. The capacitance $C$ is defined as the amount of electric charge stored ($Q$) for an electric potential ($V$) and is given by equation 3.1. The SI unit of capacitance is farad, $1 \text{farad} = 1 \text{coulomb/volt}$

$$C = \frac{Q}{V} \quad (3.1)$$

The capacitance can also be expressed as a function of the geometric and dielectric properties. If fringe fields are neglected, the capacitance $C$ is given by 3.2 where $A$ is the area, $d$ is the distance and $\varepsilon$ is the permittivity of the dielectric.

$$C = \frac{A\varepsilon}{d} \quad (3.2)$$

A principal figure of a two plate capacitor is shown in figure 3.1.

![Figure 3.1: Sketch of a capacitor](image)

From equation 3.2, making distance between the electrodes smaller, the area larger or use a dielectric with higher permittivity will result in a larger capacitance of the capacitor [3].

The measure for how much the capacitance can be changed is the tuning range. The tuning range is given by $C_{min}$ and $C_{max}$ in equation 3.3.
tuning range = 100 * (\frac{C_{\text{max}}}{C_{\text{min}}} - 1)\% \quad (3.3)

Examples on MEMS implementations of gap, area and dielectric tuning varactors are presented in the next sections.

3.2 CMOS-MEMS varactor designs

Varactors designed in MEMS can be classified in three categories, gap, dielectric and area tuning varactors. Orientation of movement in the varactor is also an important distinction. In-plane orientation is when the motion of the actuator is parallel to the substrate of the chip. Vertical orientation is when actuation is perpendicular to the chip plane. An out-of-plane orientation is when the motion is perpendicular to the substrate, and the rotor structure is levitated above or beneath the chip plane.

3.2.1 Gap tuning

Vertical gap varactors have actuators that can move one of the capacitor plates vertically to the chip substrate. The change of distance between the two plates results in a change of capacitance. Electrostatic actuators are often preferred due to low power consumption when the actuator is held in a static state. The problems encountered with electrostatic actuators are often pull-in and hysteresis. Pull-in effect is when the electrostatic force of the actuator overcomes the spring force that supports the plate. When this happens, the two capacitor plates will snap together. This limits a two-plate varactor to a tuning range of about 50%. This problem can be overcome with electrothermal actuators. It has been shown that electrothermal vertical gap varactors can be implemented with a tuning range of 170%. Vertical gap varactors can only be implemented in processes supporting sacrificial layers between the plates that can be etched away [3].

In-plane gap varactors have also been implemented. Actuators are used to reduce or increase the gap between the capacitor nodes in the plane. Two set of combs are often used. One comb is actuated and the gap between the fingers in the combs are changed. This type of gap varactor can be implemented in a standard CMOS process with post-etch.

Seen from equation 3.2 the capacitance of gap tuning capacitors is proportional to \( \frac{1}{d} \) and is unlinear by definition. This have to be handled when integrated in a RF system.
3.2.2 Area tuning

Area tuning varactors have a linear capacitance response and there is no theoretical limit in the tuning range. Comb structures are often used to get the large area variation and to maximize the area efficiency. One comb is actuated and when the combs are folded in or out of each other the area and the capacitance is varied. Both electrostatic actuators and electrothermal actuators are often used for area tuning varactors. Electrostatic actuators can be implemented the same way as the varactor itself, with comb-structures. Electrothermal actuators use less area, but can have large static power consumption. This can in lateral actuators be solved with latches that hold the actuator in a static position.

3.2.3 Gap Tuning varactor by Oz and Fedder

In the first generation gap tuning varactor by Oz and Fedder [17], the electrothermal lateral actuators are used to move the rotor frame towards a stator frame. Each frame acts as a plate in the schematic parallel plate capacitor. Moving the frames sideways toward each other reduces the gap between them. In this implementation two frames with long fingers were initially folded into each other. As the rotor frame is actuated towards the stator frame the gap between the beams is decreased.

The frames and actuators are designed not to be affected of out-of-plane curl due to variations in temperature. This is done with alignment of anchors and use of structures comprised of the same structural layers which gives the same residual stress and initial curl of both the static and moving comb. This is referred to as “curl compensating frames” [17].

However, the long beams suffered from lateral curl and the beam stuck together. This significantly limited the TR of the varactor. As the frames are moved towards each other the gap decreases and the capacitance increases from $C_{\text{min}} = 153\,f\,F$ to $C_{\text{max}} = 175f\,F$ which gives a tuning range of 14%. A Q-factor of 24 at 1.5 GHz is obtained. Figure 3.2 a) shows the whole structure.

3.2.4 Area and Gap Tuning varactor by Oz Fedder 2nd generation

In the 2nd generation area and gap tuning varactor by Oz and Fedder [17], lateral moving beams with narrow and short fingers were implemented. In this second generation implementation the actuators were used to move the combs from each other and reduce the overlapping area between them (shown in figure 3.3). The problems with stiction encountered in the first
The maximum tuning range was 352 % when the voltage was varied from 6 to 12 volt. The initial capacitance was much lower than expected due to a polymer layer on the sidewalls of the fingers. This prevented them from folding as much as expected into each other, and limited the initial capacitance and the tuning range. The Q-factor at 1.5 GHz is 52. This structure was implemented in a TSMC 0.35µm CMOS process.

A lateral latching mechanism was implemented here, as shown to the right in figure 3.3 a). The purpose of this latch was the possibility to lock the varactor to several fixed capacitance values. When the latch is in lock there is no need for heating the actuator and no power is consumed. Due to lower stress gradients than predicted the latching actuator did not have large enough displacement, and the latch did not get in lock.
3.2.5 Out-of-plane CMOS-MEMS resonator

As discussed in Chapter 4, CMOS-MEMS structures curl out of the plane when they are released. In the previous presented designs the structures are designed to be independent of the initial and temperature dependent curl. However, the initial curl can be utilized to make MEMS components.

In [18], Chiou, Lin and Shieh a vertical comb drive resonator based on out-of-plane curl was developed. A 3D sketch is shown in figure 3.4. The resonator consists of two combs. One comb is connected to the support beam and the other is fixed to the substrate. The support beam is anchored in one end. The other end is elevated over the substrate due to the initial curl in the beam.

The beam was connected to a sinusoidal wave and the frequency was swept. The displacement of the beam tip was then observed.

The resonator was implemented in a standard 0.35 \( \mu m \) process with a post-CMOS-MEMS process. After the CMOS chip is produced a passivation
layer is added, and a photo resist mask is used to define the etching pattern. An enchant is then used to remove the dielectric silicon dioxide sacrificial layers and releasing the structure from the substrate.

This work gave us the idea that the resonator presented may be used in another way.

### 3.3 Out of plane varactor proposal

The idea is based on the resonator presented in [18]. The capacitance between the combs in the resonator is given by the overlapping area and the gap between them. As seen in section 3.1, changing the area or gap in a capacitor will increase or decrease the capacitance. If the rotor comb in the resonator can be actuated towards the stator and the gap and area overlap can be changed, it can be operated as a variable capacitor.

An important measure for variable capacitors is the tuning range. And to gain a large tuning range, one of the electrodes needs to move a large distance relative to the other. The initial curl of the out-of-plane resonator is very large and gives a large initial gap between the two electrodes. If the rotor comb can be flattened and aligned with the chip plane, a large tuning range can be obtained. In [18] the rotor comb tip is levitated 50 to 60 $\mu m$ over the chip plane, and the minimum gap in typical CMOS-MEMS processes is $\approx 1.5 \mu m$. In this thesis we will try to utilize this large gap difference to make a varactor with large tuning range.

To change the gap an actuation mechanism is needed, and two different approaches are considered. First, electrostatic actuation, which is used for changing the resonant frequency in [18] is considered. If a potential difference is set on the combs electrostatic forces will pull the combs together and change the gap. The actuation voltage can be a DC overlay which can easily be filtered out. Using half of the fingers as the actuator and the other half as the capacitor can also be a solution.

The other approach is based on thermal actuation. Seen in [19], the out of plane curl of a CMOS-MEMS structure is dependent on the temperature. This effect can be interesting to investigate as an alternative actuation mechanism. The cantilever beam holding the rotor comb in the resonator, is very similar to the beams presented in [19] and the theory presented on temperature dependent curl can probably be used for the proposed varactor.
Chapter 4

Out-of-plane actuation

A MEMS varactor design is dependent on having an actuation mechanism to alter the gap and/or area and ultimately alter the capacitance. As mentioned in Chapter 3, large tuning range is important in a RF system. To get a large tuning range the actuator has to move one of the capacitor plates a long distance. A way to make a large variation in the gap or area can be to utilize the initial out-of-plane curl.

As Chiou et al proposed in [18] electrostatic force can be used to displace an out-of-plane curled comb towards the chip plane. This configuration was simulated in CoventorWare and only small displacements were seen before the structure pulled in and shorted. The curled beam stayed curled when the voltage was applied and the beam only bended near the anchor. To get high area overlap in the capacitor the actuator must fully uncurl and be totally flat and aligned to the substrate. It is also beneficial with a smooth variation of capacitance. Thermal actuation seems promising to solve these problems with simple cantilever beams that are heated [20] [21].

Theory and examples from the literature of thermal out-of-plane cantilever actuators with large displacement are explained in this Chapter. Simulations and analytic models of the actuator used in this thesis are presented in the next Chapter.

4.1 Residual stress in laminated structures

Due to residual stress in multi-layer CMOS structures a beam will curl out of the plane when the post-process is finished and structures are released [21]. Curling due to residual stress is a difficulty when designing MEMS structures and can make the structure inapplicable. Methods have
been developed to compensate for curl and make structures independent of temperature variations (curl compensating frames) [19] [22]. Instead of compensating for the temperature dependent curl, this effect can be utilized to make an actuator with displacement out of the plane.

Residual stress is usually divided into two groups, where thermal stress is due to thermal coefficient of expansion (TCE) and intrinsic stress is caused by effects built in during processing.

4.1.1 Thermal Stress

The major source of stress in a CMOS-MEMS process is the thermal stress. CMOS processes often have high TCE metal layers over low TCE silicon dioxide layers. This large difference in TCEs and the processing conditions make the metal layers highly tensile stressed.

When metals like aluminum, copper and tungsten are deposited in a CMOS process, high temperature is used to metalize the layers. And when the structure is cooled, the metal layers contract due to positive TCE. The TCE in the oxide between the layers is a fraction of the TCE in the metal (Table 4.1). The layers are tied together and when the metal contracts a tensile stress builds up in the metal layer.

<table>
<thead>
<tr>
<th>Material</th>
<th>Youngs Modulus(GPa)</th>
<th>TCE(µstrain/K)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Aluminum(Al)</td>
<td>70</td>
<td>23</td>
</tr>
<tr>
<td>Tungsten(W)</td>
<td>400</td>
<td>4.4</td>
</tr>
<tr>
<td>Copper(Cu)</td>
<td>110</td>
<td>16.4</td>
</tr>
<tr>
<td>Dielectric(SiO2)</td>
<td>80</td>
<td>0.4</td>
</tr>
<tr>
<td>Polysilicon</td>
<td>160</td>
<td>2.3</td>
</tr>
</tbody>
</table>

Table 4.1: Material properties for structural CMOS-MEMS layers [21] [23]

The thermal strain $\epsilon$ in a material sample not tied to any other material is given by 4.1

$$\epsilon = \alpha_T (T_d - T_s)$$

(4.1)

where $\alpha_T$ is the TCE, $T_d$ is the zero-stress temperature and $T_s$ is the structure temperature.

Thermal strain for layer $n$ ($\epsilon_n$) is used to compute the thermal stress for a two layer cantilever beam. Seen in figure 4.1 a), an aluminum thin film is
deposited onto a dielectric at temperature $T_d$. The stress in the aluminum layer in this example beam is given by the differential strain and the biaxial Young’s modulus.

The differential strain is given as

$$\varepsilon_{\text{al–dielectric}} = (\alpha_{T_{\text{Al}}} - \alpha_{T_{\text{dielectric}}} )(T_d - T_s) \quad (4.2)$$

Given equal strain in both plane axis, the biaxial stress in the Al layer (figure 4.1 a)) is given by

$$\sigma_{\text{Al}} = \left( \frac{E}{1 - \nu} \right)_{\text{Al}} \varepsilon_{\text{al–dielectric}} \quad (4.3)$$

where $\left( \frac{E}{1 - \nu} \right)_{\text{Al}}$ is the biaxial Young’s modulus and $\nu$ is the Poisson ratio [7].

The calculation is only valid before the structure is released. When the structure is released the stress is relieved and the beam is deformed and pulled out of the plane as seen in figure 4.1 b).

The initial out of plane curl and the temperature dependency will be more thoroughly investigated in the next sections.

### 4.1.2 Intrinsic Stress

Stress can also occur from other sources. Oxidation of silicon, rapid deposition and doping can create residual stress. The stress that do not come from thermal expansion mismatch is called intrinsic stress [7].

### 4.2 Initial Curl predictions

The initial curl is given by the stress and the flexural rigidity of the structures and is important to the overall performance of the actuator. The initial curl limits the out-of-plane actuation distance, and thus the tuning range, which is important when making a varactor.
To model the initial curl, the residual stress in all layers have to be known. This is difficult as the CMOS foundry has a closed production line. The best way to get knowledge of the initial curl is to make a set of test structures. This will give data for the different beam combinations in a given process. In [21] Lakdawala et al. made a set of 14 beams and measured the initial curl. These data have been used as a guide for the design in this thesis.

For the two layer cantilever beams (figure 4.1), tensile stress in the upper layer now wants to contract and pull the structure out of the plane. The substrate and dielectric (SiO2(S)) is holding the structure in the plane. When the dielectric and substrate are removed, the stress acts on the structure and curls it out of the plane. As the beam curls, the stress in the top metal layer is decreased until the stress is in equilibrium with the flexural rigidity of the beam. When the equilibrium state is reached, the total bending moment in the beam is zero.

The beam will now be shaped as a part of a circle with a radius of curvature $\rho$. Figure 4.1 b) illustrates how the two-layer cantilever beam curls.

4.2.1 Stress Tuning

If production steps can be controlled, the residual stress can be tuned to a certain degree. Deposition temperature, implant dose and implant energy are parameters that have most impact on the stress [24]. In [25] micro-Raman spectroscopy is presented as a residual stress monitoring method. This can be used to more accurately monitor the stress in a process. This can be important for the future of out-of-plane curling structures.

If the stress can be controlled, predictions of the out-of-plane curl can be highly accurate. In [26] out-of-plane curled cantilevers with highly predictable radius of curvature are made. To get predictable curl, thickness and stress is important to have good control over. In figure 4.2, SEM images of toroid structures comprised of curled cantilevers only are shown.

*Figure 4.2: Cantilever toroids (from [26])*
4.3 Temperature dependency

To be able to create an out-of-plane actuator based on heating, the deflection as a function of temperature has to be modeled or simulated. The bimetal beam thermostat theory by S. Timoshenko, [20], is presented in section 4.3.1. This theory is used to see how a two layer cantilever bends with temperature. In the next section, the bimetal thermostat theory is extended to cover multilayer beams (multimorphs). The temperature dependency for multimorph structures is presented by Lakdawala et al. in [21].

4.3.1 Curling of two-layer cantilever

As seen in Section 4.1 a two layer cantilever with different TCEs will curl when the temperature is changed from the zero-stress temperature. The change in radius of curvature $\rho$ for a two layer cantilever is given by

$$\frac{1}{\rho} = \frac{6(\alpha_2 - \alpha_1)(T - T_0)(1 + m)^2}{h \left( 3(1 + m)^2 + (1 + mn)(m^2 + \frac{1}{mn}) \right)}$$

(4.4)

where $h$ is the total thickness, $T$ is the structure temperature, $T_0$ is zero-stress temperature, $\alpha_1$ and $\alpha_2$ are the TCEs,

$$m = \frac{t_1}{t_2}$$

(4.5)

$t_1$ and $t_2$ is the thickness and

$$n = \frac{E_1}{E_2}$$

(4.6)

$E_1$ and $E_2$ is the Young’s modulus for layer 1 and 2. The cantilever is shown in figure 4.3.
To model a cantilever this way, certain simplifications and assumptions have been made. The simplifications and assumptions are listed below.

- TCE $\alpha_n$ constant with temperature
- friction in the anchoring structure is negligible
- width of the strip is small ($\frac{W}{L} << 1$)
- a cross-section of the cantilever remains flat and perpendicular to the axis of curvature

And given that the radius of curvature is larger than the length of the beam, the tip deflection $\delta$ can be described by a simple second order equation [27] [20]. This simplification is in agreement with the assumptions made.

$$\delta = \frac{L^2}{2\rho} \quad (4.7)$$

For the case of the proposed out-of-plane actuator, these assumptions are close to real conditions.
4.3.2 Curling of multilayer cantilever

In CMOS-MEMS, multilayer structures are used and the two layer curling models have to be extended for multilayer structures. [28] and [21] present an extended model based on S. Timoshenkos two layer theory [20]. This multilayer model is used to predict the temperature dependency of the multilayer actuator.

The change in tip deflection \( \frac{\partial \delta}{\partial T} \) with respect to change in temperature \( \partial T \) is given in equation 4.8. Figure 4.4 illustrates the different parameters and numbers used in the calculation presented below.

\[
\frac{\partial \delta}{\partial T} = L^2 \left( \frac{Y^T G^{-1}}{2\chi - Y^T G^{-1} S} \right) A 
\]  

(4.8)

where \( L \) is the length of the cantilever, \( Y \) is the moment arm vector

\[
Y = \begin{bmatrix}
t_1 + \frac{t_2}{2} \\
\vdots \\
\sum_{i=1}^{n-1} t_i + \frac{t_n}{2}
\end{bmatrix}
\]  

(4.9)

the matrix \( G \) gives the thickness \( (t_i) \), width \( (w_i) \) and Young’s modulus \( E_i \) for layer \( i \), the column vector \( A \) is the differential TCEs and \( S \) is the total thickness corresponding to \( A \) and are given as

\[
G = \begin{bmatrix}
-\frac{1}{w_1 E_1} & -\frac{1}{w_2 E_2} & \cdots & 0 & 0 \\
0 & -\frac{1}{w_2 E_2} & \cdots & 0 & 0 \\
\vdots & \vdots & \ddots & \vdots & \vdots \\
0 & 0 & \cdots & -\frac{1}{w_{n-1} E_{n-1}} & \frac{1}{w_{n-1} E_{n-1}} \\
1 & 1 & \cdots & 1 & 1
\end{bmatrix}
\]  

(4.10)

\[
A = \begin{bmatrix}
\alpha_2 - \alpha_1 \\
\alpha_3 - \alpha_2 \\
\vdots \\
\alpha_n - \alpha_{n-1} \\
0
\end{bmatrix} \quad S = \begin{bmatrix}
t_2 + t_1 \\
t_3 + t_2 \\
\vdots \\
t_n + t_{n-1} \\
0
\end{bmatrix}
\]  

(4.11)

The total flexural rigidity of the cantilever \( \chi \) is how much force is required to bend the beam and is given by the moment of inertia \( I_i = \frac{1}{12} w_i t_i^3 \) and Young’s modulus \( E_i \) for layer \( i \) and is given as
\[ \chi = \sum_{i=1}^{n-1} E_i I_i \]  

(4.12)

Figure 4.4: Curled multilayer cantilever

In the extended model, these additional assumptions are also made

- radius of curvature \( \rho \) is equal for all layers
- homogeneous materials
- total beam thickness \(<\rho\) which is near real conditions for the cantilever actuator.

This general model for a cantilever has been implemented in MatLab and can be found in appendix A.

4.3.3 Characteristic temperature

The characteristic temperature \( T_0 \) of a structure is when it is totally flat and aligned with the chip plane. The characteristic temperature is an intuitive way to describe the initial curl, and is useful when simulating initial curl of structures.

In the CoventorWare FEM simulator all structures are totally flat and aligned with the substrate at 273.15K. To simulate the initial curl of the structures, the simulation temperature has to be changed accordingly to
the observed initial curl in the test structures. This offset-temperature, to model the initial curl, is the characteristic temperature [27].

### 4.4 Experimental results

In [27], the initial tip-deflection has been measured on a set of 100\( \mu \text{m} \) long cantilevers. The beams are made with different layers, which gives large variations in tip-deflection. These data are used as a guide to predict the initial curl for the actuator. The data in [27] are obtained in a standard 0.5\( \mu \text{m} \) process, which is different from the process used in this thesis. The layer thicknesses are different and the metal-1 layer is tungsten in opposition to aluminum in the 0.5\( \mu \text{m} \) process. Radius of curvature, tip-deflection and characteristic temperatures are listed in table 4.2.

<table>
<thead>
<tr>
<th>Beam type</th>
<th>(\rho) (mm) at 292K</th>
<th>(\frac{\partial \delta}{\partial T}) (nm/K)</th>
<th>(T_0) (K)</th>
</tr>
</thead>
<tbody>
<tr>
<td>M12</td>
<td>1.6</td>
<td>-19.8</td>
<td>446</td>
</tr>
<tr>
<td>M12P</td>
<td>81</td>
<td>-17.6</td>
<td>296</td>
</tr>
</tbody>
</table>

Table 4.2: 100\( \mu \text{m} \) beam characteristics, initial curl and temperature dependency [27]

As seen in table 4.2 the initial radius of curvature for a Metal-1 + Metal-2 is small, but when polysilicon is put under (M12P) it does not curl nearly as much. M12 is mainly used for the actuator to get large initial curl and to get at fairly good deflection per Kelvin.

### 4.5 Derivation of \(\frac{\partial \delta}{\partial T}\)

Temperature dependency can be derived for a multilayer beam with the model in section 4.3.2. Only known material and geometric properties are needed to estimate the tip-deflection temperature dependency \(\frac{\partial \delta}{\partial T}\). The major limitation when using this model is knowledge about how thick the layers are. The layer thickness varies with the process and the top metal layer is thinned due to ion milling. If accurate data can be provided the error in the model is small [19].

#### 4.5.1 Ion-milling of top-metal-layer

In the post-CMOS micromachining process (section 2.4) long lasting RIE etch steps are used. The top metal layer in the MEMS structures is then
significantly thinned [29]. This can change the temperature dependency \( \frac{\partial \delta}{\partial T} \) significantly. In [27], the post processed test structures are milled \( \sim 0.38 \mu m \) in average. This is based on a single measurement and can vary from run to run and process to process. Tuning of the DRIE-process can have a large impact on the ion-milling effect. Adjusting pressure, power and gas concentration can give varied selectivity between SiO\(_2\)/Si and Al [29].

To see how the milling of an 100\( \mu m \) long M12 beam (in [27]) is affected, we have calculated the \( \frac{\partial \delta}{\partial T} \) for an milled and unmilled beam. If milling was not incorporated in to the model, the temperature dependent change of tip deflection is 30 % too large (table 4.3). In section 5.3.3 the tip deflection as a function of ion-milling for the proposed actuator is shown.

<table>
<thead>
<tr>
<th>Beam type</th>
<th>( \frac{\partial \delta}{\partial T} ) (nm/K)</th>
</tr>
</thead>
<tbody>
<tr>
<td>M12(Milled)</td>
<td>-19.8</td>
</tr>
<tr>
<td>M12(Full thickness)</td>
<td>-26.6</td>
</tr>
</tbody>
</table>

Table 4.3: 100\( \mu m \) beam, milling

### 4.6 Out-of-plane actuator discussion

A multilayer cantilever can be used as an out-of-plane actuator, as the tip-deflection \( \delta \) and radius of curvature \( \rho \) is dependent of temperature.

The initial curl and milling of the top metal layer is difficult to modulate, and can impose large errors in the analytic models if not accounted for. To model these effects, measurements of test-structures in the particular process are needed. Process variation from run to run can also give errors and must be investigated.

Tuning of DRIE etching parameters can be used to control the ion-milling of the top metal layer and control the thermal stress and curling. Another way to controll the curling can be tuning of the intrinsic stress, but access to the CMOS foundry is needed. The foundry used in this thesis does not allow tuning of the CMOS process.
Chapter 5

Models and simulations

Results from the applied analytic models and simulations of the proposed varactor structure are presented in this chapter. Analytic models and simulations give valuable data to predict the behavior and performance of the varactor. First the multilayer actuator is investigated using the theory presented in Chapter 4. The chapter proceeds with an analytic model for the capacitance with respect to the actuation displacement. The analytic results are compared with CoventorWare simulations.

5.1 Finite Element Method

All the simulations were carried out with the CoventorWare FEM simulator. The STM SiGe 0.25μm (BiCMOS7RF) process was defined in the process tool (table 5.1, layerthickness is not posted due to non-disclosure agreement). Based on the defined process and layout of the structures 3D-models were extracted. The simulations are based on solving a finite number of equations describing the structure, and to get a finite number of elements, the 3D-models were meshed with boxes. The structures were meshed with 4μm × 4μm × layerthickness Manhattan-bricks. To verify that the mesh is fine enough, a simulation with 16 times as many blocks was run. For the M12 cantilever the slope of tip-deflection with respect to temperature is found to be 275 nm/K with 4μm × 4μm mesh, and 273 nm/K with 1μm × 1μm mesh. With a difference of only 0.7 %, 4μm × 4μm mesh seems to be sufficient. An example of how the 3D-models are meshed is shown in figure 5.1.
<table>
<thead>
<tr>
<th>Step Name</th>
<th>Layer</th>
<th>Material</th>
<th>Mask Name</th>
<th>Comment</th>
</tr>
</thead>
<tbody>
<tr>
<td>Substrate</td>
<td>Substrate</td>
<td>SILICON</td>
<td>SubstrateMask</td>
<td></td>
</tr>
<tr>
<td>Planar Fill</td>
<td>tykkox</td>
<td>OXIDE</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Planar Fill</td>
<td>poly1</td>
<td>POLYSILICON</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Straight Cut</td>
<td>poly</td>
<td>POLYSILICON</td>
<td></td>
<td>poly mask</td>
</tr>
<tr>
<td>Planar Fill</td>
<td>Dielectric</td>
<td>OXIDE</td>
<td></td>
<td>Met2</td>
</tr>
<tr>
<td>Straight Cut</td>
<td>Dielectric</td>
<td>OXIDE</td>
<td></td>
<td>Met1</td>
</tr>
<tr>
<td>Planar Fill</td>
<td>Met1</td>
<td>TUNGSTEN</td>
<td></td>
<td>Met1</td>
</tr>
<tr>
<td>Straight Cut</td>
<td>Met1</td>
<td>OXIDE</td>
<td></td>
<td>Met2</td>
</tr>
<tr>
<td>Planar Fill</td>
<td>Dielec2</td>
<td>ALUMINUM</td>
<td></td>
<td>Met2</td>
</tr>
<tr>
<td>Straight Cut</td>
<td>Dielec2</td>
<td>ALUMINUM</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Planar Fill</td>
<td>Met2</td>
<td>ALUMINUM</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Straight Cut</td>
<td>Met2</td>
<td>ALUMINUM</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Straight Cut</td>
<td>Substrate</td>
<td>ALUMINUM</td>
<td></td>
<td>-30,6µm</td>
</tr>
</tbody>
</table>

**Table 5.1:** BiCMOS7RF defined in CoventorWare

**Figure 5.1:** 4µm × 4µm × layerthickness meshed 3D-model
The meshed models were then computed in the MemMech and MemElectro solvers. The MemMech solver computes the mechanical response to preset boundary conditions like temperature, fixed positions and voltage. In this thesis the MemMech was used to solve mechanical deflection with a given change of temperature. The MemElectro solver calculates the charge distribution and gives the capacitance. To combine the two solvers and get the capacitance when the structure is mechanically deflected, the CoSolve option is used. Here CoventorWare joins the two solvers together.

In the simulator the structure is flat at 273 K and to simulate the initial curl of the structure, an offset temperature is set in the MemMech solver [21]. The temperature set in the solver is given by

\begin{equation}
T_{\text{sim}} = -T_0 + T_d + T_s
\end{equation}

where \( T_0 \) is the characteristic temperature (explained in section 4.4), \( T_d \) is the initial temperature in the simulator or the zero stress temperature and \( T_s \) is the temperature of the structure [19].

### 5.2 Thermal distribution

All the analytic models shown in Chapter 4 are simplified to a uniform thermal distribution in the actuator. To investigate the thermal dissipation in the actuator the MemMech solver was used. A voltage was applied to the polysilicon heater, and the current is now joule-heating the actuator.

The sheet resistance for the polysilicon heater is \( \approx 6\Omega/sq \) and the heater is \( 414\mu m \times 2\mu m \). This gives a total resistance of \( \text{sheet resistance} \times \frac{\text{length}}{\text{width}} = 6\Omega/sq \times \frac{414\mu m}{2\mu m} = 1242\Omega \). This correlates well with the FEM simulations. However in the simulator the resistance is constant with the temperature. In real life conditions the resistance of polysilicon is highly dependent on the temperature.

An effect that is more difficult to predict is the thermal flow. The main dissipation is through conduction via the actuator anchor and convection at the top of the structure [30]. The steady-state thermal distribution is simulated in CoventorWare.

In figure 5.2 the thermal distribution with a voltage across the heating element is shown. As expected the heat is dissipating through the anchor and the lower part of the actuator is cooler that the part towards the tip.
In real life conditions the structure will have an even more uniform heat distribution. The end surface of the anchor in the simulated structure is strictly defined to 293 K and much heat is removed through this surface with zero thermal resistance. This is not the case for the real conditions where the anchor can be heated to a certain temperature and the thermal flow out of the anchor is limited. In [30] a structure is heated in a similar way, and the thermal distribution is very uniform.

An interesting observation was made in [31]. As the voltage increases and the temperature exceeds 50 °C the resistance in the polysilicon heater increases significantly. This results in a linear response between voltage and temperature when the temperature is over 50 °C.

5.3 Actuator

The proposed multilayer cantilever actuator is 340 µm long and 7 µm wide. It is mainly comprised of the metal 2 + metal 1 and dielectric layers, but a polysilicon loop is placed at the bottom of the actuator to heat it. The polysilicon heater, does not cover the whole area of the beam and can not be incorporated as a full layer in the model. But it can not be neglected as it covers about 35 % of the beam area. Only full layers can be used in the model.

To verify and compare results from the model with the results from the simulations a metal 2 + metal 1 (M12) and a M12P actuator is used. The
M12P beam is used to investigate how much the polysilicon heater affects the actuator. Figure 5.3 shows a CoventorWare 3D-model of the actuator. Here the actuator tip is levitated a distance $\delta$ above the chip plane. The chip plane is not incorporated into the simulation to reduce computing time.

![Figure 5.3: 3D-view of the actuator](image)

Due to lack of data on the production process, it is difficult to accurately model and simulate the initial curl. As mentioned in Chapter 4, the stress and in-plane alignment temperature is difficult to predict. This uncertainty makes it important to have sufficient displacement with respect to temperature to ensure that the actuator can move the combs far enough and align the rotor comb with the chip plane.

### 5.3.1 Modeled vs simulated temperature dependency $\frac{\partial \delta}{\partial T}$

To model the displacement derivative with respect to the temperature ($\frac{\partial \delta}{\partial T}$) equation (4.8) is used (MatLab script in appendix A). The model was then applied to the material constants for the given process and the geometric values of the structure. The results are presented in table 5.2.

To simulate and compare the simulation results to the analytic model, the structures were implemented in the CoventorWare FEM simulator. The
material constants were set to the same as in the analytical model and the simulator is set to vary the temperature of the whole structure and to compute the mechanical response. The tip deflection vs temperature was then plotted. In figure 5.4 we can see that the tip deflection $\delta$ is linear with temperature $T$. Thus, the derivative can be computed as the slope $\frac{\Delta \delta}{\Delta T}$ of the graph.

Figure 5.4: Deflection $\delta$ vs temperature $T$ for M12 300$\mu$m actuator simulate in CoventorWare

In table 5.2, the simulated $\frac{\Delta \delta}{\Delta T}$ for the implemented actuator is presented.

<table>
<thead>
<tr>
<th>Beam</th>
<th>Modeled $\frac{\Delta \delta}{\Delta T}$ (nm/K)</th>
<th>Simulated $\frac{\Delta \delta}{\Delta T}$ (nm/K)</th>
</tr>
</thead>
<tbody>
<tr>
<td>M12</td>
<td>267</td>
<td>273</td>
</tr>
<tr>
<td>M12P</td>
<td>210</td>
<td>207</td>
</tr>
<tr>
<td>M2</td>
<td>286</td>
<td>255</td>
</tr>
<tr>
<td>M2P</td>
<td>225</td>
<td>209</td>
</tr>
</tbody>
</table>

Table 5.2: 300$\mu$m beam deflection, different beam types, STM BiCMOS 0.25$\mu$m

The model seems to fit with the simulated results. To ensure that
the actuator can be aligned with the substrate, the in-plane alignment
temperature has to be calculated. If the alignment temperature is lower
than the CMOS-MEMS maximum temperature $T_{max}$, the actuator should
have sufficient displacement with respect to temperature.

The maximum temperature for the CMOS-MEMS, $T_{max}$, is 570K. Heating
the structure over 570K, the aluminum yields, the initial conditions change
and the structure is destroyed. If the structure is initially held at room
temperature, $T_{init} = 290K$, the temperature range is $T_{range} = T_{max} - T_{init} = 280K$. The M12 beam can give a theoretical maximum deflection of $\delta_{max} = T_{range} \times \frac{\partial \delta}{\partial T} = 280K \times 267nm/K = 75\mu m$. The predicted initial curl, based
on [21], is 50 to 30$\mu m$. The predicted max deflection is larger than the initial
curl and the actuator will then align with the plane before $T_{max}$ is reached.

With an initial curl between 50 and $30 \mu m$ and a $\frac{\partial \delta}{\partial T}$ of 267$nm/K$ the in-
plane alignment temperature ranges from 187 to 112 °C. However, these
values are dependent on process variations and how good the curling can
be predicted (discussed in 4.2.1).

5.3.2 Stress simulations

The theory used to model the actuator ([20], [28], [19]) is based on stress
distributions that are linear with the height of each layer and uniform over
the width and length of the beam. To see how the stress is distributed in
the actuator the stress is simulated in CoventorWare.

The temperature of the actuator is set below the in-plane alignment
temperature and the actuator curls out of the plane. Stress is now
distributed in the actuator. In figure 5.5 the stress in x direction (along
the beam) caused by strain in x direction when the actuator is curled out
of the plane is shown. As expected and seen in CoventorWare, the “xx
stress” it the dominant stress. The stress is marked with colors, where red is
compressive and blue is tensile stress. The “xx stress” shown in the figure
is the stress in the x direction along the beam induced by strain in the x
direction.

As expected, the layers with high TCEs have tensile stress and the silicon
oxide is compressively stressed. The stress seems uniform over the length
and width and linear with the height of the actuator. This confirms the
results obtained from the model in the previous sections.

Figure 5.6 shows the principal stress at the anchor end of the actuator. Here
the stress is not ideally distributed which can explain the different results
in the model and simulator.
Figure 5.5: Stress distribution in the actuator

Figure 5.6: Stress distribution in the actuator anchor
When the structure is heated beyond the in-plane alignment temperature and the actuator tip is beneath the chip plane the stress distribution is inversed. The metal layers then get compressive and the oxide tensile stressed.

5.3.3 Ion milling

The top metal layer can be significantly milled due to long time used for the RIE steps in the post-CMOS process, described in 4.5.1. How the ion milling will affect the actuator have been investigated. With an ion milling of 50 % of the top metal layer, which is observed in some processes, the $\frac{\partial \delta}{\partial T}$ is significantly reduced.

![Figure 5.7: $\frac{\partial \delta}{\partial T}$ for M12 and M12P actuator and milling](image)

With an initial curl of 50 µm and ion milling of 50 %, the $t_{\text{align}}$ temperature is calculated to 256 °C and 306 °C for the M12 and M12P beam, respectively. This is an increase of 37 % and 44 % in $\frac{\partial \delta}{\partial T}$ from the unmilled structure, and can be crucial for device operation as 306 °C is over $T_{\text{max}}$.

5.4 Capacitance

Simulation and modeling of the capacitance is essential when making a varactor. In this section we will look at the anticipated capacitance of the
varactor. The capacitance when the comb is aligned with the substrate is simulated in the MemElectro simulator. This is a fast and accurate simulation. The value of the capacitance can be derived analytically, but this is time consuming and the MemElectro simulation is more accurate.

Simulation of the capacitance when the comb is curled out of the plane is much more time consuming and complex. To overcome the problem with time consuming simulation, we have derived an analytic model for the change in capacitance with the change in tip deflections. The model is a simplification of the actual comb structure and thus an error is expected.

5.4.1 Field distribution

To be able to model the capacitance change as a function of the radius of curvature, the comb structure is simplified to a two-plate structure. The top plate is curved as the rotor comb, and the bottom plate is flat as the stator comb. A schematic sketch of the electric field distribution in a curled comb capacitor is shown in figure 5.8 a).

The actual field distribution in the varactor is very different from the simplified, but in the simplified case, the initial gap $g_0$ is modified to fit the actual initial capacitance. When the actuator curls, the length of the field lines is changed accordingly to the curvature of the actuator. This change in
field line-length in the simplified model is very similar to that in the actual. Seen in figure 5.16 the error with respect to the simulated capacitance is actually within 20% for a deflection from 0 to 80\(\mu m\).

5.4.2 Modeling of the capacitance

The simplified two-plate capacitor model has a length \(L\) and a width \(b\). The initial gap \(g_0\) is the actual gap in the structure when the comb capacitor is flat and aligned with the substrate. The same gap is used in the model. The maximum capacitance is when the gap is \(g_0\) for the whole capacitor. A schematic sketch of the two-plate capacitor when it is flat is shown in figure 5.9. The capacitance of the flat two-plate capacitor is the same as the actual capacitor when it is flat.

\[ g(x) = g_0 + g_{curl}(x) \]
\[ = g_0 + \frac{x^2}{2\rho} \]

The total gap \(g(x)\) is the initial gap \(g_0\) plus the gap \(g_{curl}(x)\) (equation 4.7).

A small increment along the length of the beam \(\Delta x\) gives a capacitance \(\Delta C\). \(\Delta C\) is then given by

\[ \Delta C = \frac{b\varepsilon}{g(x)} \Delta x \]

Figure 5.9: Perspective view of the two-plate capacitor

The top plate is anchored at one end and is curled out of the plane with a radius of curvature \(\rho\). The gap in the capacitor is now changed. For a point \(x\) along the length \(L\) the gap \(g(x)\) is given as
where \( g(x) \) is the gap, \( b \) is the width and \( \varepsilon \) is the electrical permittivity of air. A \( \Delta x \) increment is illustrated in figure 5.10.

![Figure 5.10: Side view of two-plate capacitor](image)

Now \( g(x) \) is replaced with 5.3

\[
\Delta C = \frac{b\varepsilon}{g_0 + \frac{x^2}{2\rho}} \Delta x
\]  

(5.5)

If we make the increment infinitesimal the total capacitance of a curled capacitor with radius of curvature \( \rho \) and length \( L \) is now given as the integral over the capacitance distribution

\[
C = \int_0^L \frac{b\varepsilon}{g_0 + \frac{x^2}{2\rho}} \, dx
\]  

(5.6)

If we assume that \( \rho > L \) we can integrate from 0 to \( L \) instead of the actual integration length. We can see from the capacitance distribution (figure 5.11) that the contribution to the total capacitance at the end of the capacitor is small even when \( \rho \) is getting small.
The maximum capacitance $C_0$ is simulated in CoventorWare and we have that $\frac{C_0}{L} = \frac{b e}{g_0}$. The capacitance $C$ is dependent on the radius $\rho$ and we denote it as a function of $\rho$.

We can now rearrange equation 5.6

\[
C(\rho) = be \int_0^L \frac{1}{g_0 + x^2/2\rho} \, dx
\]

\[
= be \int_0^L \frac{1}{g_0/g_0 + x^2/2\rho g_0} \, dx
\]

\[
= \frac{C_0}{L} \int_0^L \frac{1}{1 + x^2/2\rho g_0} \, dx
\]

The integral is solved and we get

\[
C(\rho) = \frac{C_0}{L} \sqrt{2\rho g_0} \tan^{-1}\left(\frac{L}{\sqrt{2\rho g_0}}\right)
\]
which shows the change of capacitance as function of the radius of curvature \( \rho \).

The assumption that \( \rho < L \) gives a small error when the out of plane deflection is large. For the proposed actuator the minimum anticipated \( \rho = 900 \mu m \) and the length \( L = 340 \mu m \). For structures with even larger deflections a new model that describes the curvature of the structure as an actual part of a circle and not using the simplification that the curvature of the actuator is \( \frac{1}{\rho} \). Accurate integration limits also have to be derived. However for the proposed structure the error is small and negligible.

### 5.4.3 Minimum gap

The initial gap of the structure has a huge impact on the capacitance as the capacitance is proportional to \( \frac{1}{g} \). To investigate how much this affects the tuning range of the varactor the model presented in the previous section is modified.

We assume that the area in the capacitor is the same per length \( L \). Thus the width \( b \) and length \( L \) remains the same. The gap \( g_0 \) is changed to the new initial gap \( g_1 \). The maximum capacitance is now given as

\[
C_1 = \frac{b\varepsilon L}{g_1} = \frac{C_0}{1 - \frac{g_0 - g_1}{g_0}} \tag{5.11}
\]

The capacitance for a given radius of curvature is now given as in 5.10 but with new parameters

\[
C(\rho) = \frac{C_1}{L} \sqrt{2\rho g_1} \tan^{-1}\left(\frac{L}{\sqrt{2\rho g_1}}\right) \tag{5.12}
\]

In figure 5.12 the capacitance for the test structure is plotted with an initial gap of \( 1.5 \mu m \) and \( 1 \mu m \). As expected, the in-plane aligned capacitance is much larger. To see how the tuning range is affected, the gap is changed and the tuning range is calculated for an initial curl of \( 35 \mu m \), which is \( \rho = 956 \mu m \). We will here look at initial gap \( g_1 \) from \( 0.3 \mu m \) to \( 1.5 \mu m \) (figure 5.13).

The tuning range can be increased significantly if the gap \( g_0 \) can be reduced. Reducing the gap also gives larger area efficiency.
Figure 5.12: Capacitance test structure

Figure 5.13: Tuning range
5.4.4 Comb length

The length of the comb was varied to see how it affects the performance of the varactor. In figure 5.14 the length with respect to the tuning range is plotted.

![Plot of tuning range vs comb length]

The tuning range increases linearly with the comb length. Theoretically the tuning range can be made very large by making the varactor longer.

5.4.5 Simulated vs modeled capacitance, test structure

The capacitance of the varactor was simulated with the CoSolve solver in CoventorWare. Simulation of the mechanical response and capacitance was very time consuming and was only carried out for a test structure. The test structure was simpler than the implemented structure and was used to see if the concept works. The principal operation of the test structure is very similar to the implemented structure and the geometrical dimensions are almost the same. In figure 5.15 the capacitance in one half of the varactor is plotted over a large temperature range.

With an initial curl of 50 to 30 μm which corresponds to a simulator temperature offset of 173 to 100 K, gives a minimum capacitance of 18 to 25 fF. The maximum capacitance (varactor aligned with the substrate at 394-460 K) is 74 fF and a tuning range from 200 to 310 % can be obtained.
To verify the proposed model (equation 5.10), the results are compared with the test structure simulations. MatLab was used to derive the error between the model and simulations (figure 5.16).

The analytic model seems to fit the simulations pretty well. As expected the simulated capacitance was larger than the modeled when the tip deflection is increased. This is due to fringe fields and that the model is based on two plates laying over each other. In the simulated structure the rotor comb folds into the stator and the area overlap is defined by the thickness and overlap length of the structure. In the model the area is defined by the length and width of the two plates. To consider the varactor as two-plate and not a comb gives an error in the anticipated capacitance, especially when the tip-deflection is small. However, as the tip of the comb is levitated a certain distance over the chip plane the model is more accurate and behaves more like a curled two-plate capacitor. The model does not give an accurate description, but can give an idea of how it will perform. This is important when optimizing the varactor as the simulation time for the structure is extremely long.

The tip deflection for a bi metal actuator is measured in [30], and the tip deflection is highly linear with the applied voltage. This is also consistent with [31]. At room temperature and 0 volt over the heater, the structure is held at the initial tip-deflection. As the voltage increases and the temperature rises, the tip is anticipated to move linearly towards the substrate. Figure 5.17 describes the anticipated capacitance response to voltage.
Figure 5.16: Capacitance, Modeled vs simulated and percentage error

Figure 5.17: Capacitance, Modeled vs simulated vs normalized voltage
The initial curl, which gives the 0 voltage point in the figure, is difficult to predict. In the figure this range is marked as $\delta_{\text{initial}}$. How the structure will heat and deflect with the applied voltage is also difficult to predict analytically. Seen in previous sections the tip deflection is linear with the temperature of the structure. Also the temperature, when over 50 °C, is linear with the voltage. Thus the tip deflection is predicted to be linear with the voltage. To illustrate the capacitance response to voltage, the voltage over the polysilicon heater is normalized. From the figure we can see that the capacitance can have a large tuning range, but is very unlinear with the voltage. Given the assumptions of linearity, the response seen here is proportional to a gap tuning varactor.

5.4.6 Modeled capacitance, proposed structure

When a simulation of the proposed structure was tried, the simulator did not converge to a solution and failed. To estimate the capacitance change with tip displacement for the proposed structure the analytic model was used. To use the model on the proposed structure the capacitance per length $C_L$ is simulated in the MemElectro solver and put into the model. Now we see the implemented structure as a two-plate capacitor with length $L$, capacitance per length $C_L$ and initial gap $g_0$. The initial gap $g_0$ is the actual gap in the implemented structure.

The maximum capacitance was found with the MemElectro simulation. The simulated maximum capacitance of the proposed structure is 185 fF with a gap $g_0 = 1.5 \mu m$ (figure 5.18).

If the initial curl is between 50 $\mu m$ and 30 $\mu m$ the tuning range is between 240 % and 325 %.

5.4.7 Q-factor, proposed structure

The Q-factor is an important measure in RF systems. A high Q-factor gives narrow band-width filters, which is important when selecting radio channels. Higher Q means more radio channels in a given frequency spectrum. For oscillators a high Q factor gives a highly stable frequency, which is important when transmitting at a narrow band radio channel. The Q-factor can be expressed in different ways, but here we will use equation 5.13.

$$Q = \frac{|X|}{ESR}$$ (5.13)
where $X$ is the reactance and $ESR$ is the equivalent series resistance in the capacitor [3]. The ESR is calculated as in [17], and is given as

$$ R_{ESR} = (n \ast R_{\text{finger}}) + R_{\text{act}} $$ (5.14)

where

$$ R_{\text{finger}} = \frac{L_f}{W_f} \ast R_{\text{sheet}} $$ (5.15)

and

$$ R_{\text{act}} = \frac{L_a}{W_a} \ast R_{\text{sheet}} $$ (5.16)

where $L_a$ and $W_a$ is the actuator length and width, $L_f$ and $W_f$ is the length and width of one comb finger, $n$ is the number of fingers and $R_{\text{sheet}}$ is the sheet resistance for an M12 structure.

The ESR for the proposed structure was calculated to $64 \Omega$. The reactance of a capacitor $|X|$ is

$$ |X| = \frac{1}{2\pi f C} $$ (5.17)

where $f$ is the frequency and $C$ is the capacitance.
The maximum Q-factor of the varactor is then given as

\[
Q = \frac{1}{2\pi f C_{\text{min}} R_{\text{ESR}}}
\]  

(5.18)

The Q factor is plotted in figure 5.19 for a frequency \( f \) running from 0.5 to 6 GHz.

![Graph showing Q-factor vs Frequency](image)

**Figure 5.19:** Q-factor, Modeled for the proposed structure

The Q-factor at 1.5 GHz is found to be 29 for a \( C_{\text{min}} = 55 f F \). This approach to calculating Q is not accurate [17], but gives an idea of the capacitor performance and the results can be used for comparison and optimalization of designs.
Chapter 6

Implementation

The implementation of the structure is presented in this chapter. The varactor was implemented in the STM BiCMOS7RF process. The layout is based on the design rules for the post-CMOS MEMS process (see chapter 2) to ensure structure release. The design was implemented on a multi-design research die.

The layout was sent to production in the middle of November 2008 and was expected to be delivered early March 2009. Due to failure in the CMOS production at STM the delivery was delayed a couple of weeks before shipping to CMU for post-processing.

6.1 Die layout

Together with the proposed varactor, two other varactor designs, an experimental switch, a filter and four resonators were made by other designers. The other devices can be studied in [2]. The die is the minimum size provided from the foundry, which are $3 \mu m^2$ for the BiCMOS7RF process at STM. In figure 6.1 an overview of the die is shown.

The design presented in this thesis is located at the middle on the right hand side of the die (marked Varactor 1 in Figure 6.1). There are placed 24 bond pads at the edges of the chip. The bond pads are simple metal connections without any electrostatic discharge protection. This protection is not needed as there are no electronic devices on this chip. The four pads used to connect the varactor are placed at the right to get connections as short as possible.
Figure 6.1: Die layout in Cadence
6.1.1 Dummy capacitor

To measure the capacitance of a MEMS capacitor a network analyzer will be used. The S-parameters is then extracted and the capacitance and Q-factor can be calculated. To be sure that the analyzer only measures the capacitance of the varactor and not the parasitic capacitances of the bond-pad and measurement wires, a dummy capacitor is used. The dummy capacitor is a wire layed out parallel to the varactor wire. This dummy wire should have the same capacitance as the wire to the varactor. To measure the actual capacitance of the varactor, the difference is computed. To subtract the parasitic capacitances is reasonable because the circuit where the capacitor is integrated is placed as close to the capacitor as possible.

6.2 Design considerations

The design follows the post-CMOS MEMS process rules made by CMU, which is conservative when it comes to under-etch rules. As the die only has 24 bond pads, there was only room for one design. If several structures could be made, reducing the initial gap even further than the rules allow could increase the tuning range significantly (seen in section 5.4.3). Violation of the rules impose a danger that the structure do not release from the substrate. Longer actuator and more fingers can also increase the tuning range, but as the actuator is made longer the lateral curl gets more significant. More lateral curl increases the chance for the rotor comb touching the stator comb when the actuator is flattened. Longer fingers in the comb also increases the chance for touching, not only due to lateral curl in the finger, but as a result of the lateral curl in the actuator. The lateral curl is due to metal misalignment in the photolithography and stressed polymer films on the sidewall of the beam. Having a wide actuator beam reduces the lateral curl [32]. Touching fingers as a result of lateral curl is shown in figure 6.2.

With this in our minds, the design was made conservative when it comes to gap, and length of the fingers and the actuator to increase the probability of a fully operational device.

As mentioned, to get maximum initial curl M12 layers were mainly used. Another consideration is to use ACTIVE layer under released structures or not. The ACTIVE layer defines where the thin oxide is placed, elsewhere there is thick oxide. The thick oxide has highly compressive stress and increases the initial curl. No ACTIVE layer was placed under the actuator to maximize initial curl [33].
Another reason to use thick oxide under the actuator is to ensure no etching of the polysilicon heater. Thin oxide layers can fail in the post-process etch and the polysilicon heater can be etched. Etching the heater can change the resistance and the response to voltage.

6.3 Structure layout

In figure 6.3 the layout of the varactor is presented. Here we can see the metal layers and the polysilicon heater. The white space is the etch holes. The minimum gap and hole size is defined in the post-CMOS MEMS design rules and are important to obey to assure structure release.

The actuator is a 340 $\mu m$ long and 7 $\mu m$ wide M12 beam. On each side of the actuator 40 fingers are attached. This gives a total of 80 fingers on the rotor comb. The stator comb has 39 fingers on each side and the total number of fingers in the varactor is 158. When the post-process is finished, the structure rotor comb is released and curls out of the plane.

6.3.1 Poly heater

To be able to heat the actuator a polysilicon heating element is placed under it. The polysilicon loop is in total 414 $\mu m$ long and 2 $\mu m$ wide. The loop is only stretching 200 $\mu m$ from the anchor towards the beam tip. As seen in
Figure 6.3: Layout in Cadence
section 5.2 the heat is well distributed towards the tip of the comb even if
the heater is not covering the whole beam length.

The heater can be seen in figure 6.3 and is slightly darker than the metal
layers. The left side of the heater is connected to the global earth and the
right is connected to a bonding pad.

6.3.2 Comb fingers

The comb fingers are 44\(\mu m\) long and 2.5\(\mu m\) wide. The gap between the
fingers is 1.5\(\mu m\) and the gap between the finger tip and actuator/anchor is
4\(\mu m\). The gap is defined by the post-CMOS MEMS process rules to be sure
that the structures get released. To maximize the tuning range the gaps
have to be made as small as possible. The fingers are shown in figure 6.4.

![Figure 6.4: Layout of fingers in Cadence](image)

Not shown in the figure is a polysilicon layer under each finger. This is put
under the structure to reduce the initial curl in the fingers. If the fingers are
curled significantly out of the plane the tuning range is reduced.
Chapter 7

Discussion

In this chapter the performance of the device is compared with other CMOS-MEMS implementations from the literature. Weaknesses and future possibilities for improvement will also be addressed and discussed.

To be able to vary the tuning frequency of a radio transceiver over several frequency bands and be able to create an integrated wireless device, varactors which are integrable and with large tuning range and high Q-factor are needed. This is essential when it comes to meet the vision of a low-cost fully integrated radio.

Today’s tunable passive RF components suffer from poor performance and is the largest obstruction for designing fully integrated RF front-ends [15]. The major limitations in today’s tunable RF components are the quality factor, tuning range and phase noise. Especially the tuning range and phase noise are an obstruction to improvement of RF systems. In [34] and [35] monolithic implementations of high frequency VCOs based on regular CMOS varactors are presented. The frequency tuning range of these devices is low and is insufficient to make a wide-band radio. Innocent et al in [36] made two identical VCOs. One was based on a MEMS varactor and the other was based on a CMOS varactor. The MEMS varactor had lower phase noise than the CMOS and the capacitance value is much more constant over a cycle in the VCO. However, the MEMS structure suffered from stiction and no tuning of the varactor was achieved, but the RF performance was better than the CMOS implementation. The major problem with CMOS varactors is capacitance dependency of the RF signal voltage which produces phase noise [37]. The capacitance is nearly unaffected by the RF signal in MEMS designs.

However, two requirements for commercial success for MEMS capacitors were stated by Innocent et al in [36]. The tuning voltage must be CMOS
compatible and precautions for avoiding electrostatic pull-in must be taken.

Many very high quality MEMS structures have been shown in the literature. In [38] various RF MEMS designs in the literature are presented. The varactor designs have Q-factors from 25 to 100 at frequencies from 3 to 40 GHz. Tuning range from 50 to 740 % is observed and very low ESR is obtained. The tuning range of these MEMS devices is better than today’s CMOS varactors and is promising for future transceiver designs. The difficulty with these devices is the specialized production processes used and integration with CMOS. To integrate these MEMS structures with CMOS electronics, intricate and expensive process steps must be added to the production line. Another way to integrate these MEMS devices with CMOS is a hybrid package. However, the RF signals have to be connected out of the chip and into the MEMS device. This degrades the RF signals.

The maskless CMOS-MEMS process provided by CMU used in this thesis makes it easy to monolithically integrate the MEMS passive components with the CMOS electronics. The CMOS-MEMS components presented in the literature yield good results. The high tuning range, high Q-factor and easy integrability makes them promising for future integrated transceiver designs. The easy monolithic integration can reduce production cost compared with today’s radio transceivers based on discrete components. This is a major motivation factor in electronic design.

The CMOS-MEMS varactor designs presented are large and mechanically complicated. Investigation on how new designs for even more efficient varactors are important for the success of CMOS-MEMS varactors in low-cost monolithic wide-bandwidth radios.

In this thesis we have looked at how a varactor based on out of the plane curl can be implemented in a CMOS-MEMS process. To predict the behavior of the proposed structure analytic models and FEM simulations were used.

### 7.1 Features and benefits

The varactor design is a simple structure composed of simple cantilever beams. Simplicity of the design is important in mechanical systems. The reliability of the system is increased when the number of mechanical components are reduced. The actuator in our structure is a single cantilever beam controlled by temperature. Simple operation of the system is beneficial and the proposed structure is mechanically simpler than other CMOS-MEMS varactor designs presented in [2], [17] and [15].
7.1.1 Tuning range

The implemented device have a simulated and modeled theoretical tuning range of 240 % to 325 %. The tuning range is comparable with CMOS-MEMS varactors presented in [17],[15], but is lower. However, the operation mechanism of the proposed structure is much simpler and there is room for refinement and improvement of the proposed structure. The gaps used in the implemented device are conservative when it comes to state of the art post-CMOS MEMS processes. With state of the art production equipment the gaps between the fingers in the layout can be reduced significantly. As seen in section 5.4.3, if the minimum gap can be reduced, the tuning range can be significantly increased. The length of the actuator and the number of fingers also affect the tuning range of the varactor. The tuning range is increased linearly with the length of the varactor.

A problem for lateral moving varactor structures are parasitic capacitances. In [17], the parasitic capacitances to the substrate and between the frames that holds the combs are significant and the tuning range is reduced. In our design the parasitic capacitances are minimized. The rotor comb is levitated over the substrate and the stator comb. Parasitic capacitances to the substrate and the capacitance to the frame holding the stator fingers is minimized when the structure is levitated.

7.1.2 Area efficiency

In electronic design, area efficiency is important to maximize. Saving die area for a design directly reduces cost and increases chances of commercial success. The proposed structure is area efficient as the rotor comb is moved out of the plane. In opposition to laterally moving devices, no extra area is needed when the combs are unfolded. In the designs presented no comb frames are needed to support the capacitor fingers as they are directly connected to the actuator. No curl compensating frames are needed, which also saves area. Compared to the CMOS-MEMS varactor implementations in [17] the area efficiency is within the same range. For the proposed structure the maximum simulated area efficiency is $185fF/(100\mu m \times 400\mu m) = 4.6aF/\mu m^2$. To make these CMOS-MEMS varactor designs more area efficient a more refined post-CMOS production process could be a solution. If the minimum gaps in the production process can be made smaller and the structures can be made thicker the area efficiency can be increased.
7.2 Challenges

7.2.1 Ambient temperature

A major unaddressed weakness of the proposed structures is the dependency of the ambient temperature. As the ambient temperature changes, the structure temperature can be changed, even when the polysilicon heater is held at a constant voltage. If the device is used in a communication device, a large change in the ambient temperature can result in a communication failure. In [39] it is shown that the thermal dissipation is changed with the ambient temperature. It is also suggested that improved thermal insulation can minimize the problem. Another way to decrease the ambient temperature dependency can be to use temperature dependent voltage references to control the actuator voltage. They have a linear voltage with temperature, which is also the case for the displacement of the thermal actuator. The voltage references can then be used to neutralize the ambient temperature dependency of the varactor.

7.2.2 Initial curl

A limitation when implementing the proposed structure is the initial curl. The operation of the structure is dependent on initial curl due to residual stress in the CMOS wafer. The stress can be difficult to predict and can be very different from run to run. This will directly affect the minimum capacitance and the tuning range of the varactor. It is important to have a stable and predictable initial capacitance for a RF varactor and the uncertainty in the initial curl is a major contributor to this uncertainty. How different production processes can affect the initial curl is discussed in section 7.3.

However, if the residual stress is low in the structures and the initial curl is low, the structure can be operated in another way. With low stress, the initial curl is low but the structures will still have the same temperature dependency as the TCE difference is the same. The structure can still be heated and aligned with the chip substrate and the maximum capacitance is obtained. If the actuator is heated beneath the in-plane alignment temperature, the actuator will curl under the chip plane and the capacitance will be reduced. If the thermal budget is large enough, the structure can be significantly curled beyond the chip plane. This can give a high tuning range even when the process has low residual stress. A side-view of the alternate operation of the actuator is shown in fig 7.1.
7.2.3 Lateral curl

The lateral curl in a CMOS-MEMS process can be difficult to predict. The lateral curl is an effect from misalignment of the metal layers and polymer layers on the structure sidewalls. Misalignment is random and difficult to predict. The lateral curl is also temperature dependent. If the actuator or the comb fingers experience too much lateral curl, the stator and rotor comb can touch. Electrical contact between stator and rotor is not wanted. The lateral curl limits the initial gap, finger length and actuator length of the proposed structure.

Precautions can be taken to minimize the lateral curl of a structure. The lateral curl can be minimized with wide and thin structures or by making tapered beams as described in [33].

7.2.4 Power Consumption

Generally thermal actuators have large power consumption when activated. The power consumption has not been a concern in this thesis. In future designs, to save power, thermal insulation and as high as possible temperature dependency is needed to make power efficient devices. This is especially important when the varactor is used in a wireless device where the power source is limited. In the varactor design by Oz et al. in [15], a latching mechanism is used to fix the varactor in two discrete positions which gives two fixed capacitance values. When the varactor is in the fixed
state, no power is consumed. Implementing a latching mechanism in the proposed design can be difficult.

### 7.2.5 Linearity

An inherent problem with gap tuning capacitors is the unlinearity. A linear capacitor eliminates the need for a separate processor to linearize the capacitor [40]. The proposed design is based on gap and area overlap in the comb fingers and the capacitance is unlinear with the voltage.

This problem can be overcome with altering the length of the comb fingers in the capacitor. If the fingers close to the anchor are made longer than the fingers at the end of the beam the capacitance of the varactor can be made more linear with voltage. As seen in section 5.4 the capacitance with respect to the voltage is following a $1/x$ curve. To compensate for this unlinearity the finger length must be adjusted along the capacitor length to neutralize the $1/x$ curve.

In figure 7.2 a schematic sketch of the layout of a varactor with a declined capacitance along the actuator. The fingers in the figure are only linearly declining, and are not adjusted to linearize the capacitance of a $1/x$ curve. An undesired effect of linearization of the capacitance with shorter fingers is a direct reduction in tuning range.

### 7.3 Production process

The production process used in this thesis is out of date when it comes to state of the art digital electronics. Integration with modern processes is essential for CMOS-MEMS structures to be commercially viable in the future. State of the art processes is comprised of different materials and the mechanical behavior is very different from the process used in this thesis and new behavior predictions must be made when integrating an out of the plane based structure in a new process. The models presented and developed in Chapter 4 and 5 can easily be adapted to new processes, but the initial curl must be characterized to get good predictions of the tuning range of the structures.

In state of the art CMOS processes (<90nm technology), process induced stress is used to improve the performance of transistors. Locally induced stress change the mobility of the charge carriers and the performance of the transistor can be changed [41]. This technique can be interesting to investigate for CMOS-MEMS devices based on residual stress. If the
Figure 7.2: Layout-view, modified capacitance distribution
residual stress can be controlled on a MEMS scale, much more accurate predictions of the out of curl can be made and the devices can be refined.

Another aspect with the use of state of the art CMOS processes is the fabrication accuracy. Lower mismatch between metal layers most likely induce less lateral curl in the MEMS structure. With less lateral curl in the proposed structure the gap can be reduced, the fingers can be made longer and the number of fingers can be increased. This can give a higher tuning range.

State of the art CMOS processes use Cu in all the metal layers. The resistivity in Cu is lower than in Al, which is the metal in the process used in this process. Lower resistivity can give lower equivalent series resistance in the MEMS devices and the Q-factor is increased. A drawback for state of the art production processes is thinner metal layers. This gives increased resistance and lower Q-factor.

Characterization of CMOS-MEMS structures in the STM90nm process is, at the time of writing, performed by other researchers in the research group. This will give valuable information on the lateral curl, residual stress and minimum gap in this process. With this information at hand, the development of CMOS-MEMS structures is simplified and more accurate predictions can be made when making a design.

7.4 Models

The models for temperature dependency in [21], presented in chapter 4, combined with the models developed in section 5.4.2 can simplify the development of out of plane capacitor designs based on thermal actuation. The models give an analytic approach to prediction of the temperature dependency of the actuator and the capacitance as a function of the deflection. FEM simulation of electrothermal varactors is time consuming and demands much computing power. These models can reduce time used on optimization and design of the device.

Another problem with the FEM simulator is when the structure is too complicated. The simulator do not converge to a solution and the simulation stops. No result is obtained and a lot of time was wasted.

The analytic models do not incorporate fringe fields and is and idealization to a curled two plate capacitor. Even if the results from the analytic models are not as accurate as the FEM simulations, it will always give a result fast.
Chapter 8

Conclusion

In this thesis we have investigated and designed an out of the plane CMOS-MEMS varactor. The varactor design is comprised of two combs and an actuator. The structure is layed out and implemented in a CMOS process. After the CMOS-MEMS post processing, the structures are released from the chip substrate. Due to high metallization temperatures in the production process and a large difference in the TCEs of the layers in the process, residual stress occurs. The stress is highly tensile in the aluminum layer and compressive in the dielectric layers. The result is an initial out of the plane curl at room temperature. The rotor part of the varactor is comprised of a long actuator, and it is predicted to curl significantly out of the plane after release. This curling increases the gap and reduces the area overlap between the stator and rotor comb.

In the initial condition, when the rotor comb is curled out of the plane, the minimum capacitance is obtained. A polysilicon heater is placed under the actuator and when a voltage is applied, the temperature in the actuator rises. The tip deflection of the actuator is linearly dependent of the temperature and the temperature is near linearly dependent on the voltage. As the temperature of the actuator rises, the actuator is uncurled. The capacitance of the varactor is now increased, and when the actuator reaches the characteristic temperature and is aligned with the substrate, the maximum capacitance is reached.

Models for predicting the actuator behavior is used to see if a thermal cantilever actuator can be used. To align the rotor comb with the stator comb the total deflection of the actuator must be larger than the initial curl. The total deflection of the actuator is limited by the maximum temperature of the CMOS-MEMS process. A model is derived to see how the capacitance of the varactor changes with the radius of curvature or tip deflection. The models have been compared with CoventorWare
FEM simulations, and seem to describe the behavior of the structure fairly well. The models are very useful when optimizing the design as the FEM simulation time of complicated structures is extremely long.

8.1 Results

The simulations and calculations described in this thesis show that implementation of variable capacitors based on out of plane curl and thermal actuation is possible. The simulated performance of the varactor is comparable with other CMOS-MEMS designs presented in the literature. Tuning range between 240 % and 325 % is obtained, but even larger tuning range is needed to meet the vision of a monolithically integrated wide band radio.

The analytic models used to predict the actuator deflection with respect to the temperature agrees with the simulated results. The model developed to see how the capacitance of the varactor changes with curvature of the varactor also yielded good results. These models can simplify development of out of plane curled varactors.

8.2 Future work

To make this type of structure commercially viable, a number of effects have to be further investigated. The residual stress, which controls the initial curl needs to be accurately predicted or controlled. Studies of thermal dissipation and power consumption will be important if the structure is implemented in a wireless system. Further investigation and characterization of the cantilever actuator must be done to accurately model the thermal actuator behavior.

At the time of writing, the proposed structure is under production and if this study is continued, measurements and characterization of the structure will be first priority.
Appendix A

MatLab script: Out of plane actuator model

```matlab
% Tip deflection from lakdawala,deVoes extension of timoshenkos theory

%Computing deflection for a four layer structure.(M1-M2 beam Agilent 0.5um process)

%Beam parameters
w=2.1e-6; %width layer 1-5
l=100e-6; %length beam m
t0=446.42; %Characteristic temeperature K

%Layer 1 Bottom Oxide
E1 = 57e9; %Young modulus Pa
a1 = 0.53e-6;
t1=0.45e-6;
i1=(1/12)*w*(t1^3);

%Layer 2 Polysilicon/oxide
E2 = 160e9; %Young modulus Pa
a2 = 4.3e-6;
t2=0.25e-6;
i2=(1/12)*w*(t2^3);

%Layer 3 Poly--m1 oxide:
E3 = 75e9; %Young modulus Pa
```
a3 = 0.23e−6;
t3=0.55e−6;
i3=(1/12)*w*(t3^3);

% Layer 4 Al(metal1):
E4=70e9;
a4=21e−6;
t4=0.7e−6;
i4=(1/12)*w*(t4^3);

%Oxide m1-m2
E5 = 75e9;
a5 = 0.23e−6;
t5=0.86e−6;
i5=(1/12)*w*(t5^3);

% Layer 6 Aluminum(metal2):
E6 = 70e9;
a6 = 21e−6;
t6=0.7e−6;
i6=(1/12)*w*(t6^3);

% Layer 7 oxide
E7 = 75e9;
a7 = 0.4e−6;
t7=0.86e−6;
i7=(1/12)*w*(t7^3);

%Layer 8 aluminum(metal 3)
E8 = 70e9;
a8 = 21e−6;
t8=0.66e−6;
i8=(1/12)*w*(t8^3);

%Computed vectors and scalars
i=(1/12)*w*(t^3); %moment of inertia
chi=((E1*i1)+(E2*i2)+(E3*i3)+(E4*i4)+(E5*i5)+(E6*i6)+(E7*i7)+(E8*i8)); % total flexural rigidity

y = [t1/2;(t1+t2+t3/2);(t1+t2+t3+t4/2);(t1+t2+t3+t4+t5/2);(t1+t2+t3+t4+t5+t6/2);(t1+t2+t3+t4+t5+t6+t7/2);(t1+t2+t3+t4+t5+t6+t7+t8/2)]; %moment
**arm vector**

yt = y.'; % Transpose of moment arm vector

\[ g = \begin{bmatrix} -1/(w \cdot t1 \cdot E1) & 0 & 0 & 0 & 0 & 0 \\ 0 & -1/(w \cdot t2 \cdot E2) & 0 & 0 & 0 & 0 \\ 0 & 0 & -1/(w \cdot t3 \cdot E3) & 0 & 0 & 0 \\ 0 & 0 & 0 & -1/(w \cdot t4 \cdot E4) & 0 & 0 \\ 0 & 0 & 0 & 0 & -1/(w \cdot t5 \cdot E5) & 0 \\ 0 & 0 & 0 & 0 & 0 & -1/(w \cdot t6 \cdot E6) \\ 0 & 0 & 0 & 0 & 0 & 0 & -1/(w \cdot t7 \cdot E7) \\ 1 & 1 & 1 & 1 & 1 & 1 \end{bmatrix} \] % area and width effects

\[ a = [a2-a1; a3-a2; a4-a3; a5-a4; a6-a5; a7-a6; a8-a7; 0] ; % TCE vector \]

\[ s = [t2+t1; t3+t2; t4+t3; t5+t4; t6+t5; t7+t6; t8+t7; 0] ; % thickness vector \]

defa = 0;

t = 0;

% environment

for t = 292:1:500,

\[ \text{def} = \left( l^2 \right) \left( t-t0 \right) \left( \frac{yt \cdot \text{inv}(g)}{2 \cdot \chi -(yt \cdot \text{inv}(g) \cdot s)} \right) \cdot a ; \]

\[ \text{defa}(t) = \text{def} ; \]

\[ \text{ta}(t) = t ; \]

end

% plot(defa(292:500))

\[ \text{def} = \text{defa}(292) \]

\[ \rho = l^2/(2 \cdot \text{defa}(292)) \]

\[ \text{ddefa} = (\text{defa}(500) - \text{defa}(292))/(500-292) \]
Appendix B

Published paper

RF MEMS front-end resonator, filters, varactors and a switch using a CMOS-MEMS process

J. E. Ramstad, K. G. Kjelgaard, B. E. Nordboe, O. Soeraasen

Published at symposium on Design, Test, Integration and Packaging of MEMS and MOEMS (DTIP), pp. 170-175, April 2009
RF MEMS front-end resonator, filters, varactors and a switch using a CMOS-MEMS process

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Abstract: The paper describes the design of multiple RF MEMS front-end components that could replace off-chip units in future transceivers. The components can effectively be combined and co-fabricated with CMOS circuitry. A CMOS-MEMS approach is used, which means that the microelectromechanical parts are made by multi-layer structures in a standard CMOS process. The ASIMPS procedure offered by CMP uses the CMOS processing at STMicroelectronics, and a simple post-CMOS release-etching step is performed at Carnegie Mellon University, USA. The paper presents a resonator, resonating filters, electrothermally operated varactors and an experimental switch. The components are modeled and simulated by using CoventorWare FEM software. A test chip is currently in production.

I. INTRODUCTION

To make future wireless sensor devices smaller, smarter and more autonomous, fully integrated and multifunctional nodes will be required. It is challenging to design on-chip RF front-end devices, and today’s solutions typically use discrete, off-chip components to meet the RF performance requirements (external inductors, crystals, SAW and ceramic filters). It has been shown that micromachined components (RF MEMS) can beneficially replace a great number of those bulky off-chip components with even better performance, smaller size and lower power consumption [1].

The combination of microelectromechanical components (MEMS) and microelectronics (CMOS) has traditionally been done by using multi-module packaging involving part production and assembling at diverse premises and costly handling steps. The future of radio communication is moving toward integration of multiple radio standards into a ‘single chip radio’. To see this vision come through, on-chip varactors and filters with high Q-factor and large tuning range are needed [2,3].

This paper presents one resonator, four filters, three varactors and one experimental switch that can be used as RF MEMS components. These RF front-end components are analytically modeled and simulated using FEM (Finite Element Method) software.

II. THE CMOS-MEMS PROCESS

In this paper, a circuit has been designed by using a conventional 0.25µm CMOS process from ST-Microelectronics. The MEMS parts of the circuit are etched by post-processing at Carnegie Mellon University in Pittsburgh, USA, through the broker service CMP [4].

By using laminated structures of metals and dielectrics, it is possible to make micromechanical structures that can be used as RF MEMS components, operating in close interaction with CMOS circuits. Figure 1 shows the post-CMOS process, which is used for these RF MEMS designs.

This post-CMOS technique is particularly interesting because it does not require any modifications of the original CMOS process and the technique does not need additional photomasks for post-processing. The residing top metal layer will define the microstructures and will also serve as a mask to protect the underlying CMOS circuitry from being etched.

The microstructures are etched and released using RIE etching equipment. This dry etching technique makes it possible to etch narrow gaps with a high aspect ratio. This post-CMOS technique has yielded good results for various applications from research institutes such as Carnegie Mellon University in USA, National Tsing Hua University in Taiwan and University of Oslo in Norway [5,6,7,8].

The number of metal layers used to define the structure determines the resulting thickness of a microstructure. A thick structure is in most cases preferred, but the thickness is limited by the number of metal layers in the actual CMOS process. When the materials are deposited in a CMOS process residual stress occurs, showing its effect when the structures are released. Stress tends to make the structures curl and care must be taken when designing structures that are supposed to be flat. The curling of a MEMS structure may in some cases be used as an advantage (see section V).
III. RF MEMS RESONATOR AND FILTERS

One resonator architecture and four filter architectures have been investigated. These filters and resonators are structures that move laterally, parallel to the substrate. The resonator and the filters are made by a laminate of metal and dielectric using metal layer 1 through metal layer 4 as shown in figure 2. For the filters, the coupling beam between the resonators is designed as a 45° V-shaped beam, constrained by the CMOS process. The location of a coupling beam along the beam length affects the bandwidth of the filter; placing the coupling beam close to the anchors gives a high percentage bandwidth. The number of resonators that are coupled together determines the order of the filter.

Fig. 2. A free-free resonator (middle) and a free-free filter (top left)

Fig. 2 shows a free-free resonator that has support beams with the length $L_s$ at position L/4 and 3L/4 of the length of the resonator. Because of the chosen dimensions, the free-free beam is designed so that the support beams operate at their second resonating mode (mode number two) while the beam in the middle operates at mode number one. The support beams exert extentional forces to the beam in the middle, representing “infinite” impedance. Due to the nearly infinite impedance from the support beams, a minimum of energy is lost per cycle by the device, making it possible to operate this device with a high Q-factor even at atmospheric pressure. The resonators and filters in this paper all have a length $L$, a width $W$ and a thickness $H$ as shown in figure 2.

Fig. 3 shows a top-down view of the free-free resonator and a 4th order free-free filter using the V-shaped coupling beam. The red crosses indicate the anchor points of these structures. The arrows indicate the input and output of the resonator and filters. Equation (1) shows the equation for the resonance frequency where $\kappa$ depends on the type of resonator (cantilever, clamped-clamped, free-free).

$$f_0 = \kappa \sqrt{\frac{E}{G} \frac{W}{L^2}}$$  \hspace{1cm} (1)

The input and output arrows are not shown in these figures but are situated close to the input and output arrows. The length $L_s$ for the free-free resonator and filter is described by equation (2) [9].

$$L_s = 0.5 \cdot 1.683 \left( \frac{E}{G} \frac{W}{L^2} \right)^{1/2}$$  \hspace{1cm} (2)

Figure 4 shows three other filters that have been made. One cantilever (one fixed end) and two clamped-clamped beam (two fixed ends) filters have been designed by having two and three resonators coupled together using the V-shaped coupling beam. The 6th order CC-filter gives a better stop band attenuation compared to a 4th order CC-filter.

Fig. 4. Top left: 4th order cantilever filter. Top right: 4th order clamped-clamped (CC) filter. Bottom: 6th order CC-filter
Figure 5 shows the filter response (CoventorWare, mechanical simulations) for a 4th order cantilever filter, a 4th order FF-filter and a 6th order CC-filter, respectively. It can be seen from these graphs that the 3dB value is located before and after the first and last mode of the response. The 6th order filter has a better attenuation in the stop-band of the filter. The pink line between the first and second mode in fig. 6 shows a theoretical representation of a flattened filter using termination resistors at the input and output of the filter.

![Graph showing filter response](image1)

Fig. 6. Filter response for a 4th order CC-filter

Table I summarizes the dimensions of the filters and the single resonator as well as showing their respective resonance frequency (without applied polarization voltage).

<table>
<thead>
<tr>
<th>Resonator dimensions</th>
<th>Cantilever</th>
<th>Clamped-clamped 4th order</th>
<th>Clamped-clamped 6th order</th>
<th>Free-free 4th order</th>
</tr>
</thead>
<tbody>
<tr>
<td>Thickness H (µm)</td>
<td>4.8</td>
<td>4.8</td>
<td>4.8</td>
<td></td>
</tr>
<tr>
<td>Width W (µm)</td>
<td>2</td>
<td>1</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>Length L (µm)</td>
<td>100</td>
<td>100</td>
<td>100</td>
<td></td>
</tr>
<tr>
<td>Electrode length (µm)</td>
<td>75</td>
<td>80</td>
<td>42</td>
<td></td>
</tr>
<tr>
<td>Electrode gap (µm)</td>
<td>1.2</td>
<td>1.2</td>
<td>1.2</td>
<td></td>
</tr>
<tr>
<td>Resonance freq. (kHz)</td>
<td>159.45</td>
<td>510.778</td>
<td>510.774</td>
<td></td>
</tr>
</tbody>
</table>

The bandwidth of these filters have been made by tuning the coupling beam location towards the anchor points described in equation (3) where $k_{12}$ is a normalized coefficient, $k_{12}$ is the coupling beam stiffness and $k(y)$ is the resonator stiffness [3].

![Graph showing filter response](image2)

Fig. 7. Frequency response for a 2nd to 6th order CC resonator-filter

$BW = \frac{f_0}{k_{12}} \frac{k_{s12}}{k_r(y)}$ (3)

Table II shows the performance of the filters. The free-free filter has a high bandwidth and has a good resonator Q-value. The cantilever beam has a low operational frequency but instead it has a relatively good percentage bandwidth. The 6th order CC-filter has a slightly lower percentage bandwidth than its 4th order counterpart, however the rejection ratio of a 6th order CC-filter is much better as can be shown by the Cadence simulation in figure 7.

![Graph showing filter response](image3)

Fig. 7. Frequency response for a 2nd to 6th order CC resonator-filter

Table II: Filter characteristics

<table>
<thead>
<tr>
<th></th>
<th>Cantilever 4th order</th>
<th>Clamped-clamped 4th order</th>
<th>Clamped-clamped 6th order</th>
<th>Free-free 4th order</th>
</tr>
</thead>
<tbody>
<tr>
<td>Coupling-to-anchor (µm)</td>
<td>15</td>
<td>1.5</td>
<td>1.5</td>
<td>0.5</td>
</tr>
<tr>
<td>Center frequency (kHz)</td>
<td>160.266</td>
<td>510.778</td>
<td>510.949</td>
<td>513.872</td>
</tr>
<tr>
<td>Bandwidth (kHz)</td>
<td>0.803</td>
<td>1.403</td>
<td>1.431</td>
<td>3.793</td>
</tr>
<tr>
<td>Q-filter</td>
<td>199.6</td>
<td>364.1</td>
<td>357.1</td>
<td>135.5</td>
</tr>
<tr>
<td>Termination resistance (MΩ)</td>
<td>1.19</td>
<td>4.81</td>
<td>6.94</td>
<td>12.92</td>
</tr>
</tbody>
</table>

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IV. LATERAL VARACTORS

Two lateral varactor architectures with high tuning range have been made. Both capacitors are based on area tuning of combs moving laterally, parallel to the substrate, as seen in fig 8. A common problem with post-CMOS is the out-of-plane curl that can cause offset between two electrodes or sensing nodes. Any offset between the combs will lead to a significant reduction in sidewall capacitance. The out-of-plane curl can be minimized by aligning the anchors along a common axis. A curl compensation frame is used to get equal out-of-plane curl for both the movable and the static comb.

By changing the metal offset in the beams to the other side, the actuator will contract instead of expand once released (Fig. 10). The displacement is almost equal to that of the first actuator.

A latch mechanism for keeping the beams in a fixed position is added so the actuators only require power during switching [10]. The latch used for these designs have two slots which gives two different stable positions. This means that two steady capacitor values can be obtained. The latch can be extended with more slots if desired.

There are two varactor designs: Design A and design B. In design A, both actuators are used while in design B only one of the actuators is used. The combs in design A have a small finger overlap in the layout (Fig. 11), which equals the anticipated displacement $\Delta x_{\text{released}}$ of the actuator after release. This design uses both actuators; one actuator will push the combs while the other will pull. By exploiting the self-assembly of the actuators maximum overlap $\Delta x$ will be obtained. However, because the fingers have an overlap in layout, the gap between the fingers will be restricted by the post-process design rules. Design A has a size of 626.6x424.3 µm without the anchors, with a finger gap $g = 1.2$ µm and $\Delta x = 17$ µm.

Design B has shorter fingers without any overlap in the layout and the fingers are intended to stay in the same position after release. Since the fingers have no overlap in layout, the gap can be made smaller than for design A. A smaller gap will for a given overlap area offer larger capacitance. However, the maximum overlap, LO, for design B will be less than $\Delta x_{\text{released}}$. Design B has a size of 549.6x424.3 µm without the anchors, with a finger gap $g = 0.8$ µm, $\Delta x_{\text{released}} = 12$ µm and LO = 10.8 µm.
Initial curl of 50 to 30 µm corresponds to a simulator temperature offset of 173 to 100K, which gives a minimum capacitance of 18 to 25fF. The maximum capacitance (varactor aligned with the substrate at 186-120 °C) is simulated to 74fF and the tuning range from 200 to 310 %.
VI. AN EXPERIMENTAL POST-CMOS SWITCH

An experimental lateral DC series switch is designed as a test structure to see if it is possible to make a metal-to-metal connection by using this post-CMOS process (Fig.14). Since the CMOS structure is built by using layers of aluminum and oxide, the contact area will be smaller for this CMOS-MEMS process than for other MEMS processes. If there is any vertical offset between two CMOS-MEMS structures, that should intentionally connect, then the possibility of obtaining a connection between the metal layers could fail. By this test structure we will investigate how well defined the sidewalls of the beams are. The switch is actuated with similar electrothermal actuators as used for the lateral capacitors described in section IV (only smaller dimensions). A metal-to-metal connection will be obtained after release due to the self-assembly effect of the actuators. When heated the electrodes will be drawn apart and the connection will be broken. A similar latch mechanism as described in section IV has been used to minimize the power consumption.

If the experimental electrothermal yields good results, it would be possible to try to make an electrostatic switch.

VII. CONCLUSION

Several front-end RF MEMS devices integrated in a CMOS-MEMS process has been shown. Simulation results using CoventorWare has been done for these devices. The simulations of these CMOS-MEMS components show that these components yield sufficient results to be used in an analog front-end radio transceiver. The laminate of metal and dielectric results in an adequate performance that is not as good as state-of-the-art MEMS. However, by avoiding off-chip components, these on-chip filters and varactors combined with on-chip processing electronics yields sufficient performance for a modern radio front-end transceiver.

The RF MEMS components presented in this paper shows filters operated at 160 and 510kHz, varactors with a tuning range of −450% and −300%. In addition, an experimental electrothermal switch has been presented. Figure 15 shows an overview of the chip-layout in Cadence.

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ISBN:
List of Figures

1.1 CoventorWare 3D plot out-of-plane varactor ........................ 3
2.1 System-level block diagram of a RF transceiver where the areas marked with green is RF MEMS passive components (Fig from [5]) .................................................... 6
2.2 Anisotropic wetetched bulk micromachined diaphragm ........ 7
2.3 a) After CMOS process b) Al etch c) anisotropic Si etch ...... 9
2.4 a) After CMOS process b) anisotropic oxide etch c) anisotropic Si etch d) isotropic Si etch to release structure from substrate .................................................. 12
3.1 Sketch of a capacitor .................................................... 14
3.2 1st generation gap-tuning varactor (from [17]) ................. 17
3.3 SEM of gap and area tuning varactor (Figure from [17]) ..... 18
3.4 Comb resonator (fig from [18]) ..................................... 18
4.1 Release of stressed cantilever ........................................ 23
4.2 Cantilever toroids (from [26]) ....................................... 24
4.3 Two-layer cantilever .................................................. 26
4.4 Curled multilayer cantilever ......................................... 28
5.1 4µm × 4µm × layerthickness meshed 3D-model .................. 32
5.2 Thermal distribution .................................................. 34
5.3 3D-view of the actuator ............................................. 35
5.4 Deflection δ vs temperature T for M12 300µm actuator simulate in CoventorWare ............................................. 36
5.5 Stress distribution in the actuator ................................... 38
5.6 Stress distribution in the actuator anchor ......................... 38
5.7 $\delta T$ for M12 and M12P actuator and milling .................. 39
5.8 Side-view, a) actual field distribution, b) simplified field distribution ......................................................... 40
5.9 Perspective view of the two-plate capacitor ....................... 41
5.10 Side view of two-plate capacitor ................................. 42
<table>
<thead>
<tr>
<th>Section</th>
<th>Title</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>5.11</td>
<td>Capacitance distribution $\rho = 460 \mu m$</td>
<td>43</td>
</tr>
<tr>
<td>5.12</td>
<td>Capacitance test structure</td>
<td>45</td>
</tr>
<tr>
<td>5.13</td>
<td>Tuning range</td>
<td>45</td>
</tr>
<tr>
<td>5.14</td>
<td>Tuning range vs comb length</td>
<td>46</td>
</tr>
<tr>
<td>5.15</td>
<td>Capacitance of test structure</td>
<td>47</td>
</tr>
<tr>
<td>5.16</td>
<td>Capacitance, Modeled vs simulated and percentage error</td>
<td>48</td>
</tr>
<tr>
<td>5.17</td>
<td>Capacitance, Modeled vs simulated vs normalized voltage</td>
<td>48</td>
</tr>
<tr>
<td>5.18</td>
<td>Capacitance, Modeled for the proposed structure</td>
<td>50</td>
</tr>
<tr>
<td>5.19</td>
<td>Q-factor, Modeled for the proposed structure</td>
<td>51</td>
</tr>
<tr>
<td>6.1</td>
<td>Die layout in Cadence</td>
<td>54</td>
</tr>
<tr>
<td>6.2</td>
<td>Lateral curl in actuator</td>
<td>56</td>
</tr>
<tr>
<td>6.3</td>
<td>Layout in Cadence</td>
<td>57</td>
</tr>
<tr>
<td>6.4</td>
<td>Layout of fingers in Cadence</td>
<td>58</td>
</tr>
<tr>
<td>7.1</td>
<td>Side-view actuator, normal and in plane operation of the actuator</td>
<td>63</td>
</tr>
<tr>
<td>7.2</td>
<td>Layout-view, modified capacitance distribution</td>
<td>65</td>
</tr>
</tbody>
</table>
## List of Tables

2.1 STM SiGe 0.25\(\mu m\) BiCMOS(BiCMOS7RF) process features  .  10

4.1 Material properties for structural CMOS-MEMS layers [21]
   [23]  . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 22

4.2 100\(\mu m\) beam characteristics, initial curl and temperature
   dependency [27]  . . . . . . . . . . . . . . . . . . . . . . . . . . . . 29

4.3 100\(\mu m\) beam, milling  . . . . . . . . . . . . . . . . . . . . . . 30

5.1 BiCMOS7RF defined in CoventorWare  . . . . . . . . . . . . . . . . 32

5.2 300\(\mu m\) beam deflection, different beam types ,STM BiCMOS
   0.25\(\mu m\) )  . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 36
Bibliography


